Application Note

Keep the Balance – Balancing of Supercapacitors

ANP090 // RENÉ KALBITZ

1 Introduction

Supercapacitors (SC) usually operate at low voltages of around 2.7 V. In order to reach higher operating voltages, it is necessary to build a cascade of serial connected SC cells. [1] [2] Due to production or aging related variations in capacitance and insulation resistance the voltage drop over individual capacitors may exceed the rated voltage limit. Thus, a balancing system is required to avoid accelerated aging of the capacitor cell. [3] [4] In the following, we want to explain the effect of unequal voltage division in such cascades in principle. To improve the understandability we consider a series stack of two capacitors.[1] In this note, we review the theoretical background and we provide some measurements as well as discussions on practical examples. The goal is to provide an overview on possible balancing strategies as well as an understanding of the explained concepts. The developer is invited to choose and adapt any strategy to meet specific requirements. For further information concerning the design-in process, please read our application note **ANP077**[5] "Supercapacitor – A Guide for the Design-In Process"

2 Imbalance of Serial Connected Supercapacitors

A capacitor may be modeled by a parallel connection of an R-C unit and a insulation resistance. For the moment we neglect the insulation resistance and consider a series stack of two capacitors with capacities C_1 and C_2. The conserved quantity in such a stack is the condensed charge q at the capacitor, i.e. at its internal interfaces. Using the conservation of charge $V_{1,2} = q/C_{1,2}$ the voltage drop over each capacitor is

$$V_1 = \frac{V_g}{\left(\frac{C_1}{C_2} + 1\right)}$$

and

$$V_2 = \frac{V_g}{\left(\frac{C_2}{C_1} + 1\right)}$$

with $V_g = V_1 + V_2$ as the total voltage. (For more detail see also A.1) If both capacitance values are equal, the voltage at the terminals of two serial connected capacitors is equally

$$V_1 = V_2 = \frac{V_g}{2} = V_r$$

Thus, the system is balanced and each capacitor is charged at its rated voltage V_r.

In the following we may consider the case where C_1 is larger than C_2. With above equations it can be shown (see A.1) that the voltage drop at each terminal is unequal by

$$\Delta V = \mp \frac{V_g}{2} \cdot \left| \frac{C_1 - C_2}{C_1 + C_2} \right|$$

With the voltage difference ΔV, which is in the following referred to as imbalance, we may write

$$V_1 = \frac{V_g}{2} - \Delta V$$

and

$$V_2 = \frac{V_g}{2} + \Delta V$$

Using the definition of capacitance $C = \Delta q/\Delta V$ with q as charges at the capacitor interface and V as voltage at the capacitor), the above equation may be rewritten as

$$V_1 = \frac{V_g}{2} - \frac{\Delta q}{C_1}$$

and

$$V_2 = \frac{V_g}{2} + \frac{\Delta q}{C_2}$$

In order to adjust the voltage of each capacitor to $V_r = V_1 = V_2$ the charge has to be increased at capacitor 1 and decreased at capacitor 2 by the amount of Δq. Using the definition of electrical current ($I = dq/dt$) the voltage may be written as

$$V_1 = \frac{V_g}{2} - I_1 \cdot \frac{\Delta t}{C_1}$$

and

$$V_2 = \frac{V_g}{2} + I_2 \cdot \frac{\Delta t}{C_2}$$

The current $I_{1,2}$ is interpreted as the electrical current that has to flow for a time period Δt to equalize this system. The constant current that is required to equalize a voltage difference ΔV in a given time period Δt is

$$I_{1,2} = \frac{\Delta V}{\Delta t} C_{1,2}$$

[1] Any system may be reduced to an equivalent circuit of two capacitors.

Application Note

Keep the Balance – Balancing of Supercapacitors

3 Balancing Current and Balancing Time

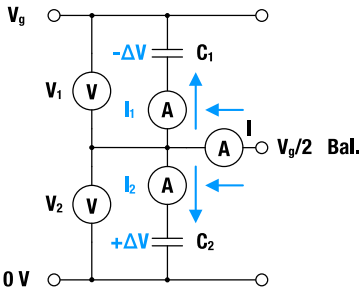

Figure 1: Balancing currents in a capacitor stack.

We may use above equations for the estimation of the current magnitude. In this example we used the full tolerance range of the capacitance, which is 40% (-10%/+30%). Hence, for $C_r = 10$ F we obtain $C_1 = 13$ F and $C_2 = 9$ F. The total voltage of 5.4 V provides then a voltage difference $\Delta V = 0.49$ V (i.e. at C_2 the voltage drop is $V_2 = 3.19$ V and at C_1 the voltage drop is $V_1 = 2.21$ V). The $\Delta V \approx 0.5$ V is the largest possible imbalance. To illustrate this situation, we use the circuit in Figure 1. The balancing current necessary to balance C_1 and C_2 within 1 sec respectively are:

$$I_1 = \frac{0.5\ \text{V}}{1\ \text{sec}}\ 13\ \text{F} = 6.5\ \text{A}$$

$$I_2 = \frac{0.5\ \text{V}}{1\ \text{sec}} 9\ \text{F} = 4.5\ \text{A}$$

Hence, C_1 needs to be charged with $I_1 = 6.5$ A and C_2 needs to be discharged $I_2 = 4.5$ A. The current that has to be provided by the balancing terminal can be calculated with Kirchhoff's current law. We may consider currents that flow out of the junction as negative and currents that flow into the junction as positive. Since I_1 and I_2 flow out of the junction and the balancing current I into the junction, the balancing current is

$$I = 11\ \text{A} = 6.5\ \text{A} + 4.5\ \text{A}$$

Although the result may vary depending on ΔV and Δt this example of calculation may show that balancing at the characteristic RC-time requires currents of several amperes. The balancing current, required to balance a strongly imbalanced system of $\Delta V = 0.5$ V (as calculated above) in within Δt can be estimated with

$$I = 2 \cdot \frac{0.5\ \text{V}}{\Delta t} \cdot C_r$$

So far we have neglected the insulation resistance, which starts to dominate the electrical behavior as soon as the SC is fully charged and the charging current becomes smaller than the leakage current I_{leak}. Most manufacturers specify a measurement time of 72 h at rated voltage V_r to determine I_{leak}. Under these conditions the capacitor may be simply modeled by an ohmic resistance $R_{iso} = V_r/I_{leak}$. Hence, if a capacitor is fully charged a serial stack of SC may be considered as a stack of serial connected resistances, which constitute a voltage divider.

4 Balancing Strategies

The literature [3,4,6,7,8] categorizes balancing strategies by different properties like

- energy dissipative behavior,
- balancing speed,
- the type of technology that is used or
- pricing

Thus, when it comes to choosing the right balancing strategy, it is important to now all the parameters and constrains of the specific application to make the right choice.

In this note, we distinguish mainly between:

- active balancing and
- passive balancing

Active balancing involves the utilization of actively controlled switches or amplifying systems.[3, 8] Passive balancing utilizes shunts or self-regulating resistors to lower the effect of overvoltage. Compared to passive balancing, active balancing may be fast, in some cases energy efficient but also relatively cost intensive. Passive balancing, on the contrary, is relatively slow, leads to reduction of the charge storing capabilities but it is more cost efficient than active balancing solutions.

4.1 Passive Balancing with Resistors

Figure 2 presents an example of passive balancing with a resistor. The red and green arrows represent the corresponding physical current flow for the case were C_1 has either over (+ΔV) or under voltage (-ΔV). The current for the balancing speed is adjusted (or restricted) by the resistance of the balancing resistors.

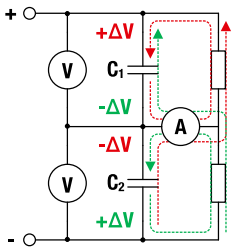

Figure 2: Circuit for passive balancing with resistors.

The balancing resistors have to meet three main requirements:

- The resistance should be as low as possible to allow a fast balancing. This will be beneficial for the lifetime.
- The resistance should be as high as possible to minimize losses and minimize the self-discharge.

Application Note

Keep the Balance – Balancing of Supercapacitors

- The accuracy of the resistors/shunt should be sufficient (≤ 1%) in order to provide an accurate reference.

Clearly, it is necessary to find an optimum between short balancing times and low self-discharge.

The balancing resistance would have to be the order of the equivalent series resistance R_{ESR}, to balance the supercaps within the characteristic RC-time. This is a theoretical consideration and not practical, since it would mean we permanently short-circuit the SC. A good rule of thumb is one tenth of the insulation resistance, i.e.

$$R_b = 0.1 \cdot \frac{V_r}{I_{leak}}$$

With V_r as rated voltage and I_{leak} as leakage current (both values are given in the data sheet of the SC). Due to its magnitude, R_b balances differences in insulation resistances.

The maximum current that can flow at ΔV is $I_{max} = \Delta V/R_b$. The time to equalize a imbalance ΔV up to 95 % can be calculated with

$$t_b = \ln\left(\frac{100\ \%}{100\ \% - 95\ \%}\right) \cdot (R_b \cdot C_r)$$

which can be well approximated with $t_b = 3 \cdot R_b\, C_r$ (as explained in A.2). The resulting balancing times, given in Table 1, are indeed in the range of days. With the given balancing resistances, the self-discharge rate per day is about 41 %. Thus, for many power applications the resistance may even be reduced, at the expense of charge storing abilities and balancing speed.

Capacitance (F)	I_{leak} (mA)	$R_b = R_{ISO}/10$ (Ω)	t_b (h)
3	0.008	33750	84
5	0.012	22500	94
7	0.020	13500	79
10	0.030	9000	75
15	0.060	4500	56
25	0.068	3971	83
50	0.105	2571	107

Table 1: Summary of balancing resistances and corresponding balancing times.

4.2 Passive Balancing with Zener Diodes

An improved balancing time can be achieved, if the resistor is replaced by a Zener Diode as indicated in Figure 3. The arrows again indicate the electrical current flow, in case of a imbalance. The Zener diodes constitutes a variable resistor or a voltage dependent switched resistor. Since the internal resistance is reduced at the breakdown voltage, it is possible to drastically reduce the balancing time in comparison the linear resistor.

Diodes may also serve as general protection against reverse polarity. Especially for larger stacks, it can be advisable to place Zener diodes in parallel to metal oxide semiconductor field effect transistors (MOSFET).

The accuracy of the breakdown voltage is, compared to the accuracy of ohmic resistors, usually relatively low. In total the tolerances could be as high as around 10 %.

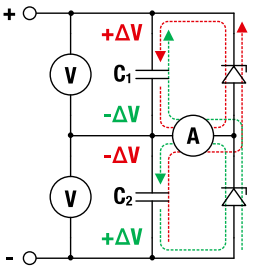

Figure 3: Circuit for balancing with Zener diodes.

Possible overvoltages could be still avoided by a reduction of working voltage. For operations at higher temperatures, it might also be necessary to consider the shift of breakdown voltage due to the temperature coefficient.

The strong voltage dependence of the reverse current makes it difficult to calculate the balancing time accurately.[8] The actual current characteristic of commercial Zener diodes are often not given in the datasheet.

It is however possible to roughly estimate the balancing time on the basis of the above expression for t_b (see section 4.1) A rough estimate can be made with the rated power dissipation of the Zener diode P_r, usually given in the datasheet. If the diode breakdown voltage is equal to actual operating voltage, V_R we may substitute $R_b^* = V_r^2/P_r$ into above expression for t_b and obtain

$$t_b^* = 3 \cdot \left(\frac{V_r^2}{f \cdot P_r} \cdot C_r\right)$$

with f as correction factor.

Due to the strong voltage dependence of the reverse current, it may be necessary to adjust f from case to case to its effective value. Since the diode will most of the time operate well below its total power dissipation we suggest f = 1/10.

4.3 Passive Balancing with MOSFETs

Another type of balancing can be utilized with a MOSFET as given Figure 4. Similar to the Zener diode, the MOSFET constitutes a voltage driven switch or variable resistor.

Application Note

Keep the Balance – Balancing of Supercapacitors

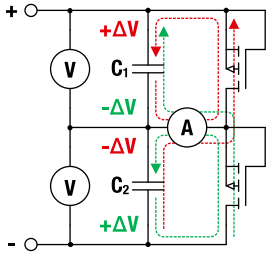

Figure 4: Circuit for balancing with MOSFET

The arrows again indicate the electrical current flow, which is similar to the passive balancing in Figure 2. As soon as the voltage imbalance exceeds the threshold voltage of the MOSFET, the increased drain voltage leads effectively to a discharge of the overcharged capacitor. It is possible to think of the MOSFET as voltage dependent resistors, which leads to improved balancing times compared to passive resistors.

4.4 Active Balancing with Operational Amplifier

Any application that needs a shorter balancing time will have to apply an active balancing. Active balancing always involves integrated circuits such as operational amplifier (OP-AMP), which is illustrated in Figure 5. The circuit contains red and green arrows, which represent the corresponding physical current flow for the case were C_1 has either over (+ΔV) or under voltage(-ΔV).

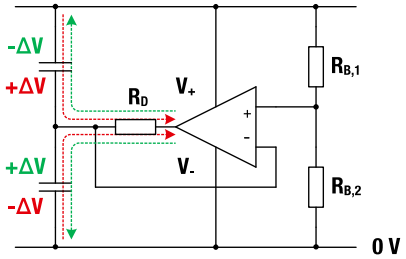

Figure 5: Circuit for active balancing with feedback amplifier.

The balancing resistance, as used for the active balancing, is determined on the basis of the designated internal resistance of the OP-AMP, which is at least the order of 10 MΩ but usually even higher. To ensure the voltage detection at the inputs the balancing resistances $R_{B,1}$ and $R_{B,2}$ should be about 10 times smaller than the internal resistance of the OP-AMP. As a result, the loss through the balancing resistance can be as small as for the internal resistance of the SC.

However, a more significant cause of loss is the supply current, delivered through contacts V_+ and V_-. Depending on the type of OP-AMP the permeant supply current may be in the range from 1 µA to 10 mA. This may pose a technical obstacle, that needs to be considered at the conceptual design-in phase.

The balancing current is provided by the output of the OP-AMP and regulated via the feedback loop. The damping resistance R_D at the output of the OP-AMP is only as high as to prevent oscillation during the current regulation.

4.5 Active Balancing with DC-DC converter

Another concept of active charge equalization consists of DC-DC converters, each connected across two neighboring cells, as illustrated in Figure 6. Due to the low losses of commercially available converters, this concept is in terms of balancing time and power burn more efficient than passive balancing.

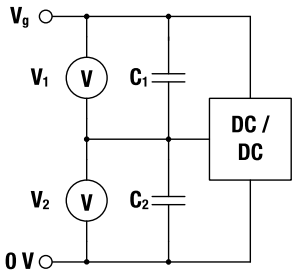

Figure 6: Schematic balancing circuit with DC-DC Conversion.

There are balanced buck-boost SC chargers available on the market, which are suitable for a range of applications. Available for instance are the

- LTC3351, Hot Swappable Backup Supercapacitor Charger

or the

- LTC3128, Supercapacitor Charger and Balancer

from Analog Devices. Additional information are also provided in the Würth Elektronik (WE) Webinar **"WE Backup Your Application – A real life SC backup solution"**.[11]

Although DC-DC converters constitute a relatively costly balancing strategy, they are on the other side also an elaborate and comprehensive solution. They may provide complete charging and hot swappable charging solutions with low power consumption. The choice at the end is always with the developer.

5 Measurements

The voltage measurements were performed with a self-developed measurement setup, based on the integrated circuit CY8CKIT-059 from PSoC. The data acquisition was utilized with an Excel-script. The measurement setup including the programming of the script were developed by Jon-Izkue Rodriguez from WE eiSos.

The power supply we used was the HMP4040 from Rohde & Schwarz. The currents for the determination of the power dissipation were measured with M252A METRAHit ESPECIAL Current Transformer Connection Multimeter from Gossen-Metrawatt.

Application Note

Keep the Balance – Balancing of Supercapacitors

We tested a series combination of two SC from WE eiSos

- Capacitor 1: $C_1 = 10$ F and
- Capacitor 2: $C_2 = 15$ F

This practically constitutes deviations from a theoretical capacitor with a rated capacitance of $C_r = 12.5$ F.

For the charging we used a

- charging voltage $V_g = 5.4$ V and
- max. charging current $I_c = 2$ A

For the sake of reliable circuit design, we want to underline that combining SC with different rated capacities is inadvisable. We only choose this combination for experimental purposes. This setup provides three advantages:

First, this set up provides a significant and reproducible imbalance of around ±0.5 V. We could change the set of capacitors without an intensive search for suitable mismatches.

Second, it also demonstrates the potential robustness of the EDLC, if operated under extreme overvoltage. Although the lifetime were drastically reduced to few weeks, none of the used SC showed a catastrophic failure.

Third, it shows the operation of the individual balancing strategies under extreme conditions.

The chosen capacitors demonstrate the operation of each strategy under extreme imbalance. In practice, the variation of capacitance is much lower than in this example, even over different production batches.

We also studied the self-discharge behavior of each circuit for a period of 24 h. Hereunto, we disconnected the entire balancing circuit from the primary power source after the capacitors were fully charged and balanced. The voltage was again measured with the PSOC CY8CKIT-059.

Based on the measurements we also give an assessment about the applicability of the circuit in stand-alone long-term applications. In that respect, the expression “long-term” describes a period of approximately several days.

5.1 Resistor, 1 kΩ

For the passive balancing, as shown in Figure 2, we used a 0.6 W, 1kΩ (1%) resistance. We have chosen the resistance in favor of a short balancing time rather than a low power loss.

The measured voltages V_1 and V_2 and the resulting voltage difference $|V_1 – V_2|$, given in Figure 7, show a complete balancing after around 600 min. V_1 and V_2 approach V_r asymptotically

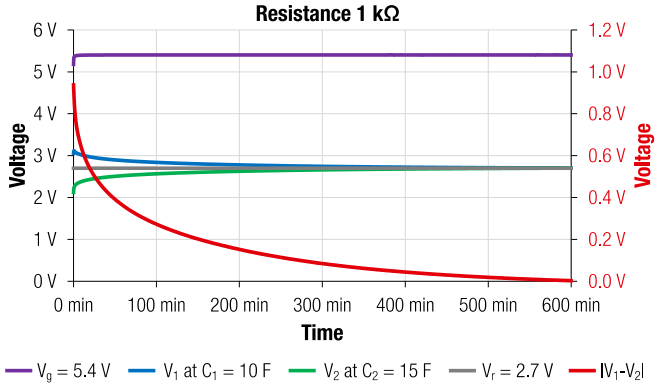

Figure 7: Time dependent cell voltages V_1, V_2 and V_g as well as the voltage difference $|V_1 – V_2|$ (corresponds to ordinate on right hand side) as measured for the passive balancing with resistors.

The measured balancing time corresponds to the estimation, given in section 4.1, $t_b = 625 \text{ min} = 3 \cdot R_b \cdot C = 3 \cdot 1 \text{ k}\Omega \cdot 12.5 \text{ F}$. The overall power dissipation (effective leakage current, I_{loss}) after 12 h is $2.8 \text{ mA} \cdot 5.4 \text{ V} \approx 15 \text{ mW}$. For low power applications or for backup solutions this balancing speed may be sufficiently fast and the power loss is acceptable. For battery driven (standalone) applications, the resistance should be increased to reduce losses. To be on the safe side, it is also advisable to reduce operating voltage, to avoid overvoltage.

The half-life, self-discharge time is estimated with

$$t_{loss} = \ln\left(\frac{100\ \%}{100\ \% - 50\%}\right) \cdot \left(\frac{V_g}{I_{loss}} \cdot C_{stack}\right)$$

with

$$C_{stack} = \left(\frac{1}{C_1} + \frac{1}{C_2}\right)^{-1}$$

Hence, in this example:

$$t_{loss} \approx 0.7 \cdot \frac{5.4 \text{ V}}{2.8 \text{ mA}} \cdot 6 \text{ F} \approx 133 \text{ min}$$

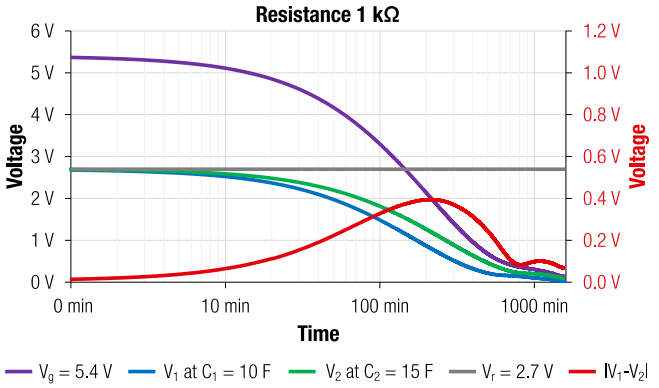

Figure 8: Measured self-discharge of balancing circuit with resistors. Graph shows time dependent cell voltages V_1, V_2 and V_g as well as the voltage difference $|V_1 – V_2|$ (corresponds to ordinate on right hand side).

Application Note

Keep the Balance – Balancing of Supercapacitors

The results of self-discharge measurement as given in Figure 8 correspond to the estimated half-life self-discharge time of around 130 min.

The self-discharge time is large enough to consider passive balancing with 1 kΩ as suitable for a standalone solution.

5.2 Zener Diode BZX79-B2V7

For the passive balancing, as shown in Figure 3, we used the voltage regulator diodes BZX79-B2V7 from NXP Semiconductors. The results, given in Figure 9, indicate a complete balancing after around 80 min. With the datasheet value of total power dissipation of 500 mW, the measured value fits roughly to the theoretical approximation of

$$t_b^* = 3 \cdot \left(\frac{V_r^2}{f \cdot P_r} \cdot C_r \right)$$

$$t_b^* = 3 \cdot \left(\frac{7.3\ \text{V}}{0.1 \cdot 0.5\ \text{W}} \cdot 12.5\ \text{F} \right) = 70\ \text{min}$$

The overall power dissipation (effective leakage current, I_{loss}) after 12 h is 5 mA · 5.4 V ≈ 27 mW. For lower voltages the power dissipation will be even lower. (The datasheet states: I_{loss}(1 V) = 20 µA)

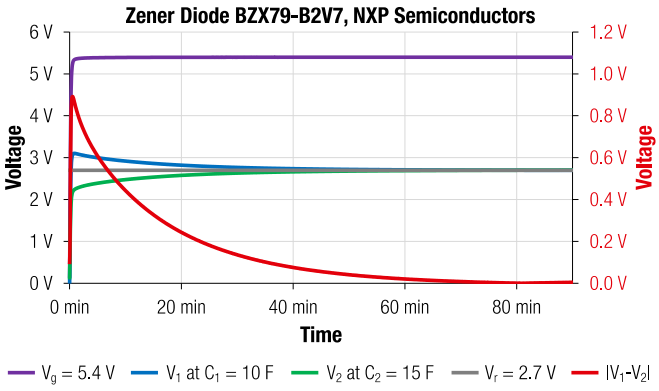

Figure 9: Time dependent cell voltages V_1, V_2 and V_g as well as the voltage difference $|V_1 – V_2|$ as measured for the balancing with Zener diode BZX79-B2V7.

Due to the strong nonlinear voltage dependence of Zener diodes, the calculation of the self-discharge characteristic is difficult. We may however use the same concept as for t_b^* and introduce a correction factor f to adjust the expression for the half-life self-discharge time.

We may estimate that the data sheet value I_{loss} (1 V) = 20 µA is in our case about 10 times higher.

With f = 10 the theoretical half-life self-discharge time for a stack, balanced with a Zener diode, can be estimated with

$$t_{loss}^* = \cdot \left(\frac{V_g}{f \cdot I_{loss}} \cdot C_{stack} \right)$$

$$t_{loss}^* \approx 0.7 \cdot \frac{5{,}4\ \text{V}}{10 \cdot 20\ \mu\text{A}} \cdot 6\ \text{F} \approx 1900\ \text{min} \qquad (1)$$

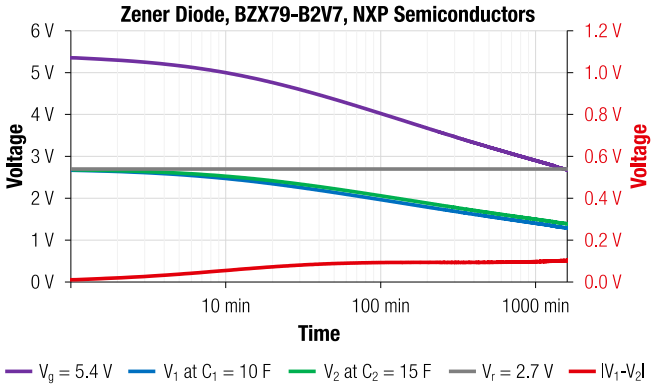

Figure 10: Measured self-discharge of balancing circuit with Zener diode. Graph shows time dependent cell voltages V_1, V_2 and V_g as well as the voltage difference $|V_1 – V_2|$ (corresponds to ordinate on right hand side).

The results of self-discharge measurement, as given in Figure 10, show that t_{loss}^* = 1900 min roughly fits the actual half-life self-discharge time.

Based on the measured self-discharge behavior, we think, the circuit could still be suitable for long-term stand-alone applications.

5.3 MOSFET, ALD910022 (Test Board SABMB2)

The MOSFET based balancing circuit, as given in Figure 4, was implemented with the test board SABMB2 for the MOSFET ALD910022 from Advanced Linear Devices.

The results in Figure 11 indicate a complete balancing after around 300 min. The overall power losses after 12 h of 1.5 mA · 5.4 V ≈ 8 mW were about as low as for the Zener diode.

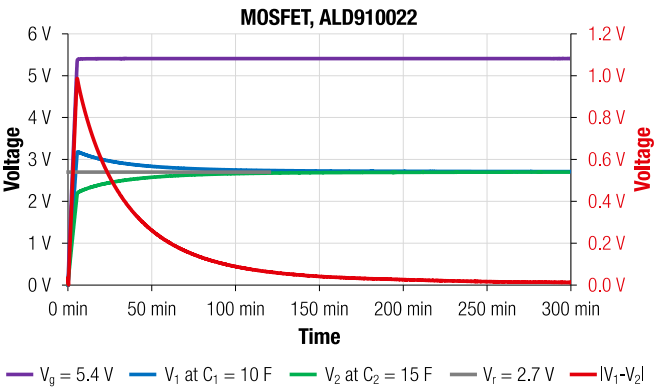

Figure 11: Time dependent cell voltages V_1, V_2 and V_g as well as the voltage difference $|V_1 – V_2|$ as measured for the active balancing with the ALD910022.

Application Note

Keep the Balance – Balancing of Supercapacitors

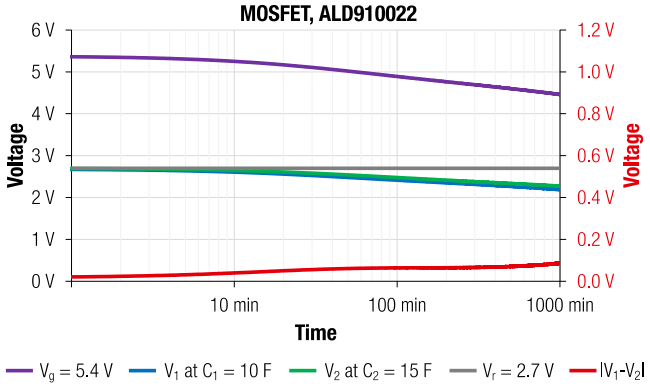

Figure 12: Measured self-discharge of balancing circuit with MOSFET. Graph shows time dependent cell voltages V_1, V_2 and V_g as well as the voltage difference $|V_1 – V_2|$ (corresponds to ordinate on right hand side).

The results of the self-discharge measurement in Figure 12 show that after 24 h the total cell voltage has decreased to about 4 V. With this rate t_{loss} will be in the order of several days. A comparison to the maintain voltage measurement at the **REDEXPERT** online tool [10] suggests that the MOSFET does not significantly increase the self-discharge rate. We therefore conclude the circuit is suitable for long-term stand-alone applications.

5.4 Amplifier; OPA2677

For the active balancing with the amplifier OPA2677 (Texas Instruments), we utilized a circuit as given in Figure 13. The advantage of the OPA2677 is the relatively high output current of 500 mA, which enables a fast balancing.

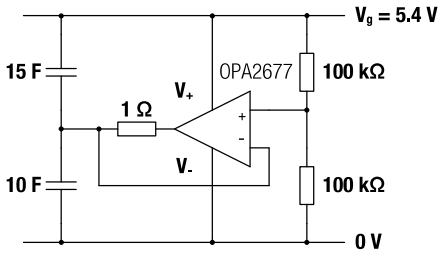

Figure 13: Active balancing circuit of OPA2677 as used for the measurements.

The measured cell voltages in Figure 14 show an instantaneous balancing within the charging time, which is in this measurement about 3 min. The balancing speed can be further increased by decreasing the damping resistor from 1 Ω to 0.4 Ω. With 0.4 Ω the balancing times of around 2 min were reached. The trade of was a noticeable decaying oscillating behavior.

The damping resistor at the output should not be below 0.4 Ω to prevent oscillation of the output voltage. We found 1 Ω to be the optimum between fast balancing and damping.

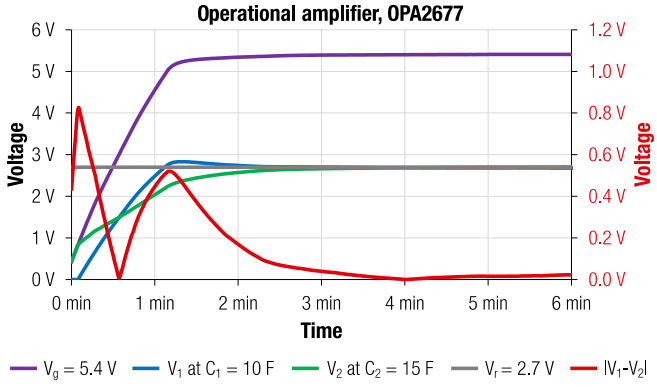

Figure 14: Time dependent cell voltages V_1, V_2 and V_g as well as the voltage difference $|V_1 – V_2|$ as measured for the active balancing with the OPA2677.

The overall power dissipation after 12 h is 50 mA · 5.4 V ≈ 270 mW. The power is manly dissipated via the supply terminals of the amplifier. This relatively high power consumption shows the main disadvantages of this type of strategy. It is fast but it also has a large permanent power burn.

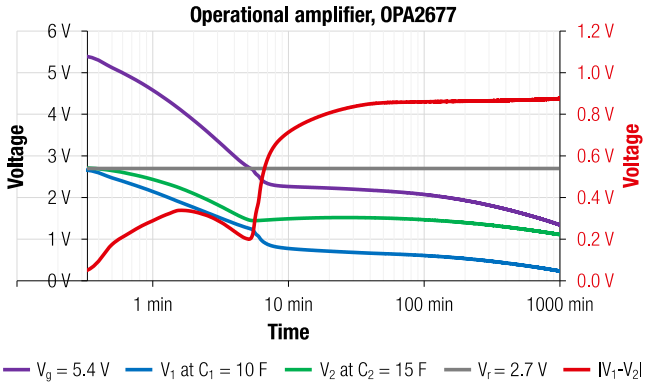

Figure 15: Measured self-discharge of balancing circuit with the OPA2677. Graph shows time dependent cell voltages V_1, V_2 and V_g as well as the voltage difference $|V_1 – V_2|$ (corresponds to ordinate on right hand side).

The results of the self-discharge measurement in Figure 15 indicate a half-life self-discharge time of t_{loss} = 5 min. Since we may only speculate about the voltage dependence of current losses at the terminals, we refrain from a mathematical estimation of t_{loss}. We do not consider the circuit suitable for long term standalone application.

Although the circuit always ensured a balanced charging, the losses via the supply channels are significant. We demonstrated, however, the feedback amplifier might work in principle. It is at the end the developers responsibility to find the best solutions for his application.

Application Note

Keep the Balance – Balancing of Supercapacitors

5.5 Balancing Board, LTC3128

The evaluation board DC1887A utilizes the buck-boost SC charger and balancer LTC3128 from Analog Devices. It is charging the SCs at a preset voltage of 4.2 V. The board operates at a supply voltage of 5.5 V. The measurement results, given in Figure 16, indicate a complete balancing after 1.5 min.

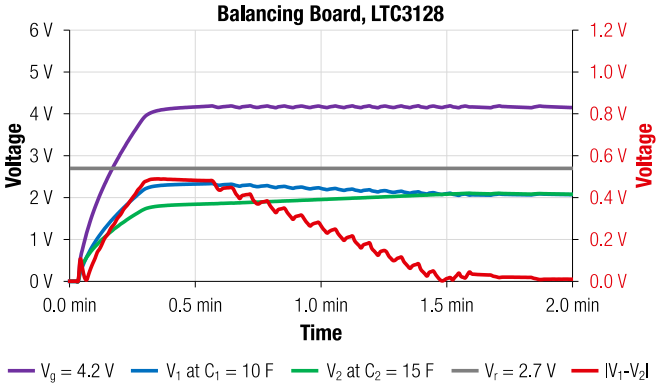

Figure 16: Time dependent cell voltages V_1, V_2 and V_g as well as the voltage difference $|V_1 – V_2|$ as measured for the active balancing with the LTC3128.

The overall power dissipation after 12 h is 0.1 mA · 5.4 V ≈ 0.5 mW.

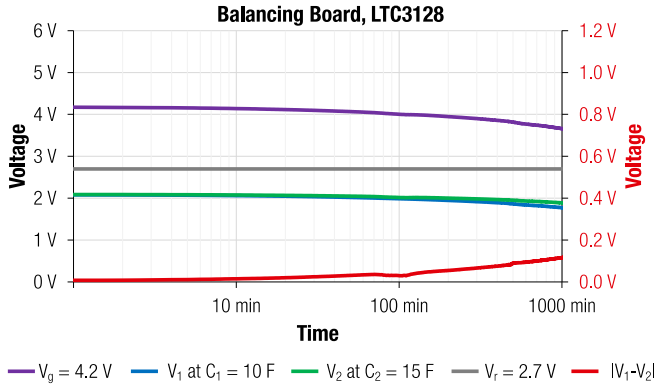

Figure 17: Measured self-discharge of balancing circuit with LTC3128. Graph shows time dependent cell voltages V_1, V_2 and V_g as well as the voltage difference $|V_1 – V_2|$ (corresponds to ordinate on right hand side).

The measurement results of the self-discharge in Figure 17 show that after 24 h the cell voltage has decreased from 4.2 V to about 3.4 V. With this rate t_{loss} will be in the order of several days. Thus the SC charger and balancer LTC3128 is suitable for long term standalone applications.

6 Summary

We have reviewed the theoretical description of active as well as passive balancing strategies and performed some practical measurements to illustrate the different characteristics of each strategy.

In the following, we assess the tested balancing circuits on the basis of balancing speed, power dissipation as well as pricing. It is however, the responsibility of the developer to find the best solution based on even more comprehensive parameters. Availability, lifetime and design-in time might also influence the choice of balancing strategy.

The balancing with the resistor is the slowest balancing strategy, but yields the advantage of low power consumption, low cost and easy circuit design. Depending on the resistors it might be suitable for long-term standalone applications. The balancing speed of the Zener diode is moderate. It yields the advantage of relatively low power consumption, low cost and easy circuit design.The relatively low power dissipation makes it suitable for long term standalone applications.

The MOSFET circuit showed a relatively low power dissipation. Its balancing speed of the given example is moderate. We found the MOSFETS might be suited for long term standalone applications. The OP-AMP certainly provides a fast balancing in comparison to the other strategies, but shows the largest power dissipation. Compared to the other strategies it constitutes the most expensive solutions. Due to the high power dissipation, it may not be suitable for standalone applications. The balancing board provided the fastest balancing and a moderate power dissipation. It is generally an overall convenient but somewhat pricey solution. Concerning the included DC/DC conversion, its overall cost can be considered as moderate. Due to its low power dissipation, it might be suitable for long-term standalone application. An overview of the summarized results is given in Table 2.

Balancing Type	Power Dissip. (mW)	Balancing Time (min)	Relative Cost
Resistor, 1 kΩ	15	600	low
Zener diode, BZX79-B2V7	27	70	low
MOSFET, ALD910022	8	300n	moderate
Amplifier, OPA2677	270	3	high
Evaluation-Board DC1887A	42	1.5	high - moderate

Table 2: Summary of the results

Application Note

Keep the Balance – Balancing of Supercapacitors

We also derived formulas for the:

- calculation of the charging voltages in a disbalanced system

$$V_1 = \frac{V_g}{\left(\frac{C_1}{C_2} + 1\right)}$$

and

$$V_2 = \frac{V_g}{\left(\frac{C_2}{C_1} + 1\right)}$$

- required balancing current

$$I = 2 \cdot \frac{\Delta V}{\Delta t} \cdot C_r$$

- resistor balancing time

$$t_b = 3 \cdot R_b \cdot C_r$$

- balancing time for balancing with Zener diodes

$$t_b^* = 3 \cdot \left(\frac{V_r^2}{f \cdot P_r} \cdot C_r\right)$$

- half-life self-discharge time

$$t_{loss} = 0.7 \cdot \left(\frac{V_g}{I_{loss}} \cdot C_{stack}\right)$$

- theoretical half-life self-discharge time for a stack, balanced with a Zener diode

$$t_{loss}^* = 0.7 \cdot \left(\frac{V_g}{f \cdot I_{loss}} \cdot C_{stack}\right)$$

We hope the measurement examples illustrated the general advantages and disadvantages of each approach.

Application Note

Keep the Balance – Balancing of Supercapacitors

A Appendix

A.1 Conservation of Charge and Disbalance

In a series connection of N capacitors with capacitance C_N the total capacitance is

$$\frac{1}{C_g} = \frac{1}{C_1} + \frac{1}{C_2} + \ldots + \frac{1}{C_N}$$

with C_g as effective (or gross) capacitance. It is a physical requirement that in a series connection the amount of charges q, stored on each capacitor, is equal, thus

$$q = q_1 = q_2 = \ldots = q_N.$$

With Kirchhoff's voltage law

$$V_g = V_1 + V_2 + \ldots + V_N$$

we arrive at a relation between the total applied voltage, capacitance and charge

$$V_g = \frac{q}{C_g} = \frac{q}{C_1} + \frac{q}{C_2} + \ldots + \frac{q}{C_N}$$

Remark: In principle any stack can be equivalently modeled as a stack of two capacitors (with its corresponding voltage division):

$$\frac{1}{C_g} = \frac{1}{C_1} + \underbrace{\left(\frac{1}{C_2} + \ldots + \frac{1}{C_N}\right)}_{= C_2'}$$

For the sake of simplicity, we continue with a system of two equally rated capacitors C_1 and C_2:

$$V_g = V_1 + V_2$$

$$V_2 = \frac{q}{C_2}$$

and

$$V_1 = \frac{q}{C_1}$$

$$\frac{V_2}{V_1} = \frac{C_1}{C_2}$$

$$V_g = V_1 + \frac{C_1}{C_2} \cdot V_1 = \left(\frac{C_1}{C_2} + 1\right) \cdot V_1$$

$$V_1 = \frac{V_g}{\left(\frac{C_1}{C_2} + 1\right)}$$

$$\frac{V_1}{V_2} = \frac{C_2}{C_1'}$$

$$V_g = \frac{C_2}{C_1} \cdot V_2 + V_2 = \left(\frac{C_2}{C_1} + 1\right) \cdot U_2$$

$$V_2 = \frac{V_g}{\left(\frac{C_2}{C_1} + 1\right)}$$

Above we have calculated the absolute voltage level V_1 and V_2 of capacitor 1 and capacitor 2, respectively.

In the following we use these expressions to calculate actual magnitude of the disbalance ΔV assuming the capacitor stack is balanced at

$$\frac{V_g}{2}$$

We may at first consider the voltage V_1 at capacitor 1

$$\Delta V_1 = \frac{V_g}{2} - \frac{V_g}{\left(\frac{C_1}{C_2} + 1\right)} = \frac{V_g\left(\frac{C_1}{C_2} + 1\right) - 2 \cdot V_g}{2\left(\frac{C_1}{C_2} + 1\right)}$$

$$\Delta V_1 = \frac{V_g\left(\frac{C_1}{C_2} + 1 - 2\right)}{2\left(\frac{C_1}{C_2} + 1\right)} = \frac{V_g}{2} \frac{\frac{C_1}{C_2} - 1}{\frac{C_1}{C_2} + 1}$$

$$\Delta V_1 = \frac{V_g}{2} \frac{\frac{C_1}{C_2} - \frac{C_2}{C_2}}{\frac{C_1}{C_2} + \frac{C_2}{C_2}}$$

$$\Delta V_1 = \frac{V_g}{2} \cdot \frac{\frac{C_1}{C_2} - \frac{C_2}{C_2}}{\frac{C_1}{C_2} + \frac{C_2}{C_2}} = \frac{V_g}{2} \cdot \frac{C_2\,(C_1 - C_2)}{C_2\,(C_1 + C_2)}$$

$$\Delta V_1 = \frac{V_g}{2} \cdot \frac{(C_1 - C_2)}{(C_1 + C_2)}$$

Similarly we arrive for V_2 at

$$\Delta V_2 = -\frac{V_g}{2} \cdot \frac{(C_1 - C_2)}{(C_1 + C_2)}$$

Hence, the magnitude of the disbalance at each capacitor is equal:

$$\Delta V = |\Delta V_1| = |\Delta V_2| = \left|\frac{V_g}{2} \cdot \frac{(C_1 - C_2)}{(C_1 + C_2)}\right|$$

Application Note

Keep the Balance – Balancing of Supercapacitors

A.2 Disbalance Voltage Level

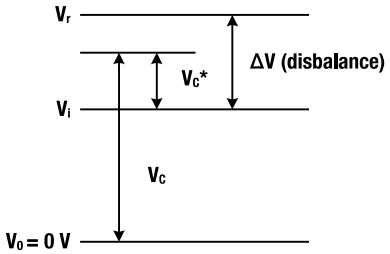

Figure 18: Voltage levels of a capacitor with imbalance ΔV.

As addressed above, charging two series-connected ideal capacitors with two different capacitances results in an unevenly distributed voltage, which results in a disbalance ΔV . Figure 18 shows the voltage levels of a capacitor relative to its nominal voltage V_r . Due to the disbalance ΔV , a capacitor has an initial state of charge V_i , which occurs after the capacitor is fully charged. Due to balancing, the capacitor reaches the actual state of charge V_c with respect to ground (V_0), which can also be specified with respect to V_i:

$$V_C^* = V_c - V_i.$$

Two ratios may now be considered:

$$p^* = \frac{V_c^*}{\Delta V} = \frac{(V_c - V_i)}{\Delta V} \qquad (I)$$

As well as

$$p = \frac{V_c}{V_r} \qquad (II)$$

The ratio p* describes the charging state in relation to the disbalance ΔV and p the charging state in relation to the rated voltage V_r. The balancing time in this R-C system, with R_b as equivalent series resistance and C as capacitance, is calculated with

$$\ln\left(\frac{1}{1 - p^*}\right) \cdot (R_b \cdot C)$$

However, p* does not explicitly contains the absolute value V_r. In order to find such a relation p and p* shall be rewritten

$$p^* + \frac{V_i}{\Delta V} = \frac{V_c}{\Delta V}$$

$$p^* \Delta V + V_i = V_c \qquad (I')$$

Substituting I' in II yields:

$$p = \frac{V_c}{V_r} = \frac{p^* \Delta V + V_i}{V_r} \qquad (II')$$

With $\Delta V = V_r - V_i$ equation II' may also rewritten as

$$p = \frac{p^*(V_r - V_i) + V_i}{V_r}$$

$$p = \frac{p^* \Delta V + V_r - \Delta V}{V_r}$$

or

$$p^* = \frac{pV_r - V_r + \Delta V}{\Delta V} = \frac{V_r (p - 1) + \Delta V}{\Delta V}$$

With $p = 0.9999$ (99.99 %) and the theoretically maximum possible disbalance of $\Delta V = 0.49$ V ($C_{tol.}$:-10%/+30%) it can be calculated that

$$p^* = \frac{2.7\ \text{V}\ (0.9999 - 1) + 0.49\ \text{V}}{0.49}$$

$$p^* = 0.99945\ (99.945\ \%)$$

With the value of p* the respective balancing time may now be calculated with $t_b = f\ (R_b C)$, where

$$f = \ln\left(\frac{1}{1 - p^*}\right)$$

The below Table 3 provides a summary of calculations of p*and f for different parameters

p	ΔV [V](C tol. [%])	p*	f
0.9999	0.49 - 10%/30%	0.99945	7.5
0.999	0.49 - 10%/30%	0.9945	5.2
0.995	0.49 - 10%/30%	0.9725	3.6
0.9999	0.27±10%	0.999	6.9
0.999	0.27±10%	0.99	4.6
0.995	0.27±10%	0.95	3.0

Table 3: Calculation of p*and f for different parameters.

Application Note

Keep the Balance – Balancing of Supercapacitors

A.3 Literature

[1] F. Beguin und E. Frackowiak (Hrsg.), Supercapacitors Materials, Systems, and Applications, WILEY-VCH Verlag, ISBN: 978-3-527-32883-3, S. 352ff (2013)

[2] R. Kötz et al., Principles and applications of electrochemical capacitors, Electrochimica Acta, 45 (15-16), 2483-2498, doi: 10.1016/s0013-4686(00)00354-6 (2000)

[3] D. Linzen et al., Analysis and Evaluation of Charge-Balancing Circuits on Performance, Reliability, and Lifetime, of Supercapacitor Systems. IEEE-Transactions on Industry Applications, 41(5), 1135-1141, doi: 10.1109/tia.2005.853375 (2005).

[4] H. Li et al., Synchronized Cell-Balancing Charging of Supercapacitors. IFAC-PapersOnLine, 50(1), 3338–3343, doi:10.1016/j.ifacol.2017.08.518 (2017)

[5] R. Kalbitz et al., Supercapacitor – A Guide for the Design-In Process, Application Note ANP077, WE eiSos (2020)

[6] Y. Qu et al., Overview of supercapacitor cell voltage balancing methods for an electric vehicle, 2013 IEEE ECCE Asia Downunder, doi: 10.1109/ecce-asia.2013.6579196 (2013)

[7] F. M. Ibanez, Analyzing the Need for a Balancing System in Supercapacitor Energy Storage Systems, IEEE Transactions on Power Electronics, 33(3), 2162-2171, doi: 10.1109/TPEL.2017.2697406 (2018)

[8] B.T. Prashant Sing et al., Extensive review on Supercapacitor cell voltage balancing. E3S Web of Conferences. 87. 01010. 10.1051/e3sconf/20198701010 (2019)

[9] K. B. McAfee et al., Observations of Zener Current in Germaniump–nJunctions, Physical Review, 83(3), 650–651. doi:10.1103/physrev.83.650 (1951)

[10] Link to Supercapacitor Modul in **REDEXPERT**

[11] Link to Online-Seminar "WE Backup Your Application – A real life Supercapacitor backup solution"

Application Note

Keep the Balance – Balancing of Supercapacitors

IMPORTANT NOTICE

The Application Note is based on our knowledge and experience of typical requirements concerning these areas. It serves as general guidance and should not be construed as a commitment for the suitability for customer applications by Würth Elektronik eiSos GmbH & Co. KG. The information in the Application Note is subject to change without notice. This document and parts thereof must not be reproduced or copied without written permission, and contents thereof must not be imparted to a third party nor be used for any unauthorized purpose.

Würth Elektronik eiSos GmbH & Co. KG and its subsidiaries and affiliates (WE) are not liable for application assistance of any kind. Customers may use WE's assistance and product recommendations for their applications and design. The responsibility for the applicability and use of WE Products in a particular customer design is always solely within the authority of the customer. Due to this fact it is up to the customer to evaluate and investigate, where appropriate, and decide whether the device with the specific product characteristics described in the product specification is valid and suitable for the respective customer application or not.

The technical specifications are stated in the current data sheet of the products. Therefore the customers shall use the data sheets and are cautioned to verify that data sheets are current. The current data sheets can be downloaded at www.we-online.com. Customers shall strictly observe any product-specific notes, cautions and warnings. WE reserves the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services.

WE DOES NOT WARRANT OR REPRESENT THAT ANY LICENSE, EITHER EXPRESS OR IMPLIED, IS GRANTED UNDER ANY PATENT RIGHT, COPYRIGHT, MASK WORK RIGHT, OR OTHER INTELLECTUAL PROPERTY RIGHT RELATING TO ANY COMBINATION, MACHINE, OR PROCESS IN WHICH WE PRODUCTS OR SERVICES ARE USED. INFORMATION PUBLISHED BY WE REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE A LICENSE FROM WE TO USE SUCH PRODUCTS OR SERVICES OR A WARRANTY OR ENDORSEMENT THEREOF.

WE products are not authorized for use in safety-critical applications, or where a failure of the product is reasonably expected to cause severe personal injury or death. Moreover, WE products are neither designed nor intended for use in areas such as military, aerospace, aviation, nuclear control, submarine, transportation (automotive control, train control, ship control), transportation signal, disaster prevention, medical, public information network etc. Customers shall inform WE about the intent of such usage before design-in stage. In certain customer applications requiring a very high level of safety and in which the malfunction or failure of an electronic component could endanger human life or health, customers must ensure that they have all necessary expertise in the safety and regulatory ramifications of their applications. Customers acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of WE products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by WE.

CUSTOMERS SHALL INDEMNIFY WE AGAINST ANY DAMAGES ARISING OUT OF THE USE OF WE PRODUCTS IN SUCH SAFETY-CRITICAL APPLICATIONS.

USEFUL LINKS

Application Notes
www.we-online.com/app-notes

REDEXPERT Design Tool
www.we-online.com/redexpert

Toolbox
www.we-online.com/toolbox

Product catalog
www.we-online.com/products

CONTACT INFORMATION

appnotes@we-online.com
Tel. +49 7942 945 - 0

Würth Elektronik eiSos GmbH & Co. KG
Max-Eyth-Str. 1 · 74638 Waldenburg · Germany
www.we-online.com