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# Telefónica views on the design, architecture, and technology of 4G/5G Open RAN networks

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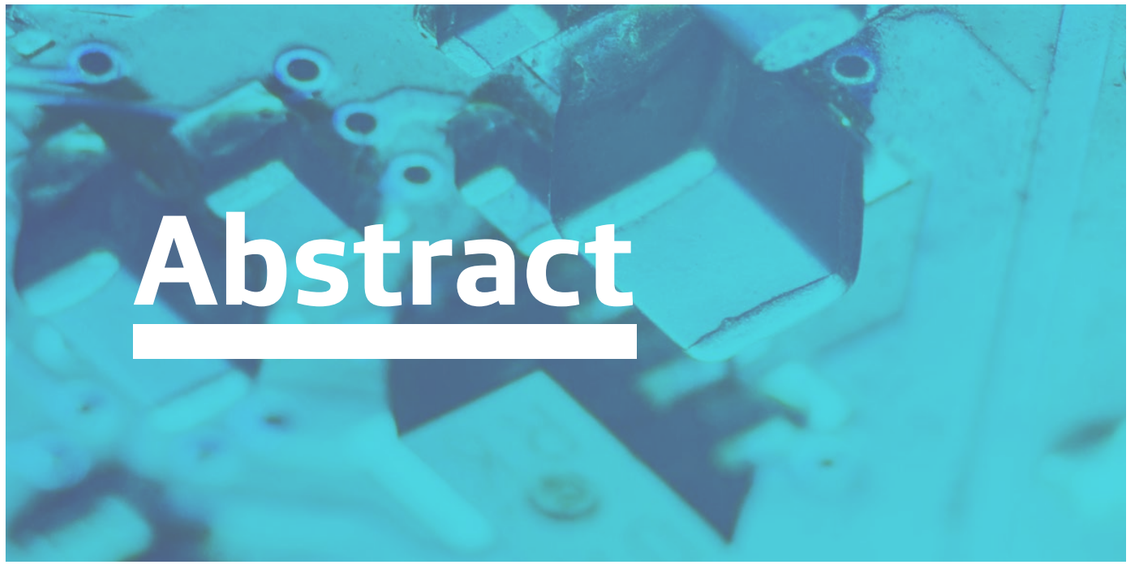
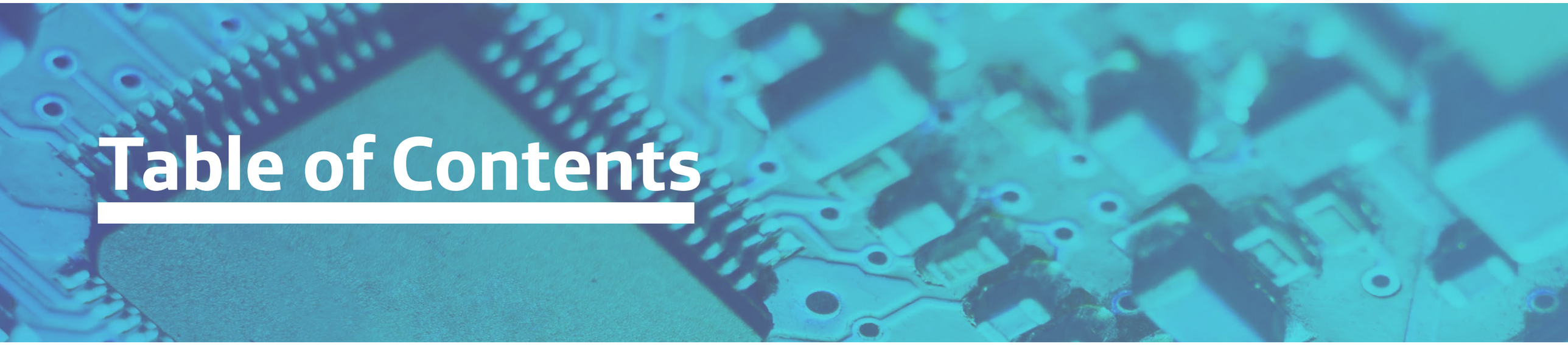


# Abstract

This paper provides an overview of the main technology elements that Telefónica is developing in collaboration with selected partners in the Open RAN ecosystem.

It describes the architectural elements, design criteria, technology choices and key chipsets employed to build a complete portfolio of radio units and baseband equipment capable of a full 4G/5G RAN rollout in any market of interest.

Open RAN White Paper



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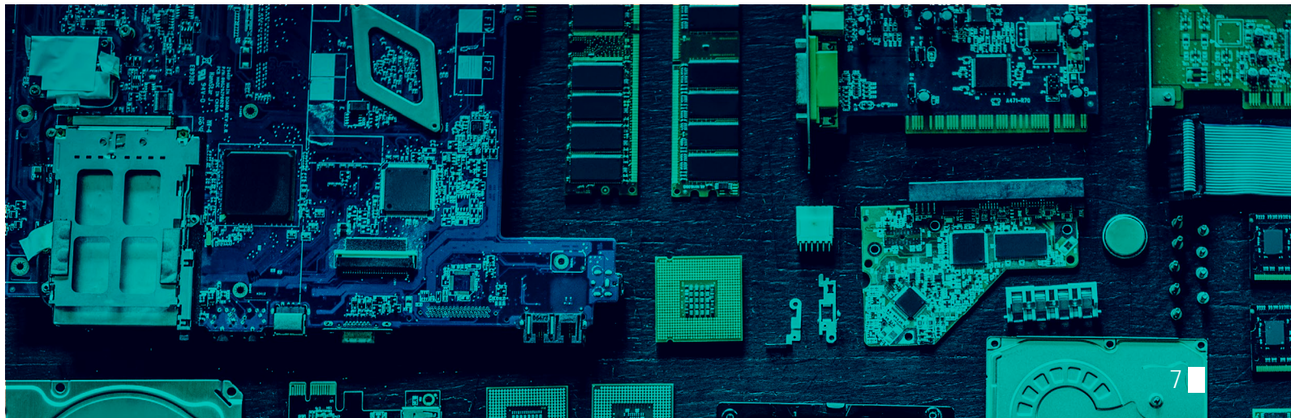
# 1. Introduction

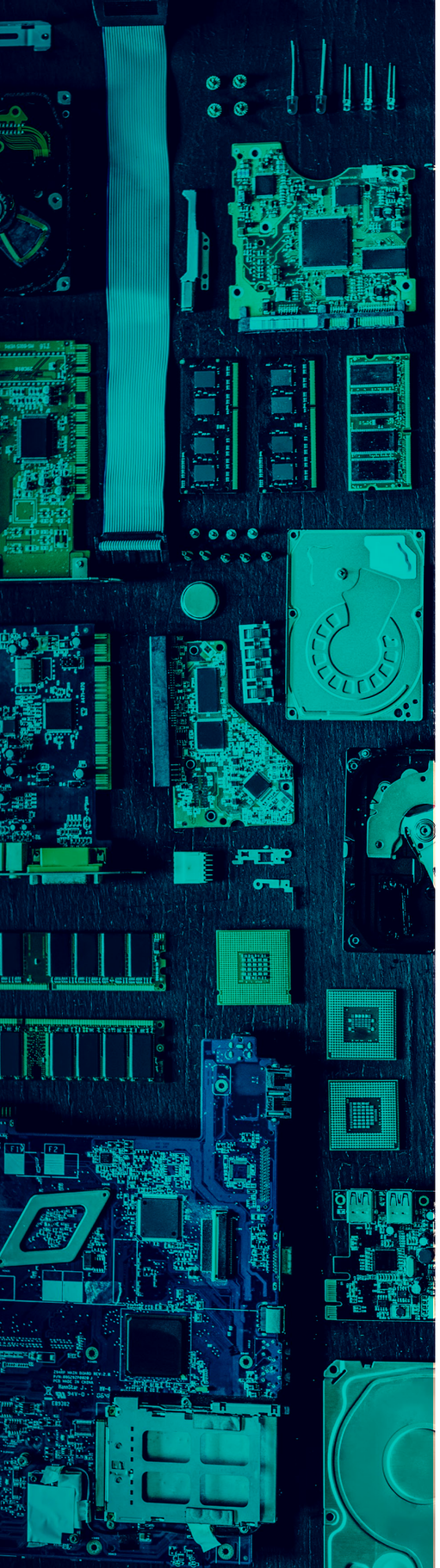
Open RAN represents a giant step forward in Radio Access Network (RAN) evolution. It constitutes a radical transformation of the RAN technology, from the design stage to the complete operation of the network. The whole radio ecosystem is evolving in this direction by giving rise to a richer landscape of vendor partners, and network operators are also evolving to encompass such transformation.

Telefónica believes that mobile networks are evolving towards an Open RAN virtualised model, built on off-the-shelf hardware and cloud-based software in a multivendor environment with open interfaces between network elements. This new architecture will have a significant impact on the telecoms industry. It will allow the entry and disruption of new entrants, enable faster software innovation, allow more network flexibility, and facilitate network exposure to third-party Multi-access Edge Computing (MEC) applications through open Application Programming Interfaces (APIs).

5G can strongly benefit from the introduction of the open network paradigm. Current RAN providers and many smaller suppliers are putting strong efforts in developing Open RAN efficient and innovative hardware and software. However, Telefónica is a firm believer that operators are the ones who must really pave the way in this endeavor. Operators should clearly set the needs and take the leadership in Open RAN development, testing, integration, rollout, and end-to-end operation. That is why Telefónica has been an early adopter and is playing a very active role in open networks.Telefónica is writing a new chapter in RAN history by leading this transformation among the traditional network operators. Other disruptive 5G operators, like Dish, Rakuten, and Reliance Jio, are already challenging their peers in the countries where they operate. Traditional cable and satellite content providers are also acquiring spectrum and becoming operators. The result is a new dynamic RAN economy in which operators, software suppliers, IT and radio hardware vendors, and system integrators will take part.

Open RAN technology is already gaining momentum. The transition from the lab to a technically demanding dense urban scenario is being aided by the works in industrial associations like the O-RAN Alliance, the Open RAN Policy Coalition, the Telecom Infra Project (TIP), the GSMA, the Broadband Forum or the Open RAN G4, to name a few. Open RAN is also part of the agenda of the European Commission to be incorporated in the next Joint Undertaking program of public/private partnerships to foster network research. All public and private stakeholders recognize the strategic importance of streamlining the adoption of Open RAN in all the relevant markets.







This paper provides an overview of the main technology elements that Telefónica is developing in collaboration with selected partners in the Open RAN ecosystem. It describes the architectural elements, design criteria, technology choices and key chipsets employed to build a complete portfolio of radio units and baseband equipment capable of a full 4G/5G RAN rollout in any market of interest.

The remaining sections in this paper are structured as follows. Section 2 summarizes the main site types found in most 4G/5G deployments, that constitute the basis for the targeted configurations of the DU and RRU. Section 3 highlights the DU design details, with strong emphasis on the case where the DU is physically located at the site. Section 4 illustrates key design considerations for remote radio units and active antenna units. Section 5 describes the elements of a Telco cloud architecture that comprises the CU and the virtualization environment. Section 6 is devoted to the site integration aspects in a fully-fledged 2G/3G/4G/5G network, and finally Section 7 is devoted to the conclusions.



# 2. Targeted 4G/5G sites based on Telefónica needs

Sites within Telefónica footprint can be broadly classified into four types, from low/medium capacity 4G to high/dense capacity 4G+5G, as illustrated in Figure 1. Each of those types correspond to a particular arrangement of DUs and RRUs whose design and dimensioning represents a key milestone that must be achieved prior to any further development. Representative frequency bands are just shown for illustration purposes, as well the number of cells that can be typically found in each site type.

In all cases, dimensioning must ensure that Open RAN fulfils all **4G/5G essential features** including massive MIMO, Dynamic Spectrum Sharing (DSS), NB-IoT or RAN sharing (to name a few), while complying with an extensive list of **Key Performance Indicators (KPIs)** aimed to verify that performance is on par with traditional RAN.

| | Low/Medium capacity 4G | High/Dense capacity 4G | Medium capacity 4G+5G | High/Dense capacity 4G+5G |
|---|---|---|---|---|
| **Environment** | Rural/Suburban | Urban/Dense urban | Urban | Urban/Dense urban |
| **Frequency bands** | Low bands (B8/B20/B28)<br>Mid bands (B1/B3/B7/B40) | Low bands (B8/B20/B28)<br>Mid bands (B1/B3/B7/B40) | Low bands (B8/B20/B28)<br>Mid bands (B1/B3/B7/B40)<br>Band C | Low bands (B8/B20/B28)<br>Mid bands (B1/B3/B7/B40)<br>Band C |
| **N° cells** | Up to 15 | Up to 18 | Up to 15 + 3 (5G) | Up to 18 + 3 (5G) |
| | 3-9 RRUs<br>RRU RRU RRU<br>DU | 3-9 RRUs 3-6 RRUs<br>RRU RRU RRU RRU RRU<br>DU DU | 3-9RRUs 3 AAU/RRUs<br>RRU RRU RRU RRU RRU<br>DU DU | 3-9 RRUs 3-6 RRUs 3 AAU/RRUs<br>RRU RRU RRU RRU RRU RRU<br>DU DU DU |

RRU: Remote Radio Unit DU: Distributed Unit

Figure 1: Types of sites typically found in 4G/5G RAN deployments.

The present paper describes the main design considerations of the key Open RAN hardware elements that Telefónica, in collaboration with key technology partners, has developed to be prepared for deployments of full-fledged 4G/5G networks based in Open RAN.

# 3. DU design details

3GPP defined a new architectural model in Release 15, where the gNB is logically split into three entities denoted as CU, DU and RRU. The RAN functions that correspond to each of the three entities are determined by the so-called **split points**. After a thorough analysis of the potential split options, 3GPP decided to focus on just two split points: so-called **split 2** and **split 7,** although, only the former one was finally standardized. The resulting partitioning of network functions is shown in Figure 2.

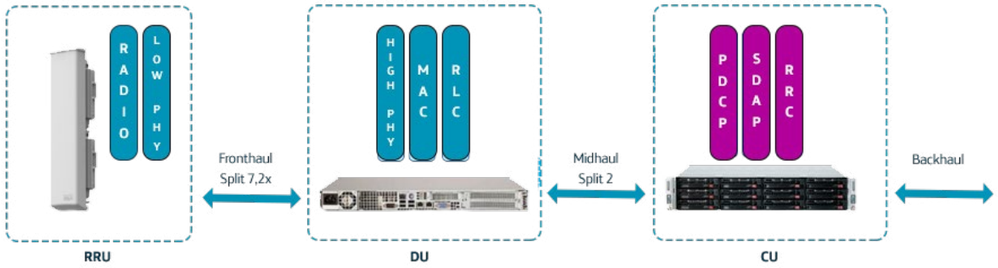



Figure 2: 3GPP split 2 and split 7 architecture.

The CU (Centralized Unit) hosts the RAN functions above split 2; the DU (Distributed Unit) runs those below split 2 and above **split 7**; and the RRU hosts the functions below split 7 as well as all the RF processing.

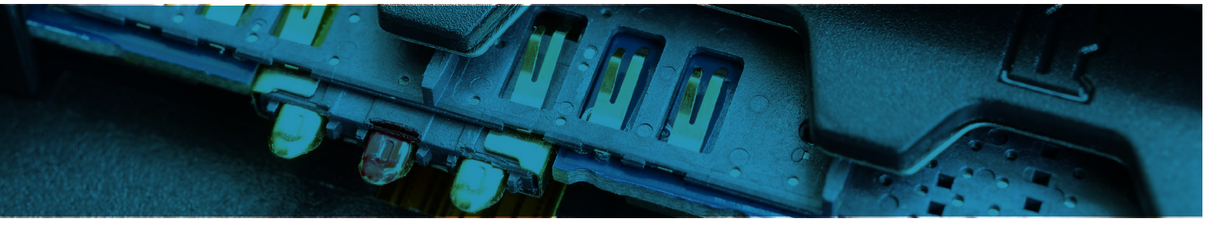
The O-RAN Alliance further specified a **multi-vendor fronthaul interface** between the RRU and DU, by introducing a specific category of split 7 called split 7-2x, whose control, data, management, and synchronization planes are perfectly defined. The midhaul interface between CU and DU is also specified by 3GPP and further upgraded by the O-RAN Alliance to work in multi-vendor scenarios.

The CU and DU can be co-located with the RRU (Remote Radio Unit) in purely distributed scenarios. However, the real benefit of the split architecture comes from the possibility to **centralize** the CU, and sometimes also the DU, in suitable data centers where all RAN functions can be fully virtualized and therefore run on suitable servers.

The infrastructure needed to build a DU is nothing else than a **server** based on **Intel Architecture** optimized to run those real-time RAN functions located below split 2, and to connect with the RRUs through a **fronthaul interface** based on O-RAN split 7-2x. It is the real-time nature of the DU which motivates the need to optimize the servers required to run DU workloads.

The DU hardware includes the chassis platform, mother board, peripheral devices, power supply and cooling devices.

When the DU must be physically located inside a cabinet, the chassis platform must meet significant mechanical restrictions like a given DU depth, maximum operating temperature, or full front access, among others. The mother board contains processing unit, memory, the internal I/O interfaces, and external connection ports. The DU design must also contain suitable expansion ports for hardware acceleration. Other hardware functional components include the hardware and system debugging interfaces, and the board management controller, just to name a few. Figure 3 shows a functional diagram of the DU as designed by Supermicro.







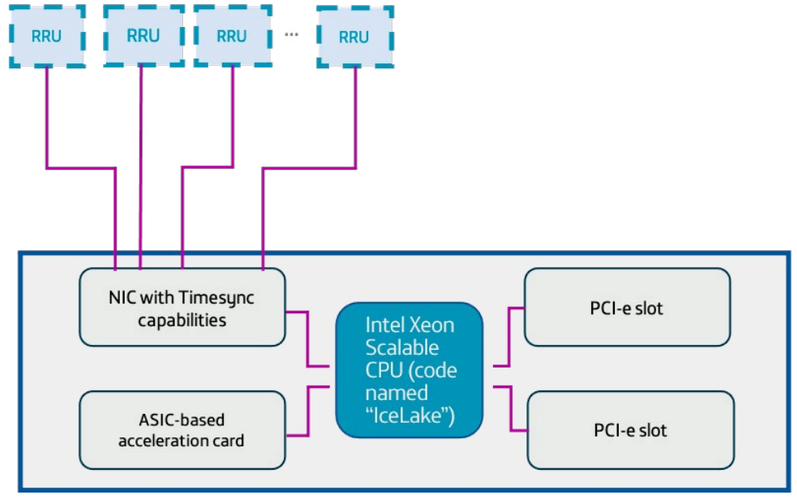



Figure 3: Example of main components that can be identified in an Open RAN DU server.

In the example shown above, the Central Processing Unit (CPU) is an Intel Xeon SP system that performs the main baseband processing tasks. To make the processing more efficient, an ASIC-based acceleration card, like Intel's ACC100, can be used to assist with the baseband workload processing. The Intel-based network cards (NICs) with Time Sync capabilities can be used for both fronthaul and midhaul interfaces, with suitable clock circuits that provide the unit with the clock signals required by digital processing tasks. PCI-e slots are standard expansion slots for additional peripheral and auxiliary cards. Other essential components not shown in the figure are random-access memory (RAM) for temporary storage of data, flash memory for codes and logs, and hard disk devices for persistent storage of data even when the unit is powered-off.
In what follows we describe in more detail the main characteristics of the key elements that comprise the DU.

### 3.1. Central Processing Unit (CPU)

To provide the DU with the best possible capacity and processing power, 3rd Generation Intel Xeon Scalable Processor **Ice Lake** is employed to benefit from the latest improvements in I/O, memory, storage, and network technologies.

Intel Xeon Scalable processors comprise a range of CPU variants (called SKUs) with different core counts and clock frequency that can support from low-capacity deployments (for rural scenarios) to higher capacity deployments (for dense urban) such as massive MIMO.

Intel Ice Lake CPU features, among other improvements, Intel Advanced Vector Extensions 512 (Intel AVX-512) and up to 2 Fused Multiply Add (FMA) instructions which boosts performance for the most demanding computational tasks[1] .

[1] https://www.intel.com/content/www/us/en/products/docs/processors/xeon/3rd-gen-xeon-scalable-processors-brief.html

### 3.2. Hardware Acceleration Card

One of the most compute-intensive 4G and 5G workloads is RAN layer 1 (L1) **forward error correction (FEC)**, which resolves data transmission errors over unreliable or noisy communication channels. FEC technology detects and corrects a limited number of errors in 4G or 5G data without the need for retransmission. FEC is a very standard processing function that is not differentiated across vendor implementations.

FEC has been typically implemented on Field Programmable Gate Arrays (FPGA) accelerator cards, like the Intel PAC N3000. However, recent accelerator cards feature a low-cost, power efficient, acceleration solution for vRAN deployments based on Intel eASIC technology, called the Intel vRAN Dedicated Accelerator ACC100.

Intel eASIC™ devices are **structured ASICs**, an intermediate technology between FPGAs and standard Application-Specific Integrated Circuits (ASICs). These devices provide lower unit-cost and lower power compared to FPGAs and faster time to market and lower non-recurring engineering cost compared to standard- ASICs. Both accelerator options connect to the server processor via a standard PCIe Gen 3 x16 interface.

Silicom's FEC Accelerator Card "Pomona Lake" utilizes Intel ACC100 dedicated accelerator to perform forward error correction (FEC) processing in real time, thus offloading such intensive task from the CPU in the host server. The ACC100 implements the Low-Density Parity Check (LDPC) FEC for 5G and Turbo FEC for 4G and supports both concurrently. The ACC100 supports the O-RAN adopted DPDK BBDev API - an API which Intel contributed to the opensource community for FEC acceleration solutions.

Intel has invested heavily in a reference software architecture called **FlexRAN** to accelerate RAN transformation. FlexRAN contains optimized libraries for LTE and for 5G NR Layer 1 workload acceleration including optimizations for massive MIMO. The FlexRAN reference software enables customers to take a cloud native approach in implementing their software utilizing containers.

As illustrated in Figure 4, the FlexRAN software reference architecture supports the ACC100 which enables users to quickly evaluate and build platforms for the wide range of vRAN networks.

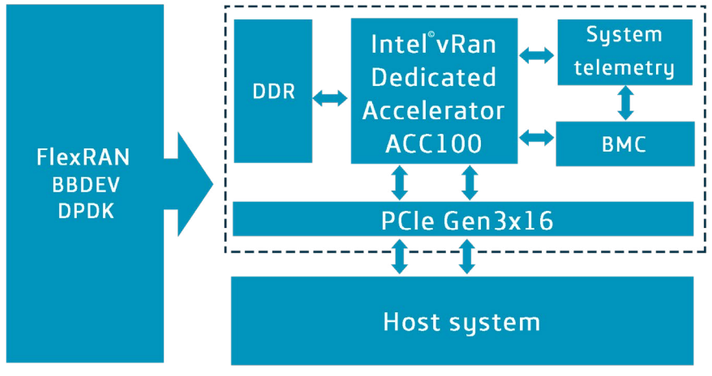



Figure 4: Integration of Silicom's Hardware Acceleration Card ACC100 into a FlexRAN-based system platform.





### 3.3. Time, Phase and Frequency Synchronization

Open RAN solutions rely on stringent **time synchronization** requirements for end-to-end latency and jitter. Timing synchronization has become a critical capability and now is fully available on COTS hardware using specific NICs with time synchronization support.

5G requires support of time synchronization accuracy across the whole network below 3 microseconds for Time-Division Duplex (TDD) carriers, and even more stringent when using MIMO or Carrier Aggregation. Contrary to non-Open RAN technologies, Frequency Division Duplex (FDD) carriers also require stringent synchronization to sustain eCPRI-based fronthaul interface.

To ensure this level of precision on COTS hardware, **network-based synchronization** protocols like Synchronous Ethernet (SyncE) and IEEE 1588v2 Precision Time Protocol (PTP) are key to ensure synchronization at the physical layer. This will be even more essential as moving to higher frequency radio spectrums like millimeter wave (mmWave) with large MIMO antenna configurations.

In addition, synchronization based on **Global Navigation Satellite Systems (GNSS)** like GPS, Galileo, Glonass or Beidou can provide essential time and phase references in those cases where network-based synchronization is not available, or as a back-up in case of network timing failure.

Open RAN DUs should be prepared for both GNSS and network synchronization when integrating them into a 4G/5G site.

### 3.4. Time Sync NIC Card

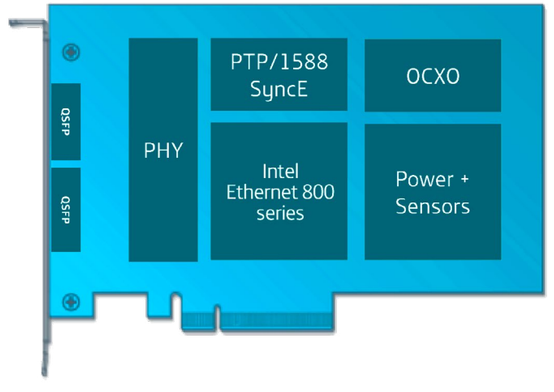
The ORAN fronthaul interface between the DU and the Radio Unit relies on the standard Ethernet protocol to enable multi-vendor interoperability between DUs and radio units.

**Network Interface Cards (NICs)** are standard elements in COTS hardware. As an example, the Intel Ethernet 800 Series card (also known as Columbiaville NIC) supports multiple port speeds (from 100 Mb/s to 100 Gb/s in Intel's E810) with a single architecture, to meet a range of fronthaul/midhaul/backhaul requirements for the transport network that makes it suitable for Enterprise, Cloud, and Telco applications.

Enhancing NICs with support of time synchronization is however essential to make NICs usable in Open RAN DUs. These cards are usually called **Time Sync NICs** (Figure 5).

Silicom design a family of NICs (called STS) for Time Synchronization services in 4 ports, 8 ports and 12 ports configurations including support for PTP and SyncE, suitable for the site types shown in Figure 1.

Figure 5: Internal architecture of a Time Sync NIC card based on Intel Ethernet 800 series.



As shown in Figure 6, Time Sync NICs allow removal of the fronthaul switch between the RU and DU, thus saving costs and reducing network complexity. Time Sync NICs can provide an accurate Clock to multiple Radio Units and at the same time recover the clock from the midhaul.

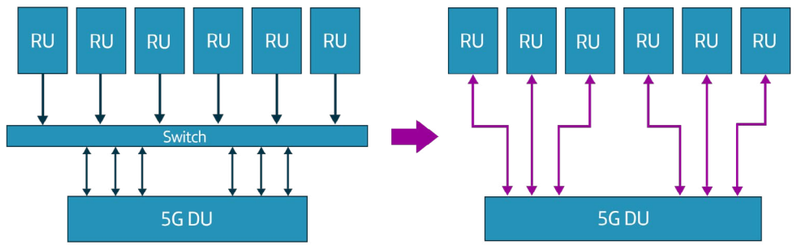



Figure 6: While former Open RAN implementations rely on fronthaul switches for connection of RUs to the DU, Time-Sync NIC cards allow direct connection for improved reliability.

Key features supported by Silicom Time Sync (STS) NICs include:

- T-TC Transparent Clock /G.8273.3
- T-BC/T-TSC Boundary Clock and TSC Slave Clock /G.8273.2
- T-GM Grand Master /G.8273.1 per G.8275.1 PTP Profile
- PRTC Primary Reference Time Clock Class B/G.8272
- OC Own Clock (Master / Slave) – Class C (Stratum 3e)
- 1588/PTP over IPv4 / IPV6, IEEE1588v2
- SyncE /G.8262
- BMCA - Best Master Clock Algorithm (OCXO, SyncE, GNSS, 1588)
- Support for ≥4 Hours Hold Over TIE @1.5uSeconds

### 3.5. Memory Channel Interfaces

As in any other server based on Intel Architecture, memory components are a standard element that must be incorporated and properly dimensioned. An example of system memory capacity, type and related information that Supermicro recommends for an Open RAN application is described in the following table.

Table 1: Memory Channel Feature List

| Item Name | Description |
|---|---|
| Memory Types | DDR4 |
| Supported Memory | 2933MHz up to 2TB |





### 3.6. External Interface Ports

The DU must be equipped with enough external ports to enable proper interfacing with hard drives, PCIe cards, Ethernet ports, and other peripherals. Below is a table with some of the main external interface ports that the DUs should have for an Open RAN application, according to Supermicro.

Table 2: External Port List

| Port Name | Feature Description |
|---|---|
| Ethernet | Dedicated IPMI Ethernet connector |
| | 10GbE Base-T Ethernet connectors |
| | 1GbE Based-T Ethernet connectors |
| PCIe | PCIe x16 slots |
| SATA | SATA 3.0 ports |
| USB | USB 3.0 ports, USB 2.0 ports |
| VGA | VGA port |
| Serial Port | COM port |

# 4. RRU design details

### 4.1. Remote Radio Unit Reference Architecture

An Open RAN Remote Radio Unit (RRU) is used to convert radio signals sent to and from the antenna into a digital baseband signal, which can be connected to the DU over the O-RAN split 7-2x fronthaul interface.

For illustration, the reference architecture of an Open RAN RRU from Gigatera Communications is shown in Figure 7. It shows the functional high-level diagram of the RRU containing the following components:

- Synchronization and Fronthaul Transport Functional Block
- Lower PHY Layer Baseband Processing Functional Block
- Digital Front End (DFE) Functional Block
- RF Front End (RFFE) Functional Block

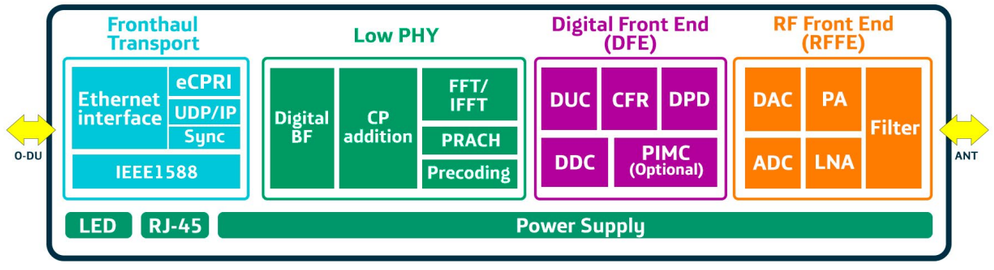



Figure 7: Reference architecture of an Open RAN RRU.

In what follows we describe the above main components of an Open RAN RRU. All the components in Figure 7 can be implemented in one or several FPGAs with the exception of the PA, LNA and Filter elements, as explained below.

#### 4.1.1. Synchronization and Fronthaul Transport Function Block

The PTP synchronization module is aimed to extract the main timing signal from the eCPRI fronthaul interface. PTP provides accurate time and phase references to the RRUs for the transmissions of all sectors to be synchronized with each other. SyncE also provides additional frequency stability, and acts as a backup source of synchronization in case PTP fails. Both PTP and SyncE are generally required and must be provided by the DU through the fronthaul link.

The fronthaul connectivity between RRU and DU is usually realized by means of an optical Ethernet interface with the aid of suitable Small-Form Factor Pluggable (SFP) modules. RRUs are usually equipped with two fronthaul ports to support daisy chain configurations where several radio units can be cascaded to minimize the number of fronthaul links towards the DU. The presence of two fronthaul ports also enables network sharing scenarios, where the same RRU is shared by two different DUs and each DU performs the baseband functions corresponding to a different operator.

The Fronthaul Transport Function block involves specific processing of data packets to ensure interoperability in a multi-vendor environment. The use of an FPGA-based solution allows the addition of features as O-RAN specifications evolve over time.

#### 4.1.2. Lower PHY Baseband Processing

The lower PHY layer processing includes blocks for performing Fast Fourier Transform (FFT)/ Inverse Fast Fourier Transform (iFFT), Cyclic Prefix addition and removal, Physical Random Access Channel (PRACH) filtering, and digital beamforming.

Beamforming is only required in Active Antenna Units (AAUs), where antennas are integrated as part of the RRU (as in massive MIMO).

#### 4.1.3. Digital Front End (DFE)

The digital front end comprises specialized blocks for the transmit (TX) and receive (RX) paths.

The TX path contains a spectrum shaping filter and a Digital Upconverter (DUC) towards the desired carrier frequency. In addition, it contains two fundamental blocks: Digital Pre-Distortion (DPD), and Crest Factor Reduction (CFR) which are provided by Xilinx and integrated by Gigatera.

CFR reduces the Peak-to-Average Ratio (PAR) of the 4G/5G signals by clipping those peaks that create highest distortion. DPD compensates the Power Amplifier (PA) distortion in RFFE to improve the RF linearity. Both CFR and DPD improve the energy efficiency of the RRU. Minimization of the PA power consumption is a source of continuous improvement and innovation because PAs represent a large fraction of the overall power consumption in the RAN. An adaptable FPGA-based solution enables customization for a range of PA output power requirements and technologies.

When digital beamforming is implemented, a beamforming calibration function in either time domain or frequency domain is also implemented.

The RX path contains a Digital Downconverter (DDC), a Low-Noise Amplifier (LNA) and an optional PIMC (Passive Inter-Modulation Canceller). PIMC aims to compensate the interference appearing on the RX path that is generated by passive intermodulation distortion caused by high-





power signals in FDD.

#### 4.1.4. RF Front End (RFFE)

The RF Front End comprises Power Amplifiers (PA), Low Noise Amplifiers (LNA), Digital to Analog Converters (DAC), and Analog to Digital Converters (ADC). Some of the latest RFSoC (RF System on Chip) devices, like Zynq RFSoC, integrate direct RF sampling Data Converters based on CMOS technology with improved power consumption [5].

The integrated RF DACs and RF ADCs perform direct RF sampling of the carrier signal instead of Intermediate Frequency (IF) sampling, thus avoiding analog up/down Converters. As a result, RRUs can have reduced sizes thus enabling dual/triple band Radios in single mechanical enclosure.

Active Antenna Units (AAU) also integrate suitable antenna arrays and bandpass filters in the same enclosure.

### 4.2. FPGA selection criteria for the RRU

Field Programmable Gate Arrays (FPGAs) from Xilinx in the RRU not only perform digital processing tasks but can also integrate some of the analog subsystems. Xilinx has integrated mixed analog-digital subsystems (including DACs and ADCs) into its RFSoC device family. This is the case of the Zynq® UltraScale+ RFSoC™ family from Xilinx used in the RRUs.

The need for wider bandwidths in the radio unit (RU) is not just about increasing data rates and performance, but also to support more complex and diverse radio configurations as needed for existing and new bands. The sheer number of global bands would be unmanageable if each required a unique radio. Radios are designed to support the widest possible bandwidth and seemingly random carrier configurations to meet these requirements. Early 5G radios supported bandwidths up to 200MHz, but future bandwidths up to 400MHz are being requested. These radios support multiple bands and hence are called multi-band. In some cases, vendors use multiple Power Amplifiers (PAs) to cover multiple bands; in other cases, advanced wideband Gallium Nitride (GaN) PAs are used, requiring state of the art wide-band DPD. Zynq UltraScale+ RFSoC family is designed for this purpose.

RFSoC devices integrate, in addition to an FPGA for digital processing, a fully hardened digital front-end (DFE) subsystem with all required processing blocks, and direct RF sampling ADC and ADC converters thus eliminating power-hungry JESD204 interface. A hardened DFE is equivalent to having an ASIC-based DFE embedded in the RFSoC with an optimized mix of programmability and ASIC functions. The benefit is a significant reduction in total power, board area, and complexity of the radio solution. This is most apparent in 64T64R massive MIMO AAUs.

State-of-the-art Xilinx Zynq RFSoC DFE devices will support up to 7.125 GHz of analog RF bandwidth in 2021.

### 4.3. O-RAN Fronthaul interface

The O-RAN Alliance has defined a multi-vendor fronthaul interface between DU and RRU based on Split 7-2x. In O-RAN terminology, RRU is denoted as O-RU and DU is denoted as O-DU.

The fronthaul specifications include Control, User and Synchronization (CUS) & Management (M) plane protocols, as indicated in Figure 8, whose elements can be summarized here:

· **Control Plane (C-Plane)** data between the O-DU and O-RU, such as data section information, scheduling information, beamforming information, etc.

· **User Plane (U-Plane)** data based on frequency-domain IQ samples.

· **Synchronization Plane (S-Plane)** including timing and synchronization information.

· **Management Plane (M-Plane)** enabling initialization, configuration, and management of the O-RU through suitable management and control commands between O-DU and O-RU.

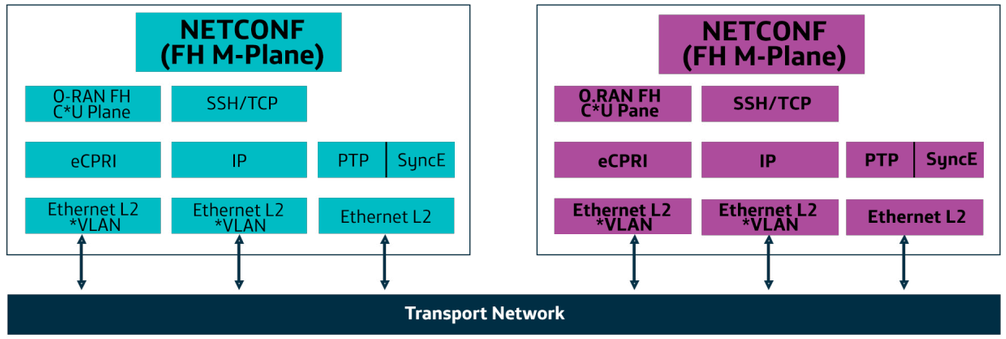



Figure 8: O-RAN Fronthaul interface protocol structure

For a complete description of O-RAN protocol structure, refer to [1]-[4].

### 4.3.1. IOT Fronthaul profiles

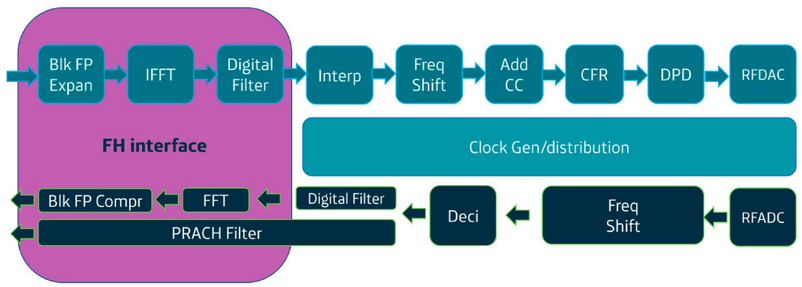
Unambiguous separation of the C-Plane, U-Plane, S-Plane and M-Plane protocol and functions enables stepwise integration of the fronthaul interface between O-DU and O-RU in a multivendor environment.

Additionally, O-RAN Alliance facilitates such multi-vendor integration by defining suitable **inter-operability (IOT) profiles**, test configurations and test cases in a non-intrusive manner, so that the 3GPP-related radio conformance testing remains independent from the O-RAN fronthaul testing. The IOT profiles describe the typical set of parameters, transport characteristics, synchronization topologies, and security considerations required for a complete conformance testing.

### 4.3.2. Implementation of O-RAN Fronthaul in an O-RU

Figure 9 illustrates the basic block diagram of the processing blocks devoted to the fronthaul interface at the O-RU. All the functions take place in the FPGA including synchronization (hardware timestamping, SyncE and PTP) and application-layer framing/de-framing.

Figure 9: Functional basic block diagram of fronthaul interface in O-RU.








Based on O-RAN split 7-2x, an RRU can be configured to operate in two different modes, denoted as "Category A" and "Category B" depending on the functionality of both the RRU and DU. Depending on these modes and on the configuration parameters allowed by O-RAN, a split 7-2x can actually correspond to three different split points (namely split 7-1, 7-2 and 7-3) depending on the configuration chosen.

#### 4.3.2.1. O-RU "Category A"

In this case the precoding function is performed at the O-DU, thus allowing for **simpler RRU design**. This is equivalent to a split 7-1 in O-RAN terminology [6].

Precoding converts so-called spatial layers into spatial streams, which can require higher fronthaul throughput in massive MIMO systems. As a result, **O-RUs Category A are typical for non-massive MIMO implementations**, where the difference between performing the precoding function at the O-DU or at the O-RU is minimal. However, O-RUs Category B are better suited for massive MIMO AAUs.

Figure 10 shows the Downlink signal processing for O-RUs Category A.

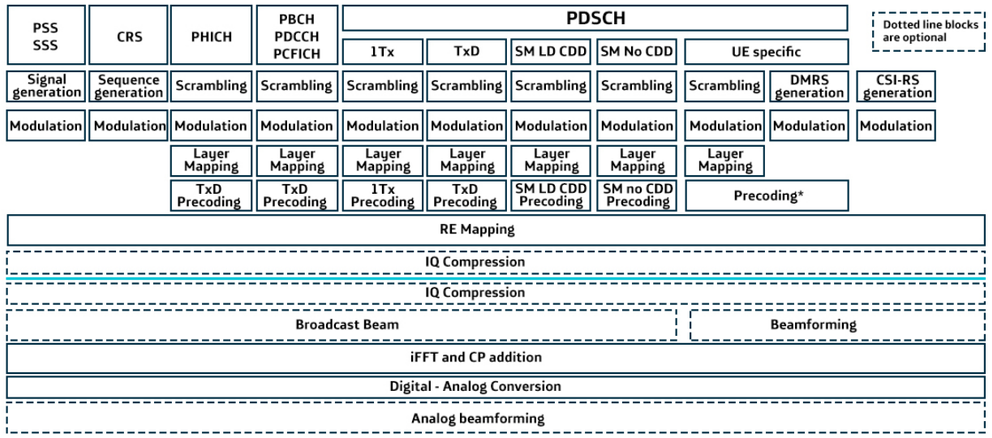



Figure 10: O-RU "Category A". Blocks above the O-RAN FH line are executed at the O-DU, whereas those below it are executed at the O-RU.

#### 4.3.2.2. O-RU "Category B"

In this case the precoding function is performed at the O-RU, hence making the radio more complex but also **reducing fronthaul bitrate in massive MIMO implementations**.

This category allows so-called "Modulation Compression", which can be performed in the downlink to effectively send only the bits equivalent to the constellation points of the complex IQ signals, hence reducing the downlink fronthaul throughput effectively. This is equivalent to a split 7-3 in O-RAN terminology [6].

Figure 11 shows the Downlink signal processing for O-RUs Category B.

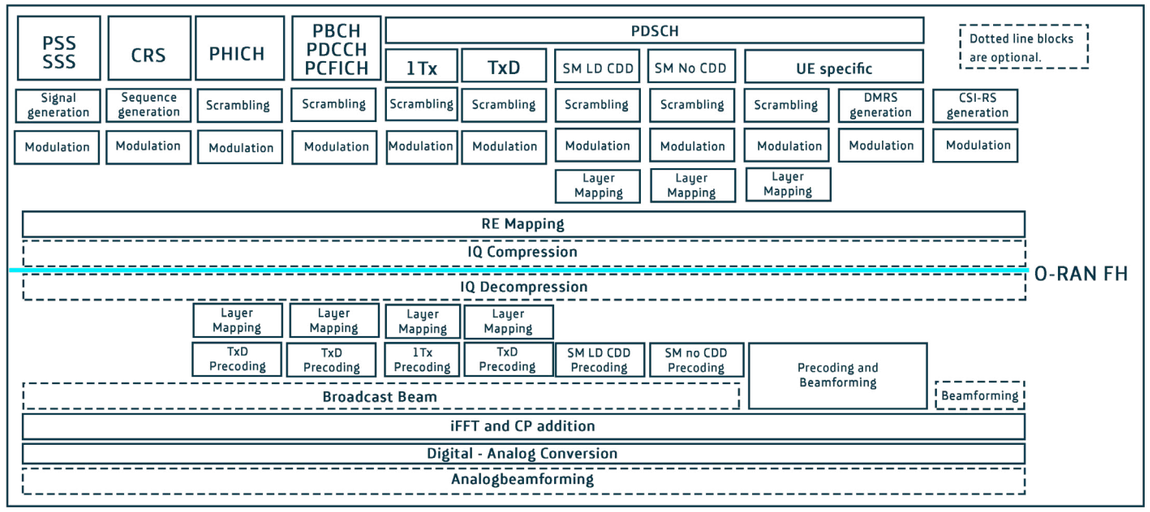



Figure 11: O-RU "Category B". Blocks above the O-RAN FH line are executed at the O-DU, whereas those below it are executed at the O-RU.





### 4.4. Radio units for 4G/5G low and mid bands (up to 3.5 GHz)

Table 3 and Table 4 contain as a reference the radio configurations required for proper 4G/5G Open RAN deployments in the most typical scenarios of Telefonica footprint.

| Item | Tri band B8/B20/B28 | Dual Band B1/B3 | B40 | B7 | B3 | B28 (APT) |
|---|---|---|---|---|---|---|
| Frequency band (MHz) | B8: DL 925-960, UL 880-915<br>B20: DL 791-821, UL 832-862<br>B28: DL 758-788, UL 703-733 | B1: DL 2110-2170, UL 1920-1980<br>B3: DL 1805-1880, UL 1710-1785 | 2350- 2390 | DL 2620-2690<br>UL 2500-2570 | DL 1805-1880<br>UL 1710-1785 | DL 758-803<br>UL 703-748 |
| Technology | 4G, 5G NR, (support Concurrent mode) | | | | | |
| Max output power | 2x40 W each band | 4x40 W each band | 4x40 W | 4x40 W | 4x40 W | 2x40 W |
| ORAN fronthaul interface | ORAN 7-2x | | | | | |
| Optical ports | 2 x 10GE eCPRI | | | | | |
| #TX/#RX | 2T4R each band | 4T4R | 4T4R, TDD | 4T4R, FDD | 4T4R, FDD | 2T2R, FDD |
| Antenna port | 4 | 4 | 4 | 4 | 4 | 2 |
| Cooling | Natural convection | | | | | |
| IP | 65 | | | | | |
| Temperature range | -40°C to 55°C | | | | | |
| DC Input Power | -37 to -57 VDC, Nominal -48V DC (with reverse polarity protection) | | | | | |

Table 3: Radio units for 4G/5G low bands (below 3 GHz)

| Item | 8T8R | 32TRX mMIMO | 64TRX mMIMO |
|---|---|---|---|
| Frequency band (MHz) | Variant 1 : n78 TDD (3400-3600 MHz)<br>Variant 2 : n78 TDD (3600-3800 MHz) | n78 TDD (3400-3800 MHz) | n78 TDD (3400-3800 MHz) |
| Technology | 5G NR | 5G NR | 5G NR |
| Max output power (W) | 8x40W | 100W | 200W |
| EIRP | NA | 74 dBm | 77 dBm |
| ORAN interface | ORAN 7.2x | | |
| Optical ports | 2 x 25GE eCPRI | | |
| #TX/#RX | 8T8R | 32T32R | 64T64R |
| Cooling | Natural convection | | |
| IP | 65 | | |
| Temperature range | -40°C to 55°C | | |
| DC Input Power | -37 to -57 VDC, Nominal -48VDC (with reverse polarity protection) | | |

Table 4: Radio Units for 5G mid band (3.5 GHz)

# 5. Cloud Architecture

## 5.1. Open RAN virtualized solution

The Open RAN solution follows a **fully cloudified** network design. The CU and DU, as well as the Element Management System (EMS) managing the RAN network elements, benefit from a software-defined architecture. Suitable **virtual instances** of the vCU, vDU and vEMS can be deployed over a scalable cloud-based platform managed by a **Service Management and Orchestration Framework**. This is graphically shown in Figure 12 as implemented by Altiostar.

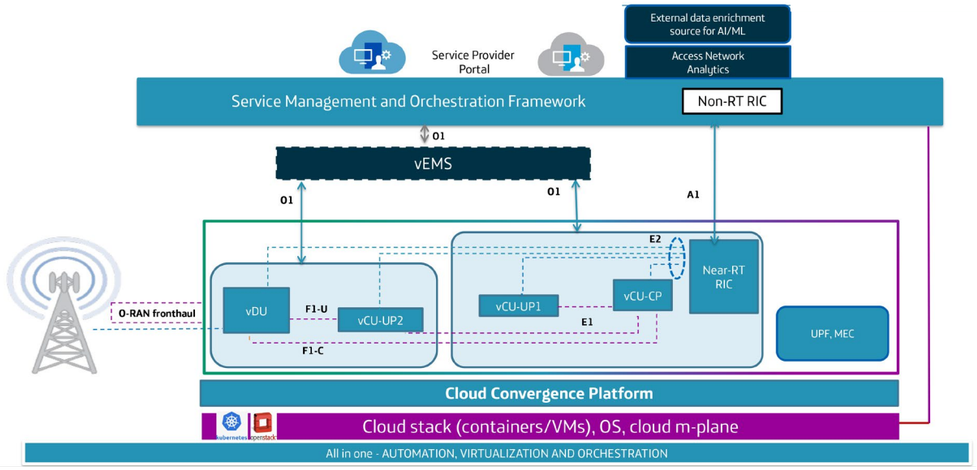



Figure 12: Illustration of a Telco Cloud Open RAN architecture.

The service management framework also allows the introduction of the **RAN Intelligent Controller (RIC)**, whose near-Real Time (Near-RT RIC) and Non-Real Time (Non-RT RIC) components are being defined in the O-RAN alliance with the goal of **optimizing RAN behavior** and **interfacing with third-party applications**.

The ability to run **RAN functions as virtual instances** for 4G and 5G brings the flexibility to deploy the vDU, vCU and vEMS workloads in **different possible locations** depending on implementation needs, as shown in Figure 13. The fronthaul interface follows the O-RAN split 7-2x, whereas the midhaul interface between the DU and the CU (called F1 for 5G, and W1 for 4G) is based on 3GPP specifications. The vCU functions are further split into UP (User Plane) and CP (Control Plane), according to 3GPP/O-RAN.





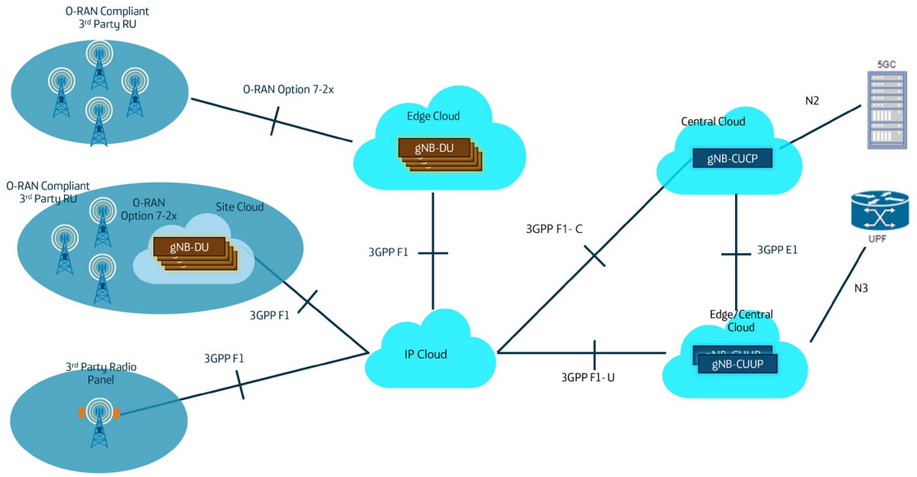



Figure 13: Schematic illustration of the main interfaces and network elements in a 5G Open vRAN architecture.

The Telco Cloud Open RAN concept can be taken one step further by implementing a **container-based cloud-native micro-service architecture**. This new architecture enables advanced cloud-based networks supporting new applications and services with advanced **automation**, newer algorithms and improved Quality of Experience (QoE), while ensuring **network slicing** and full support of Control/User-Plane Separation (CUPS). This is the means to achieve the true promise of a service-based architecture for 5G.

Altiostar's container-based 5G solution further disaggregates CUs and DUs into **micro-services** comprising transport, management, monitoring, control plane and user plane functions. Depending on the type of network slice and application being deployed, **containerized network functions** can be rapidly deployed at various locations in a very light footprint and then scaled up based on traffic.

## 5.2. vCU and vEMS

The two main virtualized elements of the Telco Cloud architecture in Open RAN technology are the vCU and the vEMS.

The vCU performs the CU functions of PDCP and RRC sublayers on an Intel Xeon server platform. Contrary to the vDU, vCU involves only higher-layer functions and can therefore fully rely on standard COTS hardware without Time Sync NICs as long as the PTP Primary Reference Timing Clock (PRTC) sits between the DU and the CU.

The role of the vEMS is to gather information with the right granularity from the different software modules to control and operate them in an automated way as commanded by the OSS.

As an example, Altiostar's vEMS is a Virtual Network Function (VNF) working on Intel Architecture-based COTS servers, running kernel-based virtual machine (KVM) and managed by OpenStack Virtual Infrastructure Management (VIM) software. It includes a set of applications for delivering Element Management System solutions like FCAPS (Fault, Configuration, Accounting, Performance and Security), 3GPP IRP (Integration Reference Point) for OSS integration, and

scripting support. The Altiostar vEMS can also be flexibly deployed as a set of containerized network functions to meet evolving 5G deployment scenarios.

Integration of the vEMS into the Service Management and Orchestration Framework paves the way to the extensive use of **Artificial Intelligence (AI)** and **Machine Learning (ML)** techniques in multiple domains, such as RAN performance enhancement, radio resource management, or advanced traffic/service optimization, to name a few. AI/ML can benefit from the use of **automation** in cloud-based software architectures, thus reducing operational complexity in multi-vendor Open RAN scenarios.

# 6. Site Integration aspects

An Open RAN site may comprise not only a certain number of RRUs and DUs, but also potentially a Cell Site Router (CSR), a GNSS antenna and receiver, and a legacy 2G/3G baseband unit (BBU). Proper interconnection of all these elements is essential to ensure seamless site integration of Open RAN technology in all the site types described in Figure 1.

Figure 14 illustrates a typical arrangement of DUs and RRUs that correspond to the site types in Figure 1, for the case where synchronization is provided by a GNSS receiver. As can be seen, a 4G/5G site can contain up to three Open RAN DUs in the most complex case. The first DU server gets proper time (Time of Day, ToD) and phase (PPS) synchronization from a GNSS receiver, while acting as a Grandmaster clock (T-GM) to the other DUs at the site by means of a daisy-chain configuration. All DUs must be interconnected with each other and to the CSR, but RRUs and AAUs can be directly connected to the DUs thanks to the use of Time Sync NICs.

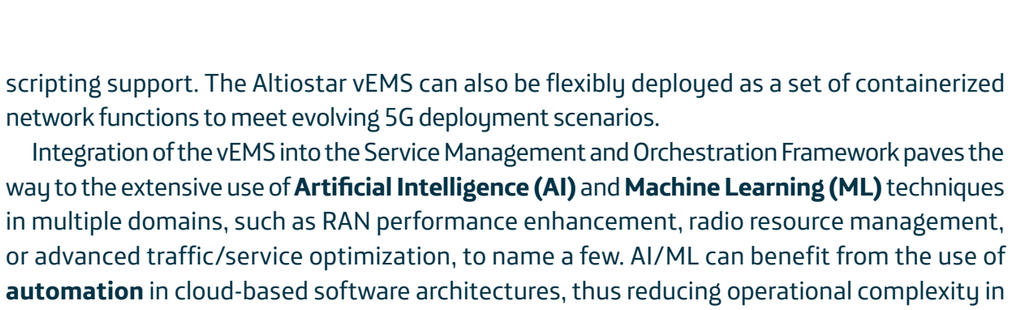



Figure 14: Interconnection of Open RAN DUs for the main four 4G/5G site types, where time and phase references are provided by a GNSS receiver.





Figure 15 illustrates another example where time and phase references are provided by the network in a 2G/3G/4G/5G site. In this case there is no GNSS receiver and the CSR must propagate PTP and SyncE towards the DUs. A legacy 2G/3G BBU is also shown that must be interconnected with the other DUs through the CSR.

Network-based synchronization is deemed as the best and most future-proof option because it avoids potential points of failure, like the GNSS receiver or the daisy-chain connection of DUs to propagate synchronization. However, it requires full network support of PTP and can therefore be applicable only in a limited set of scenarios.

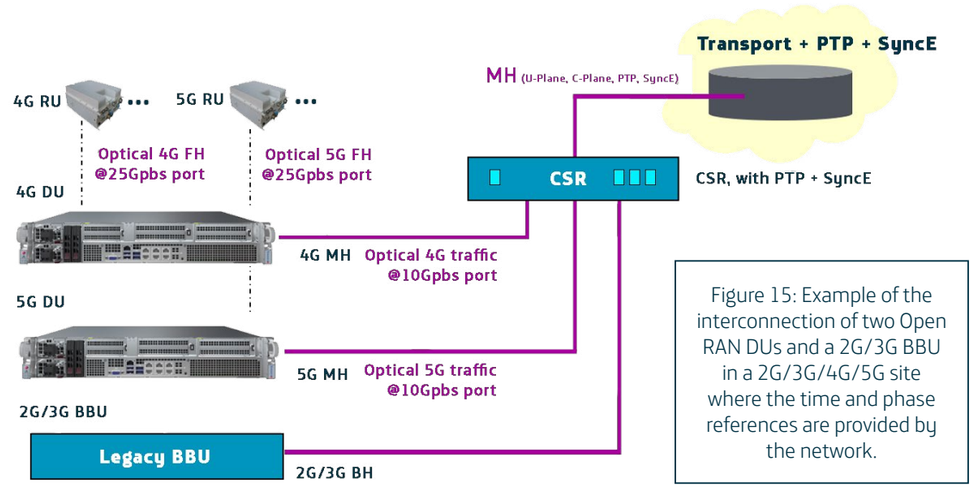



Figure 15: Example of the interconnection of two Open RAN DUs and a 2G/3G BBU in a 2G/3G/4G/5G site where the time and phase references are provided by the network.

# 7. Summary and Conclusions

The goal of this paper was to illustrate, in a technical way, how the main Open RAN network elements can be designed and dimensioned to meet the needs of operators which, like Telefónica, demand a wide portfolio of radio units, site capacities and synchronization options.

Emphasis was put in the case where the DU is physically located at the site, but all the considerations remain equally valid when the DU is centralized, except for possibly different mechanical requirements for the DU chassis as needed in a data center.

The actual portfolio of radio units and frequency bands can of course differ from network to network, but the fundamental considerations in 4G and 5G design described here will remain equally applicable. Site integration aspects are also key to secure seamless coexistence with whatever legacy 2G/3G network equipment is located at the site.

The technology components described in this paper will take Open RAN out of the lab and into a real 4G/5G network. The key steps towards making this transition are already happening in the form of pilots and field activities, whose goal is to test whether performance is on par with the traditional RAN. Such assessment cannot happen without the combined efforts of both Operators and technology partners.

# 8. References

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[2] ORAN-WG4.MP.0-v02 “Management Plane Specification”, O-RAN Allicance, Working Group 4.

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[4] O-RAN-WG4-MP-YANGs-v02.00

[5] Xilinx WP489 “An Adaptable Direct RF-Sampling Solution”, Feb 20, 2019, available for download at: https://www.xilinx.com/support/documentation/white_papers/wp489-rfsampling-solutions.pdf

[6] NGMN White Paper “5G RAN CU – DU Network Architecture, Transport Options and Dimensioning”, V1.0, available for download at: https://www.ngmn.org/wp-content/uploads/Publications/2019/190412_NGMN_RANFSX_D2a_v1.0.pdf





# 9. Glossary

**AAU:** Active Antenna Units

**ADC:** Analog to Digital Converters

**AI:** Artificial Intelligence

**APIs:** Application Programming Interfaces

**ASICs:** Application-Specific Integrated Circuits

**CFR:** Crest Factor Reduction

**CPU:** Central Processing Unit

**CSR:** Cell Site Router

**CU:** Centralized unit

**CUPS:** Control/User-Plane Separation

**DAC:** Digital to Analog Converters

**DDC:** Digital Downconverter

**DFE:** Digital Front End

**DPD:** Digital Pre-Distortion

**DUC:** Digital Upconverter

**DSS:** Dynamic Spectrum Sharing

**DU:** Distributed Unit

**EMS:** Element Management System

**FCAPS:** Fault, Configuration, Accounting, Performance and Security

**FEC:** Forward Error Correction

**FFT:** Fast Fourier Transform

**FMA:** Fused Multiply Add

**FPGA:** Field Programmable Gate Arrays

**gNB:** Next generation Node B

**GNSS:** Global Navigation Satellite Systems

**iFFT:** Inverse Fast Fourier Transform

**I/O:** Input/Output

**KPIs:** Key Performance Indicators

**KVM:** Kernel-based Virtual Machine

**LNA:** Low-Noise Amplifier

**Massive MIMO:** Massive Multiple-Input Multiple-Output

**MEC:** Multi-access Edge Computing

**ML:** Machine Learning

**NB-IoT:** Narrowband-IoT

**NICs:** Network Interface Cards

**PA:** Power Amplifier

**PAR:** Peak-to-Average Ratio

**PIMC:** Passive Inter-Modulation Canceller

**PRACH:** Physical Random Access Channel

**QoE:** Quality of Experience

**RAN:** Radio Access Network

**RAM:** Random-Access Memory

**RFFE:** RF Front End

**RFSoC:** RF System on Chip

**RIC:** RAN Intelligent Controller

**RRU:** Remote Radio Unit

**RX:** Receive

**STS:** Silicom Time Sync

**SyncE:** Synchronous Ethernet

**TDD:** Time-Division Duplex

**TIP:** Telecom Infra Project

**TX:** Transmit

**VIM:** Virtual Infrastructure Management


Telefónica