NATIONAL INSTITUTE FOR NUCLEAR AND HIGH ENERGY PHYSICS

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NIMROD, 16 channel read out driver for the Drift Chambers used in the L3+Cosmics project.

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The NIKHEF MDT read out driver is a VME module that collects data from the TDCs, connected to the Drift Chambers. The data from several MDT chambers is merged and can be read by a VME master

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Erratum:
09-09-1999 draft version 1.0
06-09-2000 draft version 1.1 document change on page 9:

Control & Status Bit Clear Register, address offset = 0x7FFFC

Changed in:

Control & Status Bit Clear Register, address offset = 0x7FFF7

30-10-2000 draft version 1.2 document change on page 11:

Channel Header	0001	1000	0001	000E	0000	Channel ID	

Changed in:

Channel Header	0001	1000	0000	000E	0000	00	Channel ID

1. NIMROD

The NIMROD (NIKHEF MDT Read Out Driver) concentrates the data from a number of TDCs[1] into a single output register. The unit receives trigger and clock from the CTP (Central Trigger Processor) and distributes this to the TDCs. In the L3 + Cosmics project the function of the CTP is fulfilled by the CTT-V2 (Cosmics Trigger and Timing module)[2] and the TDCs are interfaced to the NIMROD on a CPC (Cosmics Personality Card)[3]. A complete NIMROD consists of a set of modules; a NIMROD, a NIMROD_fanout module and four patchpanel boards. The NIMROD is a standard 6U * 160 mm VME module. Several NIMRODs may share a VME crate, controlled by a single master. This controller reads the event data and takes care of various settings in the NIMRODs.

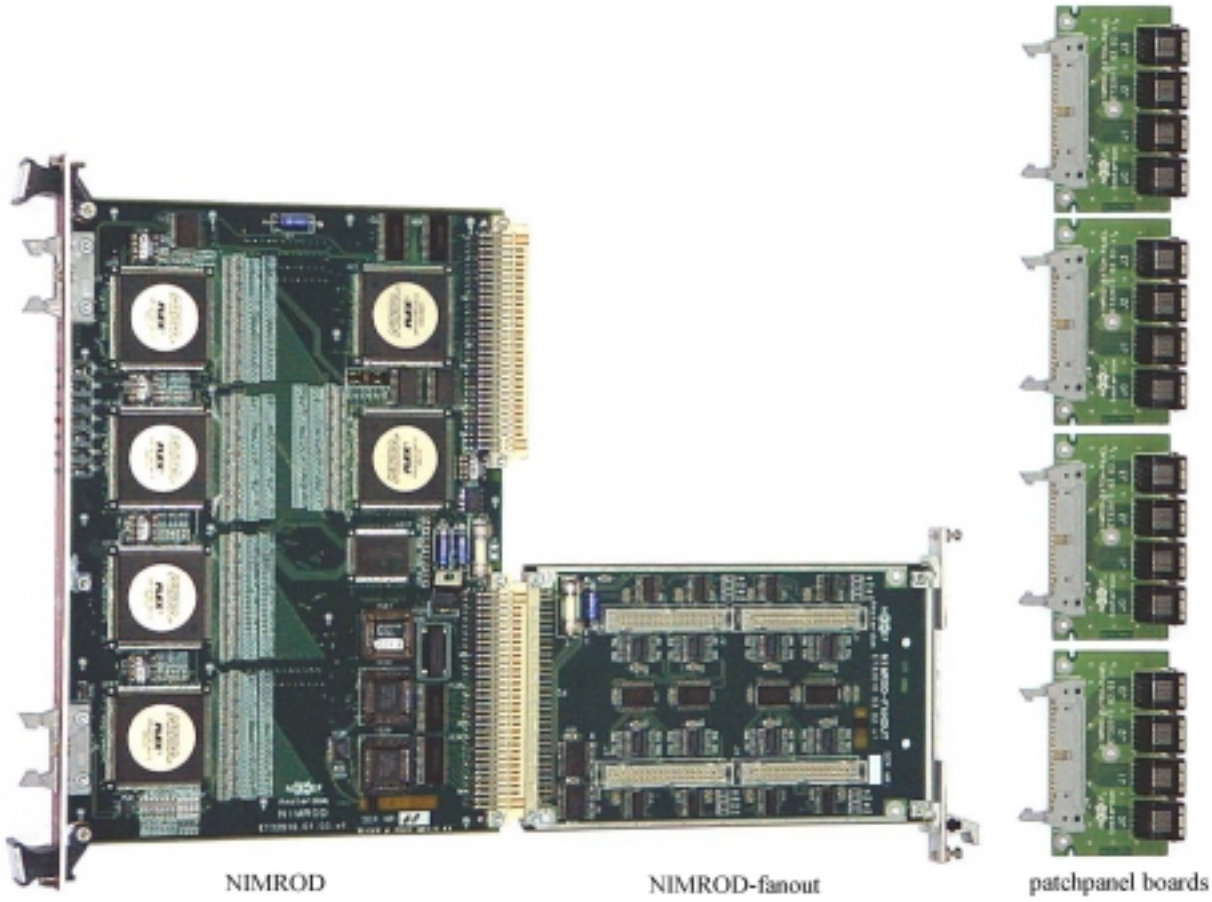

Figure 1: NIMROD modules

[1] A 24 channel TDC for the ATLAS precision muon chambers, Y. Arai (KEK) J. Christiansen (CERN).
[2] ETR 99-01: Cosmics Trigger and Timing Module, H. Verkooyen //www.nikhef.nl/pub/departments/et/L3/cosmics/.
[3] ETR 99-02: Cosmics Personality Card, H Groenstege et all //www.nikhef.nl/pub/departments/et/L3/cosmics/

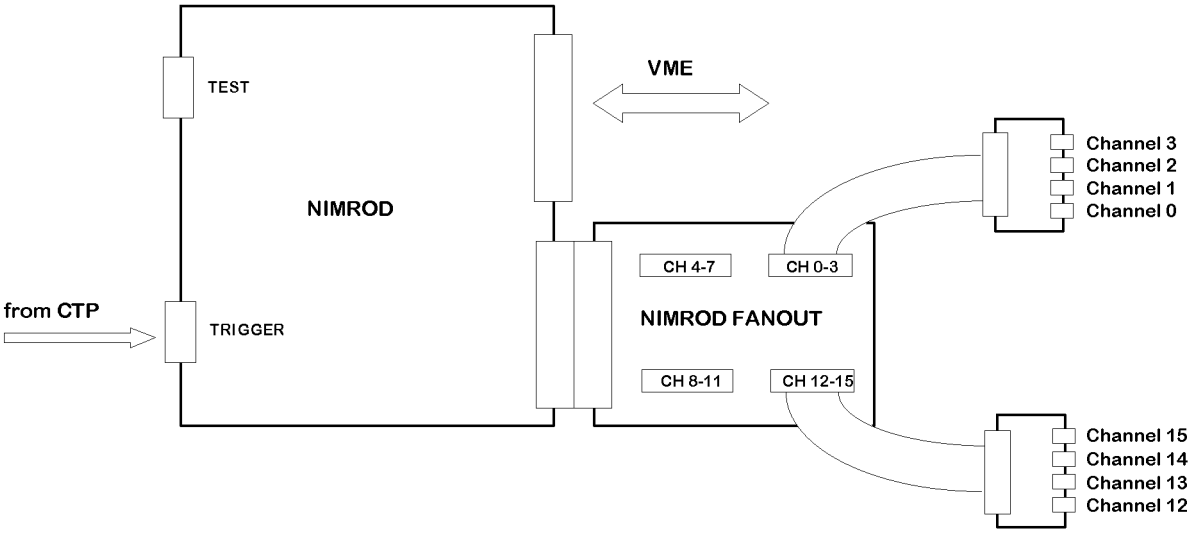

Figure 2: NIMROD connections

1.1 NIMROD connections

Each NIMROD accepts a maximum of 16 FELinks (Front-End Links) via the NIMROD_ Fanout module and a patch panel. The FELink connector is a standard shielded RJ45 and the cable is a shielded CAT 5 network cable.
The NIMROD_fanout module is connected to the NIMROD via row a and c of the VME P2 connector. It connects the TDCs to the NIMROD inputs and multiplexes the trigger and reset signals to the TDCs.
The VME interface is used to control the NIMROD, read the event data and generate test triggers and test resets.

Figure 3: NIMROD front

On the frontpanel are two 10-pin connectors. The upper connector, labeled Test, is a JTAG port used to perform in system programming of the FPGAs on the NIMROD. The lower connector, labeled Trigger, must be connected to the CTP via the trigger bus to receive the 40 MHz TDC clock, the coded trigger and reset signals and to return the *inhibit trigger* signal. The signal levels are differential Positive ECL and must be terminated with 100 Ohm after the last NIMROD. The combined *inhibit trigger* signals from the NIMRODs are terminated in the CTP. The coding of the trigger/reset signals on three sequential clock pulses is as follows:

1, 0, 0 = >Trigger
1, 0, 1 = > Event Counter Reset (ECR)
1, 1, 0 = > Bunch Counter Reset (BCR)
1, 1, 1 = > Global Reset

Due to coding of the Trigger and Reset internal in the NIMROD the maximum trigger frequency is the system clock divided by three. This is 20MHz/3 = 6.7 MHz (so the minimal deadtime is 150ns) .
All FELink signals to or from the TDCs are Low Voltage Differential Signals (LVDS). The serial data from the TDCs is received via two differential lines using DS coding without handshaking. The data consist of a startbit, followed by 32 bit TDC data, a paritybit and a stopbit. The rate on this connection is 40 Mbit/s.

The two signals from the NIMROD to the TDCs are also distributed via differential lines:

- The 40 MHz TDC clock.
  All signals are synchronous to this clock.
- The coded trigger/reset signal.
  Which is the trigger/reset signal from the CTP after a delay of four clock pulses. For test purposes the NIMROD mode register can also generate this signal.

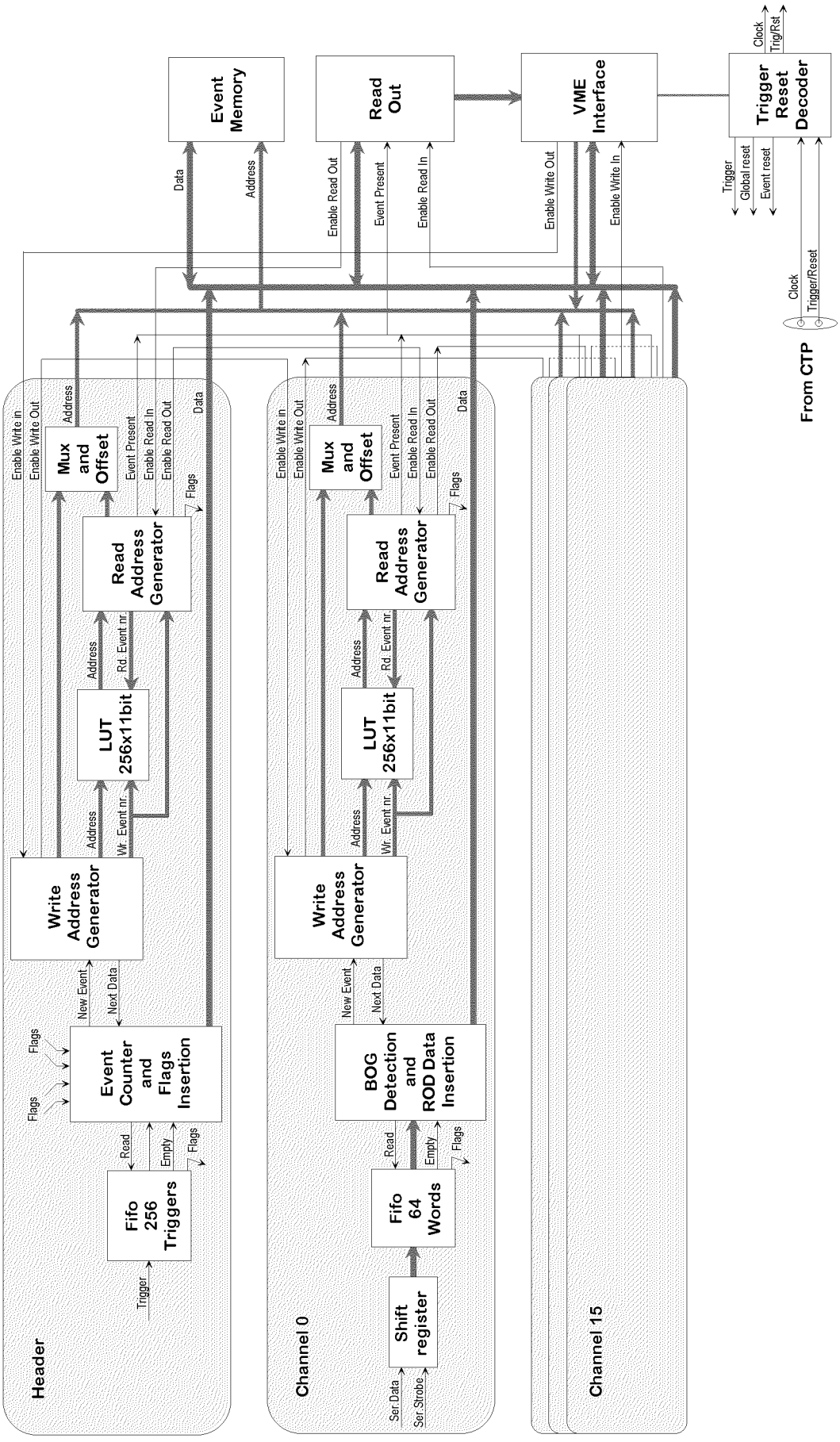

Figure 4: Block Diagram

2. General description

2.1 Block diagram

The trigger and reset from the CTP is decoded in the Trigger and Reset Decoder. The coded signals are distributed to the TDCs via the FELinks. The Global Reset is used internally to reset all counters and FIFOs in the NIMROD; the Event Counter Reset only clears the Event Counter in the Header block and the Bunch Counter Reset is not used in the NIMROD.

On a trigger, the Event Counter in the Header block is incremented and the data is stored in a circular buffer in the Event Memory. The address is stored in the Look Up Table (LUT) to be used for read out. Then, if the header enable bit is set, a flag header word (0x18100000) is stored, hereafter the flags are read and stored on the next addresses. When the circular buffer or the LUT is full, writing is inhibited and the triggers are stored in the Frontend FIFO.

Simultaneously the TDCs will sent data via the FELinks to the NIMROD. This data is converted from serial to parallel (32 bit) and stored into a FIFO. The data is read from the FIFO. If it is a leader of an event (*Begin Of Group*), the start address of the event is stored in the LUT. On the next address the *Begin Of Group* word is stored in the memory, followed by the next word from the FIFO until the trailer of the event (*End Of Group*) is detected. Then the Channel Header word is stored in the memory on the begin address of the event. When there is no data between the *Begin Of Group* (BOG) and *End Of Group* (EOG), the Event Empty bit is set in the Channel Header. After the writing of the Channel Header the event-present counter is incremented. If the event-present counter is not equal to zero, the event present flag of this channel is asserted.

When all channels have an event present, the Read-Out block starts a read-out cycle. At this point the Header block and the enabled channels get the read addresses from the LUTs, the Header block reads the *Begin Of Event* from the memory and puts it in the Output Register in the VME interface. Then Read-Out waits for the VME Master to read the output register before it enables the Header block to get the next word. If the Header block has read the data of the event it decrements its event-present counter and enables the first enabled channel to read the data until the read address is equal to the next address in the LUT or equal to the write address. Then the channel decrements its event counter and enables the next channel to send its data. This continues until all channels have read the event data from the memory. The Read-Out now terminates the read-out cycle and writes the *End Of Event* in the Output Register. If the Read-Out detects an Empty Event bit in a Channel Header, it will skip this channel, thus performing a zero-suppressed read-out. This zero-suppress is bypassed on event 1 modulo 0x1000 events. The data rate of the Read-Out via VME is 6 MB/sec (670 ns/word).

2.2 Shift Register

The serial data from the TDCs with LSB first is shifted in this register, if the last bit (MSB) is shifted in, the parity is checked. When the parity is not correct, the Serial Error Flag is asserted and the Serial Error bit (bit 26) is set in the TDC data. Then the data is loaded in the Frontend FIFO.
The serial error flag will be cleared when the flag word is written in the Event memory.

2.3 Frontend FIFO

The data in the event memory is written by 18 sources (16 Channels, the Header and the VME interface). These sources are scheduled with the system clock. Therefore a 64 words deep Frontend FIFO is implemented for every channel to store the data which is not yet written in the Event Memory. To prevent the FIFO to overrun an inhibit trigger is generated when the FIFO is half full (32 words). The inhibit trigger is released when the FIFO is empty. The input rate of the shift register is 35 bits @ 40 MHz. This results in an input rate of the FIFO of 1.14 MHz (875 ns) per word. With a system clock of 20 MHz the output rate is1.11 MHz (20 divided by 18), which is almost the same as the input rate.

So the FIFO will only be filled when the write to memory is inhibited by a memory full or a LUT full condition.

The system clock of the first version NIMROD was 7.5 MHz., So the output rate of the FIFO was 0.41 MHz. (2.44 μs) which is much lower than the input rate. Therefor a mechanism is built in that when the FIFO is almost full (56 words) only the *Begin Of Group* and *End Of Group* words are stored in the FIFO. This to prevent corruption of the bookkeeping of the event fragments.

2.4 Event memory

The event memory is a synchronous ZBT RAM that does not need the deselect cycle between a write and a read cycle. The memory clock is 40MHz; this enables a write and a read during one system clock cycle.

The memory has 17 circular buffers of 2K 32-bit words, one for every Channel plus the Header. For debugging purposes the memory is accessible from VME, the address map is given in the next chapter.

2.5 VME Interface

The VME Interface is compliant to VME64x and all devices can be accessed in the A24D32 and A32D32 addressing modes. The base address is defined by the Geographical Address pins on the backplane connector. In case the backplane does not support geographical addressing, jumpers J54 (= Ga0) to J50 (= Ga4) should be installed to define the base address of the NIMROD. If no jumpers are installed and no geographical addressing is supported, the default value of Ga(4:0) = 0x4.

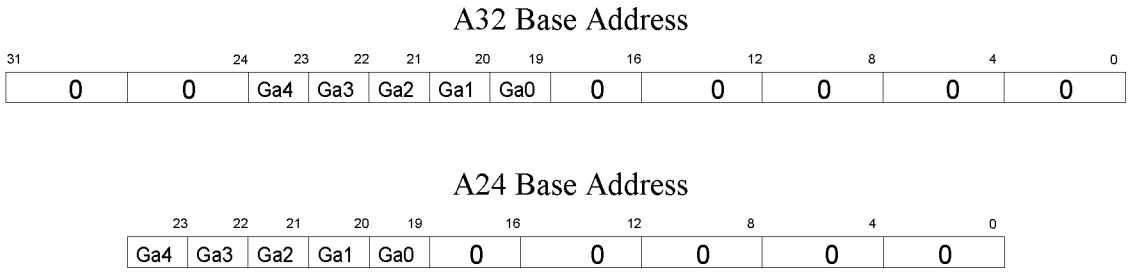

Figure 5: Base address

Valid Address Modifier codes are 0x09 and 0x0D for A24D32 transfers, 0x39 and 0x3D for A24D32 transfers and 0x2F for accessing of the Configuration ROM (CR) and Control & Status Register (CSR).

The Configuration ROM is a 64 x 8 bit ROM that contains module identification data. The ROM addresses are mapped in the VME address space from address offset 0x03 to 0xFF on every fourth byte.

The Control & Status Register:

Control & Status Bit Set Register, address offset = 0x7FFFB				
On Writes			**On Reads**	
Bit 7	1	put module in reset mode	1	module is in reset mode
	0	no effect	0	module is not in reset mode
Bit 4	1	enable module	1	module is enabled
	0	no effect	0	module is disabled
Bit 3	1	no effect	1	module generated BERR
	0	no effect	0	module did not generate BERR

Control & Status Bit Clear Register, address offset = 0x7FFF7				
On Writes			**On Reads**	
Bit 7	1	remove module from reset mode	1	module is in reset mode
	0	no effect	0	module is not in reset mode
Bit 4	1	disable module	1	module is enabled
	0	no effect	0	module is disabled
Bit 3	1	clear BERR bit	1	module generated BERR
	0	no effect	0	module did not generate BERR

The module reset can be done in two ways:

1. A short reset; Global Reset or bit 7 in CSR is asserted not longer then 16 system clock cycles. Resets all counters and FIFOs
2. A long reset; bit 7 in CSR is asserted longer then 16 system clock cycles. This reset does the same as a short reset, but also clears the LUTs. After this reset one has to wait for 786 system clock cycles for the clear LUT to complete.

The Mode Register:

Mode Bit Set Register address offset = 0x7FFF3				
On Writes			**On Reads**	
Bit 7	1	enable interrupt	1	interrupt is enabled
	0	no effect	0	interrupt is disabled
Bit 3	1	Generate bunch reset	1	bunch reset generated
	0	no effect	0	no bunch reset generated
Bit 2	1	Generate event reset	1	event reset generated
	0	no effect	0	no event reset generated
Bit 1	1	Generate global reset	1	global reset generated
	0	no effect	0	no global reset generated
Bit 0	1	Generate trigger	1	trigger generated
	0	no effect	0	no trigger generated

Mode Bit Clear Register address offset = 0x7FEF				
On Writes			**On Reads**	
Bit 7	1	Disable interrupt	1	interrupt is enabled
	0	no effect	0	interrupt is disabled
Bit 3	1	clear bunch reset bit	1	bunch reset generated
	0	no effect	0	no bunch reset generated
Bit 2	1	clear event reset bit	1	event reset generated
	0	no effect	0	no event reset generated
Bit 1	1	clear global reset bit	1	global reset generated
	0	no effect	0	no global reset generated
Bit 0	1	clear trigger bit	1	trigger generated
	0	no effect	0	no trigger generated

The Event Memory has an address offset of 0x40000. On this address the 8KB cyclic buffer of channel 0 starts, channel 1 starts at 0x42000 etc… until the buffer of the header that starts at 0x60000.
The Flags words are read-only and the address offsets are:

0x200	event present	0x210	FIFO empty
0x204	inhibit	0x214	FIFO half full
0x208	LUT full	0x218	channel enable
0x20C	memory full	0x21C	serial error

Except for the channel enable, the flags are read-only. Bit 16 of the flag words is the header flag, bit 15 to 0 are the flags of channel 15 to 0. Reading of the flags should not be done when the trigger is enabled, this corrupts the flag words in the event data.
The readout register is mapped to multiple addresses to enable block- or DMA transfers; the address offset is 0x300 to 0x1000. Reading the readout register when there is no event present will return 0x0.
The interrupter is of a single level type. An interrupt is generated when the interrupt enable is set in the mode register and the event present flags of all enabled channels are set. The interrupt request level is set in the interrupt request register at address offset 0x110. If bit 1 is set, the interrupt level is 1, if bit 2 is set, the interrupt level is 2, and so on until bit 7 then the interrupt level is 7 (bit 0 is not used). Only one bit must be set in the interrupt request level register. After reset the default interrupt request level is 2. The interrupt vector is set in the interrupt vector register at address offset 0x114.

3. Data format

The description below gives a summary of the data format that the NIMROD uses. The data format is compliant to the L3 Cosmics data format[4]. It should be noted that the NIMROD only tests on BOG and EOG for administration purposes and that all incoming data appears in the event data.

[4] KUN internal note, HEN425, The L3+Cosmics Data format, Thei Wijnen et all
//www.hef.kun.nl/l3c/

3.1 Data format of a channel input

Description	Bit 31 - 28	Bit 27 - 24	Bit 23 - 20	Bit 19 - 16	Bit 15 - 12	Bit 11 - 8	Bit 7 - 4	Bit 3 - 0
Begin Of Group	1010	0100	ECNT			Card ID		
TDC data	0011	TDC data						
More TDC data	0011	TDC data						
End Of Group	1101	0101	ECNT			Group WCNT		

3.2 Event Data format of the NIMROD

Description	Bit 31 - 28	Bit 27 - 24	Bit 23 - 20	Bit 19 - 16	Bit 15 - 12	Bit 11 - 8	Bit 7 - 4	Bit 3 - 0
Begin Of Event	1000	0000	ECNT (24bits)					
Flag Header*	0001	1000	0000	0000	0000	0000	0000	0000
LUT full flags*	0001	1001	0000	000x	xxxx	xxxx	xxxx	xxxx
Memory full flags*	0001	1001	0001	000x	xxxx	xxxx	xxxx	xxxx
FIFO half full flags*	0001	1001	0010	000x	xxxx	xxxx	xxxx	xxxx
Serial error flags*	0001	1001	0011	000x	xxxx	xxxx	xxxx	xxxx
Channel Header	0001	1000	0000	000E	0000	00	Channel ID	
Begin Of Group	1010	0100	ECNT			Card ID		
TDC data	0011	SE	TDC data					
More TDC data	0011	SE	TDC data					
End Of Group	1101	0101	ECNT			Group WCNT		
Channel Header	0001	1000	0000	000E	0000	00	Channel ID	
Begin Of Group	1010	0100	ECNT			Card ID		
TDC data	0011	SE	TDC data					
More TDC data	0011	SE	TDC data					
End Of Group	1101	0101	ECNT			Group WCNT		
End Of Event	1111	Event WCNT						

The ‘E’ bit in the channel header is the Empty Event flag. The ‘SE’ bit in the TDC data is the Serial Error flag detected by the NIMROD.

4. Test points and Jumpers settings

The NIMROD has 4 test points (TP1 to TP4) next to the memory chip IC17 and one test point (TP5) next to the Trigger Connector. TP1 to TP4 are connected to the memory control signals, TP5 is connected to pin 10 of the trigger connector and is not used.

* The flag words and header are inserted in the event data if bit 16 is set in the channel enable flag word.

TP1	Memory Chip Select
TP2	Memory Clock
TP3	Write Enable
TP4	Output Enable
TP5	not used

The user definable jumpers are the address jumpers (J50 to J55) and the 3V3 power select jumper (J5). If J5 pos. 1 is connected, the 3V3 power is obtained from the backplane, if pos 2 is connected, the 3V3 is coming from the on board power regulator. When the NIMROD is connected to a VME64x compatible backplane, all the address jumpers should be removed and J5 can be either in pos 1 or 2. In all other cases the address jumpers should be installed and J5 pos. 2 connected.

5. Connector pinout

Trigger

Pin	Signal	Pin	Signal
10	NC	9	GND
8	Trigger/Reset (-)	7	Trigger/Reset (+)
6	GND	5	GND
4	Clock (-)	3	Clock (+)
2	GND	1	Trigger Disable

Test

Pin	Signal	Pin	Signal
10	NC	9	NC
8	GND	7	TDO
6	+5V	5	TDI
4	GND	3	TMS
2	NC	1	TCK

Channel input

Pin	Signal
1	Clock(+)
2	Clock(-)
3	Trigger/Reset(+)
4	Data(-)
5	Data(+)
6	Trigger/Reset(-)
7	Strobe(+)
8	Strobe(-)
9	GND
10	GND

VME P1

Pin	Row z	Row a	Row b	Row c	Row d
1	NC	D0	NC	D8	NC
2	GND	D1	NC	D9	NC
3	NC	D2	NC	D10	NC
4	GND	D3	BG0IN_N	D11	NC
5	NC	D4	BG0OUT_N	D12	NC
6	GND	D5	BG1IN_N	D13	NC
7	NC	D6	BG1OUT_N	D14	NC
8	GND	D7	BG2IN_N	D15	NC
9	NC	GND	BG2OUT_N	GND	GAP_N
10	GND	NC	BG3IN_N	NC	GA0_N
11	NC	GND	BG3OUT_N	BERR_N	GA1_N
12	GND	DS1_N	NC	SYS_RES_N	3V3
13	NC	DS0_N	NC	LWORD_N	GA2_N
14	GND	WRITE_N	NC	AM5	3V3
15	NC	GND	NC	A23	GA3_N
16	GND	DTACK_N	AM0	A22	3V3
17	NC	GND	AM1	A21	GA4_N
18	GND	AS_N	AM2	A20	3V3
19	NC	GND	AM3	A19	NC
20	GND	IACK_N	GND	A18	3V3
21	NC	IACKIN_N	NC	A17	NC
22	GND	IACKOUT_N	NC	A16	3V3
23	NC	AM4	GND	A15	NC
24	GND	A7	IRQ7_N	A14	3V3
25	NC	A6	IRQ6_N	A13	NC
26	GND	A5	IRQ5_N	A12	3V3
27	NC	A4	IRQ4_N	A11	NC
28	GND	A3	IRQ3_N	A10	3V3
29	NC	A2	IRQ2_N	A9	NC
30	GND	A1	IRQ1_N	A8	3V3
31	NC	NC	NC	NC	NC
32	GND	+5V	+5V	+5V	NC

VME P2

Pin	Row z	Row a	Row b	Row c	Row d
1	NC	GND	+5V	GND	NC
2	GND	SER_DATA0	GND	SER_STRB0	NC
3	NC	SER_DATA1	NC	SER_STRB1	NC
4	GND	GND	A24	GND	NC
5	NC	SER_DATA2	A25	SER_STRB2	NC
6	GND	SER_DATA3	A26	SER_STRB3	NC
7	NC	GND	A27	GND	NC
8	GND	SER_DATA4	A28	SER_STRB4	NC
9	NC	SER_DATA5	A29	SER_STRB5	NC
10	GND	GND	A30	GND	NC
11	NC	SER_DATA6	A31	SER_STRB6	NC
12	GND	SER_DATA7	GND	SER_STRB7	NC
13	NC	GND	+5V	GND	NC
14	GND	SER_DATA8	D16	SER_STRB8	NC
15	NC	SER_DATA9	D17	SER_STRB9	NC
16	GND	GND	D18	GND	NC
17	NC	SER_DATAA	D19	SER_STRBA	NC
18	GND	SER_DATAB	D20	SER_STRBB	NC
19	NC	GND	D21	GND	NC
20	GND	SER_DATAC	D22	SER_STRBC	NC
21	NC	SER_DATAD	D23	SER_STRBD	NC
22	GND	GND	GND	GND	NC
23	NC	SER_DATAE	D24	SER_STRBE	NC
24	GND	SER_DATAF	D25	SER_STRBF	NC
25	NC	GND	D26	GND	NC
26	GND	GND	D27	GND	NC
27	NC	GND	D28	GND	NC
28	GND	GND	D29	GND	NC
29	NC	GND	D30	GND	NC
30	GND	CPCTRST	D31	CPCTRCLK	NV
31	NC	NC	GND	NC	NC
32	GND	NC	+5V	NC	NC

6. Abbreviations

Abbreviations and other less well known definitions used in this (and other) documents.

BCID	Bunch Crossing IDentifier. Reset by BCR.
BCR	Bunch Counter Reset, used to synchronize Front-End electronics.
CPC	Cosmics Personality Card. Contains TDCs and interface logic
CTP	Central Trigger Processor. Generates first level trigger.
CTT	Cosmics Trigger and Timing module.
ECR	Event Counter Reset.
FELink	Front-End Link. Carries the Reset/Trigger signals to the TDC and transports the TDC data to the NIMROD.
JTAG	Joint Test Action Group IEEE 1149.1. Functional test and programming facility.
LVDS	Low Voltage Differential Signaling. ±400 mV. Compatible with 3V and 5V supply voltages.
LUT	Look Up Table, contains start addresses of events in memory.