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Integrated low noise signal conditioning interface for neuroengineering applications

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Abstract – the birth of *Neuroengineering*, a new research field recently introduced by the synergic overlap between neuroscience and electronic engineering disciplines, injected a great enthusiasm in researchers. In fact, it opened a new perspective for addressing complex problems such as the understanding of the brain functions and the development of novel and advanced brain-computers. In this article, we offer a brief overview on implementations of integrated interface systems for neurobiological and electrophysiological in-vitro applications. After, we propose a system, still under development, aimed to achieving some hundreds of input channels. The architecture comprises a low-noise preamplifier stage and exhibits - for each channel - a power consumption of **90.05 µW** and a silicon area of about **0.17 mm^2**. Work is currently in progress to implement a fully integrated recording circuitry.

1. Introduction

In recent years, the knowledge about vertebrates' central nervous system functionalities has been largely increased at every descriptive level, i.e. from three-dimensional structures of a single ion channel, to real-time description of a whole living brain. Among these two edges, neuronal networks represent a good intermediate level of organization, in which emerging collective electrophysiological properties, as well as structural adaptability, play a fundamental role in the brain information processing functions.

At present, cultures of interconnected neurons can be grown and easily kept alive for weeks as experimental samples. In such a neurobiological system, synaptic connections between cells can be quantitatively modulated by means of appropriate chemical [1] and electrical [2] stimulation protocols. Moreover, thanks to the advantages offered by micro-fabrication technologies, the collective properties of these networks can be now explored with a high degree of detail.

The efforts of these new multi-disciplinary studies converge today in a new area of research: the *neuroengineering*. This new field offers the possibility to approach neuroscientific issues with new perspectives and by means of powerful tools, such as dedicated signal analysis, computer modelling and micro-transducers structures (e.g. Micro Electrode Arrays or MEAs). In particular, MEAs make feasible the development of microsystems capable of monitoring - as well as stimulating - the spatio-temporal electrophysiological activity of cultured neuronal networks (for an exhaustive

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dissertation on MEAs and on recent progresses achieved through their use, see also [3]). This kind of microsystems needs several and precise requirements, which are not easy to be satisfied if combined together. Their main features comprises multi-channel architectures, small device area and low-noise design techniques.

The goal of this article is to present an early version of such an integrated system. Nowadays, it consists in a multi-channel (several hundreds) recording and conditioning circuitry, comprising sampling, multiplexing and amplifying blocks. The system must be used in conjunction with a commercial MEA, which provides the interface with the neurons' culture.

The paper is organized as follows. In section 2 we describe the main problems concerning the design of systems devoted to record neurophysiologic signals. Section 3 offers an overview of our system, briefly describing each of its stages. Section 4 is focused on the preamplifier stage, reviewing some literature proposals and describing our own implementation. Section 5 reports our preliminary achievements and section 6 discusses some insights about further system developments.

2. Multi-channel integrated recording systems

The aim of such systems is to measure the spiking activity of a neurons' culture - placed on top of the MEA - and to extract, through a noise-filtering operation, its informative component. Our measurements indicate that this kind of activity consists in a time-varying voltage having a typical amplitude range comprised among **50** and **150 µVpp** and a bandwidth ranging between about **10 Hz** and **10 kHz** [4]. A noise component is present as well, derived from two sources: a "secondary" activity of the relevant neuron - so faint that it can't be correctly measured or interpreted - and nervous signals generated by neighbour cells, which in turn interfere with the potential being recorded. For the sake of simplicity, the noise is electrically characterized as Addictive-White-Gaussian (AWG) type and has a maximum amplitude of **10 μV_{rms}**. So, to discriminate between informative signal and noise, the adoption of a low-noise architecture appears to be an essential requirement, as well as a low-pass filtering capability. Moreover, it is convenient to design the input stage as close as possible to the transducers, so that further signal's degradation is limited. This choice, in turn, suggests the adoption of small-area circuitry. It should appear clear that designing low-noise devices having small sizes is not a trivial task.

Typically, cellular activity measurements are achieved using a reference electrode dipped in the physiological solution where neurons themselves are placed. This is done essentially because biological noise on the reference node is about the same as the one on recording electrodes. In this way, since the system's input signal is differential, the overall noise at the output should be greatly reduced. The disadvantage of using the reference consists in a slow, random drift of the dc component, caused by interaction of electrodes with the extra-cellular electrolyte. The drift can shift electrodes biasing in a maximum range of **±50 mV** [5]. This value is not negligible and must be taken in account during the design to avoid output saturation of amplifier stage. A way to cope with this problem is to implement a high-pass filter before the amplification stage. This means having very large time constants (i.e. seconds or more) and therefore extremely high resistors (GigaΩ or more). The integrated realization of such components

is indeed a very challenging task. Moreover, as electrodes drift is random, the common-mode input level varies over time. Thus, the system should exhibit a high Common Mode Rejection Ratio (CMRR) to deal with this circumstance without any problem.

Not to further interfere with the biasing conditions of the culture, it is also important to avoid current flow from electrodes through system. For this to be done, a very high input impedance at the system interface is required.

At last, low power consumption architectures are desired, especially when considering long-term portable applications provided with hundreds of channels.

3. System description

In the following, we briefly summarize some of the features that the acquisition and conditioning system needs to exhibit, according to the considerations introduced in the previous section:

- Large number of recording channels (several hundreds);
- Differential, high impedance inputs;
- Low power dissipation (some mW);
- Low noise (about $1\mu V_{rms}$), high CMRR ($\geq$ 60 dB) preamplifier;
- Pass-band filter behaviour ($f_L \approx 10$ Hz; $f_H \approx 10$ kHz);
- Limited area (some tens of square mm);

In addition, we desire to implement a simple signal-processing scheme, capable of sampling and multiplexing the channels over time. The resulting signal can be then sent to other processing units (e.g. A/D converters). The system we have conceived is shown in Fig. 2.

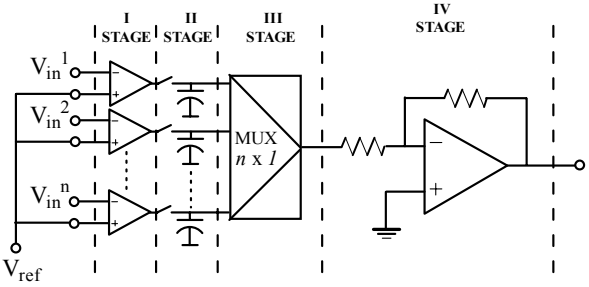

Fig. 1 – Block schematic of our system implementation

It consists of four stages: a preamplifying rack front-end (I), Sample & Hold circuits (II), an analog multiplexer (III) and an output amplifier (IV). Each input channel (i.e. recording site) is provided with a preamplifier and a S&H circuit.

The preamplifiers (I) represent the key components of the system and the most challenging ones to design. In fact, they should provide a constant gain over the signal bandwidth; include a pass-band filter behaviour to eliminate dc and high frequency noise

and harmonics; satisfy requirements of high CMRR, low noise, low power consumption, very high input impedance and small area occupation.

The S&H stage (II) is needed to sample all the pre-amplified signals at the same moment and to make them available for multiplexing. Circuitry architecture should take in account impedance adaptation and precision issues (i.e. charge injection). It should also be kept simple to avoid complex and area-hungry layouts, as it is intended to be integrated together with preamplifiers, as close as possible to the microelectrodes.

The analog multiplexer (III) provides merging over time of the n sampled waveforms. Supposing to sample at frequency f_s (i.e. about 20 kHz), the multiplexer scans periodically each channel (every $1/f_s$ seconds) and draws it to the output keeping it stable for $1/n*f_s$ seconds (circular buffer structure). Mux's output signal, whose bandwidth is $n*f_s$, is fed into a unique output amplifier. This block (IV) provides an appropriate gain to make the signal suitable for further processing (i.e. A/D conversion). The design requirements of stages III and IV comprise low power consumption and reliability.

4. Low-noise preamplifier state-of-the art

In last years, many implementations of low-noise preamplifiers for biological signal interfaces have been presented. Between all of them, we chose to compare five realizations [6-10] which should cover a large spectrum of needs and an adequate trade-off in their performances.

The first two realizations (Burke & Gleeson and the INA 125) [6,7], although interesting, were not chosen because of implementation issues regarding large components values, high precision matching and large supply currents.

Martins, Selberherr & Vaz's [8] circuit was not suffering from these problems but was quite complex, involving about 30 MOSes and was not the best choice for our needs, as it would have taken up too much space.

Ji & Wise's [9] proposal showed a good performances trade-off and simple design but, after a detailed analysis of the circuit, we discovered that the use of a feedback loop to filter the dc component presented serious reliability problems, due to extreme precise matching requirements.

Harrison & Charles' [10] realization (H&C) was the best choice, although they used dedicated components to realize very high impedance resistors (inserted in the closed-loop path), indicated as "bipolar-MOSes". Basically, they are fabricated as lateral BJT devices but, using their diode configuration in conjunction with their PMOS parasitic structure, they exhibit a very high incremental resistance (i.e. $r_{inc} \geq 10^{10}\ \Omega$) below their sub-threshold voltage. This feature permits to achieve very small high-pass cut-off frequencies (order of Hertzs) using small devices (**13.4 µm x 13.4 µm**), instead of wasting a lot of space for building standard integrated resistors.

We completely redesigned the entire circuit to improve its performances and to avoid the use of large devices - a problem experienced by H&C in their implementation. The preamplifier circuit we have designed is shown in Fig. 3.

Supposing the gain of the op-amp (denoted with g_m) very high, the preamplifier's mid-band gain results to be about C_1/C_2, whereas the low and hi-frequency cut-offs are respectively $f_L \approx 1/(2\pi 2 r_{inc} C_2)$ and $f_H \approx g_m/2\pi A_M C_L$ (where $A_M = C_1/C_2$). In Table 1 the

simulated performances of our circuit are reported and compared with the simulated ones of [10].

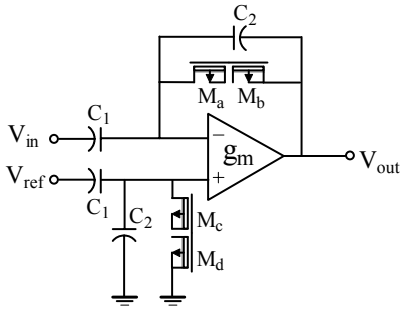

Fig. 2 – Preamplifier closed-loop schematic. M_a-M_d represent the bipolar-MOSes; g_m indicates the OTA transconductance

	This work	[10]
Supply voltage [V]	±1.65	±2.5
Supply current [μA]	10	16
Mid-band gain [dB]	40	40
f_L [Hz]	0.4	0.13
f_H [kHz]	11	7.5
IN-referred noise [10^{-6} V_{rms}]	$3.35*10^{-3}$	2.1
CMRR [dB]	≥ 68.4	≥ 42
Power dissipation [μW]	24	80
THD [dB]	-83 dB	-40 dB (*)

Table 1 – Comparison between preamplifying circuits (simulated performances); (*) indicates a measured value

5. Results

After having conceived and designed all the circuitry, we went through the physical design and post-layout simulations.
For the layout we took advantage of highly-symmetrical structures (such as common-centroid ones), in order to respect precision requirements. The technology we used consisted in a **double-poly, double-metal 0.35 μm CMOS (AMS CSI)**.

At this stage of our work, the recording system is still designed to be used together with a commercial MEA. In particular, we have chosen the planar 8x8 structure by Multi Channel Systems, which has the electrodes' diameter equal to 30 μm and the electrodes' spacing of 200 μm (whereas neurons' soma is about 20 μm).

So far, it has been possible to estimate the following performance: a single channel line occupies approximately **0.17 mm^2** of silicon area and dissipates **90.05 μW** (excluding the output amplifier). A complete 100-channels system occupies about **17.1 mm^2** and exhibits a power consumption equal to **14.4 mW**.

Thus, for a **500 channels** system, the silicon area would be around **86 mm^2** and power consumption around **45.3 mW**.

6. Future work

We presented an integrated acquisition and conditioning system, specifically designed to record electrical activity coming from in-vitro cultured neural cells. Its preamplification stage exhibits low power and low noise performances as well as a pass-band filter functionality. To realize integrated components showing large time-constants, we used a dedicated component, the "bipolar-MOS" device.

The system is currently under development: we are ready to fabricate the first test chip, which will let us to verify the behaviour of the bipolar-MOSes and the quality of recorded neural signals. Next, we will start expanding the design implementing a fully-integrated bi-directional system, provided with several hundred of channels. The main issue about it is to make channels capable to serve both as recording inputs and as stimulating outputs. Essentially, three kinds of problems arise when implementing such a functionality: the first one is the generation of electrical artefacts passing from stimulation to recording. The second one is the reliability and accuracy of stimuli, which can be compromised by the dc offset between stimulation and reference electrodes [11]. The last one consists in how to cope with high-voltage stimulating pulses (some Volts) being generated in the same silicon substrate of precision-recording electronics.

In a long-term prevision, our system could extend research areas of brain-computer interfaces - in which nervous signals are used to control external devices - and of neuro-prostheses - in which artificial devices substitute portions of cerebral tissue.

References

[1] M. Chiappalone et al., "Networks of neurons coupled to microelectrode arrays: a neuronal sensory system for pharmacological applications", *Biosensors & Bioelectronics*, vol. 18: pp. 627-634, 2003.
[2] A. Novellino et al., "Behaviors from an electrically stimulated spinal cord neuronal network cultured on microelectrode arrays.", *Neurocomputing*, 2003 (in press).
[3] S. M. Potter, "Distributed processing in cultured neuronal networks", *Progress in Brain Research*, vol. 130: Advances in Neural Population Coding (chapter 4), pp. 49-62, 2001 Elsevier Science B. V.
[4] M. Grattarola, S. Martinoia, "Modeling the Neuron-Microtransducer Junction: From Extracellular to Patch Recording", *IEEE Transaction on Biomedical Engineering*, vol. 40, No. 1, January 1993, pp. 35-41.
[5] Q. Bai and K. D. Wise, "Single-Unit Neural Recording with Active Microelectrode Arrays", *IEEE Transactions On Biomedical Egineering*, vol.48, no. 8, August 2001, pp. 911-920.
[6] M. J. Burke and D. T. Gleeson, " A Micropower Dry- Electrode ECG Preamplifier," *IEEE Transactions On Biomedical Engineering*, vol. 47, February 2002, pp.155-162.
[7] Burr-Brown's INA 125 op-amp datasheet, available at: http://focus.ti.com/docs/prod/folders/print/ina125.
[8] R. Martins, S. Selberherr and F. A. Vaz, " A CMOS IC for Portable EEG Acquisition Systems", *IEEE Transactions On Instrumentations and Measurement*, vol. 47, no. 5, October 1998, pp.1191-1196.
[9] J. Ji, K. D. Wise, "An implantable CMOS circuit interface for multiplexed microelectrode recording arrays", *IEEE Journal of Solid State Circuits*, vol. 27, no. 3, March 1992, pp.433-443.
[10] R. R. Harrison, C. Charles, "A Low-Power Low- Noise CMOS Amplifier for Neural Recording Applications," *IEEE Journal of Solid -State Circuits*, vol. 38 no 6, June 2003, pp.958-965.
[11] Y. Jimbo et al., "A System for MEA-based Multisite Stimulation", *IEEE Transactions on Biomedical Engineering*, vol. 50, no. 2, February 2003.