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A VLSI reconfigurable network of integrate–and–fire neurons with spike–based learning synapses

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Abstract. We present a VLSI device comprising an array of leaky integrate–and–fire (I&F) neurons and adaptive synapses with spike–timing dependent plasticity (STDP). The neurons transmit spikes off chip and the synapses receive spikes from external devices using a communication protocol based on the "Address–Event Representation" (AER). We studied the response properties of the neurons in the array to uniform input currents, and measured their AER outputs. We characterized the properties of the STDP synapses using AER input spike trains. Our results indicate that these circuits can be reliably used in massively parallel VLSI networks of I&F neurons to simulate real–time complex spike–based learning algorithms.

1 Introduction

A growing interest in pulse–based neural networks [10] has recently lead to the design and fabrication of an increasing number of VLSI networks of integrate–and–fire (I&F) neurons. These types of devices have great potential, allowing researchers to implement simulations of large networks of spiking neurons with complex dynamics in real time, possibly solving computationally demanding tasks. However, there are still a few practical problems that hinder the development of large–scale, massively parallel distributed networks of VLSI I&F neurons. The three main ones are: (1) how to program or set each individual synapse (synaptic weight) in the network; (2) how to access the individual neurons in the network both for providing input and for reading output signals; (3) how to (re)–configure the network topology and/or connectivity.

In this paper we present a VLSI device with a one dimensional array of I&F neurons, and a 2–D matrix of adaptive synapses with spike–timing dependent (STDP) plasticity, in which synapses receive input spikes and neurons transmit output spikes using an *Address–Event Representation* (AER) [3, 6]. The STDP circuits in the synapses allow us to solve problem (1) cited above, by setting the synaptic weights using a

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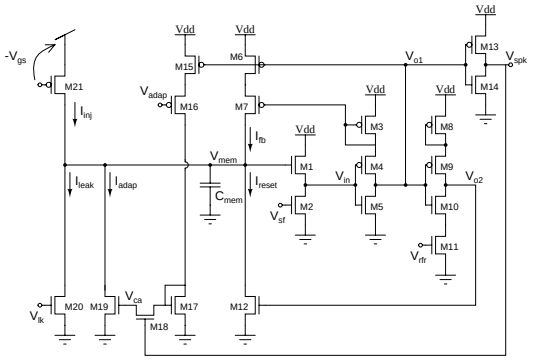

Figure 1: I&F neuron circuit.

spike–timing based learning algorithm. The use of the AER communication protocol allows us to simultaneously solve problems (2) and (3): This protocol allows the chip to exchange data while processing signals in parallel, in real time. Input and output spikes (events) are transmitted as real–time asynchronous binary data streams that carry analog information in their temporal structure. Each event is represented by a binary word encoding the address of the sending node. On–chip arbitration schemes are used to handle event "collisions" (cases in which sending nodes attempt to transmit their addresses at exactly the same time). Systems containing more than two AER chips can be constructed by implementing additional special purpose off–chip arbitration schemes [5, 6]. Once in the digital domain, address–events can be remapped from multiple sending nodes to a single receiving node, or from a single sending node to multiple receiving nodes, allowing the user to arbitrarily reconfigure the network connectivity.

In the next sections we describe the chip architecture and show experimental data demonstrating the response properties of the I&F neurons using both constant input currents and AER synaptic inputs, and show the learning properties of the STDP synapses.

2 The VLSI device

The device, implemented using a standard AMS 0.8μm CMOS process, comprises a linear array of 32 low–power I&F neurons, a 2–D array of 32$\times$8 synaptic circuits, and Input/Output AER interfacing circuits. Each neuron is connected to 2 inhibitory and 6 excitatory synapses. The synapses are divided into two groups with independent bias settings for maximum and minimum synaptic weights. The other bias parameters (time constants, bi-stability threshold, *etc.*) are global. The neuron circuitry occupies an area of $83 \times 31\mu\text{m}^2$, while the inhibitory and excitatory synapses measure $55 \times 31\mu\text{m}^2$ and $145 \times 31\mu\text{m}^2$ respectively.

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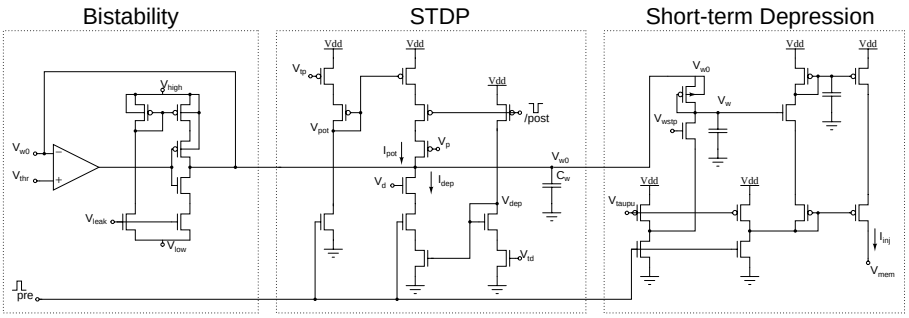

Figure 2: Excitatory synapse circuit.

2.1 The I&F neuron circuit

The circuit implementation of the I&F neurons is shown in Fig. 1. Input current is integrated onto the membrane capacitor C_{mem}. Once V_{mem} reaches the spiking threshold the neuron generates a fast digital pulse (V_{o1} is set to 0 and V_{spk} to V_{dd}), V_{mem} is reset to zero and the capacitor begins integrating the input current again. The four bias control voltages V_{lk}, V_{sf}, V_{rfr}, and V_{adap} allow the user to specify a desired leak current, a spiking threshold voltage, an absolute refractory period, and the gain of a spike–frequency dependent adaptation current respectively. A detailed description of this circuit has been presented in [9].

2.2 The synaptic circuits

The circuits that model the inhibitory synapses are implemented using a cascoded n–type current–mirror integrator [7], and do not exhibit learning properties. The excitatory synapses contain circuits that implement bi-stability, STDP type learning, and short–term depression (see Fig. 2).

Bi-stability is used to implement storage of learned states (potentiated or depotentiated) on long time scales [2]; STDP is used to implement learning, updating the synaptic weight on short–term scales [12]; and short–term depression is an adaptation mechanism, also acting on short time scales, that implements dynamic gain control [1].

The bi-stability circuit slowly drives the (*non–adapted*) synaptic weight V_{w0} to one of the two asymptotic states V_{high} or V_{low} at a rate set by V_{leak}. The STDP circuit updates V_{w0} on short time scales with each occurrence of *pre*– and *post*–synaptic spikes, increasing the weight if there is a causal relationship (the *pre*–synaptic spike precedes the *post*–synaptic one), and decreasing it otherwise. The time–window within which the STDP can occur and the maximum increase and decrease of the weight can be independently controlled by V_{tp}, V_{td}, V_p, and V_d respectively. The short–term depression adaptation circuit decrements the *effective* synaptic weight V_w with each *pre*–synaptic spike, from its steady state value V_{w0}, by an amount set by V_{wstp}, and with a rate controlled by V_{taupu}.

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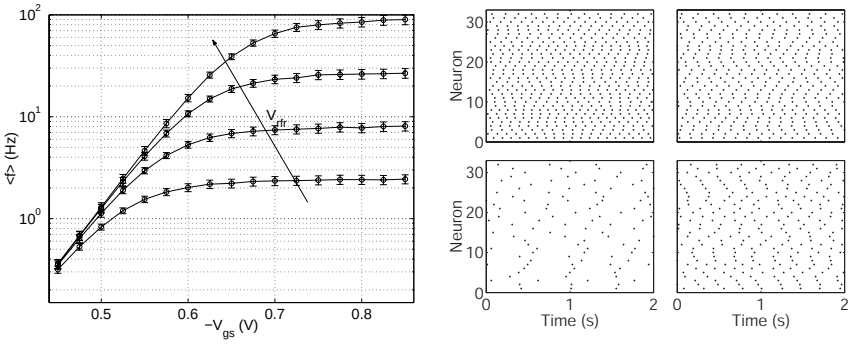

(a) (b)

Figure 3: (a) Mean response of all neurons in the array to increasing values of a global input current, for four different refractory period settings (set by biasing V_{rfr} of Fig. 1 to 0.30V, 0.35V, 0.40V, and 0.45V respectively). The error bars represent the standard deviation of the responses throughout the array. (b) Raster plots showing the activity of the whole array in response to the input current set by $V_{gs} = -0.575V$, for the same four increasing values of V_{rfr} (counterclockwise from the bottom left quadrant).

The detailed response properties of the bi-stability and STDP synaptic circuits have been described in [8], while the characteristics of the short–term depression circuits have been presented in [11, 4].

3 Experimental results

We tested the response properties of the array of I&F neurons by injecting a constant current to each neuron (bypassing the synapses) and measuring their firing rates. To measure the activity of the array of neurons we used a custom PCI–AER board, capable of monitoring and time–stamping address events on the AER bus [5]. We biased the p–FET $M21$ of Fig. 1 in weak–inversion to generate the neuron input current and measured the activity of the array for different refractory period settings (V_{rfr}). Figure 3(a) shows the mean firing rates of the neurons in the array as a function of V_{gs} on a semi–logarithmic scale. Given the exponential relationship between V_{gs} and the injected current, Fig. 3(a) shows how the firing rate increases linearly with the input current, saturating at higher asymptotic values, for increasing values of V_{rfr} (decreasing refractory period duration). Figure 3(b) shows four *raster plots* of the activity of all neurons in the array in response to uniform input current, for different refractory period settings.

The learning characteristics of the STDP circuits at a single synapse level are described in detail in [8]. To evaluate the properties of the synaptic circuits in the whole array we stimulated the STDP synapses with Poisson AER spike trains while injecting constant current into the I&F neurons, and measured their spiking activity via the AER

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output circuits. We set the Long–Term–Depotentiated (LTD) value of the synapses (V_{low} of Fig. 2) to $1V$, and their Long–Term–Potentiated (LTP) value (V_{high}) to $3.6V$. Using these values for the asymptotic synaptic weights, a depressed synapse has no measurable effect on the spiking frequency of a post-synaptic neuron. Conversely, for a potentiated synapse pre–synaptic spikes affect the post–synaptic firing rate.

Figure 4(a) shows the coefficient of variation (CV) of one post–synaptic neuron measured while stimulating the STDP synapse. If the average value of the synaptic weight is low the regular firing rate of the neuron driven by a constant current is not altered. High values of CV indicate that the synaptic weight on average is high and the Poisson pre–synaptic spikes alter the firing rate of the post–synaptic neuron. This is only an indirect measure of the average synaptic weight of one synapse and does not reflect its true probability of LTP or LTD. To assess these probabilities over the whole array, we separated the learning phase from the weight readout phase, exploiting the weight's bi-stability. During the learning phase we set the mean pre–synaptic firing rate of a row of synapses to 140Hz, either applying a $V_{gs} = -0.63$V to induce LTD, or a $V_{gs} = -0.67$V to induce LTP. After 10s of stimulation we "froze" the leaned synaptic weights by increasing V_{leak} of Fig. 2 appropriately. In the readout phase we stimulated the synapses using 40Hz Poisson spike trains and the neurons by setting the V_{gs} to 0.55V. By comparing the mean frequency of the post–synaptic neurons to the baseline (obtained in absence of synaptic stimulation) we determined which synapses were potentiated. Figure 4(b) shows the estimated LTP probabilities obtained after repeating the experiment described above 250 times, for each of the two V_{gs} settings used in the learning phase. Despite the variability observed across the array (due to device mismatch), the synapses behave as expected: The synaptic weights can be independently driven to a high or low state using appropriate pre- and post-synaptic stimuli.

4 Conclusion

We presented a VLSI array of I&F neurons with plastic adaptive synapses that use the Address–Event–Representation to receive and transmit spikes. We used a PCI–AER board [5] to stimulate the synapses with address–events and monitor the activity of the neurons in the array. We showed that the I&F neurons respond to constant currents in a consistent and reliable way, and demonstrated the possibility to change the individual synaptic weights in the array by driving their STDP learning circuits with pre– and post–synaptic spike trains with appropriate frequencies. Our results indicate that these circuits can be reliably used in massively parallel VLSI networks of I&F neurons to for real–time simulation of complex spike–based learning algorithms.

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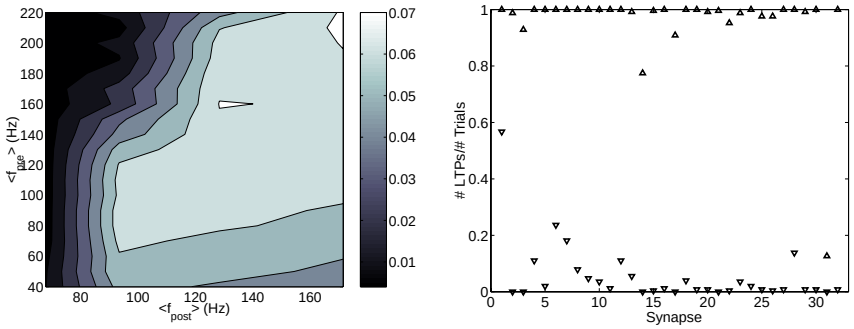

(a) (b)

Figure 4: (a) CV of post–synaptic inter-spike interval (ISI) as a function of pre– and post–synaptic firing rates, measured for one plastic synapse. (b) Probability of inducing LTP measured over the whole row of synapses. Upward triangles correspond to the stimulation experiment that was expected to induce LTP while downward triangles correspond to the stimulation experiment that was expected to induce LTD (see text for details).

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