Protection and control device for HV/MV substation – Communication profile (according to IEC 61850) for the MFP

This global standard defines the characteristics of communication profile (according to IEC 61850 series) for the multifunctional feeder protection (according to GSTP101) for HV/MV distribution substations a declared fundamental frequency of 50 Hz or 60 Hz.

Countries' I&N	Elaborated by	Collaborations by	Verified by	Approved by
Argentina	-	-	-	**Carlos Espinoza**
Brazil	-	-	-	**Romulo Thardelly**
Chile	-	-	-	**Daniel Gonzalez**
Colombia	-	-	-	**Juan Gomez**
Iberia	-	-	**Carmen Ranea Angel Corchero**	**Maria Avery**
Italy	**Luca Delli Carpini**	-	**Luca Delli Carpini**	**Gianluca Sapienza**
Peru	-	-	-	**Robert Sanchez**
Romania	-	-	-	**Vasilica Obrejan**

	Elaborated by	Collaborations by	Verified by	Approved by
Global I&N – NTI	-	-	**Christian Noce**	**Fabio Giammanco**

Revision	Data	List of modifications
00	27.07.2018	First draft
01	06.12.2018	First approved edition

INDEX

FIGURES

TABLES

1 ACRONYMS

a. **AETA** enel custom LN Class: Automatic control Enel Topological Address of an IED

b. **CID** Configured IED Description (XML file)

c. **CP** HV/MV Distribution Substation

d. **CS** MV/LV Distribution Substation

e. **DA** Data Attribute

f. **DO** Data Object

g. **DS** Distribution Substation

h. **EAC** Automatic Load Shedding: a function inside the MFP or a dedicated device

i. **HMI** Human-Machine Interface

j. **HV** High Voltage

k. **ICD** IED Capability Description (file)

l. **IED** Intelligent Electronic Device

m. **IED** Intelligent Electronic Device

n. **IEDp** Protection Relay or other IED requiring physical I/O extensions (for example the MFP)

o. **GS** Enel Global Standard

p. **LD** Logical Device

q. **LN** Logical Node

r. **LV** Low Voltage

s. **MFP** Multifunctional feeder protection

t. **MTP** Multifunctional transormer protection

u. **MV** Medium Voltage

v. **OdM** Circuit breaker / Switch

w. **PEFD** enel custom LN Class: Protection Enel Frequency based for Distribution automation

x. **PEOC** enel custom LN Class: PTOC extended with special settings and/or information

y. **PEOP** enel custom LN Class: PDOP extended with special settings and/or information

z. **PEOV** enel custom LN Class: PTOV extended with special settings and/or information

aa. **PEUV** enel custom LN Class: PTUV extended with special settings and/or information

bb. **PoD** Point of Delivery (connection with the DER Plant)

cc. **REBF** enel custom LN Class: RBRF extended with special settings and/or information

dd. **REBV** enel custom LN Class: protection Related Enel, Block of the protections based on V analysis

ee. **REDR** enel custom LN Class: RDIR extended with special settings and/or information

ff. **RGDM** Protection and control device for MV substation – RGDM by according to GSTP01X series

gg. **RIO** Remote I/O module of multifunctional feeder protection (MFP-RIO)

hh. **RTU** Remote Terminal Unit

ii. **SCD** Substation Configuration Description

jj. **SCL** Substation Configuration Language

kk. **SS** SubStation

ll. **TFN** Earthing Transformer

mm. **TPT** RTU of a CP

nn. **TPT2020** TPT new generation with IEC61850 communication (Client and Server)

2 LIST OF COMPONENTS, PRODUCT FAMILY OR SOLUTIONS TO WHICH THE GS APPLIES

The Multifunctional feeder protection (MFP) described in this GSTP10X series can be classified in several products provided in Table 1 in GSTP101.

3 NORMATIVE REFERENCES AND BIBLIOGRAPHY

All the references in this GSTP are intended in the last revision or amendment.

3.1 For all countries

IEC 61850-5	Communication networks and systems in substations - Part 5: Communication requirements for functions and device models
IEC 61850-7-3:	Communication networks and systems for power utility automation - Part 7-3: Basic communication structure – Common data classes
IEC 61850-7-4	Communication networks and systems for power utility automation - Part 7-4: Basic communication structure - Compatible logical node classes and data objec classes
IEC 61850-90-1	Communication networks and systems for power utility automation - Part 90-1: Use of IEC 61850 for the communication between substations
IEC 61850-6	Communication networks and systems for power utility automation - Part 6: Configuration description language for communication in electrical substations related to IEDs
IEC 61850-8-1	Communication networks and systems in substations - Part 8-1: Specific Communication Service Mapping (SCSM) - Mappings to MMS (ISO 9506-1 and ISO 9506-2) and to ISO/IEC 8802-3
IEEE 802.1Q	IEEE Standards for Local and Metropolitan Networks: Virtual Bridged Local Area Networks - Standard version suitable with the adopted protocols and/or IEC 61850 edition
IEC 61850-7-2	Communication networks and systems in substations - Part 7-2: Basic communication structure for substation and feeder equipment – Abstract communication service interface (ACSI)
RFC 2030	Simple Network Time Protocol (SNTP) V.4; RFC 1305 - Network Time Protocol Version 3 (NTPv3); RFC 5905 - Network Time Protocol Version 4 (NTPv4)
IEEE C37.2	Electrical Power System Device Function - Numbers and Contact Designation
GSCG002	Technical Conformity Assessment
GSTP10X series	Protection and control device for HV/MV substation – Multifunctional feeder protection (MFP)
GSTP901	Cybersecurity requirements for protection and control devices

4 REPLACED STANDARDS

Codification	Country	Title
DMI-9-00016	Italy	Requisiti costruttivi e funzionali del Pannello Multifunzione di Protezione e Controllo per Cabina Primaria

5 APPLICATION FIELDS

This document standardizes the communication profile for the devices used for protection and control purposes in the ENEL's HV/MV distribution substation (by according to GSTP101). This device accomplishes to the definition of IED, by according to IEC 61850 series.

With reference to, the devices/system that will interoperate through this standard, a set of Enel global devices is also mentioned, however some previous devices compliant to Enel country standards may assure analogous level of interoperability.

6 FEATURES OF THE MFP

6.1 Functional description

The MFP is an IED that implements a wide set of protection, control, automation, monitoring and measurement functions according to GSTP101. The IED is typically located in a HV/MV Distribution Substation (also defined Primary Substation). Depending on the type of FW loaded and running on board, the IED operates on:

a. MV feeder – Circuit breaker control, protection and Automatic Load Shedding (EAC);

b. Section circuit-breaker (or busbar coupler);

c. Earthing Transformer (TFN);

d. Power Factor Correction;

e. Bus transfer;

f. HV delivery line to the customer (radial);

g. Auxiliary Services.

The MFP will be able to implement LNs, protocol stacks and communication services as defined in the IEC 61850 standard (with particular reference to IEC 61850-5, IEC 61850-7-3, IEC 61850-7-4, IEC 61850-90-1, IEC 61850-6, IEC 61850-8-1, IEC 61850-7-2) in order to support the features described in IEC 61850-5, GSTP101 and summarized, for the reader's convenience, in the following section 6.3.

The IED implements a IEC 61850 Server comprised of six Logical Devices (LDs) each consisting of the Logical Nodes (LNs) that model the data used by the MFP to accomplish its functions.

6.1.1 Communication inside the DS

The IED will be able to communicate via LAN in the DS with:

a. the RTU (GSTR1XX series, TPT2020)
   - Client of the HV/MV IEC61850 IEDs,
   - Distributor of the CID files to the IEDs,
   - Time server for the Synchronization in according to RFC 2030;

b. (optionally) one or more clients during the development or special/temporary operation stages;

c. the IED EAC that could request the "52 MT trip" in order to full disconnect the MV feeder;

d. the MFPs controlling
   - the MV feeders of the same bus-bar Sx,
   - the MV feeders of the other bus-bar Sy,
   - the busbar coupler

e. with RIO,the MFP can have dedicated/direct connections with one or more IED(s) RIO that extend(s) the physical connectivity to the field.

in order to exchange the command of protection stages acceleration;

f. the MFPs controlling:
   - the MV feeders of the same bus-bar Sx,
   - the MV feeders of the other bus-bar Sy,

in order to exchange the event of 67Nb stage Operate;

g. the MTP to
   - exchange the command of protection stages acceleration,
   - receive the 59VoV/W (depending on the grounding systems) Residual Overcurrent stage Start;

6.1.2 Communication with other devices along the feeder

The IED will be able to communicate with the RGDMs installed on the same MV feeder in order to:

a. participate in the Logical Selectivity for the Feeder protection (by receiving the Blind signal),

b. Remotely Disconnect the Distributed Generation and Loads (by sending the TD signal);

6.2 Namespace

ENEL-specific functionalities requires extensions to the IEC 61850 Data Models via ad-hoc Logical Nodes; a dedicated namespace is defined and used accordingly:

a. Namespace id: IEC61850-ENEL-Distribution;

b. Namespace Version: 2018;

c. Namespace release: 1;

d. Namespace release date: 2018-06;

e. Namespace name: “IEC61850-ENEL-Distribution:2018”.

6.3 MFP Functions (Summary)

The functions of the MFP (refer to GSTP101), which must be supported by the IEC 61850 (data modelling and information exchange), are listed below.

6.3.1 General functions

The general functions of the MFP are listed below:

a. File Transfer (to send/receive the CID files, disturbance recordings, etc.);

b. Diagnostic (internal) – General state of the MFP;

c. Diagnostic (external) – connected VT, CV and MT Circuit Breaker;

d. Configuration management (CID);

e. Circuit Breaker tripping due to command from EAC;

f. Reference NTP server addressing and IED Time Sync status.

6.3.2 Monitoring and Measurement

The functions of monitoring and measurement of the IED are listed below:

a. Periodical Instantaneous and Average Measurements of Currents (I), frequency (f), Voltages (V), Active Power (P) and Reactive Power (Q);

b. Event-driven Measurements of phase Current (I) and Voltage (V) (Magnitude and phase angle), Frequency (f), Rate of change of frequency (df/dt); Residual current (3Io), Residual voltage (3Vo) and Phase difference angle (between 3Vo and 3Io);

c. Monitoring (Periodical Instantaneous and Average Measurements) of the THD of the Current and Voltage.

6.3.3 Protection Functions

The functions of protection of the MFP are listed below:

a. Special settings of the protections (stage-specific; please, refer to the relevant sections 6.2.x):

- operating mode of protection thresholds (Start + Operate, Start only),
- Double time calibration for stage acceleration,
- participation in the Logical Selectivity Function (FSL),
- 2nd harmonic block,
- signals exchange of Protection stage acceleration,
- selection of definite-time (Ti), in any case the accelerated stages are definite-time(Ti), and/or inverse-time (Td) operation (Td according to standard curves or to a fixed curve with dedicated parameters ; stage-specific; for details, please, refer to the relevant sections 6.2.x)
- Cold Load Pickup function;

b. Phase Overcurrent (51):

- 51.S1, 51.S2, 51.S3 and 51.S4 with double time calibration;

c. Neutral Overcurrent (51N) based on the measurements of a dedicated transformer:

- 51N.S1, 51N.S2 and 51N.S3 with double time calibration,
- 51N.S1_a and 51N.S2_a with double time calibration,
- 51N.E with double time calibration;

d. Residual Overcurrent (51NR) based on the calculation of the Residual Current:

- 51NR.S1, 51NR.S2 and 51NR.S3 with double time calibration,

e. Directional Phase Overcurrent (67):

- Common Settings for all Stages,
- 67.S1, 67.S2, 67.S3 and 67.s4 with double time calibration;

f. Directional Neutral (Residual) Overcurrent (67N):

- Common Settings for all Stages,
- 67N.S1, 67N.S2a, 67N.S2b, 67N.S3 with double time calibration,
- 67N.Sb with double time calibration and Delayed Start message exchange with other IEDs in the DS;

g. Negative Sequence Overcurrent (46):

- 46.S1 and 46.S4 with double time calibration;

h. Unbalance Overcurrent 46N.S1 with double time calibration;

i. Arcing Ground:

- 67N.S4 intermittent arcs,
- 67N.S5 evolving faults;

j. Residual overvoltage (59N):

- Common Settings for all Stages,
- 59N.S1, 59N.S2 and 59N.E;

k. Overvoltage (59):

- Common Settings for all Stages,
- 59.S1c in case of compensated neutral,
- 59.S2i in case of insulated neutral;

l. Undervoltage (27):

- Common Settings for all Stages,
- 27.S1 and 27.S2

m. Discrimination of INRUSH currents, 2nd harmonic (87 2ndH REST);

n. Directional active overpower (32P):

- 32P.S1 and 32P.S2;

o. Synchro-check:

- 25PS (Synchronous networks),
- 25PA (Asynchronous networks);

p. DC undervoltage (27X);

q. Check Resolving/Non-Resolving Petersen Coil Intervention (MOIM);

r. Internal Automatic Load Shedding (EAC) functions:

- Two protection stages, each one including:
  - Two independent frequency thresholds (Over/Under),
  - One Rate of change of frequency threshold,
  - Configuration of the operating mode of the frequency-based protection (Ena/Disabling, Over, Under, df/dt, number of measurement, semi-periods);
- Blocking Stages, meant to guarantee the reliability of the frequency-based protections:
  - Undervoltage (27),
  - Overvoltage (59),
  - Maximum unbalance β,
  - Max frequency difference γ,
  - Maximum variation allowed between consecutive periods Maxdt,
  - Reverse Active overpower;
- General Signalling of the MFP frequency-based protection stages blocking

s. Breaker Failure function (50/60 BF);

t. Broken Conductor (I2/I1) function

u. Start and Operate summarization (per stage) of 51+67 and 46N protections (Base and Accelerated).

6.3.4 Automation functions

a. Automatic Reclosing function (DRA) of the MV Circuit Breaker with programmable sequences of different closing types (RR (Fast Closing), RL (Slow Closing), RM (Memorized Closing), dedicated management and specific protection stages settings);

b. Logical selectivity (FSL) of the MV feeder faulty section (with selectable operation of the specific protections stages);

c. Remote Disconnection (TDLP) of the Distributed Generation and Loads to avoid the unintentional islanding in a faulty MV feeder.

6.3.5 Remote Inputs and Outputs

Expansion of the IED communication capability to/from the field through max. two IEDs RIO (for the MODBUS; more than 2 if the communication profile is through IEC61850), each one providing:

a. 14 Remote Inputs from the field, communicated to the MFP and reported to the RTU (GSTR1XX series, TPT2020);

b. 4 Remote Outputs applied to the field upon request from RTU (GSTR1XX series, TPT2020) and/or MFP internal logics.

6.3.6 Virtual Inputs and Outputs

Handling of experimental I/O (32 inputs and 16 outputs) ready for any future use/development and related communication.

7 LIST OF THE MFP LOGICAL NODES

This chapter specifies the MFP data model according to the formal language of the IEC61850 standard.

The Physical Device (IED) consists of six Logical Devices (LDs) relevant to the functions performed by the MFP, in according to GSTP101.

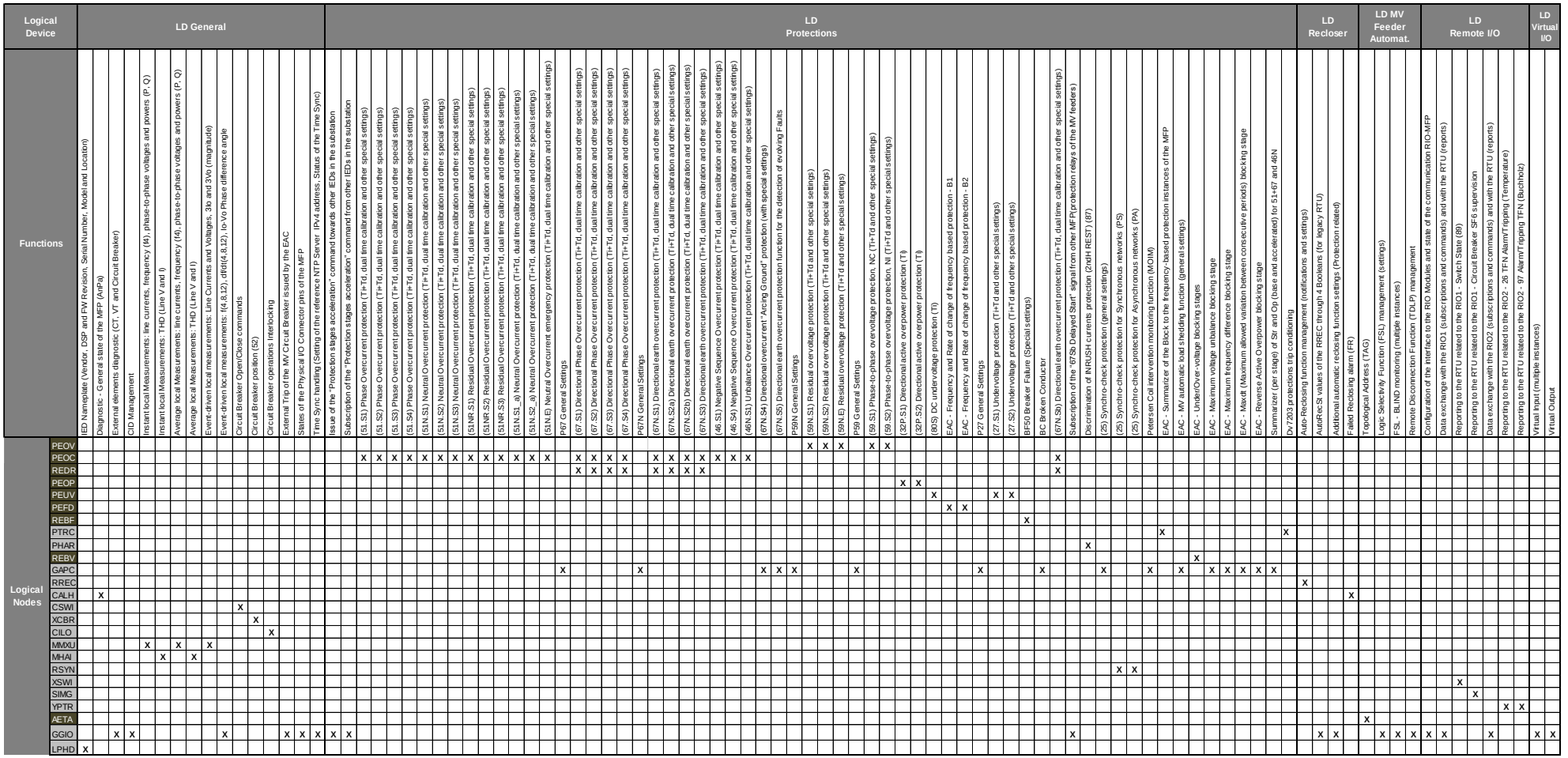

Figure 1 - MFP Logical Nodes

Figure 1 shows the association between a function (column) performed by the MFP and the dedicated logical nodes (rows) that define the data exchanged with the cooperating IEDs and the Client. LLN0 and LPHD are not mentioned as mandatory/default for the LD.

Note: in case of multiple LNs per function, the "**X**" in bold font indicates the LN that model the specific data for that function, while the "x", in normal font indicates shared information provided by the LN.

It is worth noting that only the functions requiring data and communication according to IEC 61850 are considered in this document.

When deemed necessary for specific project purposes the general classes proposed by the standard have been customized, while still remaining compliant, with the rules and constraints provided by the standard IEC 61850-7-4.

The resulting model, in terms of IED, LDs, LNs and their interrelationships is structured as shown in Figure 2.

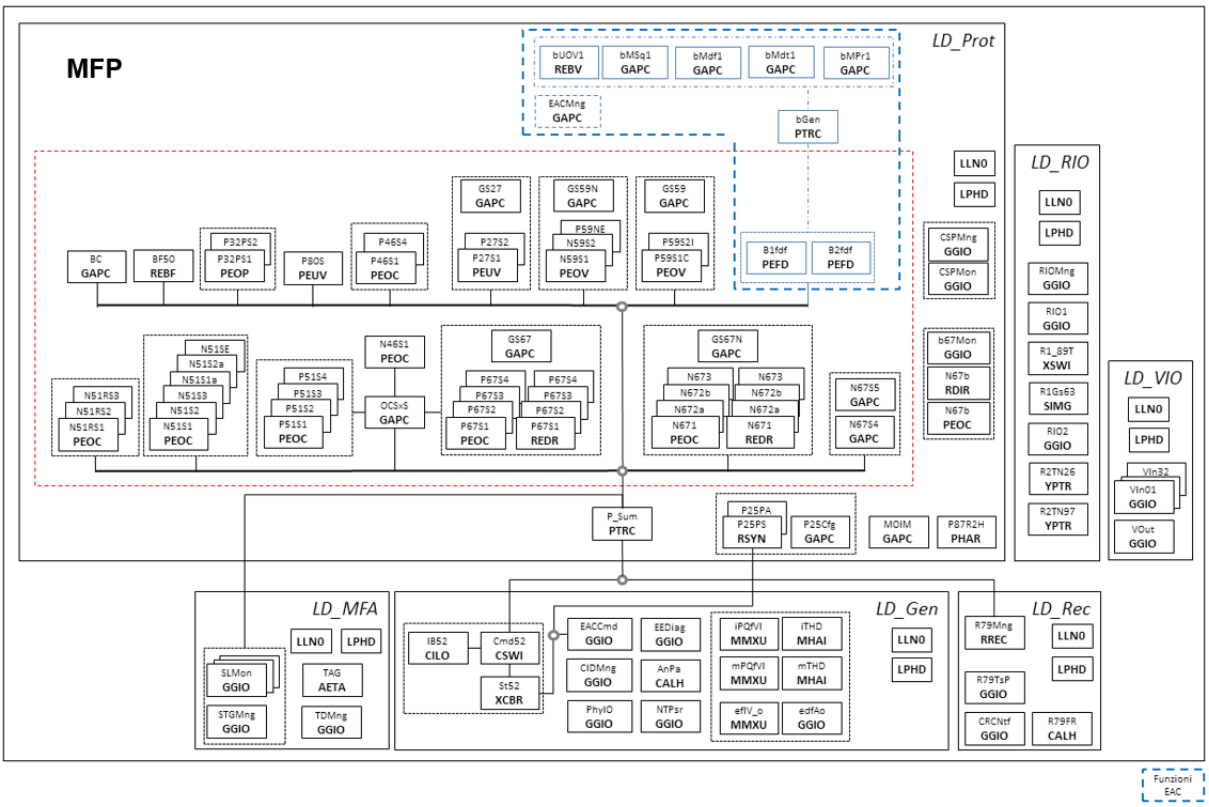

Figure 2 - Organization of the MFP's IEC61850 model

The following sections prescribe the data (DOs) included in the communication between the MFP and other IEDs with an exhaustive tabular description, refer to IEC 61850-7-4, for each selected LN.

Note that the typical values of the M/O column:

a. M = mandatory,

b. O = optional,

c. C = conditional,

are extended with the additional

d. **R = required** (that means **mandatory to achieve the requirements of the ENEL project**, regardless of what is stated in the standard).

In Table 1 is shown an example extracted from LN MMXU.

Table 1 – Example of R values of the M/O column				
…	…	…		...
Hz	MV	Frequency		O→**R**
PPV	DEL	Phase to phase voltages (VL1VL2, ...)		O→**R**
PhV	WYE	Phase to ground voltages (VL1ER, ...)		O
A	WYE	Phase currents (IL1, IL2, IL3)		O
W	WYE	Phase active power (P)		O
…	…	…		...

All of the logical nodes defined in IEC 61850-7-4 are derived from the **Common Logical Node Class**, they will inherit all its mandatory Data; for the optional data there are three possibilities for specialization:

a. the piece of data is not inherited,

b. the piece of data is inherited and left as optional,

c. the piece of data is inherited and defined as mandatory;

Table 2 – Common Logical Node Class				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Mandatory Logical Node Information (Shall be inherited by ALL LN but LPHD)				
Mod	INC	Mode		M
Beh	INS	Behaviour		M
Health	INS	Health		M
NamPlt	LPL	Name plate		M
Optional Logical Node Information				
Loc	SPS	Local operation		O
EEHealth	INS	External equipment health		O
EEName	DPL	External equipment name plate		O
OpCntRs	INC	Operation counter resetable		O
OpCnt	INS	Operation counter		O
OpTmh	INS	Operation time		O
Data Sets (see IEC 61850-7-2)				
Inherited and specialized from Logical Node class (see IEC 61850-7-2)				
Control Blocks (see IEC 61850-7-2)				
Inherited and specialized from Logical Node class (see IEC 61850-7-2)				
Services (see IEC 61850-7-2)				
Inherited and specialized from Logical Node class (see IEC 61850-7-2)				

Each table specifying a LN is followed, where necessary, by notes with details on the modelling;

As an aid to future proofing the IEDs it may be appropriate to seek the agreement of ENEL that additional information (with respect to GSTP101) could be modelled for specific LNs, thus also leveraging the scalability of the IEC-61850 standard;

Most LNs include a counter (resettable or not), which is considered an option by the standard, but is very useful for keeping track of the various states, alarms, parameters etc. depending on the functional requirements of the IED reported in the GSTP101 (e.g. number of Start/Operate of a protection, number of issued alarms, number of settings of particular parameters, etc.).

During the prototyping, special ENEL functions will be modelled using standard generic LNs such as CALH, GGIO, GAPC and applying the Extension Rules provided in the IEC 61850-7-4. In the final Data Model, as per the agreement with ENEL, these generic IEDs will be replaced with specific LNs with 'Name Space' dedicated to the ENEL project;

The activation/deactivation of a complete functionality will be achieved by controlling the DO Mod, that every specific LN inherits as Mandatory from the Common Logical Node Class;

The prefixes used in the model of a LN are, typically, acronyms/abbreviations of the underlying function (e.g. **EEDiag** is **E**xternal **E**lement **D**iagnostic).

7.1 Logical Device General: details of the Logical Nodes

The Logical Device General (LD_Gen) contains the Logical Nodes required to model the information concerning the overall IED, including the Circuit Breaker Control.

LLN0 is used to model the common parts of this Logical Device.

Table 3 – LLN01 type

Attribute Name	Attribute Type	Explanation	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
Loc	SPS	Local operation for complete logical device		O
OpTmh	INS	Operation Time		O
Controls				
Diag	SPC	Run Diagnostic		O
LEDRs	SPC	LED reset	T	O

LPHD models the common parts of the Physical Device that contains this Logical Device. In the LD_Gen it will contain all the relevant information of the IED: Vendor, DSP and FW Revision, Serial Number, Model and Location.

Table 4 – LNInstance: 1 – LPHD1 type

Attribute Name	Attribute Type	Explanation	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
PhyNam	DPL	Physical device name plate		M
PhyHealth	INS	Physical device health		M
OutOv	SPS	Output communications buffer overflow		O
Proxy	SPS	Indicates if this LN is a proxy		M
InOv	SPS	Input communications buffer overflow		O
NumPwrUp	INS	Number of Power ups		O

WrmStr	INS	Number of Warm Starts		O
WacTrg	INS	Number of watchdog device resets detected		O
PwrUp	SPS	Power Up detected		O
PwrDn	SPS	Power Down detected		O
PwrSupAlm	SPS	External power supply alarm		O
RsStat	SPC	Reset device statistics	T	O

NOTES:
Data → PhyNam: for setting the IED name plate details

a. **vendor** [M]: the supplier of the device

b. **hwRev** [R]: the DSP Rev.

c. **swRev** [R]: the FW Rev.

d. **serNum** [R]: the serial number of the device

e. **model** [R]: MFP

f. **location** [R]: HV/MV Substation (opt. in addition: - the location in the SS, if meaningful for discriminating the functional role of the IED).

7.1.1 Diagnostic – General state of the MFP

The MFP implements an internal (HW and SW) diagnostic to monitor and notify, with a specific Alarm "AnPa", its general state.

Table 5 – LNInstance: 1 - prefix: AnPa – CALH1 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
Status Information				
GrAlm	SPS	Group alarm		M
GrWrn	SPS	Group warning		O
AllmLstOv	SPS	Alarm list overflow		O

NOTES:
Status Information→ GrAlm: for sending the "AnPa" alarm in case of HW/SW faults of the equipment; it must be consistent with the available HMI (e.g. a LED) and/or log recorder of the IED:

a. 0 = MFP OK

b. 1 = AnPA.

7.1.2 MFP External elements diagnostic (CT, VT and Circuit Breaker)

Table 6 – LNInstance: 1 - prefix: EEDiag – GGIO1 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
EEHealth	INS	External equipment health (external sensor)		O
EEName	DPL	External equipment name plate		O
Loc	SPS	Local operation		O
OpCntRs	INC	Resetable operation counter		R
Measured values				
AnIn	MV	Analogue input		O
Controls				
SPCSO	SPC	Single point controllable status output		O
DPCSO	DPC	Double point controllable status output		O
ISCSO	INC	Integer status controllable status output		O
Status Information				
IntIn	INS	Integer status input		O
Alm1	SPS	General single alarm (1)		R
Alm2	SPS	General single alarm (2)		R
Alm3	SPS	General single alarm (3)		R
Alm4	SPS	General single alarm (4)		R
Alm5	SPS	General single alarm (5)		R
Ind	SPS	General indication (binary input)		O

NOTES:

Common Logical Node Information→ OpCntRs: to count and store the number of events occurred

Status Information→ Alm1: for notifying the information Circuit Breaker Anomaly:

a. 0 = OK

b. 1 = Circuit Breaker Anomaly

Status Information→ Alm2: for notifying a fault in the three-phase voltage measurement chain (VT, cabling):

c. 0 = OK

d. 1 = VTS.

Status Information→ Alm3: for notifying a fault in the three-phase current measurement chain (CT, cabling):

e. 0 = OK

f. 1 = CTS.

Status Information→ Alm4: for sending the result of the diagnostic on the maximum number of Circuit Breaker openings:

g. 0 = OK

h. 1 = Diag. Max. CB openings exceeded

Status Information→ Alm5: for sending the Anomaly, Circuit Breaker operation extra time:

i. 0 = OK

j. 1 = Anomaly, Circuit Breaker operation extra time.

7.1.3 CID Management

The CID File, defined in GSTP101, used for the configuration of the IEC61850 communication, is transferred to/from the MFP via the File Transfer Service (FTP and/or IEC61850); typically, the peer in this procedure is the RTU (GSTR1XX series, TPT2020). Upon a successful file transfer, the IED parses the file and loads the configuration into a dedicated memory area (e.g. a stand-by memory bank). When this procedure completes (successfully or not), the MFP reports the status of the reconfiguration to the peer. In case of positive result, the RTU (GSTR1XX series, TPT2020) will request the MFP to switch to the new configuration with a confirmed procedure. File management in the MFP depends on GSTP101.

Table 7 – LNInstance: 1 - prefix: CIDMng – GGIO2 type

Attribute Name	Attribute Type	Explanation	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
EEHealth	INS	External equipment health (external sensor)		O
EEName	DPL	External equipment name plate		O
Loc	SPS	Local operation		O
OpCntRs	INC	Resetable operation counter		R
Measured values				
AnIn	MV	Analogue input		O
Controls				
SPCSO	SPC	Single point controllable status output		R
DPCSO	DPC	Double point controllable status output		O
ISCSO	INC	Integer status controllable status output		O
Status Information				
IntIn	INS	Integer status input		R
Alm	SPS	General single alarm		O
Ind	SPS	General indication (binary input)		O

NOTES:

Common Logical Node Information→ OpCntRs (ready): to count and store the number of reconfigurations

Controls → SPCSO: to handle the request to change to the new configuration (Boolean = 1). The request is confirmed; at the end of the procedure, the MFP changes the value to 0

Status Information → IntIn: for sending the CIDReconfig notification, according to the outcome of the reconfiguration procedure via a new CID file:

a. 1 = OK,

b. 2 = abnormal/unexpected reconfiguration via new CID,

c. 3 = abnormal/unexpected status after reboot with new reconfiguration,

7.1.4 MFP Local Measurements

MFP, via its own CTs and VTs, carries out the measurements of the main electrical quantities as required by GSTP101; the results are sent with specific reports to the RTU (GSTR1XX series, TPT2020). There are three simultaneous measurement campaigns where the sampled quantities are:

a. averaged and reported every 10 seconds (periodic "instantaneous" measurements);

b. averaged and reported every 600 sec (periodic "average" measurements, to be logged, e.g. for MT voltage control);

c. event-driven, a snapshot of the selected electrical quantities sampled and reported when a protection operates (used for the fault analysis).

The IED, functionally, must allocate the specified measurement variables so that they are updated via Report only if the MFP protections are activated. Until the next trigger event, the values do not change to prevent inappropriate traffic to the RTU.

In addition, the THD_V and THD_I are calculated and reported together with the periodic measurements with the same granularity periods.

Hereafter the MFP local measurements are modelled with the relevant LNs.

7.1.4.1. Periodic instantaneous measurements of currents, frequency, voltages and powers (P, Q)

Table 8 – LNInstance: 1 – prefix: iPQfVI – MMXU1 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
		Common Logical Node Information		
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
EEHealth	INS	External equipment health (external sensor)		O
Measured values				
TotW	MV	Total Active Power (Total P)		R
TotVAr	MV	Total Reactive Power (Total Q)		R
TotVA	MV	Total Apparent Power (Total S)		O
TotPF	MV	Average Power Factor (Total PF)		O
Hz	MV	Frequency		R
PPV	DEL	Phase to phase voltages (VL1VL2, ...)		R
PhV	WYE	Phase to ground voltages (VL1ER, ...)		O
A	WYE	Phase currents (IL1, IL2, IL3)		R
W	WYE	Phase active power (P)		O
Var	WYE	Phase reactive power (Q)		O
VA	WYE	Phase apparent power (S)		O
PF	WYE	Phase power factor		O
Z	WYE	Phase Impedance		O

NOTES:

Measured values→ TotW: for reporting the measurement (with sign) of the Active Power P (W)

Measured values→ TotVAr: for reporting the measurement (with sign) of the Reactive Power Q (VAr)

Measured values→ Hz: for reporting the measurement of the f (Hz) of the phase 4

Measured values→ PPV: for reporting the measurement of the phase-to-phase Voltages V4-8, V8-12, V12-4 (V)

Measured values→ A: for reporting the measurement of the Line Currents I4, I8, I12 (A).

7.1.4.2. Periodic instantaneous measurements of the THD (Line V and I)

Table 9 – LNInstance: 1 - prefix: iTHD – MHAI1				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
EEHealth	INS	External equipment health (external sensor)		O
EEName	DPL	External equipment name plate		O
Measured values				
Hz	MV	Basic Frequency		C
HA	HWYE	Sequence of Harmonics or Interharmonics current		O
HPhV	HWYE	Sequence of Harmonics or Interharominics phase to ground voltages		O
HPPV	HDEL	Sequence of Harmonics or Interharmonics phase to phase voltages		O
HW	HWYE	Sequence of Harmonics or Interharmonics active power		O
HVAr	HWYE	Sequence of Harmonics or Interharmonics reactive power		O
HVA	HWYE	Sequence of Harmonics or Interharmonics apparent power		O
HRmsA	WYE	Current RMS Harmonic or Interharmonics (un-normalized Total harmonic disortion, Thd)		O
HRmsPhV	WYE	Voltage RMS Harmonic or Interharmonics (un-normalized Thd) for phase to ground		O
HRmsPPV	DEL	Voltage RMS Harmonic or Interharmonics (un-normalized Thd) for phase to phase		O
HTuW	WYE	Total phase Harmonic or Interharmonics active power (no fundamental) unsigned sum		O
HTsW	WYE	Total phase Harmonic or Interharmonic active power (no fundamental) signed sum		O
HATm	WYE	Current Time product		O
HKf	WYE	K Factor		O
HTdf	WYE	Transformer derating factor		O
ThdA	WYE	Current Total Harmonic or Interharmonic Distortion (different methods)		R
ThdOddA	WYE	Current Total Harmonic or Interharmonic Distortion (different methods – odd components)		O
ThdEvnA	WYE	Current Total Harmonic or Interharmonic Distortion (different methods – even components)		O
TddA	WYE	Current Total Demand Distortion per IEEE 519		O
TddOddA	WYE	Current Total Demand Distortion per IEEE 519 (odd components)		O
TddEvnA	WYE	Current Total Demand Distortion per IEEE 519 (even components)		O
ThdPhV	WYE	Voltage Total Harmonic or Interharmonic Distortion (different methods) for phase to ground		R
ThdOddPhV	WYE	Voltage Total Harmonic or Interharmonic Distortion (different methods) for phase to ground (odd components)		O

ThdEvnPhV	WYE	Voltage Total Harmonic or Interharmonic Distortion (different methods) for phase to ground (even components)		O
ThdPPV	DEL	Voltage Total Harmonic or Interharmonic Distortion (different methods) for phase to phase		O
ThdOddPPV	DEL	Voltage Total Harmonic or Interharmonic Distortion (different methods) for phase to phase (odd components)		O
ThdEvnPPV	DEL	Voltage Total Harmonic or Interharmonic Distortion (different methods) for phase to phase (even components)		O
HCfPhV	WYE	Voltage crest factors (peak waveform value/sqrt(2)/fundamental) for phase to ground		O
HCfPPV	DEL	Voltage crest factors (peak waveform value/sqrt(2)/fundamental) for phase to phase		O
HCfA	WYE	Current crest factors (peak waveform value/sqrt(2)/fundamental)		O
HTif	WYE	Voltage Telephone Influence Factor		O
Settings				
HzSet	ASG	Basic frequency		C
EvTmms	ASG	Evaluation time (time window) determines the lowest frequency		O
NumCyc	ING	Number of cycles of the basic frequency		O
ThdAVal	ASG	ThdA alarm Setting – value entered in %		O
ThdVVal	ASG	ThdPhV / ThdPPV alarm Setting – value entered in %		O
ThdATmms	ING	ThdA alarm time delay in ms		O
ThdVTmms	ING	ThdPhV / ThdPPV alarm time delay in ms		O
NomA	ASG	Normalising demand current used in IEEE 519 TDD calculation		O

Condition C: Hz and HzSet are exclusive.

NOTES:

Measured values→ ThdA: for reporting the measurement of the Line Current THD (all the phases)

Measured values→ ThdPhV: for reporting the measurement of the Line Voltage THD (all the phases).

7.1.4.3. Periodic average measurements of currents, frequency, voltages and powers (P, Q)

Table 10 – LNInstance: 1 - prefix: mPQfVI – MMXU1 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
EEHealth	INS	External equipment health (external sensor)		O
Measured values				
TotW	MV	Total Active Power (Total P)		R
TotVAr	MV	Total Reactive Power (Total Q)		R
TotVA	MV	Total Apparent Power (Total S)		O
TotPF	MV	Average Power Factor (Total PF)		O
Hz	MV	Frequency		R
PPV	DEL	Phase to phase voltages (VL1VL2, ...)		R
PhV	WYE	Phase to ground voltages (VL1ER, ...)		O
A	WYE	Phase currents (IL1, IL2, IL3)		R
W	WYE	Phase active power (P)		O
Var	WYE	Phase reactive power (Q)		O

VA	WYE	Phase apparent power (S)		O
PF	WYE	Phase power factor		O
Z	WYE	Phase Impedance		O

NOTES:

Measured values→ TotW: for reporting the measurement (with sign) of the Active Power P (W)

Measured values→ TotVAr: for reporting the measurement (with sign) of the Reactive Power Q (VAr)

Measured values→ Hz: for reporting the measurement of the f (Hz) of the phase 4

Measured values→ PPV: for reporting the measurement of the phase-to-phase Voltages V4-8, V8-12, V12-4 (V)

Measured values→ A: for reporting the measurement of the Line Currents I4, I8, I12 (A).

7.1.4.4. Periodic average measurements of the THD (Line V and I)

Table 11 – LNInstance: 1 - prefix: mTHD – MHAI1				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
EEHealth	INS	External equipment health (external sensor)		O
EEName	DPL	External equipment name plate		O
Measured Values				
Hz	MV	Basic Frequency		C
HA	HWYE	Sequence of Harmonics or Interharmonics current		O
HPhV	HWYE	Sequence of Harmonics or Interharominics phase to ground voltages		O
HPPV	HDEL	Sequence of Harmonics or Interharmonics phase to phase voltages		O
HW	HWYE	Sequence of Harmonics or Interharmonics active power		O
HVAr	HWYE	Sequence of Harmonics or Interharmonics reactive power		O
HVA	HWYE	Sequence of Harmonics or Interharmonics apparent power		O
HRmsA	WYE	Current RMS Harmonic or Interharmonics (un-normalized Total harmonic disortion, Thd)		O
HRmsPhV	WYE	Voltage RMS Harmonic or Interharmonics (un-normalized Thd) for phase to ground		O
HRmsPPV	DEL	Voltage RMS Harmonic or Interharmonics (un-normalized Thd) for phase to phase		O
HTuW	WYE	Total phase Harmonic or Interharmonics active power (no fundamental) unsigned sum		O
HTsW	WYE	Total phase Harmonic or Interharmonic active power (no fundamental) signed sum		O
HATm	WYE	Current Time product		O
HKf	WYE	K Factor		O
HTdf	WYE	Transformer derating factor		O
ThdA	WYE	Current Total Harmonic or Interharmonic Distortion (different methods)		R
ThdOddA	WYE	Current Total Harmonic or Interharmonic Distortion (different methods – odd components)		O
ThdEvnA	WYE	Current Total Harmonic or Interharmonic Distortion (different methods – even components)		O

TddA	WYE	Current Total Demand Distortion per IEEE 519		O
TddOddA	WYE	Current Total Demand Distortion per IEEE 519 (odd components)		O
TddEvnA	WYE	Current Total Demand Distortion per IEEE 519 (even components)		O
ThdPhV	WYE	Voltage Total Harmonic or Interharmonic Distortion (different methods) for phase to ground		R
ThdOddPhV	WYE	Voltage Total Harmonic or Interharmonic Distortion (different methods) for phase to ground (odd components)		O
ThdEvnPhV	WYE	Voltage Total Harmonic or Interharmonic Distortion (different methods) for phase to ground (even components)		O
ThdPPV	DEL	Voltage Total Harmonic or Interharmonic Distortion (different methods) for phase to phase		O
ThdOddPPV	DEL	Voltage Total Harmonic or Interharmonic Distortion (different methods) for phase to phase (odd components)		O
ThdEvnPPV	DEL	Voltage Total Harmonic or Interharmonic Distortion (different methods) for phase to phase (even components)		O
HCfPhV	WYE	Voltage crest factors (peak waveform value/sqrt(2)/fundamental) for phase to ground		O
HCfPPV	DEL	Voltage crest factors (peak waveform value/sqrt(2)/fundamental) for phase to phase		O
HCfA	WYE	Current crest factors (peak waveform value/sqrt(2)/fundamental)		O
HTif	WYE	Voltage Telephone Influence Factor		O
Settings				
HzSet	ASG	Basic frequency		C
EvTmms	ASG	Evaluation time (time window) determines the lowest frequency		O
NumCyc	ING	Number of cycles of the basic frequency		O
ThdAVal	ASG	ThdA alarm Setting – value entered in %		O
ThdVVal	ASG	ThdPhV / ThdPPV alarm Setting – value entered in %		O
ThdATmms	ING	ThdA alarm time delay in ms		O
ThdVTmms	ING	ThdPhV / ThdPPV alarm time delay in ms		O
NomA	ASG	Normalising demand current used in IEEE 519 TDD calculation		O

Condition C: Hz and HzSet are exclusive.

NOTES:

Measured values→ ThdA: for reporting the measurement of the Line Current THD (all the phases)

Measured values→ ThdPhV: for reporting the measurement of the Line Voltage THD (all the phases).

7.1.4.5. Event-driven measurements: Line Current and Voltages, 3Io and 3Vo

Table 12 – LNInstance: 1 - prefix: eIV_o – MMXU2 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
EEHealth	INS	External equipment health (external sensor)		O
Measured values				

TotW	MV	Total Active Power (Total P)		O
TotVAr	MV	Total Reactive Power (Total Q)		O
TotVA	MV	Total Apparent Power (Total S)		O
TotPF	MV	Average Power Factor (Total PF)		O
Hz	MV	Frequency		O
PPV	DEL	Phase to phase voltages (VL1VL2, ...)		O
PhV	WYE	Phase to ground voltages (VL1ER, ...)		R
A	WYE	Phase currents (IL1, IL2, IL3)		R
W	WYE	Phase active power (P)		O
Var	WYE	Phase reactive power (Q)		O
VA	WYE	Phase apparent power (S)		O
PF	WYE	Phase power factor		O
Z	WYE	Phase Impedance		O

NOTES:

Measured values→ PhV: for reporting the measurement of the Line Voltages E4, E8, E12 (magnitude (V) and angle) and 3Vo (magnitude)

Measured values→ A: for reporting the measurement of the Line Currents I4, I8, I12 (magnitude (A) and angle) and 3Io (magnitude).

7.1.4.6. Event-driven measurements: frequencies, df/dt, 3Io-3Vo phase difference angle

Table 13 – LNInstance: 1 - prefix: efdfAo – GGIO3 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
EEHealth	INS	External equipment health (external sensor)		O
EEName	DPL	External equipment name plate		O
Loc	SPS	Local operation		O
OpCntRs	INC	Resetable operation counter		O
Measured values				
AnIn1	MV	Analogue input (1)		R
AnIn2	MV	Analogue input (2)		R
AnIn3	MV	Analogue input (3)		R
AnIn4	MV	Analogue input (4)		R
AnIn5	MV	Analogue input (5)		R
AnIn6	MV	Analogue input (6)		R
AnIn7	MV	Analogue input (7)		R
Controls				
SPCSO	SPC	Single point controllable status output		O
DPCSO	DPC	Double point controllable status output		O
ISCSO	INC	Integer status controllable status output		O
Status Information				
IntIn	INS	Integer status input		O

Alm	SPS	General single alarm		O
Ind	SPS	General indication (binary input)		O

NOTES:

Measured values→ AnIn1: for reporting the measurement of the phase 4 Frequency f (Hz)

Measured values→ AnIn2: for reporting the measurement of the phase 8 Frequency f (Hz)

Measured values→ AnIn3: for reporting the measurement of the phase 12 Frequency f (Hz)

Measured values→ AnIn4: for reporting the measurement of the df4/dt (Hz/s)

Measured values→ AnIn5: for reporting the measurement of the df8/dt (Hz/s)

Measured values→ AnIn6: for reporting the measurement of the df12/dt (Hz/s)

Measured values→ AnIn7: for reporting the measurement of the 3Io-3Vo Phase difference angle.

7.1.5 Management of the Circuit Breaker controlled by the MFP

The following LNs are modelled in the MFP in order to enable the communication (Controls and Reports) concerning the commands, the position, the possible conflicts of concurrent actions and the anomalies/failures of the Circuit Breaker.

7.1.5.1. Circuit Breaker Open/Close commands

Table 14 – LNInstance: 1 - prefix: Cmd52 – CSWI1 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
Loc	SPS	Local operation		O
OpCntRs	INC	Resetable operation counter		R
Controls				
Pos	DPC	Switch, general		M
PosA	DPC	Switch L1		O
PosB	DPC	Switch L2		O
PosC	DPC	Switch L3		O
OpOpn	ACT	Operation "Open Switch"	T	R
OpCls	ACT	Operation "Close Switch"	T	R

NOTES:

Common Logical Node Information→ OpCntRs: to count and store the number of the Circuit Breaker position changes

Controls → Pos: for running the Circuit Breaker Open/Close command

Controls → OpOpn: for reporting the Circuit Breaker Open operation

Controls → OpCls: for reporting the Circuit Breaker Close operation.

7.1.5.2. Circuit Breaker position (52)

Table 15 – LNInstance: 1 - prefix: St52 – XCBR1 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
Loc	SPS	Local operation (local means without substation automation communication, hardwired direct control)		M
EEHealth	INS	External equipment health		O
EEName	DPL	External equipment name plate		O
OpCnt	INS	Operator counter		M
Controls				
Pos	DPC	Switch position		M
BlkOpn	SPC	Block opening		M
BlkCls	SPC	Block closing		M
ChaMotEna	SPC	Charger motor enabled		O
Metered Values				
SumSwARs	BCR	Sum of Switched Amperes, resettable		O
Status Information				
CBOpCap	INS	Circuit breaker operating capability		M
POWCap	INS	Point On Wave switching capability		O
MaxOpCap	INS	Circuit breaker operating capability when fully charged		O

NOTES:

Controls → Pos: for reporting the Circuit Breaker position (intermediate-state | off | on | bad-state).

7.1.5.3. Circuit Breaker operations Interlocking

The CILO LN is used to report the result of the Interlocking function (ref. GSTP101) concerning the requests of Circuit Breaker Position Change (e.g. issued by an operator) to the RTU.

Table 16 – LNInstance: 1 - prefix: IB52 – CILO1 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
Status Information				
EnaOpn	SPS	Enable Open		M
EnaCls	SPS	Enable Close		M

NOTES:

Status Information→ EnaOpn: for reporting the Enabling of any Circuit Breaker Open command.

Status Information→ EnaCls: for reporting the Enabling of any Circuit Breaker Close command.

7.1.5.4. External Trip of the MV Circuit Breaker issued by the EAC

The following LN is used to subscribe the trip command of the Circuit Breaker received via GOOSE message and issued by IED EAC.

Table 17 – LNInstance: 1 - prefix: EACCmd – GGIO4 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
EEHealth	INS	External equipment health (external sensor)		O
EEName	DPL	External equipment name plate		O
Loc	SPS	Local operation		O
OpCntRs	INC	Resetable operation counter		R
Measured values				
AnIn	MV	Analogue input		O
Controls				
SPCSO	SPC	Single point controllable status output		R
DPCSO	DPC	Double point controllable status output		O
ISCSO	INC	Integer status controllable status output		O
Status Information				
IntIn	INS	Integer status input		O
Alm	SPS	General single alarm		O
Ind	SPS	General indication (binary input)		O

NOTES:

Common Logical Node Information→ OpCntRs: to count and store the number of events occurred

Controls → SPCSO: for subscribing the External Trip of the MV Circuit Breaker issued by the EAC:

a. 1 = Circuit Breaker trip (open) command

b. 0= Circuit Breaker close command.

7.1.6 States of the Physical I/O Connector pins of the MFP

The following LN models a set of Boolean variables whose values represent the states of a set of physical I/O's (belonging to a connector) used by specific internal logics of the MFP.

Table 18 – LNInstance: 1 - prefix: PhyIO – GGIO5 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
EEHealth	INS	External equipment health (external sensor)		O
EEName	DPL	External equipment name plate		O

Loc	SPS	Local operation		O
OpCntRs	INC	Resetable operation counter		R
Measured values				
AnIn	MV	Analogue input		O
Controls				
SPCSO	SPC	Single point controllable status output		O
DPCSO	DPC	Double point controllable status output		O
ISCSO	INC	Integer status controllable status output		O
Status Information				
IntIn	INS	Integer status input		O
Alm	SPS	General single alarm		O
Ind1	SPS	General indication (binary input) (1)		R
Ind2	SPS	General indication (binary input) (2)		R
Ind3	SPS	General indication (binary input) (3)		R
Ind4	SPS	General indication (binary input) (4)		R
Ind5	SPS	General indication (binary input) (5)		R
Ind6	SPS	General indication (binary input) (6)		R
Ind7	SPS	General indication (binary input) (7)		R
Ind8	SPS	General indication (binary input) (8)		R
Ind9	SPS	General indication (binary input) (9)		R
Ind10	SPS	General indication (binary input) (10)		R
Ind11	SPS	General indication (binary input) (11)		R
Ind12	SPS	General indication (binary input) (12)		R

NOTES:

Common Logical Node Information → OpCntRs: to count and store the number of events occurred (e.g. settings)

Status Information → Ind1: MFP Physical IN 1 State

Status Information → Ind2: MFP Physical IN 2 State

Status Information → Ind3: MFP Physical IN 3 State

Status Information → Ind4: MFP Physical IN 4 State

Status Information → Ind5: MFP Physical IN 5 State

Status Information → Ind6: MFP Physical IN 6 State

Status Information → Ind7: MFP Physical OUT 1 State

Status Information → Ind8: MFP Physical OUT 2 State

Status Information → Ind9: MFP Physical OUT 3 State

Status Information → Ind10: MFP Physical OUT 4 State

Status Information → Ind11: MFP Physical OUT 5 State

Status Information → Ind12: MFP Physical OUT 6 State.

7.1.7 Reference NTP Server addressing and Time Sync status

The following LN models the

a. IP Address of the NTP Server for the time-synchronization of the MFP; as in the Ed.1 of the IEC 61850 this setting is not standardized (please, refer to IEC 61850-6 Communication section and to IEC61850 7-3, IEC61850-7-4 for the Data Modelling), here below an integer is internally used for each byte of the address (X.Y.Z.K).

b. the flag to enable/disable the communication with it;

c. the status of the IED time-synchronization (Synched or free-running, consistent with the TimeQuality in the IED TimeStamps).

Table 19 – LNInstance: 1 - prefix: NTPsr – GGIO6 type

Attribute Name	Attribute Type	Explanation	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
EEHealth	INS	External equipment health (external sensor)		O
EEName	DPL	External equipment name plate		O
Loc	SPS	Local operation		O
OpCntRs	INC	Resetable operation counter		R
Measured values				
AnIn	MV	Analogue input		O
Controls				
SPCSO	SPC	Single point controllable status output		R
DPCSO	DPC	Double point controllable status output		O
ISCSO1	INC	Integer status controllable status output (1)		R
ISCSO2	INC	Integer status controllable status output (2)		R
ISCSO3	INC	Integer status controllable status output (3)		R
ISCSO4	INC	Integer status controllable status output (4)		R
Status Information				
IntIn	INS	Integer status input		O
Alm	SPS	General single alarm		O
Ind	SPS	General indication (binary input)		R

NOTES:

Common Logical Node Information → OpCntRs: to count and store the number of events occurred (settings)

Controls → SPCSO: for enabling the time synchronization of the MFP clock via the reference NTP Server:

a. 0 = free-running (internal clock)

b. 1 = time synchronization via NTP Server

Controls → ISCSO1: for setting the byte X of the NTP Server IPv4 (X.Y.Z.K) in the range [0..255]

Controls → ISCSO2: for setting the byte Y of the NTP Server IPv4 (X.Y.Z.K) in the range [0..255]

Controls → ISCSO3: for setting the byte Z of the NTP Server IPv4 (X.Y.Z.K) in the range [0..255]

Controls → ISCSO4: for setting the byte K of the NTP Server IPv4 (X.Y.Z.K) in the range [0..255]

Status → Ind: for notifying the Time Synchronization status of the IED:

c. 0 = free running

d. 1 = synched to the reference NTP server.

7.2 Logical Device Protections: details of the Logical Nodes

The Logical Device Protections (LD_Prot) includes all the Logical Nodes which data is used in the communication supporting the Protection functions (and any related ancillary function) implemented in the MFP. Some special protections settings that are typical of the ENEL network operation, will be modeled by extension of the standard LNs according to the rules set out in the IEC 61850

Table 20 – LLN01 type				
Attribute Name	**Attribute Type**	**Explanation**	**T**	**M/O**
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
Loc	SPS	Local operation for complete logical device		O
OpTmh	INS	Operation Time		O
Controls				
Diag	SPC	Run Diagnostic		O
LEDRs	SPC	LED reset	T	O

Table 21 – LNInstance: 1 – LPHD2 type				
Attribute Name	**Attribute Type**	**Explanation**	**T**	**M/O**
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
PhyNam	DPL	Physical device name plate		M
PhyHealth	INS	Physical device health		M
OutOv	SPS	Output communications buffer overflow		O
Proxy	SPS	Indicates if this LN is a proxy		M
InOv	SPS	Input communications buffer overflow		O
NumPwrUp	INS	Number of Power ups		O
WrmStr	INS	Number of Warm Starts		O
WacTrg	INS	Number of watchdog device resets detected		O
PwrUp	SPS	Power Up detected		O
PwrDn	SPS	Power Down detected		O
PwrSupAlm	SPS	External power supply alarm		O
RsStat	SPC	Reset device statistics	T	O

7.2.1 Special settings of the MFP protection stages

Most of the MFP protection stages, compared to the models standardized in IEC61850-7-4, require the following additional parameters according to GSTP101.

7.2.1.1. Behaviour of the MFP protection stages

This parameter is used to set, for each single stage, the operating mode according to the following options:

a. 0 = Start + Operate,

b. 1 = Start only

The combination of this setting with the DO Mod, available in all Stages, allows to define the following set of statuses:

Stage x Status	Mod	SPCSOx
Disabled	5	--
Start only	1	1
Start + Operate	1	0

According to the extension rules of the IEC 61850, the LN PXXX is enhanced with the new DO **PBst**, a Setting with SPG type**.**

7.2.1.2. Participation in the Logic Selectivity function of the MFP protection stages

This parameter is used to program, for each stage using it, the participation (publication and subscription of dedicated GOOSE messages, ref. section 7.4.2) in the Logic Selectivity function.

According to the extension rules of the IEC 61850, the LN PXXX is enhanced with the new DO **FFSEna**, a Setting with SPG type**.**

7.2.1.3. Block due to harmonic restraint protection of the MFP protection stages

This parameter allows programming, for each stage using it, the possibility of blocking the protection stage due to 2nd harmonic.

According to the extension rules of the IEC 61850, the LN PXXX is enhanced with the new DO **Bl2ndHEna**, a Setting with SPG type**.**

7.2.1.4. Reset of the backup timer Tr

This parameter allows programming, for each stage using it, the reset of the backup timer Tr used in the Logic Selectivity Function.

According to the extension rules of the IEC 61850, the LN PXXX is enhanced with the new DO **RsDITEna**, a Setting with SPG type**.**

7.2.2 Protection stages acceleration

In this section are specified the LN used to:

a. Issue the “protection stages acceleration” command towards other IEDs in the substation, relevant for stages with dual time calibrations,

b. receive the “protection stages acceleration” command coming from other IEDs in the substation, relevant for stages with dual time calibrations.

7.2.2.1. Protection stages acceleration command towards other IEDs in the substation

Table 22 – LNInstance: 1 - prefix: CSPMng – GGIO4 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		

Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
EEHealth	INS	External equipment health (external sensor)		O
EEName	DPL	External equipment name plate		O
Loc	SPS	Local operation		O
OpCntRs	INC	Resetable operation counter		R
Measured values				
AnIn	MV	Analogue input		O
Controls				
SPCSO	SPC	Single point controllable status output		R
DPCSO	DPC	Double point controllable status output		O
ISCSO	INC	Integer status controllable status output		O
Status Information				
IntIn	INS	Integer status input		O
Alm	SPS	General single alarm		O
Ind	SPS	General indication (binary input)		O

NOTES:

Common Logical Node Information→ OpCntRs: to count and store the number of settings occurred

Controls→ SPCSO: for issuing the "protection stages acceleration" command towards other IEDs in the substation:

a. 0 = base threshold

b. 1 = accelerated threshold.

The MFP is ready to issue the "protection stages acceleration command" to other IEDs in the substation (typically MTP and MFP). It will publish a GOOSE message carrying the following information:

c. MFP /LD_Prot/GGIO7/CSPMngGGIO1/SPCSO

7.2.2.2. Protection stages acceleration command coming from other IEDs in the substation

Table 23 – LNInstance: 1 - prefix: CSPMon – GGIO7 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
EEHealth	INS	External equipment health (external sensor)		O
EEName	DPL	External equipment name plate		O
Loc	SPS	Local operation		O
OpCntRs	INC	Resetable operation counter		R
Measured values				
AnIn	MV	Analogue input		O
Controls				
SPCSO1	SPC	Single point controllable status output (1)		R

SPCSO2	SPC	Single point controllable status output (2)		R
…	…	…		…
SPCSO22	SPC	Single point controllable status output (22)		R
DPCSO	DPC	Double point controllable status output		O
ISCSO	INC	Integer status controllable status output		O
Status Information				
IntIn	INS	Integer status input		O
Alm	SPS	General single alarm		O
Ind	SPS	General indication (binary input)		O

NOTES:

Common Logical Node Information→ OpCntRs: to count and store the number of settings occurred

Controls→ SPCSO1…9: for subscribing the "protection stages acceleration" command coming from the other 9 MFP installed in the same busbar Sx of the substation:

a. 0 = base threshold

b. 1 = accelerated threshold

Controls→ SPCSO10…19: for subscribing the "protection stages acceleration" command coming from the 10 MFP installed in the other busbar Sy of the substation

c. 0 = base threshold

d. 1 = accelerated threshold

Controls→ SPCSO20: for subscribing the "protection stages acceleration" command coming from the MTP installed in the same busbar Sx of the substation:

e. 0 = base threshold

f. 1 = accelerated threshold

Controls→ SPCSO21: for subscribing the "protection stages acceleration" command coming from the MTP installed in the other busbar Sy of the substation

g. 0 = base threshold

h. 1 = accelerated threshold

Controls→ SPCSO22: for subscribing the "protection stages acceleration" command coming from the MFP operating as the Section circuit-breaker (or busbar coupler) of the substation

i. 0 = base threshold

j. 1 = accelerated threshold.

This LN is ready to receive via GOOSE the "protection stages acceleration command" published by other IEDs (MFP and MTP) in the substation.

7.2.3 Phase Overcurrent protection (51)

This protection consists of four stages with dual time calibration; each stage can be configured as independent-time (Ti) or dependent-time (Td) with selectable standard curves. An ad-hoc LN class is provided, according to the extension rules of the IEC 61850; it permits the selection of the operating modes, special functions and the configuration of the parameters linked to the curve (Ip, Tp).

7.2.3.1. 51.S1 (Ti+Td) stage with dual time calibration

Table 24 – LNInstance: 1 - prefix: P51S1 – PEOC1 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
OpCntRs	INC	Resetable operation counter		R
Status Information				
Str	ACD	Start		M
Op	ACT	Operate	T	M
AOp	ACT	enel Additional/Accelerated Operate	T	R
TmASt	CSD	Active curve characteristic		O
Settings				
TmACrv	CURVE	Operating Curve Type		R
StrVal	ASG	Start Value		R
TmMult	ASG	Time Dial Multiplier		O
MinOpTmms	ING	Minimum Operate Time		R
MaxOpTmms	ING	Maximum Operate Time		O
OpDlTmms	ING	Operate Delay Time		R
AOpDlTmms	ING	enel Additional/Accelerated Operate Delay Time		R
TypRsCrv	ING	Type Reset Curve		O
RsDlTmms	ING	Reset Delay Time		O
DirMod	ING	Directional Mode		O
PAccelEna	SPG	enel Protection Stage Acceleration Enabling		R
PBst	SPG	enel Protection Behaviour (1=Str 2= Str+Op)		R
FFSEna	SPG	enel Fast Fault Selection Enabling (Participation in the Logic Selectivity)		R
Bl2ndHEna	SPG	enel Block due to 2nd H Enabling		R
RsDlTEna	SPG	enel Reset Delay Time Enabling (Logical Block /Tr)		O
TmACStrVal	ASG	enel Active curve characteristic Start Value (Ip for Td curve)		R
TmACOpDlTm	ING	enel Active curve characteristic Operate Delay Time (Tp for Td curve)		R
CLPMod	ING	enel Cold Load Pickup Mode		R
CLPOpPer	ASG	enel Cold Load Pickup Operating Period		R

NOTES:

Common Logical Node Information→ Mod: for handling the **Enabling/Disabling** command (1/5) of this protection stage (base and accelerated).

Common Logical Node Information→ OpCntRs: to count and store the number of operations of this stage (base and accelerated)

Status Information→ Str: for issuing the Start signal of this stage (base and accelerated)

Status Information→ Op: for issuing the Tripping signal of this stage (base only)

Status Information→ AOp: for sending the Tripping signal of this stage (accelerated only)

Settings→ TmACrv: for setting the **IEC curve type** in case the stage is Td (base only) or if the stage is Ti:

a. 9 = NIT (IEC Normal Inverse)

b. 10 = VIT (IEC Very Inverse)

c. 12 = EIT (IEC Extremely Inverse)

d. 14 = LIT (IEC Long – Time Inverse)

e. 15 = Ti (IEC Definite Time)

Settings→ StrVal: for setting the current threshold of this stage (base and accelerated) when Ti (min..max; step; default; m.u.)

Settings→ MinOpTmms: for setting the minimum duration time of the accelerated (only) stage (min..max; step; default; m.u.)

Settings→ OpDlTmms: for setting the operate delay time of the stage **T51.S1** (base only) when Ti (min..max; step; default; m.u.)

Settings→ AOpDlTmms: for setting the operate delay time of the stage **T51.S1_c** (accelerated only) when Ti (min..max; step; default; m.u.)

Settings→ PAccelEna: for enabling the dual time calibration (acceleration) of this stage:

f. 0 = base only

g. 1 = base + accelerated

Settings→ PBst: for setting the behaviour of this stage (base and accelerated):

h. 0 = Start + Operate

i. 1 = Start only

Settings → FFSEna: for setting the participation in the Logic Selectivity function (publishing and subscribing) of this stage (base and accelerated):

j. 0 = excluded

k. 1 = participating

Settings → Bl2ndHEna: for allowing the blocking, due to 2nd harmonic restraint protection, of this stage (base and accelerated):

l. 0 = not blockable

m. 1 = stage Sx blockable due to 2nd harmonic

Settings → TmACStrVal: for setting the Ip of the curve in case of Td stage (base only) (min..max; step; default; m.u.)

Settings → TmACOpDlTm: for setting the Tp of the curve in case of Td stage (base only) (min..max; step; default; m.u.)

Settings → CLPMod: for setting the mode of the Cold Load Pickup function for this stage:

n. 0 = Off (Default)

o. 1 = On – Stage Block

p. 2 = On – Stage Modification

Settings → CLPOpPer: for setting the Operating Period of the Cold Load Pickup for this stage (0..100;0.01;0.1 sec).

7.2.3.2. 51.S2 (Ti+Td) stage with dual time calibration

Table 25 – LNInstance: 1 - prefix: P51S2 – PEOC1 type

Attribute Name	Attribute Type	Explanation	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
OpCntRs	INC	Resetable operation counter		R
Status Information				
Str	ACD	Start		M
Op	ACT	Operate	T	M
AOp	ACT	enel Additional/Accelerated Operate	T	R
TmASt	CSD	Active curve characteristic		O
Settings				
TmACrv	CURVE	Operating Curve Type		R
StrVal	ASG	Start Value		R
TmMult	ASG	Time Dial Multiplier		O
MinOpTmms	ING	Minimum Operate Time		R
MaxOpTmms	ING	Maximum Operate Time		O
OpDlTmms	ING	Operate Delay Time		R
AOpDlTmms	ING	enel Additional/Accelerated Operate Delay Time		R
TypRsCrv	ING	Type Reset Curve		O
RsDlTmms	ING	Reset Delay Time		O
DirMod	ING	Directional Mode		O
PAccelEna	SPG	enel Protection Stage Acceleration Enabling		R
PBst	SPG	enel Protection Behaviour (1=Str 2= Str+Op)		R
FFSEna	SPG	enel Fast Fault Selection Enabling (Participation in the Logic Selectivity)		R
Bl2ndHEna	SPG	enel Block due to 2nd H Enabling		R
RsDlTEna	SPG	enel Reset Delay Time Enabling (Logical Block /Tr)		O
TmACStrVal	ASG	enel Active curve characteristic Start Value (Ip for Td curve)		R
TmACOpDlTm	ING	enel Active curve characteristic Operate Delay Time (Tp for Td curve)		R
CLPMod	ING	enel Cold Load Pickup Mode		R
CLPOpPer	ASG	enel Cold Load Pickup Operating Period		R

NOTES:

Common Logical Node Information→ Mod: for handling the *Enabling/Disabling* command (1/5) of this protection stage (base and accelerated)

Common Logical Node Information→ OpCntRs: to count and store the number of operations of this stage (base and accelerated)

Status Information→ Str: for issuing the Start signal of this stage (base and accelerated)

Status Information→ Op: for issuing the Tripping signal of this stage (base only)

Status Information→ AOp: for sending the Tripping signal of this stage (accelerated only)

Settings→ TmACrv: for setting the **IEC curve type** in case the stage is Td (base only) or if the stage is Ti:

a. 9 = NIT (IEC Normal Inverse)

b. 10 = VIT (IEC Very Inverse)

c. 12 = EIT (IEC Extremely Inverse)

d. 14 = LIT (IEC Long – Time Inverse)

e. 15 = Ti (IEC Definite Time)

Settings→ StrVal: for setting the current threshold of this stage (base and accelerated) when Ti (min..max; step; default; m.u.)

Settings→ MinOpTmms: for setting the minimum duration time of the accelerated (only) stage (min..max; step; default; m.u.)

Settings→ OpDlTmms: for setting the operate delay time of the stage **T51.S2** (base only) when Ti (min..max; step; default; m.u.)

Settings→ AOpDlTmms: for setting the operate delay time of the stage **T51.S2_c** (accelerated only) when Ti (min..max; step; default; m.u.)

Settings→ PAccelEna: for enabling the dual time calibration (acceleration) of this stage:

f. 0 = base only

g. 1 = base + accelerated

Settings→ PBst: for setting the behaviour of this stage (base and accelerated):

h. 0 = Start + Operate

i. 1 = Start only

Settings → FFSEna: for setting the participation in the Logic Selectivity function (publishing and subscribing) of this stage (base and accelerated):

j. 0 = excluded

k. 1 = participating

Settings → Bl2ndHEna: for allowing the blocking, due to 2nd harmonic restraint protection, of this stage (base and accelerated):

l. 0 = not blockable

m. 1 = stage Sx blockable due to 2nd harmonic

Settings → TmACStrVal: for setting the Ip of the curve in case of Td stage (base only) (min..max; step; default; m.u.)

Settings → TmACOpDlTm: for setting the Tp of the curve in case of Td stage (base only) (min..max; step; default; m.u.)

Settings → CLPMod: for setting the mode of the Cold Load Pickup function for this stage:

n. 0 = Off (Default)

o. 1 = On – Stage Block

p. 2 = On – Stage Modification

Settings → CLPOpPer: for setting the Operating Period of the Cold Load Pickup for this stage (0..100;0.01;0.1 sec).

7.2.3.3. 51.S3 (Ti+Td) stage with dual time calibration

Table 26 – LNInstance: 1 - prefix: P51S3 – PEOC1 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
OpCntRs	INC	Resetable operation counter		R
Status Information				
Str	ACD	Start		M
Op	ACT	Operate	T	M
AOp	ACT	enel Additional/Accelerated Operate	T	R
TmASt	CSD	Active curve characteristic		O
Settings				
TmACrv	CURVE	Operating Curve Type		R
StrVal	ASG	Start Value		R
TmMult	ASG	Time Dial Multiplier		O
MinOpTmms	ING	Minimum Operate Time		R
MaxOpTmms	ING	Maximum Operate Time		O
OpDlTmms	ING	Operate Delay Time		R
AOpDlTmms	ING	enel Additional/Accelerated Operate Delay Time		R
TypRsCrv	ING	Type Reset Curve		O
RsDlTmms	ING	Reset Delay Time		O
DirMod	ING	Directional Mode		O
PAccelEna	SPG	enel Protection Stage Acceleration Enabling		R
PBst	SPG	enel Protection Behaviour (1=Str 2= Str+Op)		R
FFSEna	SPG	enel Fast Fault Selection Enabling (Participation in the Logic Selectivity)		R
Bl2ndHEna	SPG	enel Block due to 2nd H Enabling		R
RsDlTEna	SPG	enel Reset Delay Time Enabling (Logical Block /Tr)		O
TmACStrVal	ASG	enel Active curve characteristic Start Value (Ip for Td curve)		R
TmACOpDlTm	ING	enel Active curve characteristic Operate Delay Time (Tp for Td curve)		R
CLPMod	ING	enel Cold Load Pickup Mode		R
CLPOpPer	ASG	enel Cold Load Pickup Operating Period		R

NOTES:

Common Logical Node Information→ Mod: for handling the **Enabling/Disabling** command (1/5) of this protection stage (base and accelerated)

Common Logical Node Information→ OpCntRs: to count and store the number of operations of this stage (base and accelerated)

Status Information→ Str: for issuing the Start signal of this stage (base and accelerated)

Status Information→ Op: for issuing the Tripping signal of this stage (base only)

Status Information→ AOp: for sending the Tripping signal of this stage (accelerated only)

Settings→ TmACrv: for setting the **IEC curve type** in case the stage is Td (base only) or if the stage is Ti:

a. 9 = NIT (IEC Normal Inverse)

b. 10 = VIT (IEC Very Inverse)

c. 12 = EIT (IEC Extremely Inverse)

d. 14 = LIT (IEC Long – Time Inverse)

e. 15 = Ti (IEC Definite Time)

Settings→ StrVal: for setting the current threshold of this stage (base and accelerated) when Ti (min..max; step; default; m.u.)

Settings→ MinOpTmms: for setting the minimum duration time of the accelerated (only) stage (min..max; step; default; m.u.)

Settings→ OpDlTmms: for setting the operate delay time of the stage **T51.S3** (base only) when Ti (min..max; step; default; m.u.)

Settings→ AOpDlTmms: for setting the operate delay time of the stage **T51.S3_c** (accelerated only) when Ti (min..max; step; default; m.u.)

Settings→ PAccelEna: for enabling the dual time calibration (acceleration) of this stage:

f. 0 = base only

g. 1 = base + accelerated

Settings→ PBst: for setting the behaviour of this stage (base and accelerated):

h. 0 = Start + Operate

i. 1 = Start only

Settings → FFSEna: for setting the participation in the Logic Selectivity function (publishing and subscribing) of this stage (base and accelerated):

j. 0 = excluded

k. 1 = participating

Settings → Bl2ndHEna: for allowing the blocking, due to 2nd harmonic restraint protection, of this stage (base and accelerated):

l. 0 = not blockable

m. 1 = stage Sx blockable due to 2nd harmonic

Settings → TmACStrVal: for setting the Ip of the curve in case of Td stage (base only) (min..max; step; default; m.u.)

Settings → TmACOpDlTm: for setting the Tp of the curve in case of Td stage (base only) (min..max; step; default; m.u.)

Settings → CLPMod: for setting the mode of the Cold Load Pickup function for this stage:

n. 0 = Off (Default)

o. 1 = On – Stage Block

p. 2 = On – Stage Modification

Settings → CLPOpPer: for setting the Operating Period of the Cold Load Pickup for this stage (0..100;0.01;0.1 sec).

7.2.3.4. 51.S4 (Ti+Td) stage with dual time calibration

Table 27 – LNInstance: 1 - prefix: P51S4 – PEOC1 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
OpCntRs	INC	Resetable operation counter		R
Status Information				
Str	ACD	Start		M
Op	ACT	Operate	T	M
AOp	ACT	enel Additional/Accelerated Operate	T	R
TmASt	CSD	Active curve characteristic		O
Settings				
TmACrv	CURVE	Operating Curve Type		R
StrVal	ASG	Start Value		R
TmMult	ASG	Time Dial Multiplier		O
MinOpTmms	ING	Minimum Operate Time		R
MaxOpTmms	ING	Maximum Operate Time		O
OpDlTmms	ING	Operate Delay Time		R
AOpDlTmms	ING	enel Additional/Accelerated Operate Delay Time		R
TypRsCrv	ING	Type Reset Curve		O
RsDlTmms	ING	Reset Delay Time		O
DirMod	ING	Directional Mode		O
PAccelEna	SPG	enel Protection Stage Acceleration Enabling		R
PBst	SPG	enel Protection Behaviour (1=Str 2= Str+Op)		R
FFSEna	SPG	enel Fast Fault Selection Enabling (Participation in the Logic Selectivity)		R
Bl2ndHEna	SPG	enel Block due to 2nd H Enabling		R
RsDlTEna	SPG	enel Reset Delay Time Enabling (Logical Block /Tr)		O
TmACStrVal	ASG	enel Active curve characteristic Start Value (Ip for Td curve)		R
TmACOpDlTm	ING	enel Active curve characteristic Operate Delay Time (Tp for Td curve)		R
CLPMod	ING	enel Cold Load Pickup Mode		R
CLPOpPer	ASG	enel Cold Load Pickup Operating Period		R

NOTES:

Common Logical Node Information→ Mod: for handling the **Enabling/Disabling** command (1/5) of this protection stage (base and accelerated)

Common Logical Node Information→ OpCntRs: to count and store the number of operations of this stage (base and accelerated)

Status Information→ Str: for issuing the Start signal of this stage (base and accelerated)

Status Information→ Op: for issuing the Tripping signal of this stage (base only)

Status Information→ AOp: for sending the Tripping signal of this stage (accelerated only)

Settings→ TmACrv: for setting the **IEC curve type** in case the stage is Td (base only) or if the stage is Ti:

a. 9 = NIT (IEC Normal Inverse)

b. 10 = VIT (IEC Very Inverse)

c. 12 = EIT (IEC Extremely Inverse)

d. 14 = LIT (IEC Long – Time Inverse)

e. 15 = Ti (IEC Definite Time)

Settings→ StrVal: for setting the current threshold of this stage (base and accelerated) when Ti (min..max; step; default; m.u.)

Settings→ MinOpTmms: for setting the minimum duration time of the accelerated (only) stage (min..max; step; default; m.u.)

Settings→ OpDlTmms: for setting the operate delay time of the stage **T51.S4** (base only) when Ti (min..max; step; default; m.u.)

Settings→ AOpDlTmms: for setting the operate delay time of the stage **T51.S4_c** (accelerated only) when Ti (min..max; step; default; m.u.)

Settings→ PAccelEna: for enabling the dual time calibration (acceleration) of this stage:

f. 0 = base only

g. 1 = base + accelerated

Settings→ PBst: for setting the behaviour of this stage (base and accelerated):

h. 0 = Start + Operate

i. 1 = Start only

Settings → FFSEna: for setting the participation in the Logic Selectivity function (publishing and subscribing) of this stage (base and accelerated):

j. 0 = excluded

k. 1 = participating

Settings → Bl2ndHEna: for allowing the blocking, due to 2nd harmonic restraint protection, of this stage (base and accelerated):

l. 0 = not blockable

m. 1 = stage Sx blockable due to 2nd harmonic

Settings → TmACStrVal: for setting the Ip of the curve in case of Td stage (base only) (min..max; step; default; m.u.)

Settings → TmACOpDlTm: for setting the Tp of the curve in case of Td stage (base only) (min..max; step; default; m.u.)

Settings → CLPMod: for setting the mode of the Cold Load Pickup function for this stage:

n. 0 = Off (Default)

o. 1 = On – Stage Block

p. 2 = On – Stage Modification

Settings → CLPOpPer: for setting the Operating Period of the Cold Load Pickup for this stage (0..100;0.01;0.1 sec).

7.2.4 Neutral Overcurrent protection (51N)

This protection consists of three stages with dual time calibration; each stage can be configured as independent-time (Ti) or dependent-time (Td) with selectable standard curves. An ad-hoc LN class is provided, according to the extension rules of the IEC 61850; it permits the selection of the operating modes, special functions and the configuration of the parameters linked to the curve (Ip, Tp).

7.2.4.1. 51N.S1 (Ti+Td) stage with dual time calibration

Table 28 – LNInstance: 1 - prefix: N51S1 – PEOC1 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
OpCntRs	INC	Resetable operation counter		R
Status Information				
Str	ACD	Start		M
Op	ACT	Operate	T	M
AOp	ACT	enel Additional/Accelerated Operate	T	R
TmASt	CSD	Active curve characteristic		O
Settings				
TmACrv	CURVE	Operating Curve Type		R
StrVal	ASG	Start Value		R
TmMult	ASG	Time Dial Multiplier		O
MinOpTmms	ING	Minimum Operate Time		R
MaxOpTmms	ING	Maximum Operate Time		O
OpDlTmms	ING	Operate Delay Time		R
AOpDlTmms	ING	enel Additional/Accelerated Operate Delay Time		R
TypRsCrv	ING	Type Reset Curve		O
RsDlTmms	ING	Reset Delay Time		O
DirMod	ING	Directional Mode		O
PAccelEna	SPG	enel Protection Stage Acceleration Enabling		R
PBst	SPG	enel Protection Behaviour (1=Str 2= Str+Op)		R
FFSEna	SPG	enel Fast Fault Selection Enabling (Participation in the Logic Selectivity)		R
Bl2ndHEna	SPG	enel Block due to 2nd H Enabling		R
RsDlTEna	SPG	enel Reset Delay Time Enabling (Logical Block /Tr)		O
TmACStrVal	ASG	enel Active curve characteristic Start Value (Ip for Td curve)		R
TmACOpDlTm	ING	enel Active curve characteristic Operate Delay Time (Tp for Td curve)		R
CLPMod	ING	enel Cold Load Pickup Mode		R
CLPOpPer	ASG	enel Cold Load Pickup Operating Period		R

NOTES:

Common Logical Node Information→ Mod: for handling the **Enabling/Disabling** command (1/5) of this protection stage (base and accelerated)

Common Logical Node Information→ OpCntRs: to count and store the number of operations of this stage (base and accelerated)

Status Information→ Str: for issuing the Start signal of this stage (base and accelerated)

Status Information→ Op: for issuing the Tripping signal of this stage (base only)

Status Information→ AOp: for sending the Tripping signal of this stage (accelerated only)

Settings→ TmACrv: for setting the **IEC curve type** in case the stage is Td (base only) or if the stage is Ti:

a. 9 = NIT (IEC Normal Inverse)

b. 10 = VIT (IEC Very Inverse)

c. 12 = EIT (IEC Extremely Inverse)

d. 14 = LIT (IEC Long – Time Inverse)

e. 15 = Ti (IEC Definite Time)

Settings→ StrVal: for setting the current threshold of this stage (base and accelerated) when Ti (min..max; step; default; m.u.)

Settings→ MinOpTmms: for setting the minimum duration time of the accelerated (only) stage (min..max; step; default; m.u.)

Settings→ OpDlTmms: for setting the operate delay time of the stage **T51N.S1** (base only) when Ti (min..max; step; default; m.u.)

Settings→ AOpDlTmms: for setting the operate delay time of the stage **T51N.S1_c** (accelerated only) when Ti (min..max; step; default; m.u.)

Settings→ PAccelEna: for enabling the dual time calibration (acceleration) of this stage:

f. 0 = base only

g. 1 = base + accelerated

Settings→ PBst: for setting the behaviour of this stage (base and accelerated):

h. 0 = Start + Operate

i. 1 = Start only

Settings → FFSEna: for setting the participation in the Logic Selectivity function (publishing and subscribing) of this stage (base and accelerated):

j. 0 = excluded

k. 1 = participating

Settings → Bl2ndHEna: for allowing the blocking, due to 2nd harmonic restraint protection, of this stage (base and accelerated):

l. 0 = not blockable

m. 1 = stage Sx blockable due to 2nd harmonic

Settings → TmACStrVal: for setting the Ip of the curve in case of Td stage (base only) (min..max; step; default; m.u.)

Settings → TmACOpDlTm: for setting the Tp of the curve in case of Td stage (base only) (min..max; step; default; m.u.)

Settings → CLPMod: for setting the mode of the Cold Load Pickup function for this stage:

n. 0 = Off (Default)

o. 1 = On – Stage Block

p. 2 = On – Stage Modification

Settings → CLPOpPer: for setting the Operating Period of the Cold Load Pickup for this stage (0..100;0.01;0.1 sec).

7.2.4.2. 51N.S2 (Ti+Td) stage with dual time calibration

Table 29 – LNInstance: 1 - prefix: N51S2 – PEOC1 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
OpCntRs	INC	Resetable operation counter		R
Status Information				
Str	ACD	Start		M
Op	ACT	Operate	T	M
AOp	ACT	enel Additional/Accelerated Operate	T	R
TmASt	CSD	Active curve characteristic		O
Settings				
TmACrv	CURVE	Operating Curve Type		R
StrVal	ASG	Start Value		R
TmMult	ASG	Time Dial Multiplier		O
MinOpTmms	ING	Minimum Operate Time		R
MaxOpTmms	ING	Maximum Operate Time		O
OpDlTmms	ING	Operate Delay Time		R
AOpDlTmms	ING	enel Additional/Accelerated Operate Delay Time		R
TypRsCrv	ING	Type Reset Curve		O
RsDlTmms	ING	Reset Delay Time		O
DirMod	ING	Directional Mode		O
PAccelEna	SPG	enel Protection Stage Acceleration Enabling		R
PBst	SPG	enel Protection Behaviour (1=Str 2= Str+Op)		R
FFSEna	SPG	enel Fast Fault Selection Enabling (Participation in the Logic Selectivity)		R
Bl2ndHEna	SPG	enel Block due to 2nd H Enabling		R
RsDlTEna	SPG	enel Reset Delay Time Enabling (Logical Block /Tr)		O
TmACStrVal	ASG	enel Active curve characteristic Start Value (Ip for Td curve)		R
TmACOpDlTm	ING	enel Active curve characteristic Operate Delay Time (Tp for Td curve)		R
CLPMod	ING	enel Cold Load Pickup Mode		R
CLPOpPer	ASG	enel Cold Load Pickup Operating Period		R

NOTES:

Common Logical Node Information→ Mod: for handling the **Enabling/Disabling** command (1/5) of this protection stage (base and accelerated)

Common Logical Node Information→ OpCntRs: to count and store the number of operations of this stage (base and accelerated)

Status Information→ Str: for issuing the Start signal of this stage (base and accelerated)

Status Information→ Op: for issuing the Tripping signal of this stage (base only)

Status Information→ AOp: for sending the Tripping signal of this stage (accelerated only)

Settings→ TmACrv: for setting the **IEC curve type** in case the stage is Td (base only) or if the stage is Ti:

a. 9 = NIT (IEC Normal Inverse)

b. 10 = VIT (IEC Very Inverse)

c. 12 = EIT (IEC Extremely Inverse)

d. 14 = LIT (IEC Long – Time Inverse)

e. 15 = Ti (IEC Definite Time)

Settings→ StrVal: for setting the current threshold of this stage (base and accelerated) when Ti (min..max; step; default; m.u.)

Settings→ MinOpTmms: for setting the minimum duration time of the accelerated (only) stage (min..max; step; default; m.u.)

Settings→ OpDlTmms: for setting the operate delay time of the stage **T51N.S2** (base only) when Ti (min..max; step; default; m.u.)

Settings→ AOpDlTmms: for setting the operate delay time of the stage **T51N.S2_c** (accelerated only) when Ti (min..max; step; default; m.u.)

Settings→ PAccelEna: for enabling the dual time calibration (acceleration) of this stage:

f. 0 = base only

g. 1 = base + accelerated

Settings→ PBst: for setting the behaviour of this stage (base and accelerated):

h. 0 = Start + Operate

i. 1 = Start only

Settings → FFSEna: for setting the participation in the Logic Selectivity function (publishing and subscribing) of this stage (base and accelerated):

j. 0 = excluded

k. 1 = participating

Settings → Bl2ndHEna: for allowing the blocking, due to 2nd harmonic restraint protection, of this stage (base and accelerated):

l. 0 = not blockable

m. 1 = stage Sx blockable due to 2nd harmonic

Settings → TmACStrVal: for setting the Ip of the curve in case of Td stage (base only) (min..max; step; default; m.u.)

Settings → TmACOpDlTm: for setting the Tp of the curve in case of Td stage (base only) (min..max; step; default; m.u.)

Settings → CLPMod: for setting the mode of the Cold Load Pickup function for this stage:

n. 0 = Off (Default)

o. 1 = On – Stage Block

p. 2 = On – Stage Modification

Settings → CLPOpPer: for setting the Operating Period of the Cold Load Pickup for this stage (0..100;0.01;0.1 sec).

7.2.4.3. 51N.S3 (Ti+Td) stage with dual time calibration

Table 30 – LNInstance: 1 - prefix: N51S3 – PEOC1 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
OpCntRs	INC	Resetable operation counter		R
Status Information				
Str	ACD	Start		M
Op	ACT	Operate	T	M
AOp	ACT	enel Additional/Accelerated Operate	T	R
TmASt	CSD	Active curve characteristic		O
Settings				
TmACrv	CURVE	Operating Curve Type		R
StrVal	ASG	Start Value		R
TmMult	ASG	Time Dial Multiplier		O
MinOpTmms	ING	Minimum Operate Time		R
MaxOpTmms	ING	Maximum Operate Time		O
OpDlTmms	ING	Operate Delay Time		R
AOpDlTmms	ING	enel Additional/Accelerated Operate Delay Time		R
TypRsCrv	ING	Type Reset Curve		O
RsDlTmms	ING	Reset Delay Time		O
DirMod	ING	Directional Mode		O
PAccelEna	SPG	enel Protection Stage Acceleration Enabling		R
PBst	SPG	enel Protection Behaviour (1=Str 2= Str+Op)		R
FFSEna	SPG	enel Fast Fault Selection Enabling (Participation in the Logic Selectivity)		R
Bl2ndHEna	SPG	enel Block due to 2nd H Enabling		R
RsDlTEna	SPG	enel Reset Delay Time Enabling (Logical Block /Tr)		O
TmACStrVal	ASG	enel Active curve characteristic Start Value (Ip for Td curve)		R
TmACOpDlTm	ING	enel Active curve characteristic Operate Delay Time (Tp for Td curve)		R
CLPMod	ING	enel Cold Load Pickup Mode		R
CLPOpPer	ASG	enel Cold Load Pickup Operating Period		R

NOTES:

Common Logical Node Information→ Mod: for handling the **Enabling/Disabling** command (1/5) of this protection stage (base and accelerated)

Common Logical Node Information→ OpCntRs: to count and store the number of operations of this stage (base and accelerated)

Status Information→ Str: for issuing the Start signal of this stage (base and accelerated)

Status Information→ Op: for issuing the Tripping signal of this stage (base only)

Status Information→ AOp: for sending the Tripping signal of this stage (accelerated only)

Settings→ TmACrv: for setting the **IEC curve type** in case the stage is Td (base only) or if the stage is Ti:

a. 9 = NIT (IEC Normal Inverse)

b. 10 = VIT (IEC Very Inverse)

c. 12 = EIT (IEC Extremely Inverse)

d. 14 = LIT (IEC Long – Time Inverse)

e. 15 = Ti (IEC Definite Time)

Settings→ StrVal: for setting the current threshold of this stage (base and accelerated) when Ti (min..max; step; default; m.u.)

Settings→ MinOpTmms: for setting the minimum duration time of the accelerated (only) stage (min..max; step; default; m.u.)

Settings→ OpDlTmms: for setting the operate delay time of the stage **T51N.S3** (base only) when Ti (min..max; step; default; m.u.)

Settings→ AOpDlTmms: for setting the operate delay time of the stage **T51N.S3_c** (accelerated only) when Ti (min..max; step; default; m.u.)

Settings→ PAccelEna: for enabling the dual time calibration (acceleration) of this stage:

f. 0 = base only

g. 1 = base + accelerated

Settings→ PBst: for setting the behaviour of this stage (base and accelerated):

h. 0 = Start + Operate

i. 1 = Start only

Settings → FFSEna: for setting the participation in the Logic Selectivity function (publishing and subscribing) of this stage (base and accelerated):

j. 0 = excluded

k. 1 = participating

Settings → Bl2ndHEna: for allowing the blocking, due to 2nd harmonic restraint protection, of this stage (base and accelerated):

l. 0 = not blockable

m. 1 = stage Sx blockable due to 2nd harmonic

Settings → TmACStrVal: for setting the Ip of the curve in case of Td stage (base only) (min..max; step; default; m.u.)

Settings → TmACOpDlTm: for setting the Tp of the curve in case of Td stage (base only) (min..max; step; default; m.u.)

Settings → CLPMod: for setting the mode of the Cold Load Pickup function for this stage:

n. 0 = Off (Default)

o. 1 = On – Stage Block

p. 2 = On – Stage Modification

Settings → CLPOpPer: for setting the Operating Period of the Cold Load Pickup for this stage (0..100;0.01;0.1 sec).

The MFP, when installed as an Earthing Transformer (TFN) protection, implements two addition 51N stages with dual time calibration.

7.2.4.4. 51N.S1_a (Ti+Td) stage with dual time calibration

Table 31 – LNInstance: 1 - prefix: N51S1a PEOC1 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
OpCntRs	INC	Resetable operation counter		R
Status Information				
Str	ACD	Start		M
Op	ACT	Operate	T	M
AOp	ACT	enel Additional/Accelerated Operate	T	R
TmASt	CSD	Active curve characteristic		O
Settings				
TmACrv	CURVE	Operating Curve Type		R
StrVal	ASG	Start Value		R
TmMult	ASG	Time Dial Multiplier		O
MinOpTmms	ING	Minimum Operate Time		R
MaxOpTmms	ING	Maximum Operate Time		O
OpDlTmms	ING	Operate Delay Time		R
AOpDlTmms	ING	enel Additional/Accelerated Operate Delay Time		R
TypRsCrv	ING	Type Reset Curve		O
RsDlTmms	ING	Reset Delay Time		O
DirMod	ING	Directional Mode		O
PAccelEna	SPG	enel Protection Stage Acceleration Enabling		R
PBst	SPG	enel Protection Behaviour (1=Str 2= Str+Op)		R
FFSEna	SPG	enel Fast Fault Selection Enabling (Participation in the Logic Selectivity)		R
Bl2ndHEna	SPG	enel Block due to 2nd H Enabling		R
RsDlTEna	SPG	enel Reset Delay Time Enabling (Logical Block /Tr)		O
TmACStrVal	ASG	enel Active curve characteristic Start Value (Ip for Td curve)		R
TmACOpDlTm	ING	enel Active curve characteristic Operate Delay Time (Tp for Td curve)		R
CLPMod	ING	enel Cold Load Pickup Mode		R
CLPOpPer	ASG	enel Cold Load Pickup Operating Period		R

NOTES:

Common Logical Node Information→ Mod: for handling the **Enabling/Disabling** command (1/5) of this protection stage (base and accelerated)

Common Logical Node Information→ OpCntRs: to count and store the number of operations of this stage (base and accelerated)

Status Information→ Str: for issuing the Start signal of this stage (base and accelerated)

Status Information→ Op: for issuing the Tripping signal of this stage (base only)

Status Information→ AOp: for sending the Tripping signal of this stage (accelerated only)

Settings→ TmACrv: for setting the **IEC curve type** in case the stage is Td (base only) or if the stage is Ti:

a. 9 = NIT (IEC Normal Inverse)

b. 10 = VIT (IEC Very Inverse)

c. 12 = EIT (IEC Extremely Inverse)

d. 14 = LIT (IEC Long – Time Inverse)

e. 15 = Ti (IEC Definite Time)

Settings→ StrVal: for setting the current threshold of this stage (base and accelerated) when Ti (min..max; step; default; m.u.)

Settings→ MinOpTmms: for setting the minimum duration time of the accelerated (only) stage (min..max; step; default; m.u.)

Settings→ OpDlTmms: for setting the operate delay time of the stage **T51N.S1_a** (base only) when Ti (min..max; step; default; m.u.)

Settings→ AOpDlTmms: for setting the operate delay time of the stage **T51N.S1a _c** (accelerated only) when Ti (min..max; step; default; m.u.)

Settings→ PAccelEna: for enabling the dual time calibration (acceleration) of this stage:

f. 0 = base only

g. 1 = base + accelerated

Settings→ PBst: for setting the behaviour of this stage (base and accelerated):

h. 0 = Start + Operate

i. 1 = Start only

Settings → FFSEna: for setting the participation in the Logic Selectivity function (publishing and subscribing) of this stage (base and accelerated):

j. 0 = excluded

k. 1 = participating

Settings → Bl2ndHEna: for allowing the blocking, due to 2nd harmonic restraint protection, of this stage (base and accelerated):

l. 0 = not blockable

m. 1 = stage Sx blockable due to 2nd harmonic

Settings → TmACStrVal: for setting the Ip of the curve in case of Td stage (base only) (min..max; step; default; m.u.)

Settings → TmACOpDlTm: for setting the Tp of the curve in case of Td stage (base only) (min..max; step; default; m.u.)

Settings → CLPMod: for setting the mode of the Cold Load Pickup function for this stage:

n. 0 = Off (Default)

o. 1 = On – Stage Block

p. 2 = On – Stage Modification

Settings → CLPOpPer: for setting the Operating Period of the Cold Load Pickup for this stage (0..100;0.01;0.1 sec).

7.2.4.5. 51N.S2_a (Ti+Td) stage with dual time calibration

Table 32 – LNInstance: 1 - prefix: N51S2a – PEOC1 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
OpCntRs	INC	Resetable operation counter		R
Status Information				
Str	ACD	Start		M
Op	ACT	Operate	T	M
AOp	ACT	enel Additional/Accelerated Operate	T	R
TmASt	CSD	Active curve characteristic		O
Settings				
TmACrv	CURVE	Operating Curve Type		R
StrVal	ASG	Start Value		R
TmMult	ASG	Time Dial Multiplier		O
MinOpTmms	ING	Minimum Operate Time		R
MaxOpTmms	ING	Maximum Operate Time		O
OpDlTmms	ING	Operate Delay Time		R
AOpDlTmms	ING	enel Additional/Accelerated Operate Delay Time		R
TypRsCrv	ING	Type Reset Curve		O
RsDlTmms	ING	Reset Delay Time		O
DirMod	ING	Directional Mode		O
PAccelEna	SPG	enel Protection Stage Acceleration Enabling		R
PBst	SPG	enel Protection Behaviour (1=Str 2= Str+Op)		R
FFSEna	SPG	enel Fast Fault Selection Enabling (Participation in the Logic Selectivity)		R
Bl2ndHEna	SPG	enel Block due to 2nd H Enabling		R
RsDlTEna	SPG	enel Reset Delay Time Enabling (Logical Block /Tr)		O
TmACStrVal	ASG	enel Active curve characteristic Start Value (Ip for Td curve)		R
TmACOpDlTm	ING	enel Active curve characteristic Operate Delay Time (Tp for Td curve)		R
CLPMod	ING	enel Cold Load Pickup Mode		R
CLPOpPer	ASG	enel Cold Load Pickup Operating Period		R

NOTES:

Common Logical Node Information→ Mod: for handling the **Enabling/Disabling** command (1/5) of this protection stage (base and accelerated)

Common Logical Node Information→ OpCntRs: to count and store the number of operations of this stage (base and accelerated)

Status Information→ Str: for issuing the Start signal of this stage (base and accelerated)

Status Information→ Op: for issuing the Tripping signal of this stage (base only)

Status Information→ AOp: for sending the Tripping signal of this stage (accelerated only)

Settings→ TmACrv: for setting the IEC curve type in case the stage is Td (base only) or if the stage is Ti:

a. 9 = NIT (IEC Normal Inverse)

b. 10 = VIT (IEC Very Inverse)

c. 12 = EIT (IEC Extremely Inverse)

d. 14 = LIT (IEC Long – Time Inverse)

e. 15 = Ti (IEC Definite Time)

Settings→ StrVal: for setting the current threshold of this stage (base and accelerated) when Ti (min..max; step; default; m.u.)

Settings→ MinOpTmms: for setting the minimum duration time of the accelerated (only) stage (min..max; step; default; m.u.)

Settings→ OpDlTmms: for setting the operate delay time of the stage **T51N.S2_a** (base only) (min..max; step; default; m.u.)

Settings→ AOpDlTmms: for setting the operate delay time of the stage **T51N.S2a _c** (accelerated only) when Ti (min..max; step; default; m.u.)

Settings→ PAccelEna: for enabling the dual time calibration (acceleration) of this stage:

f. 0 = base only

g. 1 = base + accelerated

Settings→ PBst: for setting the behaviour of this stage (base and accelerated):

h. 0 = Start + Operate

i. 1 = Start only

Settings → FFSEna: for setting the participation in the Logic Selectivity function (publishing and subscribing) of this stage (base and accelerated):

j. 0 = excluded

k. 1 = participating

Settings → Bl2ndHEna: for allowing the blocking, due to 2nd harmonic restraint protection, of this stage (base and accelerated):

l. 0 = not blockable

m. 1 = stage Sx blockable due to 2nd harmonic

Settings → TmACStrVal: for setting the Ip of the curve in case of Td stage (base only) (min..max; step; default; m.u.)

Settings → TmACOpDlTm: for setting the Tp of the curve in case of Td stage (base only) (min..max; step; default; m.u.)

Settings → CLPMod: for setting the mode of the Cold Load Pickup function for this stage:

n. 0 = Off (Default)

o. 1 = On – Stage Block

p. 2 = On – Stage Modification

Settings → CLPOpPer: for setting the Operating Period of the Cold Load Pickup for this stage (0..100;0.01;0.1 sec).

Additionally, the MFP implements a 51N Emergency stage with dual time calibration to operate in case of Voltage (voltmetric) Analog Inputs of the IED or voltage transduction chain failure.

7.2.4.6. 51N.E (Ti+Td) stage with dual time calibration

Table 33 – LNInstance: 1 - prefix: N51SE – PEOC1 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
OpCntRs	INC	Resetable operation counter		R
Status Information				
Str	ACD	Start		M
Op	ACT	Operate	T	M
AOp	ACT	enel Additional/Accelerated Operate	T	R
TmASt	CSD	Active curve characteristic		O
Settings				
TmACrv	CURVE	Operating Curve Type		R
StrVal	ASG	Start Value		R
TmMult	ASG	Time Dial Multiplier		O
MinOpTmms	ING	Minimum Operate Time		R
MaxOpTmms	ING	Maximum Operate Time		O
OpDlTmms	ING	Operate Delay Time		R
AOpDlTmms	ING	enel Additional/Accelerated Operate Delay Time		R
TypRsCrv	ING	Type Reset Curve		O
RsDlTmms	ING	Reset Delay Time		O
DirMod	ING	Directional Mode		O
PAccelEna	SPG	enel Protection Stage Acceleration Enabling		R
PBst	SPG	enel Protection Behaviour (1=Str 2= Str+Op)		R
FFSEna	SPG	enel Fast Fault Selection Enabling (Participation in the Logic Selectivity)		R
Bl2ndHEna	SPG	enel Block due to 2nd H Enabling		R
RsDlTEna	SPG	enel Reset Delay Time Enabling (Logical Block /Tr)		O
TmACStrVal	ASG	enel Active curve characteristic Start Value (Ip for Td curve)		R
TmACOpDlTm	ING	enel Active curve characteristic Operate Delay Time (Tp for Td curve)		R
CLPMod	ING	enel Cold Load Pickup Mode		R
CLPOpPer	ASG	enel Cold Load Pickup Operating Period		R

NOTES:

Common Logical Node Information→ Mod: for handling the **Enabling/Disabling** command (1/5) of this protection stage (base and accelerated)

Common Logical Node Information→ OpCntRs: to count and store the number of operations of this stage (base and accelerated)

Status Information→ Str: for issuing the Start signal of this stage (base and accelerated)

Status Information→ Op: for issuing the Tripping signal of this stage (base only)

Status Information→ AOp: for sending the Tripping signal of this stage (accelerated only)

Settings→ TmACrv: for setting the IEC curve type in case the stage is Td (base only) or if the stage is Ti:

a. 9 = NIT (IEC Normal Inverse)

b. 10 = VIT (IEC Very Inverse)

c. 12 = EIT (IEC Extremely Inverse)

d. 14 = LIT (IEC Long – Time Inverse)

e. 15 = Ti (IEC Definite Time)

Settings→ StrVal: for setting the current threshold of this stage (base and accelerated) when Ti (min..max; step; default; m.u.)

Settings→ MinOpTmms: for setting the minimum duration time of the accelerated (only) stage (min..max; step; default; m.u.)

Settings→ OpDlTmms: for setting the operate delay time of the stage **T51N.E** (base only) when Ti (min..max; step; default; m.u.)

Settings→ AOpDlTmms: for setting the operate delay time of the stage **T51N.E_c** (accelerated only) when Ti (min..max; step; default; m.u.)

Settings→ PAccelEna: for enabling the dual time calibration (acceleration) of this stage:

f. 0 = base only

g. 1 = base + accelerated

Settings→ PBst: for setting the behaviour of this stage (base and accelerated):

h. 0 = Start + Operate

i. 1 = Start only

Settings → FFSEna: for setting the participation in the Logic Selectivity function (publishing and subscribing) of this stage (base and accelerated):

j. 0 = excluded

k. 1 = participating

Settings → Bl2ndHEna: for allowing the blocking, due to 2nd harmonic restraint protection, of this stage (base and accelerated):

l. 0 = not blockable

m. 1 = stage Sx blockable due to 2nd harmonic

Settings → TmACStrVal: for setting the Ip of the curve in case of Td stage (base only) (min..max; step; default; m.u.)

Settings → TmACOpDlTm: for setting the Tp of the curve in case of Td stage (base only) (min..max; step; default; m.u.)

Settings → CLPMod: for setting the mode of the Cold Load Pickup function for this stage:

n. 0 = Off (Default)

o. 1 = On – Stage Block

p. 2 = On – Stage Modification

Settings → CLPOpPer: for setting the Operating Period of the Cold Load Pickup for this stage (0..100;0.01;0.1 sec).

7.2.5 Residual Overcurrent protection (51NR)

This protection consists of three stages with dual time calibration; each stage can be configured as independent-time (Ti) or dependent-time (Td) with selectable standard curves. An ad-hoc LN class is provided, according to the extension rules of the IEC 61850; it that permits the selection of the operating modes, special functions and the configuration of the parameters linked to the curve (Ip, Tp).

7.2.5.1. 51NR.S1 (Ti+Td) stage with dual time calibration

Table 34 –LNInstance: 1 - prefix: N51RS1 – PEOC1 type

Attribute Name	Attribute Type	Explanation	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
OpCntRs	INC	Resetable operation counter		R
Status Information				
Str	ACD	Start		M
Op	ACT	Operate	T	M
AOp	ACT	enel Additional/Accelerated Operate	T	R
TmASt	CSD	Active curve characteristic		O
Settings				
TmACrv	CURVE	Operating Curve Type		R
StrVal	ASG	Start Value		R
TmMult	ASG	Time Dial Multiplier		O
MinOpTmms	ING	Minimum Operate Time		R
MaxOpTmms	ING	Maximum Operate Time		O
OpDlTmms	ING	Operate Delay Time		R
AOpDlTmms	ING	enel Additional/Accelerated Operate Delay Time		R
TypRsCrv	ING	Type Reset Curve		O
RsDlTmms	ING	Reset Delay Time		O
DirMod	ING	Directional Mode		O
PAccelEna	SPG	enel Protection Stage Acceleration Enabling		R
PBst	SPG	enel Protection Behaviour (1=Str 2= Str+Op)		R
FFSEna	SPG	enel Fast Fault Selection Enabling (Participation in the Logic Selectivity)		R
Bl2ndHEna	SPG	enel Block due to 2nd H Enabling		R
RsDlTEna	SPG	enel Reset Delay Time Enabling (Logical Block /Tr)		O
TmACStrVal	ASG	enel Active curve characteristic Start Value (Ip for Td curve)		R
TmACOpDlTm	ING	enel Active curve characteristic Operate Delay Time (Tp for Td curve)		R
CLPMod	ING	enel Cold Load Pickup Mode		R
CLPOpPer	ASG	enel Cold Load Pickup Operating Period		R

NOTES:

Common Logical Node Information→ Mod: for handling the **Enabling/Disabling** command (1/5) of this protection stage (base and accelerated)

Common Logical Node Information→ OpCntRs: to count and store the number of operations of this stage (base and accelerated)

Status Information→ Str: for issuing the Start signal of this stage (base and accelerated)

Status Information→ Op: for issuing the Tripping signal of this stage (base only)

Status Information→ AOp: for sending the Tripping signal of this stage (accelerated only)

Settings→ TmACrv: for setting the **IEC curve type** in case the stage is Td (base only) or if the stage is Ti:

a. 9 = NIT (IEC Normal Inverse)

b. 10 = VIT (IEC Very Inverse)

c. 12 = EIT (IEC Extremely Inverse)

d. 14 = LIT (IEC Long – Time Inverse)

e. 15 = Ti (IEC Definite Time)

Settings→ StrVal: for setting the current threshold of this stage (base and accelerated) when Ti (min..max; step; default; m.u.)

Settings→ MinOpTmms: for setting the minimum duration time of the accelerated (only) stage (min..max; step; default; m.u.)

Settings→ OpDlTmms: for setting the operate delay time of the stage **T51NR.S1** (base only) when Ti (min..max; step; default; m.u.)

Settings→ AOpDlTmms: for setting the operate delay time of the stage **T51NR.S1_c** (accelerated only) when Ti (min..max; step; default; m.u.)

Settings→ PAccelEna: for enabling the dual time calibration (acceleration) of this stage:

f. 0 = base only

g. 1 = base + accelerated

Settings→ PBst: for setting the behaviour of this stage (base and accelerated):

h. 0 = Start + Operate

i. 1 = Start only

Settings → FFSEna: for setting the participation in the Logic Selectivity function (publishing and subscribing) of this stage (base and accelerated):

j. 0 = excluded

k. 1 = participating

Settings → Bl2ndHEna: for allowing the blocking, due to 2nd harmonic restraint protection, of this stage (base and accelerated):

l. 0 = not blockable

m. 1 = stage Sx blockable due to 2nd harmonic

Settings → TmACStrVal: for setting the Ip of the curve in case of Td stage (base only) (min..max; step; default; m.u.)

Settings → TmACOpDlTm: for setting the Tp of the curve in case of Td stage (base only) (min..max; step; default; m.u.)

Settings → CLPMod: for setting the mode of the Cold Load Pickup function for this stage:

n. 0 = Off (Default)

o. 1 = On – Stage Block

p. 2 = On – Stage Modification

Settings → CLPOpPer: for setting the Operating Period of the Cold Load Pickup for this stage (0..100;0.01;0.1 sec).

7.2.5.2. 51NR.S2 (Ti+Td) stage with dual time calibration

Table 35 –LNInstance: 1 - prefix: N51RS2 – PEOC1 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/ O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
OpCntRs	INC	Resetable operation counter		R
Status Information				
Str	ACD	Start		M
Op	ACT	Operate	T	M
AOp	ACT	enel Additional/Accelerated Operate	T	R
TmASt	CSD	Active curve characteristic		O
Settings				
TmACrv	CURVE	Operating Curve Type		R
StrVal	ASG	Start Value		R
TmMult	ASG	Time Dial Multiplier		O
MinOpTmms	ING	Minimum Operate Time		R
MaxOpTmms	ING	Maximum Operate Time		O
OpDlTmms	ING	Operate Delay Time		R
AOpDlTmms	ING	enel Additional/Accelerated Operate Delay Time		R
TypRsCrv	ING	Type Reset Curve		O
RsDlTmms	ING	Reset Delay Time		O
DirMod	ING	Directional Mode		O
PAccelEna	SPG	enel Protection Stage Acceleration Enabling		R
PBst	SPG	enel Protection Behaviour (1=Str 2= Str+Op)		R
FFSEna	SPG	enel Fast Fault Selection Enabling (Participation in the Logic Selectivity)		R
Bl2ndHEna	SPG	enel Block due to 2nd H Enabling		R
RsDlTEna	SPG	enel Reset Delay Time Enabling (Logical Block /Tr)		O
TmACStrVal	ASG	enel Active curve characteristic Start Value (Ip for Td curve)		R
TmACOpDlTm	ING	enel Active curve characteristic Operate Delay Time (Tp for Td curve)		R
CLPMod	ING	enel Cold Load Pickup Mode		R
CLPOpPer	ASG	enel Cold Load Pickup Operating Period		R

NOTES:

Common Logical Node Information→ Mod: for handling the **Enabling/Disabling** command (1/5) of this protection stage (base and accelerated)

Common Logical Node Information→ OpCntRs: to count and store the number of operations of this stage (base and accelerated)

Status Information→ Str: for issuing the Start signal of this stage (base and accelerated)

Status Information→ Op: for issuing the Tripping signal of this stage (base only)

Status Information→ AOp: for sending the Tripping signal of this stage (accelerated only)

Settings→ TmACrv: for setting the **IEC curve type** in case the stage is Td (base only) or if the stage is Ti:

a. 9 = NIT (IEC Normal Inverse)

b. 10 = VIT (IEC Very Inverse)

c. 12 = EIT (IEC Extremely Inverse)

d. 14 = LIT (IEC Long – Time Inverse)

e. 15 = Ti (IEC Definite Time)

Settings→ StrVal: for setting the current threshold of this stage (base and accelerated) when Ti (min..max; step; default; m.u.)

Settings→ MinOpTmms: for setting the minimum duration time of the accelerated (only) stage (min..max; step; default; m.u.)

Settings→ OpDlTmms: for setting the operate delay time of the stage **T51NR.S2** (base only) when Ti (min..max; step; default; m.u.)

Settings→ AOpDlTmms: for setting the operate delay time of the stage **T51NR.S2_c** (accelerated only) when Ti (min..max; step; default; m.u.)

Settings→ PAccelEna: for enabling the dual time calibration (acceleration) of this stage:

f. 0 = base only

g. 1 = base + accelerated

Settings→ PBst: for setting the behaviour of this stage (base and accelerated):

h. 0 = Start + Operate

i. 1 = Start only

Settings → FFSEna: for setting the participation in the Logic Selectivity function (publishing and subscribing) of this stage (base and accelerated):

j. 0 = excluded

k. 1 = participating

Settings → Bl2ndHEna: for allowing the blocking, due to 2nd harmonic restraint protection, of this stage (base and accelerated):

l. 0 = not blockable

m. 1 = stage Sx blockable due to 2nd harmonic

Settings → TmACStrVal: for setting the Ip of the curve in case of Td stage (base only) (min..max; step; default; m.u.)

Settings → TmACOpDlTm: for setting the Tp of the curve in case of Td stage (base only) (min..max; step; default; m.u.)

Settings → CLPMod: for setting the mode of the Cold Load Pickup function for this stage:

n. 0 = Off (Default)

o. 1 = On – Stage Block

p. 2 = On – Stage Modification

Settings → CLPOpPer: for setting the Operating Period of the Cold Load Pickup for this stage (0..100;0.01;0.1 sec).

7.2.5.3. 51NR.S3 (Ti+Td) stage with dual time calibration

Table 36 –LNInstance: 1 - prefix: N51RS3 – PEOC1 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
OpCntRs	INC	Resetable operation counter		R
Status Information				
Str	ACD	Start		M
Op	ACT	Operate	T	M
AOp	ACT	enel Additional/Accelerated Operate	T	R
TmASt	CSD	Active curve characteristic		O
Settings				
TmACrv	CURVE	Operating Curve Type		R
StrVal	ASG	Start Value		R
TmMult	ASG	Time Dial Multiplier		O
MinOpTmms	ING	Minimum Operate Time		R
MaxOpTmms	ING	Maximum Operate Time		O
OpDlTmms	ING	Operate Delay Time		R
AOpDlTmms	ING	enel Additional/Accelerated Operate Delay Time		R
TypRsCrv	ING	Type Reset Curve		O
RsDlTmms	ING	Reset Delay Time		O
DirMod	ING	Directional Mode		O
PAccelEna	SPG	enel Protection Stage Acceleration Enabling		R
PBst	SPG	enel Protection Behaviour (1=Str 2= Str+Op)		R
FFSEna	SPG	enel Fast Fault Selection Enabling (Participation in the Logic Selectivity)		R
Bl2ndHEna	SPG	enel Block due to 2nd H Enabling		R
RsDlTEna	SPG	enel Reset Delay Time Enabling (Logical Block /Tr)		O
TmACStrVal	ASG	enel Active curve characteristic Start Value (Ip for Td curve)		R
TmACOpDlTm	ING	enel Active curve characteristic Operate Delay Time (Tp for Td curve)		R
CLPMod	ING	enel Cold Load Pickup Mode		R
CLPOpPer	ASG	enel Cold Load Pickup Operating Period		R

NOTES:

Common Logical Node Information→ Mod: for handling the Enabling/Disabling command (1/5) of this protection stage (base and accelerated)

Common Logical Node Information→ OpCntRs: to count and store the number of operations of this stage (base and accelerated)

Status Information→ Str: for issuing the Start signal of this stage (base and accelerated)

Status Information→ Op: for issuing the Tripping signal of this stage (base only)

Status Information→ AOp: for sending the Tripping signal of this stage (accelerated only)

Settings→ TmACrv: for setting the **IEC curve type** in case the stage is Td (base only) or if the stage is Ti:

a. 9 = NIT (IEC Normal Inverse)

b. 10 = VIT (IEC Very Inverse)

c. 12 = EIT (IEC Extremely Inverse)

d. 14 = LIT (IEC Long – Time Inverse)

e. 15 = Ti (IEC Definite Time)

Settings→ StrVal: for setting the current threshold of this stage (base and accelerated) when Ti (min..max; step; default; m.u.)

Settings→ MinOpTmms: for setting the minimum duration time of the accelerated (only) stage (min..max; step; default; m.u.)

Settings→ OpDlTmms: for setting the operate delay time of the stage **T51NR.S3** (base only) when Ti (min..max; step; default; m.u.)

Settings→ AOpDlTmms: for setting the operate delay time of the stage **T51NR.S3_c** (accelerated only) when Ti (min..max; step; default; m.u.)

Settings→ PAccelEna: for enabling the dual time calibration (acceleration) of this stage:

f. 0 = base only

g. 1 = base + accelerated

Settings→ PBst: for setting the behaviour of this stage (base and accelerated):

h. 0 = Start + Operate

i. 1 = Start only

Settings → FFSEna: for setting the participation in the Logic Selectivity function (publishing and subscribing) of this stage (base and accelerated):

j. 0 = excluded

k. 1 = participating

Settings → Bl2ndHEna: for allowing the blocking, due to 2nd harmonic restraint protection, of this stage (base and accelerated):

l. 0 = not blockable

m. 1 = stage Sx blockable due to 2nd harmonic

Settings → TmACStrVal: for setting the Ip of the curve in case of Td stage (base only) (min..max; step; default; m.u.)

Settings → TmACOpDlTm: for setting the Tp of the curve in case of Td stage (base only) (min..max; step; default; m.u.)

Settings → CLPMod: for setting the mode of the Cold Load Pickup function for this stage:

n. 0 = Off (Default)

o. 1 = On – Stage Block

p. 2 = On – Stage Modification

Settings → CLPOpPer: for setting the Operating Period of the Cold Load Pickup for this stage (0..100;0.01;0.1 sec).

7.2.6 Directional Phase Overcurrent protection (67)

This protection consists of three directional stages with dual time calibration; each stage can be configured as independent-time (Ti) or dependent-time (Td) with selectable standard curves. Ad-hoc LN classes are provided, according to the extension rules of the IEC 61850; they permit the selection of the operating modes, special functions and the configuration of the parameters linked to the curve (Ip, Tp).

In addition a LN is used for the common and general settings of the P67 stages.

7.2.6.1. P67 general settings

Table 37 – LNInstance: 1 - prefix: GS67 – GAPC1 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
Loc	SPS	Local operation		O
OpCntRs	INC	Resetable operation counter		R
Controls				
SPCSO1	SPC	Single point controllable status output (1)		R
SPCSO2	SPC	Single point controllable status output (2)		R
DPCSO	DPC	Double point controllable status output		O
ISCSO	INC	Integer status controllable status output		O
Status Information				
Auto	SPS	Automatic operation		O
Str	ACD	Start		M
Op	ACT	Operate	T	M
Settings				
StrVal	ASG	Start Value		R

NOTES:

Common Logical Node Information → OpCntRs: to count and store the number of P67 general reconfigurations

Controls → SPCSO1: for setting the measuring operating mode of the P67 stages:

a. 0 = current (Default)

b. 1 = current*cosfi

Controls → SPCSO2: for setting the operating logic of the P67 stages:

c. 0 = 1/3 (Default)

d. 1 = 2/3

Settings → StrVal: for setting the half width of the Tripping Sector of the 67 (0..90; 1; 88).

7.2.6.2. 67.S1 (Ti+Td) stage with dual time calibration

Table 38 –LNInstance: 1 - prefix: P67S1 – PEOC2 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
OpCntRs	INC	Resetable operation counter		R
Status Information				
Str	ACD	Start		M
Op	ACT	Operate	T	M
AOp	ACT	enel Additional/Accelerated Operate	T	R
TmASt	CSD	Active curve characteristic		O
Settings				
TmACrv	CURVE	Operating Curve Type		R
StrVal	ASG	Start Value		R
TmMult	ASG	Time Dial Multiplier		O
MinOpTmms	ING	Minimum Operate Time		R
MaxOpTmms	ING	Maximum Operate Time		O
OpDlTmms	ING	Operate Delay Time		R
AOpDlTmms	ING	enel Additional/Accelerated Operate Delay Time		R
TypRsCrv	ING	Type Reset Curve		O
RsDlTmms	ING	Reset Delay Time		R
DirMod	ING	Directional Mode		O
PAccelEna	SPG	enel Protection Acceleration Enabling		R
PBst	SPG	enel Protection Behaviour (1=Str 2= Str+Op)		R
FFSEna	SPG	enel Fast Fault Selection Enabling (Participation in the Logic Selectivity)		R
Bl2ndHEna	SPG	enel Block due to 2nd H Enabling		R
RsDlTEna	SPG	enel Reset Delay Time Enabling (Logical Block /Tr)		R
TmACStrVal	ASG	enel Active curve characteristic Start Value (Ip for Td curve)		R
TmACOpDlTm	ING	enel Active curve characteristic Operate Delay Time (Tp for Td curve)		R
CLPMod	ING	enel Cold Load Pickup Mode		R
CLPOpPer	ASG	enel Cold Load Pickup Operating Period		R

NOTES:

Common Logical Node Information→ Mod: for handling the Enabling/Disabling command (1/5) of this protection stage (base and accelerated)

Common Logical Node Information→ OpCntRs: to count and store the number of operations of this stage (base and accelerated)

Status Information→ Str: for issuing the Start signal of this stage (base and accelerated)

Status Information→ Op: for issuing the Tripping signal of this stage (base only)

Status Information→ AOp: for sending the Tripping signal of this stage (accelerated only)

Settings→ TmACrv: for setting the IEC curve type in case the stage is Td (base only) or if the stage is Ti:

a. 9 = NIT (IEC Normal Inverse)

b. 10 = VIT (IEC Very Inverse)

c. 12 = EIT (IEC Extremely Inverse)

d. 14 = LIT (IEC Long – Time Inverse)

e. 15 = Ti (IEC Definite Time)

Settings→ StrVal: for setting the current threshold of this stage (base and accelerated) when Ti (min..max; step; default; m.u.)

Settings→ MinOpTmms: for setting the minimum duration time of the accelerated (only) stage (min..max; step; default; m.u.)

Settings→ OpDlTmms: for setting the operate delay time of the stage **T67.S1** (base only) when Ti (min..max; step; default; m.u.)

Settings→ AOpDlTmms: for setting the operate delay time of the stage **T67.S1_c** (accelerated only) when Ti (min..max; step; default; m.u.)

Settings→ RsDlTmms: for setting the backup time of the stage **Tr67.S1** when Ti

Settings→ PAccelEna: for enabling the dual time calibration (acceleration) of this stage:

f. 0 = base only

g. 1 = base + accelerated

Settings→ PBst: for setting the behaviour of this stage (base and accelerated):

h. 0 = Start + Operate

i. 1 = Start only

Settings → FFSEna: for setting the participation in the Logic Selectivity function (publishing and subscribing) of this stage (base and accelerated):

j. 0 = excluded

k. 1 = participating

Settings → Bl2ndHEna: for allowing the blocking, due to 2nd harmonic restraint protection, of this stage (base and accelerated):

l. 0 = not blockable

m. 1 = stage Sx blockable due to 2nd harmonic

Settings → RsDlTEna: for setting the lock of the Backup Time Tr reset (used in the FSL) of this stage (base and accelerated):

n. 0 = reset not locked

o. 1 = reset locked

Settings → TmACStrVal: for setting the Ip of the curve in case of Td stage (base only) (min..max; step; default; m.u.)

Settings → TmACOpDlTm: for setting the Tp of the curve in case of Td stage (base only) (min..max; step; default; m.u.)

Settings → CLPMod: for setting the mode of the Cold Load Pickup function for this stage:

p. 0 = Off (Default)

q. 1 = On – Stage Block

r. 2 = On – Stage Modification

Settings → CLPOpPer: for setting the Operating Period of the Cold Load Pickup for this stage (0..100;0.01;0.1 sec).

The following REDR LN models the directional data and characteristics of the 67.S1 stage (base and accelerated).

Table 39 –LNInstance: 1 - prefix: P67S1 – REDR1 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
Status Information				
Dir	ACD	Direction		M
Settings				
ChrAng	ASG	Characteristic Angle		R
AChrAng	ASG	enel Additional Characteristic Angle		R
MinFwdAng	ASG	Minimum Phase Angle in Forward Direction		R
MinRvAng	ASG	Minimum Phase Angle in Reverse Direction		O
MaxFwdAng	ASG	Maximum Phase Angle in Forward Direction		O
MaxRvAng	ASG	Maximum Phase Angle in Reverse Direction		O
BlkValA	ASG	Minimum operating current		R
BlkValV	ASG	Minimum operating voltage		R
PolQty	ING	Polarising Quantity		O
MinPPV	ASG	Min Phase-Phase Voltage		O

NOTES:

Settings→ ChrAng: for setting the bisector of the Tripping Sector of the 67.S1 (Ti) stage

Settings→ AChrAng: for setting the bisector of the Tripping Sector of the 67.S1 (Td) stage

Settings→ MinFwdAng: for setting the halfwidth of the Tripping Sector of the 67.S1 (Ti+Td) stage

Settings→ BlkValA: for setting the residual current value 3**Io** of the 67.S1 (Ti+Td) stage

Settings→ BlkValV: for setting the residual voltage value 3**Vo** of the 67.S1 (Ti+Td) stage.

7.2.6.3. 67.S2 (Ti+Td) stage with dual time calibration

Table 40 – LNInstance: 1 - prefix: P67S2 – PEOC2 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
OpCntRs	INC	Resetable operation counter		R
Status Information				
Str	ACD	Start		M

Op	ACT	Operate	T	M
AOp	ACT	enel Additional/Accelerated Operate	T	R
TmASt	CSD	Active curve characteristic		O
Settings				
TmACrv	CURVE	Operating Curve Type		R
StrVal	ASG	Start Value		R
TmMult	ASG	Time Dial Multiplier		O
MinOpTmms	ING	Minimum Operate Time		R
MaxOpTmms	ING	Maximum Operate Time		O
OpDlTmms	ING	Operate Delay Time		R
AOpDlTmms	ING	enel Additional/Accelerated Operate Delay Time		R
TypRsCrv	ING	Type Reset Curve		O
RsDlTmms	ING	Reset Delay Time		R
DirMod	ING	Directional Mode		O
PAccelEna	SPG	enel Protection Acceleration Enabling		R
PBst	SPG	enel Protection Behaviour (1=Str 2= Str+Op)		R
FFSEna	SPG	enel Fast Fault Selection Enabling (Participation in the Logic Selectivity)		R
Bl2ndHEna	SPG	enel Block due to 2nd H Enabling		R
RsDlTEna	SPG	enel Reset Delay Time Enabling (Logical Block /Tr)		R
TmACStrVal	ASG	enel Active curve characteristic Start Value (Ip for Td curve)		R
TmACOpDlTm	ING	enel Active curve characteristic Operate Delay Time (Tp for Td curve)		R
CLPMod	ING	enel Cold Load Pickup Mode		R
CLPOpPer	ASG	enel Cold Load Pickup Operating Period		R

NOTES:

Common Logical Node Information→ Mod: for handling the Enabling/Disabling command (1/5) of this protection stage (base and accelerated)

Common Logical Node Information→ OpCntRs: to count and store the number of operations of this stage (base and accelerated)

Status Information→ Str: for issuing the Start signal of this stage (base and accelerated)

Status Information→ Op: for issuing the Tripping signal of this stage (base only)

Status Information→ AOp: for sending the Tripping signal of this stage (accelerated only)

Settings→ TmACrv: for setting the IEC curve type in case the stage is Td (base only) or if the stage is Ti:

a. 9 = NIT (IEC Normal Inverse)

b. 10 = VIT (IEC Very Inverse)

c. 12 = EIT (IEC Extremely Inverse)

d. 14 = LIT (IEC Long – Time Inverse)

e. 15 = Ti (IEC Definite Time)

Settings→ StrVal: for setting the current threshold of this stage (base and accelerated) when Ti (min..max; step; default; m.u.)

Settings→ MinOpTmms: for setting the minimum duration time of the accelerated (only) stage (min..max; step; default; m.u.)

Settings→ OpDlTmms: for setting the operate delay time of the stage **T67.S2** (base only) when Ti (min..max; step; default; m.u.)

Settings→ AOpDlTmms: for setting the operate delay time of the stage **T67.S2_c** (accelerated only) when Ti (min..max; step; default; m.u.)

Settings→ RsDlTmms: for setting the backup time of the stage **Tr67.S2** when Ti

Settings→ PAccelEna: for enabling the dual time calibration (acceleration) of this stage:

f. 0 = base only

g. 1 = base + accelerated

Settings→ PBst: for setting the behaviour of this stage (base and accelerated):

h. 0 = Start + Operate

i. 1 = Start only

Settings → FFSEna: for setting the participation in the Logic Selectivity function (publishing and subscribing) of this stage (base and accelerated):

j. 0 = excluded

k. 1 = participating

Settings → Bl2ndHEna: for allowing the blocking, due to 2nd harmonic restraint protection, of this stage (base and accelerated):

l. 0 = not blockable

m. 1 = stage Sx blockable due to 2nd harmonic

Settings → RsDlTEna: for setting the lock of the Backup Time Tr reset (used in the FSL) of this stage (base and accelerated):

n. 0 = reset not locked

o. 1 = reset locked

Settings → TmACStrVal: for setting the Ip of the curve in case of Td stage (base only) (min..max; step; default; m.u.)

Settings → TmACOpDlTm: for setting the Tp of the curve in case of Td stage (base only) (min..max; step; default; m.u.)

Settings → CLPMod: for setting the mode of the Cold Load Pickup function for this stage:

p. 0 = Off (Default)

q. 1 = On – Stage Block

r. 2 = On – Stage Modification

Settings → CLPOpPer: for setting the Operating Period of the Cold Load Pickup for this stage (0..100;0.01;0.1 sec).

The following REDR LN models the directional data and characteristics of the 67.S2 stage (base and accelerated).

Table 41 –LNInstance: 1 - prefix: P67S2 – REDR1 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				

		LN shall inherit all Mandatory Data from Common Logical Node Class		M
Status Information				
Dir	ACD	Direction		M
Settings				
ChrAng	ASG	Characteristic Angle		R
AChrAng	ASG	enel Additional Characteristic Angle		R
MinFwdAng	ASG	Minimum Phase Angle in Forward Direction		R
MinRvAng	ASG	Minimum Phase Angle in Reverse Direction		O
MaxFwdAng	ASG	Maximum Phase Angle in Forward Direction		O
MaxRvAng	ASG	Maximum Phase Angle in Reverse Direction		O
BlkValA	ASG	Minimum operating current		R
BlkValV	ASG	Minimum operating voltage		R
PolQty	ING	Polarising Quantity		O
MinPPV	ASG	Min Phase-Phase Voltage		O

NOTES:

Settings→ ChrAng: for setting the bisector of the Tripping Sector of the 67.S2 (Ti) stage

Settings→ AChrAng: for setting the bisector of the Tripping Sector of the 67.S2 (Td) stage

Settings→ MinFwdAng: for setting the halfwidth of the Tripping Sector of the 67.S2 (Ti+Td) stage

Settings→ BlkValA: for setting the residual current value 3Io of the 67.S2 (Ti+Td) stage

Settings→ BlkValV: for setting the residual voltage value 3Vo of the 67.S2 (Ti+Td) stage.

7.2.6.4. 67.S3 (Ti+Td) stage with dual time calibration

Table 42 – LNInstance: 1 - prefix: P67S3 PEOC2 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
OpCntRs	INC	Resetable operation counter		R
Status Information				
Str	ACD	Start		M
Op	ACT	Operate	T	M
AOp	ACT	enel Additional/Accelerated Operate	T	R
TmASt	CSD	Active curve characteristic		O
Settings				
TmACrv	CURVE	Operating Curve Type		R
StrVal	ASG	Start Value		R
TmMult	ASG	Time Dial Multiplier		O
MinOpTmms	ING	Minimum Operate Time		R
MaxOpTmms	ING	Maximum Operate Time		O
OpDlTmms	ING	Operate Delay Time		R
AOpDlTmms	ING	enel Additional/Accelerated Operate Delay Time		R

TypRsCrv	ING	Type Reset Curve		O
RsDlTmms	ING	Reset Delay Time		R
DirMod	ING	Directional Mode		O
PAccelEna	SPG	enel Protection Acceleration Enabling		R
PBst	SPG	enel Protection Behaviour (1=Str 2= Str+Op)		R
FFSEna	SPG	enel Fast Fault Selection Enabling (Participation in the Logic Selectivity)		R
Bl2ndHEna	SPG	enel Block due to 2nd H Enabling		R
RsDlTEna	SPG	enel Reset Delay Time Enabling (Logical Block /Tr)		R
TmACStrVal	ASG	enel Active curve characteristic Start Value (Ip for Td curve)		R
TmACOpDlTm	ING	enel Active curve characteristic Operate Delay Time (Tp for Td curve)		R
CLPMod	ING	enel Cold Load Pickup Mode		R
CLPOpPer	ASG	enel Cold Load Pickup Operating Period		R

NOTES:

Common Logical Node Information→ Mod: for handling the Enabling/Disabling command (1/5) of this protection stage (base and accelerated)

Common Logical Node Information→ OpCntRs: to count and store the number of operations of this stage (base and accelerated)

Status Information→ Str: for issuing the Start signal of this stage (base and accelerated)

Status Information→ Op: for issuing the Tripping signal of this stage (base only)

Status Information→ AOp: for sending the Tripping signal of this stage (accelerated only)

Settings→ TmACrv: for setting the IEC curve type in case the stage is Td (base only) or if the stage is Ti:

a. 9 = NIT (IEC Normal Inverse)

b. 10 = VIT (IEC Very Inverse)

c. 12 = EIT (IEC Extremely Inverse)

d. 14 = LIT (IEC Long – Time Inverse)

e. 15 = Ti (IEC Definite Time)

Settings→ StrVal: for setting the current threshold of this stage (base and accelerated) when Ti (min..max; step; default; m.u.)

Settings→ MinOpTmms: for setting the minimum duration time of the accelerated (only) stage (min..max; step; default; m.u.)

Settings→ OpDlTmms: for setting the operate delay time of the stage **T67.S3** (base only) when Ti (min..max; step; default; m.u.)

Settings→ AOpDlTmms: for setting the operate delay time of the stage **T67.S3_c** (accelerated only) when Ti (min..max; step; default; m.u.)

Settings→ RsDlTmms: for setting the backup time of the stage **Tr67.S3** when Ti

Settings→ PAccelEna: for enabling the dual time calibration (acceleration) of this stage:

f. 0 = base only

g. 1 = base + accelerated

Settings→ PBst: for setting the behaviour of this stage (base and accelerated):

h. 0 = Start + Operate

i. 1 = Start only

Settings → FFSEna: for setting the participation in the Logic Selectivity function (publishing and subscribing) of this stage (base and accelerated):

j. 0 = excluded

k. 1 = participating

Settings → BI2ndHEna: for allowing the blocking, due to 2nd harmonic restraint protection, of this stage (base and accelerated):

l. 0 = not blockable

m. 1 = stage Sx blockable due to 2nd harmonic

Settings → RsDITEna: for setting the lock of the Backup Time Tr reset (used in the FSL) of this stage (base and accelerated):

n. 0 = reset not locked

o. 1 = reset locked

Settings → TmACStrVal: for setting the Ip of the curve in case of Td stage (base only) (min..max; step; default; m.u.)

Settings → TmACOpDlTm: for setting the Tp of the curve in case of Td stage (base only) (min..max; step; default; m.u.)

Settings → CLPMod: for setting the mode of the Cold Load Pickup function for this stage:

p. 0 = Off (Default)

q. 1 = On – Stage Block

r. 2 = On – Stage Modification

Settings → CLPOpPer: for setting the Operating Period of the Cold Load Pickup for this stage (0..100;0.01;0.1 sec).

The following REDR LN models the directional data and characteristics of the 67.S3 stage (base and accelerated).

Table 43 –LNInstance: 1 - prefix: P67S3 – REDR1 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/ O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
Status Information				
Dir	ACD	Direction		M
Settings				
ChrAng	ASG	Characteristic Angle		R
AChrAng	ASG	enel Additional Characteristic Angle		R
MinFwdAng	ASG	Minimum Phase Angle in Forward Direction		R
MinRvAng	ASG	Minimum Phase Angle in Reverse Direction		O
MaxFwdAng	ASG	Maximum Phase Angle in Forward Direction		O
MaxRvAng	ASG	Maximum Phase Angle in Reverse Direction		O

BlkValA	ASG	Minimum operating current		R
BlkValV	ASG	Minimum operating voltage		R
PolQty	ING	Polarising Quantity		O
MinPPV	ASG	Min Phase-Phase Voltage		O

NOTES:

Settings→ ChrAng: for setting the bisector of the Tripping Sector of the 67.S3 (Ti) stage

Settings→ AChrAng: for setting the bisector of the Tripping Sector of the 67.S3 (Td) stage

Settings→ MinFwdAng: for setting the halfwidth of the Tripping Sector of the 67.S3 stage

Settings→ BlkValA: for setting the residual current value 3**Io** of the 67.S3 stage

Settings→ BlkValV: for setting the residual voltage value 3**Vo** of the 67.S3 stage.

7.2.6.5. 67.S4 (Ti+Td) stage with dual time calibration

Table 44 – LNInstance: 1 - prefix: P67S4 – PEOC2 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
OpCntRs	INC	Resetable operation counter		R
Status Information				
Str	ACD	Start		M
Op	ACT	Operate	T	M
AOp	ACT	enel Additional/Accelerated Operate	T	R
TmASt	CSD	Active curve characteristic		O
Settings				
TmACrv	CURVE	Operating Curve Type		R
StrVal	ASG	Start Value		R
TmMult	ASG	Time Dial Multiplier		O
MinOpTmms	ING	Minimum Operate Time		R
MaxOpTmms	ING	Maximum Operate Time		O
OpDlTmms	ING	Operate Delay Time		R
AOpDlTmms	ING	enel Additional/Accelerated Operate Delay Time		R
TypRsCrv	ING	Type Reset Curve		O
RsDlTmms	ING	Reset Delay Time		R
DirMod	ING	Directional Mode		O
PAccelEna	SPG	enel Protection Acceleration Enabling		R
PBst	SPG	enel Protection Behaviour (1=Str 2= Str+Op)		R
FFSEna	SPG	enel Fast Fault Selection Enabling (Participation in the Logic Selectivity)		R
Bl2ndHEna	SPG	enel Block due to 2nd H Enabling		R
RsDlTEna	SPG	enel Reset Delay Time Enabling (Logical Block /Tr)		R
TmACStrVal	ASG	enel Active curve characteristic Start Value (Ip for Td curve)		R

TmACOpDlTm	ING	enel Active curve characteristic Operate Delay Time (Tp for Td curve)		R
CLPMod	ING	enel Cold Load Pickup Mode		R
CLPOpPer	ASG	enel Cold Load Pickup Operating Period		R

NOTES:

Common Logical Node Information→ Mod: for handling the Enabling/Disabling command (1/5) of this protection stage (base and accelerated)

Common Logical Node Information→ OpCntRs: to count and store the number of operations of this stage (base and accelerated)

Status Information→ Str: for issuing the Start signal of this stage (base and accelerated)

Status Information→ Op: for issuing the Tripping signal of this stage (base only)

Status Information→ AOp: for sending the Tripping signal of this stage (accelerated only)

Settings→ TmACrv: for setting the IEC curve type in case the stage is Td (base only) or if the stage is Ti:

a. 9 = NIT (IEC Normal Inverse)

b. 10 = VIT (IEC Very Inverse)

c. 12 = EIT (IEC Extremely Inverse)

d. 14 = LIT (IEC Long – Time Inverse)

e. 15 = Ti (IEC Definite Time)

Settings→ StrVal: for setting the current threshold of this stage (base and accelerated) when Ti (min..max; step; default; m.u.)

Settings→ MinOpTmms: for setting the minimum duration time of the accelerated (only) stage (min..max; step; default; m.u.)

Settings→ OpDlTmms: for setting the operate delay time of the stage **T67.S4** (base only) when Ti (min..max; step; default; m.u.)

Settings→ AOpDlTmms: for setting the operate delay time of the stage **T67.S4_c** (accelerated only) when Ti (min..max; step; default; m.u.)

Settings→ RsDlTmms: for setting the backup time of the stage **Tr67.S4** when Ti

Settings→ PAccelEna: for enabling the dual time calibration (acceleration) of this stage:

f. 0 = base only

g. 1 = base + accelerated

Settings→ PBst: for setting the behaviour of this stage (base and accelerated):

h. 0 = Start + Operate

i. 1 = Start only

Settings → FFSEna: for setting the participation in the Logic Selectivity function (publishing and subscribing) of this stage (base and accelerated):

j. 0 = excluded

k. 1 = participating

Settings → Bl2ndHEna: for allowing the blocking, due to 2nd harmonic restraint protection, of this stage (base and accelerated):

l. 0 = not blockable

m. 1 = stage Sx blockable due to 2nd harmonic

Settings → RsDlTEna: for setting the lock of the Backup Time Tr reset (used in the FSL) of this stage (base and accelerated):

n. 0 = reset not locked

o. 1 = reset locked

Settings → TmACStrVal: for setting the Ip of the curve in case of Td stage (base only) (min..max; step; default; m.u.)

Settings → TmACOpDlTm: for setting the Tp of the curve in case of Td stage (base only) (min..max; step; default; m.u.)

Settings → CLPMod: for setting the mode of the Cold Load Pickup function for this stage:

p. 0 = Off (Default)

q. 1 = On – Stage Block

r. 2 = On – Stage Modification

Settings → CLPOpPer: for setting the Operating Period of the Cold Load Pickup for this stage (0..100;0.01;0.1 sec).

The following REDR LN models the directional data and characteristics of the 67.S4 stage (base and accelerated)

Table 45 –LNInstance: 1 - prefix: P67S4 – REDR1 type

Attribute Name	Attribute Type	Explanation	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
Status Information				
Dir	ACD	Direction		M
Settings				
ChrAng	ASG	Characteristic Angle		R
AChrAng	ASG	enel Additional Characteristic Angle		R
MinFwdAng	ASG	Minimum Phase Angle in Forward Direction		R
MinRvAng	ASG	Minimum Phase Angle in Reverse Direction		O
MaxFwdAng	ASG	Maximum Phase Angle in Forward Direction		O
MaxRvAng	ASG	Maximum Phase Angle in Reverse Direction		O
BlkValA	ASG	Minimum operating current		R
BlkValV	ASG	Minimum operating voltage		R
PolQty	ING	Polarising Quantity		O
MinPPV	ASG	Min Phase-Phase Voltage		O

NOTES:

Settings→ ChrAng: for setting the bisector of the Tripping Sector of the 67.S4 (Ti) stage

Settings→ AChrAng: for setting the bisector of the Tripping Sector of the 67.S4 (Td) stage

Settings→ MinFwdAng: for setting the halfwidth of the Tripping Sector of the 67.S4 (Ti+Td) stage

Settings→ BlkValA: for setting the residual current value 3Io of the 67.S4 (Ti+Td) stage

Settings→ BlkValV: for setting the residual voltage value 3Vo of the 67.S4 (Ti+Td) stage.

7.2.7 Directional earth Overcurrent protection (67N)

The 67N directional earth overcurrent protection must detect earth faults downstream of the installation point in grids with insulated neutral, neutral earthed through an impedance or a simple resistor.

This protection consists of five directional stages with dual time calibration; each stage can be configured as independent-time (Ti) or dependent-time (Td) with selectable standard curves. Ad-hoc LN classes are provided, according to the extension rules of the IEC 61850; they permit the selection of the operating mode, special functions and the configuration of the parameters linked to the curve (Ip, Tp).

The 67Nb stage doesn't' trip the Circuit Breaker, it is only used for cross-signalling (delayed start) between the MFP IEDs installed in the Substation as protection relays of the MV feeders.

In addition a LN is used for the common and general settings of the P67N stages.

7.2.7.1. P67N general settings

Table 46 – LNInstance: 1 - prefix: GS67N – GAPC2 type

Attribute Name	Attribute Type	Explanation	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
Loc	SPS	Local operation		O
OpCntRs	INC	Resetable operation counter		R
Controls				
SPCSO1	SPC	Single point controllable status output (1)		R
SPCSO2	SPC	Single point controllable status output (2)		R
SPCSO3	SPC	Single point controllable status output (3)		R
DPCSO	DPC	Double point controllable status output		O
ISCSO	INC	Integer status controllable status output		O
Status Information				
Auto	SPS	Automatic operation		O
Str	ACD	Start		M
Op	ACT	Operate	T	M
Settings				
StrVal	ASG	Start Value		R

NOTES:

Common Logical Node Information → OpCntRs: to count and store the number of P67N general reconfigurations

Controls → SPCSO1: for setting the measuring operating mode of the P67N stages:

a. 0 = current (Default)

b. 1 = current*cosfi

Controls → SPCSO2: for setting the Voltage reference type of the P67N stages:

c. 0 = Calculated Residual

d. 1 = Open Delta (Default)

Controls → SPCSO3: for setting the dead band of the P67N stages:

e. 0 = Off (Default)

f. 1 = On

Settings → StrVal: for setting the dead band multiplier of the P67N stages (1.5..10; 0.1; 1.5).

7.2.7.2. 67N.S1 (Ti+Td) stage with dual time calibration

Table 47 – LNInstance: 1 - prefix: N671 – PEOC2 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
OpCntRs	INC	Resetable operation counter		R
Status Information				
Str	ACD	Start		M
Op	ACT	Operate	T	M
AOp	ACT	enel Additional/Accelerated Operate	T	R
TmASt	CSD	Active curve characteristic		O
Settings				
TmACrv	CURVE	Operating Curve Type		R
StrVal	ASG	Start Value		R
TmMult	ASG	Time Dial Multiplier		O
MinOpTmms	ING	Minimum Operate Time		R
MaxOpTmms	ING	Maximum Operate Time		O
OpDlTmms	ING	Operate Delay Time		R
AOpDlTmms	ING	enel Additional/Accelerated Operate Delay Time		R
TypRsCrv	ING	Type Reset Curve		O
RsDlTmms	ING	Reset Delay Time		R
DirMod	ING	Directional Mode		O
PAccelEna	SPG	enel Protection Acceleration Enabling		R
PBst	SPG	enel Protection Behaviour (1=Str 2= Str+Op)		R
FFSEna	SPG	enel Fast Fault Selection Enabling (Participation in the Logic Selectivity)		R
Bl2ndHEna	SPG	enel Block due to 2nd H Enabling		R
RsDlTEna	SPG	enel Reset Delay Time Enabling (Logical Block /Tr)		R
TmACStrVal	ASG	enel Active curve characteristic Start Value (Ip for Td curve)		R
TmACOpDlTm	ING	enel Active curve characteristic Operate Delay Time (Tp for Td curve)		R
CLPMod	ING	enel Cold Load Pickup Mode		R
CLPOpPer	ASG	enel Cold Load Pickup Operating Period		R

NOTES:

Common Logical Node Information→ Mod: for handling the Enabling/Disabling command (1/5) of this protection stage (base and accelerated)

Common Logical Node Information→ OpCntRs: to count and store the number of operations of this stage (base and accelerated)

Status Information→ Str: for issuing the Start signal of this stage (base and accelerated)

Status Information→ Op: for issuing the Tripping signal of this stage (base only)

Status Information→ AOp: for sending the Tripping signal of this stage (accelerated only)

Settings→ TmACrv: for setting the IEC curve type in case the stage is Td (base only) or if the stage is Ti:

a. 9 = NIT (IEC Normal Inverse)

b. 10 = VIT (IEC Very Inverse)

c. 12 = EIT (IEC Extremely Inverse)

d. 14 = LIT (IEC Long – Time Inverse)

e. 15 = Ti (IEC Definite Time)

Settings→ StrVal: for setting the current threshold of this stage (base and accelerated) when Ti (min..max; step; default; m.u.)

Settings→ MinOpTmms: for setting the minimum duration time of the accelerated (only) stage (min..max; step; default; m.u.)

Settings→ OpDlTmms: for setting the operate delay time of the stage **T67N.S1** (base only) when Ti (min..max; step; default; m.u.)

Settings→ AOpDlTmms: for setting the operate delay time of the stage **T67N.S1_c** (accelerated only) when Ti (min..max; step; default; m.u.)

Settings→ RsDlTmms: for setting the backup time of the stage **Tr67N.S1** when Ti

Settings→ PAccelEna: for enabling the dual time calibration (acceleration) of this stage:

f. 0 = base only

g. 1 = base + accelerated

Settings→ PBst: for setting the behaviour of this stage (base and accelerated):

h. 0 = Start + Operate

i. 1 = Start only

Settings → FFSEna: for setting the participation in the Logic Selectivity function (publishing and subscribing) of this stage (base and accelerated):

j. 0 = excluded

k. 1 = participating

Settings → Bl2ndHEna: for allowing the blocking, due to 2nd harmonic restraint protection, of this stage (base and accelerated):

l. 0 = not blockable

m. 1 = stage Sx blockable due to 2nd harmonic

Settings → RsDlTEna: for setting the lock of the Backup Time Tr reset (used in the FSL) of this stage (base and accelerated):

n. 0 = reset not locked

o. 1 = reset locked

Settings → TmACStrVal: for setting the Ip of the curve in case of Td stage (base only) (min..max; step; default; m.u.)

Settings → TmACOpDlTm: for setting the Tp of the curve in case of Td stage (base only) (min..max; step; default; m.u.)

Settings → CLPMod: for setting the mode of the Cold Load Pickup function for this stage:

p. 0 = Off (Default)

q. 1 = On – Stage Block

r. 2 = On – Stage Modification

Settings → CLPOpPer: for setting the Operating Period of the Cold Load Pickup for this stage (0..100;0.01;0.1 sec).

The following REDR LN models the directional data and characteristics of the 67.S1 stage (base and accelerated).

Table 48 – LNInstance: 1 - prefix: N671 – REDR1 type

Attribute Name	Attribute Type	Explanation	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
Status Information				
Dir	ACD	Direction		M
Settings				
ChrAng	ASG	Characteristic Angle		R
AChrAng	ASG	enel Additional Characteristic Angle		R
MinFwdAng	ASG	Minimum Phase Angle in Forward Direction		R
MinRvAng	ASG	Minimum Phase Angle in Reverse Direction		O
MaxFwdAng	ASG	Maximum Phase Angle in Forward Direction		O
MaxRvAng	ASG	Maximum Phase Angle in Reverse Direction		O
BlkValA	ASG	Minimum operating current		R
BlkValV	ASG	Minimum operating voltage		R
PolQty	ING	Polarising Quantity		O
MinPPV	ASG	Min Phase-Phase Voltage		O

NOTES:

Settings→ ChrAng: for setting the bisector of the Tripping Sector of the 67N.S1 (Ti) stage

Settings→ AChrAng: for setting the bisector of the Tripping Sector of the 67N.S1 (Td) stage

Settings→ MinFwdAng: for setting the halfwidth of the Tripping Sector of the 67N.S1 (Ti+Td) stage

Settings→ BlkValA: for setting the residual current value 3Io of the 67N.S1 (Ti+Td) stage

Settings→ BlkValV: for setting the residual voltage value 3Vo of the 67N.S1 (Ti+Td) stage.

7.2.7.3. 67N.S2a (Ti+Td) stage with dual time calibration

Table 49 –LNInstance: 1 - prefix: N672a – PEOC2 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
OpCntRs	INC	Resetable operation counter		R
Status Information				
Str	ACD	Start		M
Op	ACT	Operate	T	M
AOp	ACT	enel Additional/Accelerated Operate	T	R
TmASt	CSD	Active curve characteristic		O
Settings				
TmACrv	CURVE	Operating Curve Type		R
StrVal	ASG	Start Value		R
TmMult	ASG	Time Dial Multiplier		O
MinOpTmms	ING	Minimum Operate Time		R
MaxOpTmms	ING	Maximum Operate Time		O
OpDlTmms	ING	Operate Delay Time		R
AOpDlTmms	ING	enel Additional/Accelerated Operate Delay Time		R
TypRsCrv	ING	Type Reset Curve		O
RsDlTmms	ING	Reset Delay Time		R
DirMod	ING	Directional Mode		O
PAccelEna	SPG	enel Protection Acceleration Enabling		R
PBst	SPG	enel Protection Behaviour (1=Str 2= Str+Op)		R
FFSEna	SPG	enel Fast Fault Selection Enabling (Participation in the Logic Selectivity)		R
Bl2ndHEna	SPG	enel Block due to 2nd H Enabling		R
RsDlTEna	SPG	enel Reset Delay Time Enabling (Logical Block /Tr)		R
TmACStrVal	ASG	enel Active curve characteristic Start Value (Ip for Td curve)		R
TmACOpDlTm	ING	enel Active curve characteristic Operate Delay Time (Tp for Td curve)		R
CLPMod	ING	enel Cold Load Pickup Mode		R
CLPOpPer	ASG	enel Cold Load Pickup Operating Period		R

NOTES:

Common Logical Node Information→ Mod: for handling the Enabling/Disabling command (1/5) of this protection stage (base and accelerated)

Common Logical Node Information→ OpCntRs: to count and store the number of operations of this stage (base and accelerated)

Status Information→ Str: for issuing the Start signal of this stage (base and accelerated)

Status Information→ Op: for issuing the Tripping signal of this stage (base only)

Status Information→ AOp: for sending the Tripping signal of this stage (accelerated only)

Settings→ TmACrv: for setting the **IEC curve type** in case the stage is Td (base only) or if the stage is Ti:

a. 9 = NIT (IEC Normal Inverse)

b. 10 = VIT (IEC Very Inverse)

c. 12 = EIT (IEC Extremely Inverse)

d. 14 = LIT (IEC Long – Time Inverse)

e. 15 = Ti (IEC Definite Time)

Settings→ StrVal: for setting the current threshold of this stage (base and accelerated) when Ti (min..max; step; default; m.u.)

Settings→ MinOpTmms: for setting the minimum duration time of the accelerated (only) stage (min..max; step; default; m.u.)

Settings→ OpDlTmms: for setting the operate delay time of the stage **T67N.S2a** (base only) when Ti (min..max; step; default; m.u.)

Settings→ AOpDlTmms: for setting the operate delay time of the stage **T67N. S2a_c** (accelerated only) when Ti (min..max; step; default; m.u.)

Settings→ RsDlTmms: for setting the backup time of the stage **Tr67N.S2a** when Ti

Settings→ PAccelEna: for enabling the dual time calibration (acceleration) of this stage:

f. 0 = base only

g. 1 = base + accelerated

Settings→ PBst: for setting the behaviour of this stage (base and accelerated):

h. 0 = Start + Operate

i. 1 = Start only

Settings → FFSEna: for setting the participation in the Logic Selectivity function (publishing and subscribing) of this stage (base and accelerated):

j. 0 = excluded

k. 1 = participating

Settings → Bl2ndHEna: for allowing the blocking, due to 2nd harmonic restraint protection, of this stage (base and accelerated):

l. 0 = not blockable

m. 1 = stage Sx blockable due to 2nd harmonic

Settings → RsDlTEna: for setting the lock of the Backup Time Tr reset (used in the FSL) of this stage (base and accelerated):

n. 0 = reset not locked

o. 1 = reset locked

Settings → TmACStrVal: for setting the Ip of the curve in case of Td stage (base only) (min..max; step; default; m.u.)

Settings → TmACOpDlTm: for setting the Tp of the curve in case of Td stage (base only) (min..max; step; default; m.u.)

Settings → CLPMod: for setting the mode of the Cold Load Pickup function for this stage:

p. 0 = Off (Default)

q. 1 = On – Stage Block

r. 2 = On – Stage Modification

Settings → CLPOpPer: for setting the Operating Period of the Cold Load Pickup for this stage (0..100;0.01;0.1 sec).

The following REDR LN models the directional data and characteristics of the 67N.S2a stage (base and accelerated).

Table 50 – LNInstance: 1 - prefix: N672a – REDR1 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
Status Information				
Dir	ACD	Direction		M
Settings				
ChrAng	ASG	Characteristic Angle		R
AChrAng	ASG	enel Additional Characteristic Angle		R
MinFwdAng	ASG	Minimum Phase Angle in Forward Direction		R
MinRvAng	ASG	Minimum Phase Angle in Reverse Direction		O
MaxFwdAng	ASG	Maximum Phase Angle in Forward Direction		O
MaxRvAng	ASG	Maximum Phase Angle in Reverse Direction		O
BlkValA	ASG	Minimum operating current		R
BlkValV	ASG	Minimum operating voltage		R
PolQty	ING	Polarising Quantity		O
MinPPV	ASG	Min Phase-Phase Voltage		O

NOTES:

Settings→ ChrAng: for setting the bisector of the Tripping Sector of the 67N.S2a (Ti) stage

Settings→ AChrAng: for setting the bisector of the Tripping Sector of the 67N.S2a (Td) stage

Settings→ MinFwdAng: for setting the halfwidth of the Tripping Sector of the 67N.S2a (Ti+Td) stage

Settings→ BlkValA: for setting the residual current value 3Io of the 67N.S2a (Ti+Td) stage

Settings→ BlkValV: for setting the residual voltage value 3Vo of the 67N.S2a (Ti+Td) stage.

7.2.7.4. 67N.S2b (Ti+Td) stage with dual time calibration

Table 51 –LNInstance: 1 - prefix: N672b – PEOC2 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
OpCntRs	INC	Resetable operation counter		R
Status Information				
Str	ACD	Start		M
Op	ACT	Operate	T	M
AOp	ACT	enel Additional/Accelerated Operate	T	R

TmASt	CSD	Active curve characteristic		O
Settings				
TmACrv	CURVE	Operating Curve Type		R
StrVal	ASG	Start Value		R
TmMult	ASG	Time Dial Multiplier		O
MinOpTmms	ING	Minimum Operate Time		R
MaxOpTmms	ING	Maximum Operate Time		O
OpDlTmms	ING	Operate Delay Time		R
AOpDlTmms	ING	enel Additional/Accelerated Operate Delay Time		R
TypRsCrv	ING	Type Reset Curve		O
RsDlTmms	ING	Reset Delay Time		R
DirMod	ING	Directional Mode		O
PAccelEna	SPG	enel Protection Acceleration Enabling		R
PBst	SPG	enel Protection Behaviour (1=Str 2= Str+Op)		R
FFSEna	SPG	enel Fast Fault Selection Enabling (Participation in the Logic Selectivity)		R
Bl2ndHEna	SPG	enel Block due to 2nd H Enabling		R
RsDlTEna	SPG	enel Reset Delay Time Enabling (Logical Block /Tr)		R
TmACStrVal	ASG	enel Active curve characteristic Start Value (Ip for Td curve)		R
TmACOpDlTm	ING	enel Active curve characteristic Operate Delay Time (Tp for Td curve)		R
CLPMod	ING	enel Cold Load Pickup Mode		R
CLPOpPer	ASG	enel Cold Load Pickup Operating Period		R

NOTES:

Common Logical Node Information→ Mod: for handling the Enabling/Disabling command (1/5) of this protection stage (base and accelerated)

Common Logical Node Information→ OpCntRs: to count and store the number of operations of this stage (base and accelerated)

Status Information→ Str: for issuing the Start signal of this stage (base and accelerated)

Status Information→ Op: for issuing the Tripping signal of this stage (base only)

Status Information→ AOp: for sending the Tripping signal of this stage (accelerated only)

Settings→ TmACrv: for setting the **IEC curve type** in case the stage is Td (base only) or if the stage is Ti:

a. 9 = NIT (IEC Normal Inverse)

b. 10 = VIT (IEC Very Inverse)

c. 12 = EIT (IEC Extremely Inverse)

d. 14 = LIT (IEC Long – Time Inverse)

e. 15 = Ti (IEC Definite Time)

Settings→ StrVal: for setting the current threshold of this stage (base and accelerated) when Ti (min..max; step; default; m.u.)

Settings→ MinOpTmms: for setting the minimum duration time of the accelerated (only) stage (min..max; step; default; m.u.)

Settings→ OpDlTmms: for setting the operate delay time of the stage **T67N.S2b** (base only) when Ti (min..max; step; default; m.u.)

Settings→ AOpDlTmms: for setting the operate delay time of the stage **T67N. S2b_c** (accelerated only) when Ti (min..max; step; default; m.u.)

Settings→ RsDlTmms: for setting the backup time of the stage **Tr67N.S2b** when Ti

Settings→ PAccelEna: for enabling the dual time calibration (acceleration) of this stage:

f. 0 = base only

g. 1 = base + accelerated

Settings→ PBst: for setting the behaviour of this stage (base and accelerated):

h. 0 = Start + Operate

i. 1 = Start only

Settings → FFSEna: for setting the participation in the Logic Selectivity function (publishing and subscribing) of this stage (base and accelerated):

j. 0 = excluded

k. 1 = participating

Settings → Bl2ndHEna: for allowing the blocking, due to 2nd harmonic restraint protection, of this stage (base and accelerated):

l. 0 = not blockable

m. 1 = stage Sx blockable due to 2nd harmonic

Settings → RsDITEna: for setting the lock of the Backup Time Tr reset (used in the FSL) of this stage (base and accelerated):

n. 0 = reset not locked

o. 1 = reset locked

Settings → TmACStrVal: for setting the Ip of the curve in case of Td stage (base only) (min..max; step; default; m.u.)

Settings → TmACOpDlTm: for setting the Tp of the curve in case of Td stage (base only) (min..max; step; default; m.u.)

Settings → CLPMod: for setting the mode of the Cold Load Pickup function for this stage:

p. 0 = Off (Default)

q. 1 = On – Stage Block

r. 2 = On – Stage Modification

Settings → CLPOpPer: for setting the Operating Period of the Cold Load Pickup for this stage (0..100;0.01;0.1 sec).

The following REDR LN models the directional data and characteristics of the 67N.S2b stage (base and accelerated).

Table 52 – LNInstance: 1 - prefix: N672b – REDR1 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				

		LN shall inherit all Mandatory Data from Common Logical Node Class		M
Status Information				
Dir	ACD	Direction		M
Settings				
ChrAng	ASG	Characteristic Angle		R
AChrAng	ASG	enel Additional Characteristic Angle		R
MinFwdAng	ASG	Minimum Phase Angle in Forward Direction		R
MinRvAng	ASG	Minimum Phase Angle in Reverse Direction		O
MaxFwdAng	ASG	Maximum Phase Angle in Forward Direction		O
MaxRvAng	ASG	Maximum Phase Angle in Reverse Direction		O
BlkValA	ASG	Minimum operating current		R
BlkValV	ASG	Minimum operating voltage		R
PolQty	ING	Polarising Quantity		O
MinPPV	ASG	Min Phase-Phase Voltage		O

NOTES:

Settings→ ChrAng: for setting the bisector of the Tripping Sector of the 67N.S2b (Ti) stage

Settings→ AChrAng: for setting the bisector of the Tripping Sector of the 67.S2b (Td) stage

Settings→ MinFwdAng: for setting the halfwidth of the Tripping Sector of the 67N.S2b stage

Settings→ BlkValA: for setting the residual current value 3Io of the 67N.S2b stage

Settings→ BlkValV: for setting the residual voltage value 3Vo of the 67N.S2b stage.

7.2.7.5. 67N.S3 (Ti+Td) stage with dual time calibration

Table 53 – LNInstance: 1 - prefix: N673 PEOC2 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
OpCntRs	INC	Resetable operation counter		R
Status Information				
Str	ACD	Start		M
Op	ACT	Operate	T	M
AOp	ACT	enel Additional/Accelerated Operate	T	R
TmASt	CSD	Active curve characteristic		O
Settings				
TmACrv	CURVE	Operating Curve Type		R
StrVal	ASG	Start Value		R
TmMult	ASG	Time Dial Multiplier		O
MinOpTmms	ING	Minimum Operate Time		R
MaxOpTmms	ING	Maximum Operate Time		O
OpDlTmms	ING	Operate Delay Time		R
AOpDlTmms	ING	enel Additional/Accelerated Operate Delay Time		R
TypRsCrv	ING	Type Reset Curve		O

RsDlTmms	ING	Reset Delay Time		R
DirMod	ING	Directional Mode		O
PAccelEna	SPG	enel Protection Acceleration Enabling		R
PBst	SPG	enel Protection Behaviour (1=Str 2= Str+Op)		R
FFSEna	SPG	enel Fast Fault Selection Enabling (Participation in the Logic Selectivity)		R
Bl2ndHEna	SPG	enel Block due to 2nd H Enabling		R
RsDlTEna	SPG	enel Reset Delay Time Enabling (Logical Block /Tr)		R
TmACStrVal	ASG	enel Active curve characteristic Start Value (Ip for Td curve)		R
TmACOpDlTm	ING	enel Active curve characteristic Operate Delay Time (Tp for Td curve)		R
CLPMod	ING	enel Cold Load Pickup Mode		R
CLPOpPer	ASG	enel Cold Load Pickup Operating Period		R

NOTES:

Common Logical Node Information→ Mod: for handling the Enabling/Disabling command (1/5) of this protection stage (base and accelerated)

Common Logical Node Information→ OpCntRs: to count and store the number of operations of this stage (base and accelerated)

Status Information→ Str: for issuing the Start signal of this stage (base and accelerated)

Status Information→ Op: for issuing the Tripping signal of this stage (base only)

Status Information→ AOp: for sending the Tripping signal of this stage (accelerated only)

Settings→ TmACrv: for setting the IEC curve type in case the stage is Td (base only) or if the stage is Ti:

a. 9 =0 NIT (IEC Normal Inverse)

b. 10 = VIT (IEC Very Inverse)

c. 12 = EIT (IEC Extremely Inverse)

d. 14 = LIT (IEC Long – Time Inverse)

e. 15 = Ti (IEC Definite Time)

Settings→ StrVal: for setting the current threshold of this stage (base and accelerated) when Ti (min..max; step; default; m.u.)

Settings→ MinOpTmms: for setting the minimum duration time of the accelerated (only) stage (min..max; step; default; m.u.)

Settings→ OpDlTmms: for setting the operate delay time of the stage **T67N.S3** (base only) when Ti (min..max; step; default; m.u.)

Settings→ AOpDlTmms: for setting the operate delay time of the stage **T67N.S3_c** (accelerated only) when Ti (min..max; step; default; m.u.)

Settings→ RsDlTmms: for setting the backup time of the stage **Tr67N.S3** when Ti

Settings→ PAccelEna: for enabling the dual time calibration (acceleration) of this stage:

f. 0 = base only

g. 1 = base + accelerated

Settings→ PBst: for setting the behaviour of this stage (base and accelerated):

h. 0 = Start + Operate

i. 1 = Start only

Settings → FFSEna: for setting the participation in the Logic Selectivity function (publishing and subscribing) of this stage (base and accelerated):

j. 0 = excluded

k. 1 = participating

Settings → Bl2ndHEna: for allowing the blocking, due to 2nd harmonic restraint protection, of this stage (base and accelerated):

l. 0 = not blockable

m. 1 = stage Sx blockable due to 2nd harmonic

Settings → RsDlTEna: for setting the lock of the Backup Time Tr reset (used in the FSL) of this stage (base and accelerated):

n. 0 = reset not locked

o. 1 = reset locked

Settings → TmACStrVal: for setting the Ip of the curve in case of Td stage (base only) (min..max; step; default; m.u.)

Settings → TmACOpDlTm: for setting the Tp of the curve in case of Td stage (base only) (min..max; step; default; m.u.)

Settings → CLPMod: for setting the mode of the Cold Load Pickup function for this stage:

p. 0 = Off (Default)

q. 1 = On – Stage Block

r. 2 = On – Stage Modification

Settings → CLPOpPer: for setting the Operating Period of the Cold Load Pickup for this stage (0..100;0.01;0.1 sec).

The following REDR LN models the directional data and characteristics of the 67N.S3 stage (base and accelerated).

Table 54 –LNInstance: 1 - prefix: N673 – REDR1 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
Status Information				
Dir	ACD	Direction		M
Settings				
ChrAng	ASG	Characteristic Angle		R
MinFwdAng	ASG	Minimum Phase Angle in Forward Direction		R
AChrAng	ASG	enel Additional Characteristic Angle		R
MinRvAng	ASG	Minimum Phase Angle in Reverse Direction		O
MaxFwdAng	ASG	Maximum Phase Angle in Forward Direction		O
MaxRvAng	ASG	Maximum Phase Angle in Reverse Direction		O
BlkValA	ASG	Minimum operating current		R
BlkValV	ASG	Minimum operating voltage		R

PolQty	ING	Polarising Quantity		O
MinPPV	ASG	Min Phase-Phase Voltage		O

NOTES:

Settings→ ChrAng: for setting the bisector of the Tripping Sector of the 67N.S3 (Ti) stage

Settings→ AChrAng: for setting the bisector of the Tripping Sector of the 67.S3 (Td) stage

Settings→ MinFwdAng: for setting the halfwidth of the Tripping Sector of the 67N.S3 stage

Settings→ BlkValA: for setting the residual current value 3Io of the 67N.S3 stage

Settings→ BlkValV: for setting the residual voltage value 3Vo of the 67N.S3 stage.

7.2.7.6. 67N.Sb (Ti+Td) stage with dual time calibration

Table 55 – LNInstance: 1 - prefix: N67b – PEOC2 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
OpCntRs	INC	Resetable operation counter		R
Status Information				
Str	ACD	Start		M
Op	ACT	Operate	T	M
AOp	ACT	enel Additional/Accelerated Operate	T	R
TmASt	CSD	Active curve characteristic		O
Settings				
TmACrv	CURVE	Operating Curve Type		R
StrVal	ASG	Start Value		R
TmMult	ASG	Time Dial Multiplier		O
MinOpTmms	ING	Minimum Operate Time		R
MaxOpTmms	ING	Maximum Operate Time		O
OpDlTmms	ING	Operate Delay Time		R
AOpDlTmms	ING	enel Additional/Accelerated Operate Delay Time		R
TypRsCrv	ING	Type Reset Curve		O
RsDlTmms	ING	Reset Delay Time		R
DirMod	ING	Directional Mode		O
PAccelEna	SPG	enel Protection Acceleration Enabling		R
PBst	SPG	enel Protection Behaviour (1=Str 2= Str+Op)		R
FFSEna	SPG	enel Fast Fault Selection Enabling (Participation in the Logic Selectivity)		R
Bl2ndHEna	SPG	enel Block due to 2nd H Enabling		R
RsDlTEna	SPG	enel Reset Delay Time Enabling (Logical Block /Tr)		R
TmACStrVal	ASG	enel Active curve characteristic Start Value (Ip for Td curve)		R
TmACOpDlTm	ING	enel Active curve characteristic Operate Delay Time (Tp for Td curve)		R
CLPMod	ING	enel Cold Load Pickup Mode		R
CLPOpPer	ASG	enel Cold Load Pickup Operating Period		R

NOTES:

Common Logical Node Information→ Mod: for handling the Enabling/Disabling command (1/5) of this protection stage (base and accelerated)

Common Logical Node Information→ OpCntRs: to count and store the number of operations of this stage (base and accelerated)

Status Information→ Str: for issuing the Start signal of this stage (base and accelerated)

Status Information→ Op: for issuing the Tripping signal of this stage (base only)

Status Information→ AOp: for sending the Tripping signal of this stage (accelerated only)

Settings→ TmACrv: for setting the **IEC curve type** in case the stage is Td (base only) or if the stage is Ti:

a. 9 = NIT (IEC Normal Inverse)

b. 10 = VIT (IEC Very Inverse)

c. 12 = EIT (IEC Extremely Inverse)

d. 14 = LIT (IEC Long – Time Inverse)

e. 15 = Ti (IEC Definite Time)

Settings→ StrVal: for setting the current threshold of this stage (base and accelerated) when Ti (min..max; step; default; m.u.)

Settings→ MinOpTmms: for setting the minimum duration time of the accelerated (only) stage (min..max; step; default; m.u.)

Settings→ OpDlTmms: for setting the operate delay time of the stage T67N.Sb (base only) when Ti (min..max; step; default; m.u.)

Settings→ AOpDlTmms: for setting the operate delay time of the stage T67N.Sb_c (accelerated only) when Ti (min..max; step; default; m.u.)

Settings→ RsDlTmms: for setting the backup time of the stage Tr67N.Sb when Ti

Settings→ PAccelEna: for enabling the dual time calibration (acceleration) of this stage:

f. 0 = base only

g. 1 = base + accelerated

Settings→ PBst: for setting the behaviour of this stage (base and accelerated):

h. 0 = Start + Operate

i. 1 = Start only

Settings → FFSEna: for setting the participation in the Logic Selectivity function (publishing and subscribing) of this stage (base and accelerated):

j. 0 = excluded

k. 1 = participating

Settings → Bl2ndHEna: for allowing the blocking, due to 2nd harmonic restraint protection, of this stage (base and accelerated):

l. 0 = not blockable

m. 1 = stage Sx blockable due to 2nd harmonic

Settings → RsDITEna: for setting the lock of the Backup Time Tr reset (used in the FSL) of this stage (base and accelerated):

n. 0 = reset not locked

o. 1 = reset locked

Settings → TmACStrVal: for setting the Ip of the curve in case of Td stage (base only) (min..max; step; default; m.u.)

Settings → TmACOpDlTm: for setting the Tp of the curve in case of Td stage (base only) (min..max; step; default; m.u.)

Settings → CLPMod: for setting the mode of the Cold Load Pickup function for this stage:

p. 0 = Off (Default)

q. 1 = On – Stage Block

r. 2 = On – Stage Modification

Settings → CLPOpPer: for setting the Operating Period of the Cold Load Pickup for this stage (0..100;0.01;0.1 sec).

The following REDR LN models the directional data and characteristics of the 67N.Sb stage (base and accelerated).

Table 56 – LNInstance: 1 - prefix: N67b – REDR1 type

Attribute Name	Attribute Type	Explanation	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
Status Information				
Dir	ACD	Direction		M
Settings				
ChrAng	ASG	Characteristic Angle		R
AChrAng	ASG	enel Additional Characteristic Angle		R
MinFwdAng	ASG	Minimum Phase Angle in Forward Direction		R
MinRvAng	ASG	Minimum Phase Angle in Reverse Direction		O
MaxFwdAng	ASG	Maximum Phase Angle in Forward Direction		O
MaxRvAng	ASG	Maximum Phase Angle in Reverse Direction		O
BlkValA	ASG	Minimum operating current		R
BlkValV	ASG	Minimum operating voltage		R
PolQty	ING	Polarising Quantity		O
MinPPV	ASG	Min Phase-Phase Voltage		O

NOTES:

Settings→ ChrAng: for setting the bisector of the Tripping Sector of the 67N.Sb (Ti) stage

Settings→ AChrAng: for setting the bisector of the Tripping Sector of the 67N.Sb (Td) stage

Settings→ MinFwdAng: for setting the halfwidth of the Tripping Sector of the 67N.Sb stage

Settings→ BlkValA: for setting the residual current value 3Io of the 67N.Sb stage

Settings→ BlkValV: for setting the residual voltage value 3Vo of the 67N.Sb stage.

The MFP is ready to issue the "67Sb Delayed Start" to other IEDs in the substation (other MFP installed as protection relay of the MV feeders). It will publish a GOOSE message carrying the following information:

a. MFP/LD_Prot/PEOC2/N67bPEOC1/Op

7.2.7.7. Subscription of the "67Sb Delayed Start" signal issued via GOOSE message by other MFP (protection relays of the MV feeders

Table 57 – LNInstance: 1 - prefix: b67Mon – GGIO8 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
EEHealth	INS	External equipment health (external sensor)		O
EEName	DPL	External equipment name plate		O
Loc	SPS	Local operation		O
OpCntRs	INC	Resetable operation counter		R
Measured values				
AnIn	MV	Analogue input		O
Controls				
SPCSO1	SPC	Single point controllable status output (1)		R
SPCSO2	SPC	Single point controllable status output (2)		R
…	…	…		…
SPCSO19	SPC	Single point controllable status output (19)		R
DPCSO	DPC	Double point controllable status output		O
ISCSO	INC	Integer status controllable status output		O
Status Information				
IntIn	INS	Integer status input		O
Alm	SPS	General single alarm		O
Ind	SPS	General indication (binary input)		O

NOTES:

Common Logical Node Information→ OpCntRs: to count and store the number of events occurred

Controls→ SPCSO1…9: for subscribing the "67Sb Delayed Start" issued by other MFP of the same bus-bar Sx:

a. 0 = reset

b. 1 = Started

Controls→ SPCSO10…19: for subscribing the "67Sb Delayed Start" issued by 67Sb other MFP of the other bus-bar Sy:

c. 0 = reset

d. 1 = Started

This LN is ready to receive via GOOSE the "67Sb Delayed Start" published by other MFP installed as protection relays of the MV feeders of the substation.

7.2.8 Negative Sequence Overcurrent protection (46)

This protection consists of two stages with dual time calibration; each stage can be configured as independent-time (Ti) or dependent-time (Td) with selectable standard curves. An ad-hoc LN class is provided, according to the extension rules of the IEC 61850; it permits the selection of the operating modes, special functions and the configuration of the parameters linked to the curve (Ip, Tp).

7.2.8.1. 46.S1 (Ti+Td) stage with dual time calibration

Table 58 – LNInstance: 1 - prefix: P46S1 – PEOC1 type

Attribute Name	Attribute Type	Explanation	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
OpCntRs	INC	Resetable operation counter		R
Status Information				
Str	ACD	Start		M
Op	ACT	Operate	T	M
AOp	ACT	enel Additional/Accelerated Operate	T	R
TmASt	CSD	Active curve characteristic		O
Settings				
TmACrv	CURVE	Operating Curve Type		R
StrVal	ASG	Start Value		R
TmMult	ASG	Time Dial Multiplier		O
MinOpTmms	ING	Minimum Operate Time		R
MaxOpTmms	ING	Maximum Operate Time		O
OpDlTmms	ING	Operate Delay Time		R
AOpDlTmms	ING	enel Additional/Accelerated Operate Delay Time		R
TypRsCrv	ING	Type Reset Curve		O
RsDlTmms	ING	Reset Delay Time		O
DirMod	ING	Directional Mode		O
PAccelEna	SPG	enel Protection Stage Acceleration Enabling		R
PBst	SPG	enel Protection Behaviour (1=Str 2= Str+Op)		R
FFSEna	SPG	enel Fast Fault Selection Enabling (Participation in the Logic Selectivity)		R
Bl2ndHEna	SPG	enel Block due to 2nd H Enabling		R
RsDlTEna	SPG	enel Reset Delay Time Enabling (Logical Block /Tr)		O
TmACStrVal	ASG	enel Active curve characteristic Start Value (Ip for Td curve)		R
TmACOpDlTm	ING	enel Active curve characteristic Operate Delay Time (Tp for Td curve)		R
CLPMod	ING	enel Cold Load Pickup Mode		R
CLPOpPer	ASG	enel Cold Load Pickup Operating Period		R

NOTES:

Common Logical Node Information→ Mod: for handling the Enabling/Disabling command (1/5) of this protection stage (base and accelerated)

Common Logical Node Information→ OpCntRs: to count and store the number of operations of this stage (base and accelerated)

Status Information→ Str: for issuing the Start signal of this stage (base and accelerated)

Status Information→ Op: for issuing the Tripping signal of this stage (base only)

Status Information→ AOp: for sending the Tripping signal of this stage (accelerated only)

Settings→ TmACrv: for setting the IEC curve type in case the stage is Td (base only) or if the stage is Ti:

a. 9 = NIT (IEC Normal Inverse)

b. 10 = VIT (IEC Very Inverse)

c. 12 = EIT (IEC Extremely Inverse)

d. 14 = LIT (IEC Long – Time Inverse)

e. 15 = Ti (IEC Definite Time)

Settings→ StrVal: for setting the current threshold of this stage (base and accelerated) when Ti (min..max; step; default; m.u.)

Settings→ MinOpTmms: for setting the minimum duration time of the accelerated (only) stage (min..max; step; default; m.u.)

Settings→ OpDlTmms: for setting the operate delay time of the stage **T46.S1** (base only) when Ti (min..max; step; default; m.u.)

Settings→ AOpDlTmms: for setting the operate delay time of the stage **T46.S1_c** (accelerated only) when Ti (min..max; step; default; m.u.)

Settings→ PAccelEna: for enabling the dual time calibration (acceleration) of this stage:

f. 0 = base only

g. 1 = base + accelerated

Settings→ PBst: for setting the behaviour of this stage (base and accelerated):

h. 0 = Start + Operate

i. 1 = Start only

Settings → FFSEna: for setting the participation in the Logic Selectivity function (publishing and subscribing) of this stage (base and accelerated):

j. 0 = excluded

k. 1 = participating

Settings → Bl2ndHEna: for allowing the blocking, due to 2nd harmonic restraint protection, of this stage (base and accelerated):

l. 0 = not blockable

m. 1 = stage Sx blockable due to 2nd harmonic

Settings → TmACStrVal: for setting the Ip of the curve in case of Td stage (base only) (min..max; step; default; m.u.)

Settings → TmACOpDlTm: for setting the Tp of the curve in case of Td stage (base only) (min..max; step; default; m.u.)

Settings → CLPMod: for setting the mode of the Cold Load Pickup function for this stage:

n. 0 = Off (Default)

o. 1 = On – Stage Block

p. 2 = On – Stage Modification

Settings → CLPOpPer: for setting the Operating Period of the Cold Load Pickup for this stage (0..100;0.01;0.1 sec).

7.2.8.2. 46.S4 (Ti+Td) stage with dual time calibration

Table 59 –LNInstance: 1 - prefix: P46S4 – PEOC1 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
OpCntRs	INC	Resetable operation counter		R
Status Information				
Str	ACD	Start		M
Op	ACT	Operate	T	M
AOp	ACT	enel Additional/Accelerated Operate	T	R
TmASt	CSD	Active curve characteristic		O
Settings				
TmACrv	CURVE	Operating Curve Type		R
StrVal	ASG	Start Value		R
TmMult	ASG	Time Dial Multiplier		O
MinOpTmms	ING	Minimum Operate Time		R
MaxOpTmms	ING	Maximum Operate Time		O
OpDlTmms	ING	Operate Delay Time		R
AOpDlTmms	ING	enel Additional/Accelerated Operate Delay Time		R
TypRsCrv	ING	Type Reset Curve		O
RsDlTmms	ING	Reset Delay Time		O
DirMod	ING	Directional Mode		O
PAccelEna	SPG	enel Protection Acceleration Enabling		R
PBst	SPG	enel Protection Behaviour (1=Str 2= Str+Op)		R
FFSEna	SPG	enel Fast Fault Selection Enabling (Participation in the Logic Selectivity)		R
Bl2ndHEna	SPG	enel Block due to 2nd H Enabling		R
RsDlTEna	SPG	enel Reset Delay Time Enabling (Logical Block /Tr)		O
TmACStrVal	ASG	enel Active curve characteristic Start Value (Ip for Td curve)		R
TmACOpDlTm	ING	enel Active curve characteristic Operate Delay Time (Tp for Td curve)		R
CLPMod	ING	enel Cold Load Pickup Mode		R
CLPOpPer	ASG	enel Cold Load Pickup Operating Period		R

NOTES:

Common Logical Node Information→ Mod: for handling the Enabling/Disabling command (1/5) of this protection stage (base and accelerated)

Common Logical Node Information→ OpCntRs: to count and store the number of operations of this stage (base and accelerated)

Status Information→ Str: for issuing the Start signal of this stage (base and accelerated)

Status Information→ Op: for issuing the Tripping signal of this stage (base only)

Status Information→ AOp: for sending the Tripping signal of this stage (accelerated only)

Settings→ TmACrv: for setting the IEC curve type in case the stage is Td (base only) or if the stage is Ti:

a. 9 = NIT (IEC Normal Inverse)

b. 10 = VIT (IEC Very Inverse)

c. 12 = EIT (IEC Extremely Inverse)

d. 14 = LIT (IEC Long – Time Inverse)

e. 15 = Ti (IEC Definite Time)

Settings→ StrVal: for setting the current threshold of this stage (base and accelerated) when Ti (min..max; step; default; m.u.)

Settings→ MinOpTmms: for setting the minimum duration time of the accelerated (only) stage (min..max; step; default; m.u.)

Settings→ OpDlTmms: for setting the operate delay time of the stage **T46.S4** (base only) when Ti (min..max; step; default; m.u.)

Settings→ AOpDlTmms: for setting the operate delay time of the stage **T46.S4_c** (accelerated only) when Ti (min..max; step; default; m.u.)

Settings→ PAccelEna: for enabling the dual time calibration (acceleration) of this stage:

f. 0 = base only

g. 1 = base + accelerated

Settings→ PBst: for setting the behaviour of this stage (base and accelerated):

h. 0 = Start + Operate

i. 1 = Start only

Settings → FFSEna: for setting the participation in the Logic Selectivity function (publishing and subscribing) of this stage (base and accelerated):

j. 0 = excluded

k. 1 = participating

Settings → Bl2ndHEna: for allowing the blocking, due to 2nd harmonic restraint protection, of this stage (base and accelerated):

l. 0 = not blockable

m. 1 = stage Sx blockable due to 2nd harmonic

Settings → TmACStrVal: for setting the Ip of the curve in case of Td stage (base only) (min..max; step; default; m.u.)

Settings → TmACOpDlTm: for setting the Tp of the curve in case of Td stage (base only) (min..max; step; default; m.u.)

Settings → CLPMod: for setting the mode of the Cold Load Pickup function for this stage:

n. 0 = Off (Default)

o. 1 = On – Stage Block

p. 2 = On – Stage Modification

Settings → CLPOpPer: for setting the Operating Period of the Cold Load Pickup for this stage (0..100;0.01;0.1 sec).

7.2.9 Unbalance Overcurrent protection (46N)

The unbalance protection function 46N must detect the unbalance between two banks of capacitors. It consists of one stage with dual time calibration; it can be configured as independent-time (Ti) or dependent-time (Td) with selectable standard curves. An ad-hoc LN classes is provided, according to the extension rules of the IEC 61850; it permits the selection of the operating modes, special functions and the configuration of the parameters linked to the curve (Ip, Tp).

7.2.9.1. 46N.S1 (Ti+Td) stage with dual time calibration

Table 60 – LNInstance: 1 - prefix: N46S1 –PEOC1 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
OpCntRs	INC	Resetable operation counter		R
Status Information				
Str	ACD	Start		M
Op	ACT	Operate	T	M
AOp	ACT	enel Additional/Accelerated Operate	T	R
TmASt	CSD	Active curve characteristic		O
Settings				
TmACrv	CURVE	Operating Curve Type		R
StrVal	ASG	Start Value		R
TmMult	ASG	Time Dial Multiplier		O
MinOpTmms	ING	Minimum Operate Time		R
MaxOpTmms	ING	Maximum Operate Time		O
OpDlTmms	ING	Operate Delay Time		R
AOpDlTmms	ING	enel Additional/Accelerated Operate Delay Time		R
TypRsCrv	ING	Type Reset Curve		O
RsDlTmms	ING	Reset Delay Time		O
DirMod	ING	Directional Mode		O
PAccelEna	SPG	enel Protection Stage Acceleration Enabling		R
PBst	SPG	enel Protection Behaviour (1=Str 2= Str+Op)		R
FFSEna	SPG	enel Fast Fault Selection Enabling (Participation in the Logic Selectivity)		R
Bl2ndHEna	SPG	enel Block due to 2nd H Enabling		R
RsDlTEna	SPG	enel Reset Delay Time Enabling (Logical Block /Tr)		O
TmACStrVal	ASG	enel Active curve characteristic Start Value (Ip for Td curve)		R
TmACOpDlTm	ING	enel Active curve characteristic Operate Delay Time (Tp for Td curve)		R
CLPMod	ING	enel Cold Load Pickup Mode		R
CLPOpPer	ASG	enel Cold Load Pickup Operating Period		R

NOTES:

Common Logical Node Information→ Mod: for handling the Enabling/Disabling command (1/5) of this protection stage (base and accelerated)

Common Logical Node Information→ OpCntRs: to count and store the number of operations of this stage (base and accelerated)

Status Information→ Str: for issuing the Start signal of this stage (base and accelerated)

Status Information→ Op: for issuing the Tripping signal of this stage (base only)

Status Information→ AOp: for sending the Tripping signal of this stage (accelerated only)

Settings→ TmACrv: for setting the IEC curve type in case the stage is Td (base only) or if the stage is Ti:

a. 9 = NIT (IEC Normal Inverse)

b. 10 = VIT (IEC Very Inverse)

c. 12 = EIT (IEC Extremely Inverse)

d. 14 = LIT (IEC Long – Time Inverse)

e. 15 = Ti (IEC Definite Time)

Settings→ StrVal: for setting the current threshold of this stage (base and accelerated) when Ti (min..max; step; default; m.u.)

Settings→ MinOpTmms: for setting the minimum duration time of the accelerated (only) stage (min..max; step; default; m.u.)

Settings→ OpDlTmms: for setting the operate delay time of the stage **T46N.S1** (base only) when Ti (min..max; step; default; m.u.)

Settings→ AOpDlTmms: for setting the operate delay time of the stage **T46N.S1_c** (accelerated only) when Ti (min..max; step; default; m.u.)

Settings→ PAccelEna: for enabling the dual time calibration (acceleration) of this stage:

f. 0 = base only

g. 1 = base + accelerated

Settings→ PBst: for setting the behaviour of this stage (base and accelerated):

h. 0 = Start + Operate

i. 1 = Start only

Settings → FFSEna: for setting the participation in the Logic Selectivity function (publishing and subscribing) of this stage (base and accelerated):

j. 0 = excluded

k. 1 = participating

Settings → Bl2ndHEna: for allowing the blocking, due to 2nd harmonic restraint protection, of this stage (base and accelerated):

l. 0 = not blockable

m. 1 = stage Sx blockable due to 2nd harmonic

Settings → TmACStrVal: for setting the Ip of the curve in case of Td stage (base only) (min..max; step; default; m.u.)

Settings → TmACOpDlTm: for setting the Tp of the curve in case of Td stage (base only) (min..max; step; default; m.u.)

Settings → CLPMod: for setting the mode of the Cold Load Pickup function for this stage:

n. 0 = Off (Default)

o. 1 = On – Stage Block

p. 2 = On – Stage Modification

Settings → CLPOpPer: for setting the Operating Period of the Cold Load Pickup for this stage (0..100;0.01;0.1 sec).

7.2.10 Directional overcurrent "Arcing Ground" protection (67N.S4)

The protection trips the MV Circuit Breaker according to internal logics based on the settings of timers, the state of 67N.S1, 67N.S2a and 67N.S2b stages and the start of the 59N or, alternatively, the reception of the GOOSE with the starting state of 59VoV/W (depending on the neutral operation) issued by the MTP.

Additionally, it calculates the sign of the product Io*Vo of the first samples of the two residual quantities after a contingency to determine the direction of the fault. It communicates this information at Start time.

This protection consists of one stage only; the directionality is derived from the internal logics, therefore no Directional element LN is provided.

7.2.10.1. 67N.S4 stage

Table 61 – LNInstance: 1 - prefix: N67S4 – GAPC3 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
Loc	SPS	Local operation		O
OpCntRs	INC	Resetable operation counter		R
Controls				
SPCSO	SPC	Single point controllable status output		R
DPCSO	DPC	Double point controllable status output		O
ISCSO	INC	Integer status controllable status output		O
Status Information				
Auto	SPS	Automatic operation		O
Str	ACD	Start		M
Op	ACT	Operate	T	M
Settings				
StrVal1	ASG	Start Value (1)		R
StrVal2	ASG	Start Value (2)		R
StrVal3	ASG	Start Value (3)		R
StrVal4	ASG	Start Value (4)		R
StrVal5	ASG	Start Value (5)		R
PBst	SPG	enel Protection Behaviour (1=Str 2= Str+Op)		R
FFSEna	SPG	enel Fast Fault Selection Enabling (Participation in the Logic Selectivity)		R
Bl2ndHEna	SPG	enel Block due to 2nd H Enabling		R

NOTES:

Common Logical Node Information→ Mod: for handling the Enabling/Disabling command (1/5) of this protection stage

Common Logical Node Information→ OpCntRs: to count and store the number of operations of this stage

Status Information→ Str: for issuing the Start signal of this stage (mandatory)

Status Information→ Op: for issuing the Tripping signal of this stage (mandatory)

Settings → SPCSO: for subscribing the residual overvoltage starting signal VoV/W issued by the MTP

Settings → StrVal1: for setting the timer T1 –T67.4a of the 67N.S4 internal logics (0..80s; 0.010s; 80s)

Settings → StrVal2: for setting the timer T2 – T674.b of the 67N.S4 internal logics (0..80s; 0.010s; 80s)

Settings → StrVal3: for setting the timer T3 – T674 of the 67N.S4 internal logics (0..80s; 0.010s; 80s)

Settings → StrVal4: for setting the timer T4 - T674R of the 67N.S4 internal logics (0..80s; 0.010s; 80s)

Settings → StrVal5: for setting the timer T5 – T674I of the 67N.S4 internal logics (0..1.000s; 0.010s; 0.010s)

Settings→ PBst: for setting the behaviour of this stage:

q. 0 = Start + Operate

a. 1 = Start only

Settings → FFSEna: for setting the participation in the Logic Selectivity function (publishing and subscribing) of this stage:

b. 0 = excluded

c. 1 = participating

Settings → Bl2ndHEna: for allowing the blocking, due to 2nd harmonic restraint protection, of this stage (base and accelerated):

d. 0 = not blockable

e. 1 = stage Sx blockable due to 2nd harmonic.

This LN is ready to receive via GOOSE the “59VoV/W Start” published by the MTP that protects the Transformer feeding the same bus-bar of the IED (installed as protection relays of the MV feeders of the substation).

7.2.11 Directional earth Overcurrent protection function for the detection of evolving Faults (67N.S5)

This protection function must detect the intermittent faults that originate on different feeders in the sequence they occur and in the operating conditions of the network.

The detection is performed by internal logics based on the settings of timers, the state of 67N.S1, 67N.S2a and 67N.S2b stages and the start of the 59N or, alternatively, the reception of the GOOSE with the starting state of 59VoV/W (depending on the neutral operation) issued by the MTP.

This protection consists of one stage only; the directionality is derived from the internal logics, therefore no Directional element LN is provided.

7.2.11.1. 67N.S5 stage

Table 62 – LNInstance: 1 - prefix: N67S5 – GAPC3 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
Loc	SPS	Local operation		O

OpCntRs	INC	Resetable operation counter		R
Controls				
SPCSO	SPC	Single point controllable status output		R
DPCSO	DPC	Double point controllable status output		O
ISCSO	INC	Integer status controllable status output		O
Status Information				
Auto	SPS	Automatic operation		O
Str	ACD	Start		M
Op	ACT	Operate	T	M
Settings				
StrVal1	ASG	Start Value (1)		R
StrVal2	ASG	Start Value (2)		R
StrVal3	ASG	Start Value (3)		R
StrVal4	ASG	Start Value (4)		R
StrVal5	ASG	Start Value (5)		R
PBst	SPG	enel Protection Behaviour (1=Str 2= Str+Op)		R
FFSEna	SPG	enel Fast Fault Selection Enabling (Participation in the Logic Selectivity)		R
Bl2ndHEna	SPG	enel Block due to 2nd H Enabling		R

NOTES:

Common Logical Node Information→ Mod: for handling the Enabling/Disabling command (1/5) of this protection stage

Common Logical Node Information→ OpCnt**Rs**: to count and store the number of operations of this stage

Status Information→ Str: for issuing the Start signal of this stage (mandatory)

Status Information→ Op: for issuing the Tripping signal of this stage (mandatory)

Settings → SPCSO: for subscribing the residual overvoltage starting signal VoV/W issued by the MTP

Settings → StrVal1: for setting the timer T1 – T67N5a of the 67N.S5 internal logics (0..80s; 0.010s; 80s)

Settings → StrVal2: for setting the timer T2 – T67N5 of the 67N.S5 internal logics (0..80s; 0.010s; 80s)

Settings → StrVal3: for setting the timer T3 – T67N5c of the 67N.S5 internal logics (0..80s; 0.010s; 80s)

Settings → StrVal4: or setting the timer T4 of the 67N.S5 internal logics (0..80s; 0.010s; 80s)

Settings → StrVal5: for setting the timer T5 of the 67N.S5 internal logics (0..1.000s; 0.010s; 0.010s)

Settings→ PBst: for setting the behaviour of this stage:

a. 0 = Start + Operate

b. 1 = Start only

Settings → FFSEna: for setting the participation in the Logic Selectivity function (publishing and subscribing) of this stage:

c. 0 = excluded

d. 1 = participating

Settings → Bl2ndHEna: for allowing the blocking, due to 2nd harmonic restraint protection, of this stage (base and accelerated):

e. 0 = not blockable

f. 1 = stage Sx blockable due to 2nd harmonic.

This LN is ready to receive via GOOSE the “59VoV/W Start” published by the MTP that protects the Transformer feeding the same bus-bar of the IED (installed as protection relays of the MV feeders of the substation).

7.2.12 Residual Overvoltage protection (59N)

This protection consists of three stages (one for emergency handling); each stage can be configured as independent-time (Ti) or dependent-time (Td) with a pre-defined curve. An ad-hoc LN class is provided, according to the extension rules of the IEC 61850; it permits the selection of the operating modes, special functions and the configuration of the parameters linked to the curve.

In addition a LN is used for the common and general settings of the P59N stages.

7.2.12.1. P59N general settings

Table 63 – LNInstance: 1 - prefix: GS59N – GAPC4 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
Loc	SPS	Local operation		O
OpCntRs	INC	Resetable operation counter		R
Controls				
SPCSO1	SPC	Single point controllable status output (1)		R
SPCSO2	SPC	Single point controllable status output (2)		R
DPCSO	DPC	Double point controllable status output		O
ISCSO	INC	Integer status controllable status output		O
Status Information				
Auto	SPS	Automatic operation		O
Str	ACD	Start		M
Op	ACT	Operate	T	M
Settings				
StrVal	ASG	Start Value		O

NOTES:

Common Logical Node Information → OpCntRs: to count and store the number of P59N general reconfigurations

Controls → SPCSO1: for setting the Voltage reference type of the P59N.S1 and P59N.S2 stages:

a. 0 = Calculated Residual

b. 1 = Open Delta (Default)

Controls → SPCSO2: for setting the Voltage reference type of the P59N.E stage:

c. 0 = Calculated Residual

d. 1 = Open Delta (Default).

7.2.12.2. 59N.S1 (Ti+Td) stage

Table 64 –LNInstance: 1 - prefix: N59S1 – PEOV1 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
OpCntRs	INC	Resetable operation counter		R
Status Information				
Str	ACD	Start		M
Op	ACT	Operate	T	R
TmVSt	CSD	Active curve characteristic		O
Settings				
TmVCrv	CURVE	Operating Curve Type		R
StrVal	ASG	Start Value		R
StrValTd	ASG	enel Start Value when Td		R
TmMult	ASG	Time Dial Multiplier		O
MinOpTmms	ING	Minimum Operate Time		O
MaxOpTmms	ING	Maximum Operate Time		O
OpDlTmms	ING	Operate Delay Time		R
OpDlTmmsTd	ING	enel Operate Delay Time when Td		R
PBst	SPG	enel Protection Behaviour (1=Str 2= Str+Op)		R

NOTES:

Common Logical Node Information→ Mod: for handling the Enabling/Disabling command (1/5) of this protection stage

Common Logical Node Information→ OpCntRs: to count and store the number of operations of this stage

Status Information→ Str: for issuing the Start signal of this stage

Status Information→ Op: for issuing the Tripping signal of this stage

Settings→ TmVCrv: for setting the curve type in case the stage is Td or if the stage is Ti:

a. 15 = Ti (IEC Definite Time)

b. 17 = Fixed Curve Type based on StrValTd and OpDlTmmsTd parameters

Settings→ StrVal: for setting the voltage threshold V0 of this stage when Ti (min..max; step; default; m.u.)

Settings→ StrValTd: for setting the voltage threshold V0 of this stage when Td (min..max; step; default; m.u.)

Settings→ OpDlTmms: for setting the operate delay time of the stage **T59N.S1** when Ti (min..max; step; default; m.u.)

Settings→ OpDlTmmsTd: for setting the operate delay time of the stage **T59N.S1** when Td (min..max; step; default; m.u.)

Settings→ PBst: for setting the behaviour of this stage:

c. 0 = Start + Operate

d. 1 = Start only.

7.2.12.3. 59N.S2 (Ti+Td) stage

Table 65 –LNInstance: 1 - prefix: N59S2 – PEOV1 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
OpCntRs	INC	Resetable operation counter		R
Status Information				
Str	ACD	Start		M
Op	ACT	Operate	T	R
TmVSt	CSD	Active curve characteristic		O
Settings				
TmVCrv	CURVE	Operating Curve Type		R
StrVal	ASG	Start Value		R
StrValTd	ASG	enel Start Value when Td		R
TmMult	ASG	Time Dial Multiplier		O
MinOpTmms	ING	Minimum Operate Time		O
MaxOpTmms	ING	Maximum Operate Time		O
OpDlTmms	ING	Operate Delay Time		R
OpDlTmmsTd	ING	enel Operate Delay Time when Td		R
PBst	SPG	enel Protection Behaviour (1=Str 2= Str+Op)		R

NOTES:

Common Logical Node Information→ Mod: for handling the Enabling/Disabling command (1/5) of this protection stage

Common Logical Node Information→ OpCntRs: to count and store the number of operations of this stage

Status Information→ Str: for issuing the Start signal of this stage

Status Information→ Op: for issuing the Tripping signal of this stage

Settings→ TmVCrv: for setting the curve type in case the stage is Td or if the stage is Ti:

a. 15 = Ti (IEC Definite Time)

b. 17 = Fixed Curve Type based on StrValTd and OpDlTmmsTd parameters

Settings→ StrVal: for setting the voltage threshold V0 of this stage when Ti (min..max; step; default; m.u.)

Settings→ StrValTd: for setting the voltage threshold V0 of this stage when Td (min..max; step; default; m.u.)

Settings→ OpDlTmms: for setting the operate delay time of the stage **T59N.S2** when Ti (min..max; step; default; m.u.)

Settings→ OpDlTmmsTd: for setting the operate delay time of the stage **T59N.E** when Td (min..max; step; default; m.u.)

Settings→ PBst: for setting the behaviour of this stage:

c. 0 = Start + Operate

d. 1 = Start only.

7.2.12.4. 59N.E (Ti+Td) emergency stage

This emergency stage must operate in case of Voltage (voltmetric) Analog Inputs of the IED or voltage transduction chain failure. When programmed via configuration SW the IED must autonomously deactivate all the protection functions that rely on current measurements.

Table 66 – LNInstance: 1 - prefix: P59NE – PEOV1 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
OpCntRs	INC	Resetable operation counter		R
Status Information				
Str	ACD	Start		M
Op	ACT	Operate	T	R
TmVSt	CSD	Active curve characteristic		O
Settings				
TmVCrv	CURVE	Operating Curve Type		R
StrVal	ASG	Start Value		R
StrValTd	ASG	enel Start Value when Td		R
TmMult	ASG	Time Dial Multiplier		O
MinOpTmms	ING	Minimum Operate Time		O
MaxOpTmms	ING	Maximum Operate Time		O
OpDlTmms	ING	Operate Delay Time		R
OpDlTmmsTd	ING	enel Operate Delay Time when Td		R
PBst	SPG	enel Protection Behaviour (1=Str 2= Str+Op)		R

NOTES:

Common Logical Node Information→ Mod: for handling the Enabling/Disabling command (1/5) of this protection stage

Common Logical Node Information→ OpCntRs: to count and store the number of operations of this stage

Status Information→ Str: for issuing the Start signal of this stage

Status Information→ Op: for issuing the Tripping signal of this stage

Settings→ TmVCrv: for setting the curve type in case the stage is Td or if the stage is Ti:

a. 15 = Ti (IEC Definite Time)

b. 17 = Fixed Curve Type based on StrValTd and OpDlTmmsTd parameters

Settings→ StrVal: for setting the voltage threshold V0 of this stage when Ti (min..max; step; default; m.u.)

Settings→ StrValTd: for setting the voltage threshold V0 of this stage when Td (min..max; step; default; m.u.)

Settings→ OpDlTmms: for setting the operate delay time of the stage T59N.E when Ti (min..max; step; default; m.u.)

Settings→ OpDlTmmsTd: for setting the operate delay time of the stage T59N.E when Td (min..max; step; default; m.u.)

Settings→ PBst: for setting the behaviour of this stage:

c. 0 = Start + Operate

d. 1 = Start only.

7.2.13 Phase-to-phase Overvoltage protection (59)

The phase-to-phase overvoltage protection function 59 must measure three phase voltages. This protection consists of two stages; each stage can be configured as independent-time (Ti) or dependent-time (Td) with a pre-defined curve. An ad-hoc LN class is provided, according to the extension rules of the IEC 61850; it permits the selection of the operating modes, special functions and the configuration of the parameters linked to the curve.

In addition a LN is used for the common and general settings of the P59 stages.

7.2.13.1. P59 general settings

Table 67 – LNInstance: 1 - prefix: GS59 – GAPC4 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
Loc	SPS	Local operation		O
OpCntRs	INC	Resetable operation counter		R
Controls				
SPCSO1	SPC	Single point controllable status output (1)		R
SPCSO2	SPC	Single point controllable status output (2)		R
DPCSO	DPC	Double point controllable status output		O
ISCSO	INC	Integer status controllable status output		O
Status Information				
Auto	SPS	Automatic operation		O
Str	ACD	Start		M
Op	ACT	Operate	T	M
Settings				
StrVal	ASG	Start Value		O

NOTES:

Common Logical Node Information → OpCntRs: to count and store the number of P59 general reconfigurations

Controls → SPCSO1: for setting the Voltage reference type of the P59 stages:

a. 0 = phase-to-phase V (Default)

b. 1 = phase V

Controls → SPCSO2: for setting the operating logic of the P59 stages:

c. 0 = S1 OR S2 (Default)

d. 1 = S1 AND S2.

7.2.13.2. 59.S1 (Ti+Td) stage operating in case of neutral earthed through a Petersen Coil

Table 68 –: 1 - prefix: P59S1C PEOV1 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
OpCntRs	INC	Resetable operation counter		R
Status Information				
Str	ACD	Start		M
Op	ACT	Operate	T	R
TmVSt	CSD	Active curve characteristic		O
Settings				
TmVCrv	CURVE	Operating Curve Type		R
StrVal	ASG	Start Value		R
StrValTd	ASG	enel Start Value when Td		R
TmMult	ASG	Time Dial Multiplier		O
MinOpTmms	ING	Minimum Operate Time		O
MaxOpTmms	ING	Maximum Operate Time		O
OpDlTmms	ING	Operate Delay Time		R
OpDlTmmsTd	ING	enel Operate Delay Time when Td		R
PBst	SPG	enel Protection Behaviour (1=Str 2= Str+Op)		R

NOTES:

Common Logical Node Information→ Mod: for handling the Enabling/Disabling command (1/5) of this protection stage

Common Logical Node Information→ OpCntRs: to count and store the number of operations of this stage

Status Information→ Str: for issuing the Start signal of this stage

Status Information→ Op: for issuing the Tripping signal of this stage

Settings→ TmVCrv: for setting the curve type in case the stage is Td or if the stage is Ti:

a. 15 = Ti (IEC Definite Time)

b. 17 = Fixed Curve Type based on StrValTd and OpDlTmmsTd parameters

Settings→ StrVal: for setting the voltage threshold V of this stage when Ti (min..max; step; default; m.u.)

Settings→ StrValTd: for setting the voltage threshold V of this stage when Td (min..max; step; default; m.u.)

Settings→ OpDlTmms: for setting the operate delay time of the stage **T59.S1** when Ti (min..max; step; default; m.u.)

Settings→ OpDlTmmsTd: for setting the operate delay time of the stage **T59.S1** when Td (min..max; step; default; m.u.)

Settings→ PBst: for setting the behaviour of this stage:

c. 0 = Start + Operate

d. 1 = Start only.

7.2.13.3. 59.S2 (Ti+Td) stage operating in case of insulated neutral

Table 69 – LNInstance: 1 - prefix: P59S2I – PEOV1 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
OpCntRs	INC	Resetable operation counter		R
Status Information				
Str	ACD	Start		M
Op	ACT	Operate	T	R
TmVSt	CSD	Active curve characteristic		O
Settings				
TmVCrv	CURVE	Operating Curve Type		R
StrVal	ASG	Start Value		R
StrValTd	ASG	enel Start Value when Td		R
TmMult	ASG	Time Dial Multiplier		O
MinOpTmms	ING	Minimum Operate Time		O
MaxOpTmms	ING	Maximum Operate Time		O
OpDlTmms	ING	Operate Delay Time		R
OpDlTmmsTd	ING	enel Operate Delay Time when Td		R
PBst	SPG	enel Protection Behaviour (1=Str 2= Str+Op)		R

NOTES:

Common Logical Node Information→ Mod: for handling the Enabling/Disabling command (1/5) of this protection stage

Common Logical Node Information→ OpCntRs: to count and store the number of operations of this stage

Status Information→ Str: for issuing the Start signal of this stage

Status Information→ Op: for issuing the Tripping signal of this stage

Settings→ TmVCrv: for setting the curve type in case the stage is Td or if the stage is Ti:

a. 15 = Ti (IEC Definite Time)

b. 17 = Fixed Curve Type based on StrValTd and OpDlTmmsTd parameters

Settings→ StrVal: for setting the voltage threshold V of this stage when Ti (min..max; step; default; m.u.)

Settings→ StrValTd: for setting the voltage threshold V of this stage when Td (min..max; step; default; m.u.)

Settings→ OpDlTmms: for setting the operate delay time of the stage **T59.S2** when Ti (min..max; step; default; m.u.)

Settings→ OpDlTmmsTd: for setting the operate delay time of the stage **T59.S2** when Td (min..max; step; default; m.u.)

Settings→ PBst: for setting the behaviour of this stage:

c. 0 = Start + Operate

d. 1 = Start only.

7.2.14 Discrimination of INRUSH currents (2nd H) protection

This protection doesn't issue tripping commands to the MV Circuit Breaker. It blocks (for a time T_ini_2ndH) the 51, 51N, 67 and 67N protections to avoid unwanted operations when the 2nd harmonic current overcomes a predetermined fraction of the fundamental component due to the energization of the transformers installed along the feeder.

Table 70 –LNInstance: 1- prefix: P87R2H – PHAR1 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
OpCntRs	INC	Resetable operation counter		R
Status Information				
Str	ACD	Start		M
Settings				
HaRst	ING	Number of harmonic restained		R
PhStr	ASG	Start Value		R
PhStop	ING	Stop Value		O
OpDlTmms	ING	Operate Delay Time		R
RsDlTmms	ING	Reset Delay Time		O

NOTES:

Common Logical Node Information→ Mod: for handling the Enabling/Disabling command (1/5) of this protection stage

Common Logical Node Information→ OpCntRs: to count and store the number of operations of this stage

Status Information→ Str: for reporting the blocking signal 87R2H

Settings→ HaRst: for setting the harmonic (the 2nd) that activate the restraint of the blockable protections' stages (if equipped with Bl2ndHEna set to value = 1)

Settings→ PhStr: for setting the operating threshold (%) of the 2nd harmonic current

Settings→ OpDlTmms: for setting the blocking time T_ini_2ndH of the blockable protections' stages (if equipped with Bl2ndHEna set to value = 1).

7.2.15 Directional active Overpower protection (32P)

This function is mainly used when the IED protects a bay exclusively dedicated to a self-producer customer. This protection consists of two independent-time stages.

7.2.15.1. 32P.S1 (Ti) stage

Table 71 – LNInstance: 1 - prefix: P32PS1 – PEOP1 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/ O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
OpCntRs	INC	Resetable operation counter		R
Status Information				
Str	ACD	Start		M
Op	ACT	Operate	T	M
Settings				
DirMod	ING	Directional Mode		R
StrVal	ASG	Start Value		R
OpDlTmms	ING	Operate Delay Time		R
RsDlTmms	ING	Reset Delay Time		R
PBst	SPG	enel Protection Behaviour (1=Str 2= Str+Op)		R
FFSEna	SPG	enel Fast Fault Selection Enabling (Participation in the Logic Selectivity)		R
RsDlTEna	SPG	enel Reset Delay Time Enabling (Logical Block /Tr)		R

NOTES:

Common Logical Node Information→ Mod: for handling the Enabling/Disabling command (1/5) of this protection stage

Common Logical Node Information→ OpCntRs: to count and store the number of operations of this stage

Status Information→ Str: for issuing the Start signal of this stage

Status Information→ Op: for issuing the Tripping signal of this stage

Settings→ DirMod: for setting the operating mode according to the direction of the active power flow:

a. 1 = operation based on the magnitude of the P (Non Directional)

b. 2 = operation based on the positive direction of the P (Direct)

c. 3 = operation based on the negative direction of the P (Inverse)

Settings→ StrVal: or setting the active power threshold of the 32P.S1 stage (min..max; step; default; m.u.)

Settings→ OpDlTmms: for setting the operate delay time of the stage **32P.S1** (min..max; step; default; m.u.)

Settings→ RsDlTmms: for setting the backup time of the stage **Tr32P.S1** (min..max; step; default; m.u.)

Settings→ PBst: for setting the behaviour of this stage:

d. 0 = Start + Operate

e. 1 = Start only

Settings → FFSEna: for setting the participation in the Logic Selectivity function (publishing and subscribing) of this stage:

f. 0 = excluded

g. 1 = participating

Settings → RsDlTEna: for setting the lock of the Backup Time Tr reset (used in the FSL) of this stage:

h. 0 = reset not locked

i. 1 = reset locked.

7.2.15.2. 32P.S2 (Ti) stage

Table 72 – LNInstance: 1 - prefix: P32PS2 – PEOP1 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
OpCntRs	INC	Resetable operation counter		R
Status Information				
Str	ACD	Start		M
Op	ACT	Operate	T	M
Settings				
DirMod	ING	Directional Mode		R
StrVal	ASG	Start Value		R
OpDlTmms	ING	Operate Delay Time		R
RsDlTmms	ING	Reset Delay Time		R
PBst	SPG	enel Protection Behaviour (1=Str 2= Str+Op)		R
FFSEna	SPG	enel Fast Fault Selection Enabling (Participation in the Logic Selectivity)		R
RsDlTEna	SPG	enel Reset Delay Time Enabling (Logical Block /Tr)		R

NOTES:

Common Logical Node Information→ Mod: for handling the Enabling/Disabling command (1/5) of this protection stage

Common Logical Node Information→ OpCntRs: to count and store the number of operations of this stage

Status Information→ Str: for issuing the Start signal of this stage

Status Information→ Op: for issuing the Tripping signal of this stage

Settings→ DirMod: for setting the operating mode according to the direction of the active power flow:

a. 1 = operation based on the magnitude of the P (Non Directional)

b. 2 = operation based on the positive direction of the P (Direct)

c. 3 = operation based on the negative direction of the P (Inverse)

Settings→ StrVal: or setting the active power threshold of the **32P.S2** stage (min..max; step; default; m.u.)

Settings→ OpDlTmms: for setting the operate delay time of the stage **32P.S2** (min..max; step; default; m.u.)

Settings→ RsDlTmms: for setting the backup time of the stage **Tr32P.S2** (min..max; step; default; m.u.)

Settings→ PBst: for setting the behaviour of this stage:

d. 0 = Start + Operate

e. 1 = Start only

Settings → FFSEna: for setting the participation in the Logic Selectivity function (publishing and subscribing) of this stage:

f. 0 = excluded

g. 1 = participating

Settings → RsDlTEna: for setting the lock of the Backup Time Tr reset (used in the FSL) of this stage:

h. 0 = reset not locked

i. 1 = reset locked.

7.2.16 Synchro-check protection (25)

The Synchro-check protection function is designed to allow the interconnection in safe conditions of two grids, each one in the presence of electrical generation.

The Synchro-check protection function must satisfy all the requisites that allow the interconnection (or paralleling) between:

a. Synchronous networks (PS).

b. Asynchronous networks (PA).

The following LNs model the two paralleling functions and their settings.

Note: the synchro-check is performed for each Circuit Breaker closing, no matter the originator of the operation (automatic recloser, RTU, etc.).

7.2.16.1. Paralleling functions configuration

Table 73 – LNInstance: 1 - prefix: P25Cfg – GAPC5 type

Attribute Name	Attribute Type	Explanation	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
Loc	SPS	Local operation		O
OpCntRs	INC	Resetable operation counter		R
Controls				
SPCSO1	SPC	Single point controllable status output (1)		R
SPCSO2	SPC	Single point controllable status output (2)		R
SPCSO3	SPC	Single point controllable status output (3)		R
SPCSO4	SPC	Single point controllable status output (4)		R
DPCSO	DPC	Double point controllable status output		O
ISCSO1	INC	Integer status controllable status output (1)		R
ISCSO2	INC	Integer status controllable status output (2)		R
ISCSO3	INC	Integer status controllable status output (3)		R
Status Information				
Auto	SPS	Automatic operation		O
Str	ACD	Start		M
Op	ACT	Operate	T	M
Settings				
StrVal1	ASG	Start Value (1)		R

StrVal2	ASG	Start Value (2)		R
StrVal3	ASG	Start Value (3)		R
StrVal4	ASG	Start Value (4)		R
StrVal5	ASG	Start Value (5)		R
StrVal6	ASG	Start Value (6)		R
StrVal7	ASG	Start Value (7)		R
StrVal8	ASG	Start Value (8)		R
StrVal9	ASG	Start Value (9)		R
StrVal10	ASG	Start Value (10)		R
StrVal11	ASG	Start Value (11)		R
StrVal12	ASG	Start Value (12)		R
StrVal13	ASG	Start Value (12)		R
StrVal14	ASG	Start Value (14)		R
StrVal15	ASG	Start Value (15)		R
StrVal16	ASG	Start Value (16)		R

NOTES:

Common Logical Node Information→ OpCntRs: to count and store the number of operations of this stage

Controls → SPCSO1: for setting the Voltage Presence threshold V1 (0=Off..1=On; 1=On)

Controls → SPCSO2: for setting the Voltage Presence threshold V2 (0=Off..1=On; 1=On)

Controls → SPCSO3: for setting the Voltage Absence threshold V1 (0=Off..1=On; 1=On)

Controls → SPCSO4: for setting the Voltage Absence threshold V2 (0=Off..1=On; 1=On)

Controls → ISCSO1: for setting the Max. difference between the phase angles of the voltages, V2 in advance on V1 (1..60°; 1°; 3°)

Controls → ISCSO2: for setting the Max. difference between the phase angles of the voltages, V2 delayed on V1 (1..60°; 1°; 3°)

Controls → ISCSO3: for setting the phase voltage compared with the VRIF (1=V4-0, 2=V8-0, 3=V12-0; 1=V4-0)

Settings → StrVal1: for setting the min. stabilization time (0.10..10.00s; 0.01s; 0.10s)

Settings → StrVal2: for setting the Max. synchronization attempt time (1..20min; 1min; 10min)

Settings → StrVal3: for setting the Synchronism emission delay (0..60s; 0.01s; 0,1s)

Settings → StrVal4: for setting the Upper limit voltage threshold (0.50..1.50p.u.; 0.01p.u.; 1.10p.u.)

Settings → StrVal5: for setting the Lower limit voltage threshold (0.20..1.50p.u.; 0.01p.u.; 0.3p.u.)

Settings → StrVal6: for setting the Max. allowed frequency variation compared with the rated frequency (0.50..3.00Hz; 0.10Hz; 1.0Hz)

Settings → StrVal7: for setting the Max. allowed variation between frequency measurements (0.0..0.60Hz; 0.05Hz; 0Hz)

Settings → StrVal8: for setting the Max. frequency deviation threshold for fV1 > fV2 – Meaningful for Asynchronous networks (0.02..1Hz; 0.01Hz; 0.05Hz)

Settings → StrVal9: for setting the Max. frequency deviation threshold for fV2 > fV1 – Meaningful for Synchronous networks (0.02..1Hz; 0.01Hz; 0.05Hz)

Settings → StrVal10: for setting the Max. voltage deviation threshold for V1 > V2 (0.01..0.40V; 0.01V; 0.05V)

Settings → StrVal11: for setting the Max. voltage deviation threshold for V2 > V1 (0.01..0.40V; 0.01V; 0.05V)

Settings → StrVal12: for setting the operation Time V1>sync (0.05..0.60s; 0.01s; 0.20s)

Settings → StrVal13: for setting the operation Time V2>sync (0..10s; 0.01s; 0.25s)

Settings → StrVal14: for setting the operation Time V1<sync (0.05..0.60s; 0.01s; 0.20s)

Settings → StrVal15: for setting the operation Time V2<sync (0..10s; 0.01s; 0.25s)

Settings → StrVal16: for setting the synchro-check time TSYNC [s] (0..60s; 0,01s; 0,1s).

7.2.16.2. Synchro-check for Synchronous networks (PS)

Table 74 – LNInstance: 1 - prefix: P25PS – RSYN1 type

Attribute Name	Attribute Type	Explanation	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
Controls				
RHz	SPC	Raise Frequency		O
LHz	SPC	Lower Frequency		O
RV	SPC	Raise Voltage		O
LV	SPC	Lower Voltage		O
Status Information				
Rel	SPS	Release		M
VInd	SPS	Voltage Difference Indicator		O
AngInd	SPS	Angle Difference Indicator		O
HzInd	SPS	Frequency Difference Indicator		O
SynPrg	SPS	Synchronising in progress	T	O
Measured values				
DifVClc	MV	Calculated Difference in Voltage		O
DifHzClc	MV	Calculated Difference in Frequency		O
DifAngClc	MV	Calculated Difference of Phase Angle		O
Settings				
DifV	ASG	Difference Voltage		O
DifHz	ASG	Difference Frequency		R
DifAng	ASG	Difference Phase Angle		O
LivDeaMod	ING	Live Dead Mode		O
DeaLinVal	ASG	Dead Line Value		O
LivLinVal	ASG	Live Line Value		O
DeaBusVal	ASG	Dead Bus Value		O
LivBusVal	ASG	Live Bus Value		O
PlsTmms	ING	Close Pulse Time		O
BkrTmms	ING	Closing time of breaker		O

NOTES:

Common Logical Node Information→ Mod: for handling the Enabling/Disabling command (1/5) of the Synchro-Check function (default: Disabled)

Status Information → Rel: for reporting the Synchro-Check operation in case of Synchronous networks:

a. 1 = Closing enabled

b. 0 = Closing inhibited

Settings → DifHz: for setting the maximum frequency deviation (Slip) threshold value to establish whether the networks are Synchronous (0.01..0.10Hz; 0.001Hz; 0.02Hz).

7.2.16.3. Synchro-check for Asynchronous networks (PA)

Table 75 – LNInstance: 1 - prefix: P25PA – RSYN2 type

Attribute Name	Attribute Type	Explanation	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
Controls				
RHz	SPC	Raise Frequency		O
LHz	SPC	Lower Frequency		O
RV	SPC	Raise Voltage		O
LV	SPC	Lower Voltage		O
Status Information				
Rel	SPS	Release		M
VInd	SPS	Voltage Difference Indicator		O
AngInd	SPS	Angle Difference Indicator		O
HzInd	SPS	Frequency Difference Indicator		O
SynPrg	SPS	Synchronising in progress	T	O
Measured values				
DifVClc	MV	Calculated Difference in Voltage		O
DifHzClc	MV	Calculated Difference in Frequency		O
DifAngClc	MV	Calculated Difference of Phase Angle		O
Settings				
DifV	ASG	Difference Voltage		O
DifHz	ASG	Difference Frequency		O
DifAng	ASG	Difference Phase Angle		O
LivDeaMod	ING	Live Dead Mode		O
DeaLinVal	ASG	Dead Line Value		O
LivLinVal	ASG	Live Line Value		O
DeaBusVal	ASG	Dead Bus Value		O
LivBusVal	ASG	Live Bus Value		O
PlsTmms	ING	Close Pulse Time		O
BkrTmms	ING	Closing time of breaker		R

NOTES:

Common Logical Node Information→ Mod: for handling the Enabling/Disabling command (1/5) of the Synchro-Check function (default: Disabled)

Status Information → Rel: for reporting the Synchro-Check operation in case of Asynchronous networks:

a. 1 = Closing enabled

b. 0= Closing inhibited

Settings → BkrTmms: for setting the closing time of the Circuit Breaker in ms (20..200ms, 1ms, 20 ms).

7.2.17 DC undervoltage protection (27X)

The DC undervoltage protection function of the Primary Substation must have a single opening Digital Output. It consists of one independent-time (Ti) stage; it has the capability to trip the MV Circuit Breaker when the IED is installed as a MV feeder protection relay.

When the settable delay time of the stage has expired, the logical trip signal (80.S) must be issued. When the voltage value returns above the threshold values, the protection must release.

Table 76 –LNInstance: 1 - prefix: P27X – PEUV1 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
OpCntRs	INC	Resetable operation counter		R
Status Information				
Str	ACD	Start		M
Op	ACT	Operate	T	R
TmVSt	CSD	Active curve characteristic		O
Settings				
TmVCrv	CURVE	Operating Curve Type		O
StrVal	ASG	Start Value		R
StrValTd	ASG	enel Start Value when Td		O
TmMult	ASG	Time Dial Multiplier		O
MinOpTmms	ING	Minimum Operate Time		O
MaxOpTmms	ING	Maximum Operate Time		O
OpDlTmms	ING	Operate Delay Time		R
OpDlTmmsTd	ING	enel Operate Delay Time when Td		O
PBst	SPG	enel Protection Behaviour (1=Str 2= Str+Op)		R

NOTES:

Common Logical Node Information→ Mod: for handling the Enabling/Disabling command (1/5) of this protection

Common Logical Node Information→ OpCntRs: to count and store the number of operations of this stage

Status Information→ Str: for issuing the Start signal of the 27X CC

Status Information→ Op: for issuing the Tripping signal of the 27X CC

Settings→ StrVal: for setting the voltage threshold of this stage (min..max; step; default; m.u.)

Settings→ OpDlTmms: for setting the operate delay time of this stage (fixed value)

Settings→ PBst: for setting the behaviour of this stage:

a. 0 = Start + Operate

b. 1 = Start only.

7.2.18 Petersen Coil intervention monitoring function (MOIM)

The following LN models the settings and info related to the MOIM internal logics, a system monitoring function that is able to diagnose if a 67N fault was cleared by the Petersen Coil or by the operation of a 67N tripping the controlled circuit-breaker.

7.2.18.1. MOIM: Resolving and non-resolving coil intervention

Table 77 – LNInstance: 1 - prefix: MOIM – GAPC6 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
Loc	SPS	Local operation		O
OpCntRs	INC	Resetable operation counter		R
Controls				
SPCSO1	SPC	Single point controllable status output (1)		R
SPCSO2	SPC	Single point controllable status output (2)		R
SPCSO3	SPC	Single point controllable status output (3)		R
SPCSO4	SPC	Single point controllable status output (4)		R
SPCSO5	SPC	Single point controllable status output (5)		R
DPCSO	DPC	Double point controllable status output		O
ISCSO	INC	Integer status controllable status output		O
Status Information				
Auto	SPS	Automatic operation		O
Str	ACD	Start		M
Op1	ACT	Operate (1)	T	M
Op2	ACT	Operate (2)	T	M
Settings				
StrVal1	ASG	Start Value (1)		R
StrVal2	ASG	Start Value (2)		R
StrVal3	ASG	Start Value (3)		R
StrVal4	ASG	Start Value (4)		R
StrVal5	ASG	Start Value (5)		R
StrVal6	ASG	Start Value (6)		R

NOTES:

Common Logical Node Information→ Mod: for handling the Enabling/Disabling command (1/5) of the MOIM function

Common Logical Node Information→ OpCntRs: to count and store the number of operations of this function

Controls → SPCSO1: EN_67N1 – for enabling the monitoring of the 67N.S1 state in the MOIM logics

a. 0 = disabled (Default)

b. 1 = enabled

Controls → SPCSO2: EN_67N.2a – for enabling the monitoring of the 67N.S2a state in the MOIM logics

c. 0 = disabled (Default)

d. 1 = enabled

Controls → SPCSO3: EN_67N.2b – for enabling the monitoring of the 67N.S2b state in the MOIM logics

e. 0 = disabled (Default)

f. 1 = enabled

Controls → SPCSO4: EN_59U2 – for enabling the monitoring of the 59U2 state in the MOIM logics

g. 0 = disabled (Default)

h. 1 = enabled

Controls → SPCSO5: EN_51.67 – for enabling the monitoring of the 51.X and 67.X states in the MOIM logics

i. 0 = disabled (Default)

j. 1 = enabled

Status Information→ Str: for issuing the Start signal of the MOIM function

Status Information → Op1: for reporting the **RisBob** - resolving coil intervention to the RTU (transient signal, relevant the state =1):

k. 0 = none,

l. 1 = RisBob - resolving coil intervention

Status Information → Op2: for reporting the **NRisBob** – non-resolving coil intervention to the RTU (transient signal, relevant the state =1):

m. 0 = none,

n. 1 = NRisBob - resolving coil intervention

Settings → StrVal1: for setting the T1 - Circuit Breaker Opening delay (0..0.1s; 0.01s; 0.1s)

Settings → StrVal2: for setting the T2 - 67N Start delay (0..0.1s; 0.01s; 0.1s)

Settings → StrVal3: T3 - for setting the Circuit Breaker Closing delay (0..200s; 0.01s; 1.0s)

Settings → StrVal4: T4 - for setting the resolving coil intervention delay (0..10.0s; 0.01s; 6.0s)

Settings → StrVal5: for setting the T5 - 67N Start Max. time (0..10.0s; 0.01s; 5.0s)

Settings → StrVal6: for setting the intervention voltage value referred to the rated phase voltage (0.04..1.5p.u.; 0.001p.u.; 0.1p.u.).

7.2.19 MV automatic load shedding function (EAC)

The MFP (ref. GSTP101) implements a set of functionalities and data models to perform the automatic load shedding of the controlled MV feeder. The following LNs model:

a. The general settings of the EAC function

b. The Blocking protection stages of the MFP frequencies protections due to
- Undervoltage (27),
- Overvoltage (59),
- Maximum voltage unbalance β,
- Maximum frequency difference γ,
- Maximum allowed variation between consecutive periods Maxdt (salto di fase),

- Reverse Active Overpower,
- Summarised frequency protection block;

c. Two tripping protections, all of which with
- Two independent frequency stages (settable as under/over-frequency),
- One rate of change of frequency (df/dt) stage.

Table 78 – LNInstance: 1 - prefix: EACMng – GAPC7 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
Loc	SPS	Local operation		O
OpCntRs	INC	Resetable operation counter		R
Controls				
SPCSO	SPC	Single point controllable status output		O
DPCSO	DPC	Double point controllable status output		O
ISCSO	INC	Integer status controllable status output		O
Status Information				
Auto	SPS	Automatic operation		O
Str	ACD	Start		M
Op	ACT	Operate	T	M
Settings				
StrVal1	ASG	Start Value (1)		R
StrVal2	ASG	Start Value (2)		R
StrVal3	ASG	Start Value (3)		R
StrVal4	ASG	Start Value (4)		R
StrVal5	ASG	Start Value (5)		R
StrVal6	ASG	Start Value (6)		R
StrVal7	ASG	Start Value (7)		R
StrVal8	ASG	Start Value (8)		R
StrVal9	ASG	Start Value (9)		R
StrVal10	ASG	Start Value (10)		R
StrVal11	ASG	Start Value (11)		R

NOTES:

Common Logical Node Information→ OpCntRs: to count and store the number of events occurred (settings)

Settings→ StrVal1: for setting the number of semi-periods for the calculation of the average of the frequencies (1..32; step 1; default 10)

Settings→ StrVal2: for setting the number of semi-periods for the calculation of the df/dt first scale (0..20; step 1; default 15)

Settings→ StrVal3: for setting the number of semi-periods for the calculation of the df/dt second scale (0..20; step 1; default 10)

Settings→ StrVal4: for setting the number of semi-periods for the calculation of the df/dt third scale (0..20; step 1; default 5)

Settings→ StrVal5: for setting the number of averages for the calculation of the df/dt first scale (enumerative Averages 1, 2, 4, 8; default 8)

Settings→ StrVal6: for setting the number of averages for the calculation of the df/dt second scale (enumerative Averages 1, 2, 4, 8; default 4)

Settings→ StrVal7: for setting the number of averages for the calculation of the df/dt third scale (enumerative Averages 1, 2, 4, 8; default 2)

Settings→ StrVal8: for setting the enabling delay of the frequency protections (0..20 s; step 0.01 s; default 0.05 s)

Settings→ StrVal9: for setting the enabling delay of the df/dt protections from L1 (0..20 s; step 0.01 s; default 0.05 s)

Settings→ StrVal10: for setting the enabling delay of the df/dt protections from L2 (0..20 s; step 0.01 s; default 0.05 s)

Settings→ StrVal11: for setting the enabling delay of the df/dt protections from L3 (0..20 s; step 0.01 s; default 0.05 s).

7.2.19.1. Under/Over-voltage blocking stages

This function, able to block the operation of the frequency protections of the IED, consists of:

a. One Overvoltage stage,

b. One Undervoltage stage.

Table 79 – LNInstance: 1 - prefix: bUOV – REBV1 type

Attribute Name	Attribute Type	Explanation	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
Loc	SPS	Local operation		O
OpCntRs	INC	Resetable operation counter		R
Controls				
IBPrUV	SPC	Inclusion of protection-blocking function due to Under Voltage		R
IBPrOV	SPC	Inclusion of protection-blocking function due to Ovder Voltage		R
Status Information				
StrBUV	ACD	Start due to Under Voltage		O
StrBOV	ACD	Start due to Over Voltage		O
OpBUV	ACT	Block to the Protection(s) due to Under Voltage	T	R
OpBOV	ACT	Block to the Protection(s) due to Over Voltage	T	R
Settings				
StrValUV	ASG	Start Value		R
StrValOV	ASG	Start Value Over Voltage		R
OpDlTmsUV	ASG	Operate Delay Time due to Over Voltage		R
OpDlTmsOV	ASG	Operate Delay Time due to Over Voltage		R
OpPTmsUV	ASG	Operate Persistency Time due to Under Voltage		R
OpPTmsOV	ASG	Operate Persistency Time due to Overer Voltage		R

NOTES:

Common Logical Node Information→ OpCntRs: to count and store the number of blocking operations of this stage

Controls→ IBPrUV: for Enabling/Disabling the Undervoltage blocking function:

a. 0 = UV Disabled

b. 1 = UV Enabled

Controls→ IBPrOV: for Enabling/Disabling the Overvoltage blocking function:

c. 0 = OV Disabled

d. 1 = OV Enabled

Status Information→ OpBUV: for notifying the blocking of the frequency protections due to the Undervoltage blocking function

Status Information→ OpBOV: for notifying the blocking of the frequency protections due to the Overvoltage blocking function

Settings→ StrValUV: for setting the voltage threshold of the Undervoltage blocking stage (0 ÷ 1.4 Vn; step di 0,05 Vn)

Settings→ StrValOV: for setting the voltage threshold of the Overvoltage blocking stage (0 ÷ 1.4 Vn; step di 0,05 Vn)

Settings→ OpDlTmsUV: for setting the operate delay time of the Undervoltage blocking stage in seconds (0.1 ÷ 60 s, step di 0,05 s)

Settings→ OpDlTmsOV: for setting the operate delay time of the Overvoltage blocking stage in seconds (0.1 ÷ 60 s, step di 0,05 s)

Settings→ OpPTmsUV: for setting the blocking duration time due to the operation of the Undervoltage blocking stage in seconds (0.1 ÷ 1000 s, step di 0,05 s)

Settings→ OpPTmsOV: for setting the blocking duration time due to the operation of the Overvoltage blocking stage in seconds (0.1 ÷ 1000 s, step di 0,05 s).

7.2.19.2. Maximum voltage unbalance blocking stage

This function, able to block the operation of the frequency protections of the IED, consists of one Maximum voltage unbalance stage, operating when the Beta ratio (ref. [1]) supersedes a programmed threshold value.

Table 80 – LNInstance: 1 - prefix: bMSq – GAPC8 type

Attribute Name	Attribute Type	Explanation	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
Loc	SPS	Local operation		O
OpCntRs	INC	Resetable operation counter		R
Controls				
SPCSO	SPC	Single point controllable status output		O
DPCSO	DPC	Double point controllable status output		O
ISCSO	INC	Integer status controllable status output		O
Status Information				

Auto	SPS	Automatic operation		O
Str	ACD	Start		M
Op	ACT	Operate	T	M
Settings				
StrVal1	ASG	Start Value (1)		R
StrVal2	ASG	Start Value (2)		R
StrVal3	ASG	Start Value (3)		R

NOTES:

Common Logical Node Information→ Mod: for handling the Enabling/Disabling command (1/5) of this protection (default: Disabled)

Common Logical Node Information→ OpCntRs: to count and store the number of blocking operations of this stage

Status Information→ Op: for notifying the blocking of the frequency protections due to the Max. V unbalance blocking function

Settings→ StrVal1: for setting the **Beta** value of this stage (0,05 ÷ 1, step di 0,05)

Settings→ StrVal2: for setting the reset delay time of this stage in seconds (0.1 ÷ 60 s, step di 0,05 s)

Settings→ StrVal3: for setting the operate delay time of this stage in seconds (0.05 ÷ 1000 s, step di 0,01 s).

7.2.19.3. Maximum frequency difference blocking stage

This function, able to block the operation of the frequency protections of the IED, consists of one Maximum frequency difference stage, operating when the Gamma ratio (ref. [1]) supersedes a programmed threshold value.

Table 81 – LNInstance: 1 - prefix: bMdf – GAPC8 type

Attribute Name	Attribute Type	Explanation	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
Loc	SPS	Local operation		O
OpCntRs	INC	Resetable operation counter		R
Controls				
SPCSO	SPC	Single point controllable status output		O
DPCSO	DPC	Double point controllable status output		O
ISCSO	INC	Integer status controllable status output		O
Status Information				
Auto	SPS	Automatic operation		O
Str	ACD	Start		M
Op	ACT	Operate	T	M
Settings				
StrVal1	ASG	Start Value (1)		R
StrVal2	ASG	Start Value (2)		R
StrVal3	ASG	Start Value (3)		R

NOTES:

Common Logical Node Information→ Mod: for handling the Enabling/Disabling command (1/5) of this protection (default: Disabled)

Common Logical Node Information→ OpCntRs: to count and store the number of blocking operations of this stage

Status Information→ Op: for notifying the blocking of the frequency protections due to the Max. frequency difference function

Settings→ StrVal1: for setting the **Gamma** value of this stage (10 ÷ 100 mHz, step di 1 mHz)

Settings→ StrVal2: for setting the reset delay time of this stage in seconds (0 ÷ 100 s, step di 0,01 s)

Settings→ StrVal3: for setting the operate delay time of this stage in seconds (0.05 ÷ 1000 s, step di 0,01 s).

7.2.19.4. Maxdt (Maximum allowed variation between consecutive periods) blocking stage

This function, able to block the operation of the frequency protections of the IED, consists of one stage, operating due to discontinuous frequency variations (ref. GSTP101).

Table 82 –LNInstance: 1 - prefix: bMdt – GAPC9 type

Attribute Name	Attribute Type	Explanation	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
Loc	SPS	Local operation		O
OpCntRs	INC	Resetable operation counter		R
Controls				
SPCSO	SPC	Single point controllable status output		O
DPCSO	DPC	Double point controllable status output		O
ISCSO	INC	Integer status controllable status output		O
Status Information				
Auto	SPS	Automatic operation		O
Str	ACD	Start		M
Op	ACT	Operate	T	M
Settings				
StrVal	ASG	Start Value (1)		R

NOTES:

Common Logical Node Information→ Mod: for handling the Enabling/Disabling command (1/5) of this protection (default: Disabled)

Common Logical Node Information→ OpCntRs: to count and store the number of blocking operations of this stage

Status Information→ Op: for notifying the blocking of the frequency protections due to the Maxdt function

Settings→ StrVal: for setting the Maximum allowed variation between consecutive periods ΔT (50..7000μs, step 1μs; default 10μs) for the measurements of f and df/dt.

7.2.19.5. Reverse Active Overpower blocking stage

This function, able to block the operation of the frequency protections of the IED, consists of one stage (ref. GSTP101).

Table 83 – LNInstance: 1 - prefix: bMPr – GAPC8 type

Attribute Name	Attribute Type	Explanation	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
Loc	SPS	Local operation		O
OpCntRs	INC	Resetable operation counter		R
Controls				
SPCSO	SPC	Single point controllable status output		O
DPCSO	DPC	Double point controllable status output		O
ISCSO	INC	Integer status controllable status output		O
Status Information				
Auto	SPS	Automatic operation		O
Str	ACD	Start		M
Op	ACT	Operate	T	M
Settings				
StrVal1	ASG	Start Value (1)		R
StrVal2	ASG	Start Value (2)		R
StrVal3	ASG	Start Value (3)		R

NOTES:

Common Logical Node Information→ Mod: for handling the Enabling/Disabling command (1/5) of this protection (default: Disabled)

Common Logical Node Information→ OpCntRs: to count and store the number of blocking operations of this stage

Status Information→ Op: for notifying the blocking of the frequency protections due to the Reverse Active Overpower function

Settings→ StrVal1: for setting the P threshold value **StrValMV** of this stage (-1 ÷ 0 p.u.; step di 0,01 p.u.; default -0.1 p.u.)

Settings→ StrVal2: for setting the reset delay time **OpDlTmsR** of this stage in seconds (0 ÷ 100 s, step di 0,01 s)

Settings→ StrVal3: for setting the operate delay time **OpPTms** of this stage in seconds (0.05 ÷ 1000 s, step di 0,01 s).

7.2.19.6. Summarizer of the Block to the frequency-based protection instances of the MFP

This LN is used to connect the “operate” outputs of the above described blocking stages to a common “operate” that will block the two frequency based protection instances (B1 and B2) of the MFP.

Table 84 – LNInstance: 1- prefix: bGen – PTRC1 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
OpCntRs	INC	Resetable operation counter		R
Status Information				
Tr	ACT	Trip		(C) O
Op	ACT	Operate (combination of subscribed Op from protection functions)		(C) R
Str	ACD	Sum of all starts of all connected Logical Nodes		O
Settings				
TrMod	ING	Trip Mode		O
TrPlsTmms	ING	Trip Pulse Time		O

Condition C: At least one of the two status information (Tr, Op) shall be used.

NOTES:

Common Logical Node Information→ OpCntRs: to count and store the number of blockings to the frequency-based protections of the EAC

Status Information→ Op: for notifying the block of the two frequency based protection instances (B1 and B2) of the MFP due to one or more blocking stage.

7.2.19.7. Frequency and Rate of change of frequency based protection

The MFP implements two instances (B1 and B2) of this composite protection; each instance consists of:

a. Two independent frequency stages (settable as under/over-frequency),

b. One rate of change of frequency (df/dt) stage.

c. Ad-hoc settings of the stages (ranges, timers, logic types,…),

d. Summarizer of the frequency-based stage operation.

Table 85 – LNInstance: 1 - prefix: B1fdf – PEFD1 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
Loc	SPS	Local operation		O
OpCntRs	INC	Resetable operation counter		R
Controls				
IProtF1	SPC	Inclusion of frequency protection (1)		R
IProtF2	SPC	Inclusion of frequency protection (2)		R
IProtdF	SPC	Inclusion of df/dt protection		R
Status Information				
Str	ACD	Start		M
Op	ACT	Operate	T	M
Settings				
IWsCh	SPG	Inclusion of active power sign check		R
SFPThy1	SPG	Selection of Frequency protection type (1)		R

SFPThy2	SPG	Selection of Frequency protection type (2)		R
SdFPThy	ING	Selection of df/dt protection type (2)		R
StrValF1	ASG	Start Value of frequency protection (1)		R
StrValF2	ASG	Start Value of frequency protection (2)		R
StrValdF	ASG	Start Value of df/dt protection		R
OpDlTmsF1	ASG	Operate Delay Time of frequency protection (1)		R
OpDlTmsF2	ASG	Operate Delay Time of frequency protection (2)		R
OpDlTmsdF	ASG	Operate Delay Time of df/dt protection		R

NOTES:

Common Logical Node Information→ Mod: for handling the Enabling/Disabling command (1/5) of the whole B1 protection instance (default: Disabled)

Common Logical Node Information→ OpCntRs: to count and store the number of operations of this stage

Controls→ IProtF1: for Enabling/Disabling the f1 stage of the B1 protection instance:

a. 0 = f1 Disabled

b. 1 = f1 Enabled

Controls→ IProtF2: for Enabling/Disabling the f2 stage of the B1 protection instance:

c. 0 = f2 Disabled

d. 1 = f2 Enabled

Controls→ IProtdF: for Enabling/Disabling the df/dt stage of the B1 protection instance:

e. 0 = df Disabled

f. 1 = df Enabled

Status Information→ Str: for notifying the Start signal of the B1 protection instance

Status Information→ Op: for notifying the Operate signal of the B1 protection instance

Settings → IWsCh: for Enabling/Disabling the P sign check of the B1 protection instance:

g. 0 = Off

h. 1 = On

Controls→ SFPThy1: for selecting the protection type of the f1 stage of the B1 protection instance:

i. 0 = Underfrequency f1

j. 1 = Overfrequency f1

Controls→ SFPThy2: for selecting the protection type of the f2 stage of the B1 protection instance:

k. 0 = Underfrequency f2

l. 1 = Overfrequency f2

Controls→ SdFPThy: for selecting the protection type of the df/dt stage of the B1 protection instance:

m. 1 = Magnitude

n. 2 = Positive

o. 3 = Negative

Settings → StrValF1: for setting the f1 threshold value of the B1 protection instance (45.00 ÷ 55.00 Hz; step di 0,01 Hz)

Settings → StrValF2: for setting the f2 threshold value of the B1 protection instance (45.00 ÷ 55.00 Hz; step di 0,01 Hz)

Settings → StrValdF: for setting the df/dt threshold value of the B1 protection instance (0.1 ÷ 10 Hz/s; step di 0,1 Hz/s)

Settings → OpDlTmsF1: for setting the f1 operate delay time of the B1 protection instance in seconds (0 ÷ 60 s, step di 0,01 s)

Settings → OpDlTmsF2: for setting the f2 operate delay time of the B1 protection instance in seconds (0 ÷ 60 s, step di 0,01 s)

Settings → OpDlTmsdF: for setting the df/dt operate delay time of the B1 protection instance in seconds (0 ÷ 60 s, step di 0,01 s).

Table 86 – LNInstance: 1 - prefix: B2fdf – PEFD1 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
Loc	SPS	Local operation		O
OpCntRs	INC	Resetable operation counter		R
Controls				
IProtF1	SPC	Inclusion of frequency protection (1)		R
IProtF2	SPC	Inclusion of frequency protection (2)		R
IProtdF	SPC	Inclusion of df/dt protection		R
Status Information				
Str	ACD	Start		M
Op	ACT	Operate	T	M
Settings				
IWsCh	SPG	Inclusion of active power sign check		R
SFPThy1	SPG	Selection of Frequency protection type (1)		R
SFPThy2	SPG	Selection of Frequency protection type (2)		R
SdFPThy	ING	Selection of df/dt protection type (2)		R
StrValF1	ASG	Start Value of frequency protection (1)		R
StrValF2	ASG	Start Value of frequency protection (2)		R
StrValfdF	ASG	Start Value of df/dt protection		R
OpDlTmsF1	ASG	Operate Delay Time of frequency protection (1)		R
OpDlTmsF2	ASG	Operate Delay Time of frequency protection (2)		R
OpDlTmsdF	ASG	Operate Delay Time of df/dt protection		R

NOTES:

Common Logical Node Information→ Mod: for handling the Enabling/Disabling command (1/5) of the whole B2 protection instance (default: Disabled)

Common Logical Node Information→ OpCntRs: to count and store the number of operations of this stage

Controls→ IProtF1: for Enabling/Disabling the f1 stage of the B2 protection instance:

a. 0 = f1 Disabled

b. 1 = f1 Enabled

Controls→ IProtF2: for Enabling/Disabling the f2 stage of the B2 protection instance:

0 = f2 Disabled

1 = f3 Enabled

Controls→ IProtdF: for Enabling/Disabling the df/dt stage of the B2 protection instance:

c. 0 = df Disabled

d. 1 = df Enabled

Status Information→ Str: for notifying the Start signal of the B2 protection instance

Status Information→ Op: for notifying the Operate signal of the B2 protection instance

Settings → IWsCh: for Enabling/Disabling the P sign check of the B2 protection instance:

e. 0 = Off

f. 1 = On

Controls→ SFPThy1: for selecting the protection type of the f1 stage of the B2 protection instance:

g. 0 = Underfrequency f1

h. 1 = Overfrequency f1

Controls→ SFPThy2: for selecting the protection type of the f2 stage of the B2 protection instance:

i. 0 = Underfrequency f2

j. 1 = Overfrequency f2

Controls→ SdFPThy: for selecting the protection type of the df/dt stage of the B2 protection instance:

k. 1 = Magnitude

l. 2 = Positive

m. 3 = Negative

Settings → StrValF1: for setting the f1 threshold value of the B2 protection instance (45.00 ÷ 55.00 Hz; step di 0,01 Hz)

Settings → StrValF2: for setting the f2 threshold value of the B2 protection instance (45.00 ÷ 55.00 Hz; step di 0,01 Hz)

Settings → StrValdF: for setting the df/dt threshold value of the B2 protection instance (0.1 ÷ 10 Hz/s; step di 0,1 Hz/s)

Settings → OpDlTmsF1: for setting the f1 operate delay time of the B2 protection instance in seconds (0 ÷ 60 s, step di 0,01 s)

Settings → OpDlTmsF2: for setting the f2 operate delay time of the B2 protection instance in seconds (0 ÷ 60 s, step di 0,01 s)

Settings → OpDlTmsdF: for setting the df/dt operate delay time of the B2 protection instance in seconds (0 ÷ 60 s, step di 0,01 s).

7.2.20 Undervoltage protection (27)

The undervoltage protection 27 must measure the voltage at the MV busbar. This protection consists of two stages; each stage can be configured as independent-time (Ti) or dependent-time (Td) with a pre-

defined curve. An ad-hoc LN class is provided, according to the extension rules of the IEC 61850; it permits the selection of the operating modes, special functions and the configuration of the parameters linked to the curve.

In addition a LN is used for the common and general settings of the P27 stages.

7.2.20.1. P27 general settings

Table 87 –LNInstance: 1 - prefix: GS27 – GAPC4 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
Loc	SPS	Local operation		O
OpCntRs	INC	Resetable operation counter		R
Controls				
SPCSO1	SPC	Single point controllable status output (1)		R
SPCSO2	SPC	Single point controllable status output (2)		R
DPCSO	DPC	Double point controllable status output		O
ISCSO	INC	Integer status controllable status output		O
Status Information				
Auto	SPS	Automatic operation		O
Str	ACD	Start		M
Op	ACT	Operate	T	M
Settings				
StrVal	ASG	Start Value		O

NOTES:

Common Logical Node Information → OpCntRs: to count and store the number of P27 general reconfigurations

Controls → SPCSO1: for setting the Voltage reference type of the P27 stages:

a. 0 = phase-to-phase V (Default)

b. 1 = phase V

Controls → SPCSO2: for setting the operating logic of the P27 stages:

c. 0 = S1 OR S2 (Default)

d. 1 = S1 AND S2.

7.2.20.2. 27.S1 (Ti+Td) stage

Table 88 – LNInstance: 1 - prefix: P27S1 – PEUV2 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M

OpCntRs	INC	Resetable operation counter		R
Status Information				
Str	ACD	Start		M
Op	ACT	Operate	T	R
TmVSt	CSD	Active curve characteristic		O
Settings				
TmVCrv	CURVE	Operating Curve Type		R
StrVal	ASG	Start Value		R
StrValTd	ASG	enel Start Value when Td		R
TmMult	ASG	Time Dial Multiplier		O
MinOpTmms	ING	Minimum Operate Time		O
MaxOpTmms	ING	Maximum Operate Time		O
OpDlTmms	ING	Operate Delay Time		R
OpDlTmmsTd	ING	enel Operate Delay Time when Td		R
PBst	SPG	enel Protection Behaviour (1=Str 2= Str+Op)		R

NOTES:

Common Logical Node Information→ Mod: for handling the Enabling/Disabling command (1/5) of this protection stage

Common Logical Node Information→ OpCntRs: to count and store the number of operations of this stage

Status Information→ Str: for issuing the Start signal of this stage

Status Information→ Op: for issuing the Tripping signal of this stage

Settings→ TmVCrv: for setting the curve type in case the stage is Td or if the stage is Ti:

a. 15 = Ti (IEC Definite Time)

b. 17 = Fixed Curve Type based on StrValTd and OpDlTmmsTd parameters

Settings→ StrVal: for setting the voltage threshold V of this stage when Ti (min..max; step; default; m.u.)

Settings→ StrValTd: for setting the voltage threshold V of this stage when Td (min..max; step; default; m.u.)

Settings→ OpDlTmms: for setting the operate delay time of the stage **T27.S1** when Ti (min..max; step; default; m.u.)

Settings→ OpDlTmmsTd: for setting the operate delay time of the stage **T27.S1** when Td (min..max; step; default; m.u.)

Settings→ PBst: for setting the behaviour of this stage:

c. 0 = Start + Operate

d. 1 = Start only.

7.2.20.3. 27.S2 (Ti+Td) stage

Table 89 – LNInstance: 1 - prefix: P27S2 – PEUV2 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				

		LN shall inherit all Mandatory Data from Common Logical Node Class		M
OpCntRs	INC	Resetable operation counter		R
Status Information				
Str	ACD	Start		M
Op	ACT	Operate	T	R
TmVSt	CSD	Active curve characteristic		O
Settings				
TmVCrv	CURVE	Operating Curve Type		R
StrVal	ASG	Start Value		R
StrValTd	ASG	enel Start Value when Td		R
TmMult	ASG	Time Dial Multiplier		O
MinOpTmms	ING	Minimum Operate Time		O
MaxOpTmms	ING	Maximum Operate Time		O
OpDlTmms	ING	Operate Delay Time		R
OpDlTmmsTd	ING	enel Operate Delay Time when Td		R
PBst	SPG	enel Protection Behaviour (1=Str 2= Str+Op)		R

NOTES:

Common Logical Node Information→ Mod: for handling the Enabling/Disabling command (1/5) of this protection stage

Common Logical Node Information→ OpCntRs: to count and store the number of operations of this stage

Status Information→ Str: for issuing the Start signal of this stage

Status Information→ Op: for issuing the Tripping signal of this stage

Settings→ TmVCrv: for setting the curve type in case the stage is Td or if the stage is Ti:

a. 15 = Ti (IEC Definite Time)

b. 17 = Fixed Curve Type based on StrValTd and OpDlTmmsTd parameters

Settings→ StrVal: for setting the voltage threshold V of this stage when Ti (min..max; step; default; m.u.)

Settings→ StrValTd: for setting the voltage threshold V of this stage when Td (min..max; step; default; m.u.)

Settings→ OpDlTmms: for setting the operate delay time of the stage **T27.S2** when Ti (min..max; step; default; m.u.)

Settings→ OpDlTmmsTd: for setting the operate delay time of the stage **T27.S2** when Td (min..max; step; default; m.u.)

Settings→ PBst: for setting the behaviour of this stage:

c. 0 = Start + Operate

d. 1 = Start only.

7.2.21 Breaker Failure Protection related Function

This function consists of a single stage.

Table 90 –LNInstance: 1 - prefix: BF50 – REBF1 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
OpCntRs	INC	Resetable operation counter		R
Status Information				
Str	ACD	Start		M
OpIn	ACT	Operate, retrip (“internal trip”)	T	R
Settings				
TPTrTms	ASG	Three Pole Retrip Time Delay (seconds)		R
ValAPEna	SPG	Enabling BF Activation for Phase Current Threshold		R
StrValAP	ASG	Phase Current Threshold Value		R
ValAREna	SPG	Enabling BF Activation for Residual Current Threshold		R
StrValAR	ASG	Residual Current Threshold Value		R
StrCBSig	SPG	BF Activation based on CB Signals		R
PeA46S1	SPG	Protection Stage enabling the BF - 46S1 (Set A)		R
PeA46S4	SPG	Protection Stage enabling the BF - 46S4 (Set A)		R
PeAN46S1	SPG	Protection Stage enabling the BF - N46S1 (Set A)		R
PeA51S1	SPG	Protection Stage enabling the BF - 51S1 (Set A)		R
PeA51S2	SPG	Protection Stage enabling the BF - 51S2 (Set A)		R
PeA51S3	SPG	Protection Stage enabling the BF - 51S3 (Set A)		R
PeA51S4	SPG	Protection Stage enabling the BF - 51S4 (Set A)		R
PeA51NS1	SPG	Protection Stage enabling the BF - N51S1 (Set A)		R
PeA51NS2	SPG	Protection Stage enabling the BF - N51S2 (Set A)		R
PeAN51S3	SPG	Protection Stage enabling the BF - N51S3 (Set A)		R
PeAN51S1a	SPG	Protection Stage enabling the BF - N51S1a (Set A)		R
PeAN51S2a	SPG	Protection Stage enabling the BF - N51S2a (Set A)		R
PeAN51SE	SPG	Protection Stage enabling the BF - N51SE (Set A)		R
PeAN51S1	SPG	Protection Stage enabling the BF - N51RS1 (Set A)		R
PeAN51RS2	SPG	Protection Stage enabling the BF - N51RS2 (Set A)		R
PeAN51RS3	SPG	Protection Stage enabling the BF - N51RS3 (Set A)		R
PeA67S1	SPG	Protection Stage enabling the BF - 67S1 (Set A)		R
PeA67S2	SPG	Protection Stage enabling the BF - 67S2 (Set A)		R
PeA67S3	SPG	Protection Stage enabling the BF - 67S3 (Set A)		R
PeA67S4	SPG	Protection Stage enabling the BF - 67S4 (Set A)		R
PeAN67S1	SPG	Protection Stage enabling the BF - N67S1 (Set A)		R
PeAN67S2a	SPG	Protection Stage enabling the BF - N672a (Set A)		R
PeAN67S2b	SPG	Protection Stage enabling the BF - N672b (Set A)		R
PeAN67S3	SPG	Protection Stage enabling the BF - N673 (Set A)		R
PeAN67b	SPG	Protection Stage enabling the BF - N67b (Set A)		R
PeB46S1	SPG	Protection Stage enabling the BF - 46S1 (Set B)		R
PeB46S4	SPG	Protection Stage enabling the BF - 46S4 (Set B)		R
PeBN46S1	SPG	Protection Stage enabling the BF - N46S1 (Set B)		R
PeB51S1	SPG	Protection Stage enabling the BF - 51S1 (Set B)		R
PeB51S2	SPG	Protection Stage enabling the BF - 51S2 (Set B)		R
PeB51S3	SPG	Protection Stage enabling the BF - 51S3 (Set B)		R

PeB51S4	SPG	Protection Stage enabling the BF - 51S4 (Set B)		R
PeB51NS1	SPG	Protection Stage enabling the BF - N51S1 (Set B)		R
PeB51NS2	SPG	Protection Stage enabling the BF - N51S2 (Set B)		R
PeBN51S3	SPG	Protection Stage enabling the BF - N51S3 (Set B)		R
PeBN51S1a	SPG	Protection Stage enabling the BF - N51S1a (Set B)		R
PeBN51S2a	SPG	Protection Stage enabling the BF - N51S2a (Set B)		R
PeBN51SE	SPG	Protection Stage enabling the BF - N51SE (Set B)		R
PeBN51S1	SPG	Protection Stage enabling the BF - N51RS1 (Set B)		R
PeBN51RS2	SPG	Protection Stage enabling the BF - N51RS2 (Set B)		R
PeBN51RS3	SPG	Protection Stage enabling the BF - N51RS3 (Set B)		R
PeB67S1	SPG	Protection Stage enabling the BF - 67S1 (Set B)		R
PeB67S2	SPG	Protection Stage enabling the BF - 67S2 (Set B)		R
PeB67S3	SPG	Protection Stage enabling the BF - 67S3 (Set B)		R
PeB67S4	SPG	Protection Stage enabling the BF - 67S4 (Set B)		R
PeBN67S1	SPG	Protection Stage enabling the BF - N67S1 (Set B)		R
PeBN67S2a	SPG	Protection Stage enabling the BF - N672a (Set B)		R
PeBN67S2b	SPG	Protection Stage enabling the BF - N672b (Set B)		R
PeBN67S3	SPG	Protection Stage enabling the BF - N673 (Set B)		R
PeBN67b	SPG	Protection Stage enabling the BF - N67b (Set B)		R

NOTES:

Common Logical Node Information→ Mod: for handling the Enabling/Disabling command (1/5) of this function

Common Logical Node Information→ OpCntRs: to count and store the number of operations of this function

Status Information→ Str: for issuing the Start signal of the 50BF

Status Information→ OpIn: for issuing the Tripping signal of the 50BF

Settings→ TPTrTms: for setting the operate delay time of the stage T50BF (0.06..10; 0.01 sec; 1s)

Settings→ ValAPEna: for Enabling/Disabling the BF function activation due to the Phase Current Threshold:

a. 0 = Phase Current Threshold Disabled

b. 1 = Phase Current Threshold Enabled (Default)

Settings→ StrValAP: for setting the Phase Current Threshold of this stage (0.05..1; 0.01; 0.1 p.u.)

Settings→ ValAREna: for Enabling/Disabling the BF function activation due to the Residual Current Threshold:

c. 0 = Residual Current Threshold Disabled

d. 1 = Residual Current Threshold Enabled (Default)

Settings→ StrValAR: for setting the Residual Current Threshold of this stage (0.01..2; 0.01; 0.1 p.u.)

Settings→ StrCBSig: for setting the BF function activation based on Signals from the Circuit Breaker:

e. 0 = CB Signals Triggering Disabled

f. 1 = CB Signals Triggering Enabled (Default)

Settings→ PeA46S1: for Enabling/Disabling the BF function activation due to the Operations of the Protection Stage 46.S1 (Set A):

g. 0 = 46.S1 (Set A) Op Triggering Disabled (Default)

h. 1 = 46.S1 (Set A) Op Triggering Enabled

Settings→ PeAN67b: for Enabling/Disabling the BF function activation due to the Operations of the Protection Stage 67N.Sb (Set A):

i. 0 = 67N.Sb (Set A) Op Triggering Disabled (Default)

j. 1 = 67N.Sb (Set A) Op Triggering Enabled

Settings→ PeB46S1: for Enabling/Disabling the BF function activation due to the Operations of the Protection Stage 46.S1 (Set B):

k. 0 = 46.S1 (Set B) Op Triggering Disabled (Default)

l. 1 = 46.S1 (Set B) Op Triggering Enabled

Settings→ PeBN67b: for Enabling/Disabling the BF function activation due to the Operations of the Protection Stage 67N.Sb (Set B):

m. 0 = 67N.Sb (Set B) Op Triggering Disabled (Default)

n. 1 = 67N.Sb (Set B) Op Triggering Enabled.

7.2.22 Broken Conductor Protection Function (I2/I1)

This function consists of a single stage.

Table 91 – LNInstance: 1 - prefix: BC GAPC10 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
Loc	SPS	Local operation		O
OpCntRs	INC	Resetable operation counter		R
Controls				
SPCSO	SPC	Single point controllable status output		O
DPCSO	DPC	Double point controllable status output		O
ISCSO	INC	Integer status controllable status output		O
Status Information				
Auto	SPS	Automatic operation		O
Str	ACD	Start		M
Op	ACT	Operate	T	M
Settings				
StrVal1	ASG	Start Value (1)		R
StrVal2	ASG	Start Value (2)		R

NOTES:

Common Logical Node Information→ Mod: for handling the Enabling/Disabling command (1/5) of this protection stage

Common Logical Node Information→ OpCntRs: to count and store the number of operations of this stage

Status Information→ Str: for issuing the Start signal of this stage (mandatory)

Status Information→ Op: for issuing the Tripping signal of this stage (mandatory)

Settings → StrVal1: for setting the (I1/I2) threshold value of the BC function (0.1..1,0.01,0.5 p.u.)

Settings → StrVal2: for setting the operate delay time of the BC function (0.04..15000,0.01,1 sec).

7.2.23 Summarizer (per stage) of the Str and Op for 51+67 and 46N protections

This LN models the conditioning of the trip of 51, 67 and 46N stages with the following rules:

a. The Strn (n = 1..4) is the sum of 51.Sn and 67.Sn Starts without directional information (base and accelerated)

b. The Opn (n = 1..4) is the combination of:
- Op 51.S_n
- AOp 51.S_n
- Op 67.S_n
- AOp 67.S_n

c. The Str5 and Op5 combines the Start and Operation of the 46N.S1 (base and accelerated) with the ENEL specific (87A+87B) digital signal status, without directional information.

d. The Op (i=6..10) is the combination, for each 67N.Sx (X = 1,2a,2b,3,b), of:
- Op 67N.Sx
- AOp 67N.Sx

e. The Op_k (k=11,12) is the combination, for each 46.Sy (y=1,4), of:
- Op 67N.Sx
- AOp 67N.Sx

Table 92 – LNInstance: 1 - prefix: OCSxS – GAPC11 type

Attribute Name	Attribute Type	Explanation	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
Loc	SPS	Local operation		O
OpCntRs	INC	Resetable operation counter		R
Controls				
SPCSO	SPC	Single point controllable status output		O
DPCSO	DPC	Double point controllable status output		O
ISCSO	INC	Integer status controllable status output		O
Status Information				
Auto	SPS	Automatic operation		O
Str1	ACD	Start (1)		M
Op1	ACT	Operate (1)	T	M
Str2	ACD	Start (2)		R
Op2	ACT	Operate (2)	T	R
Str3	ACD	Start (3)		R
Op3	ACT	Operate (3)	T	R
Str4	ACD	Start (4)		R
Op4	ACT	Operate (4)	T	R
Str5	ACD	Start (5)		R
Op5	ACT	Operate (5)	T	R
Op6	ACT	Operate (6)	T	R

Op7	ACT	Operate (7)	T	R
Op8	ACT	Operate (8)	T	R
Op9	ACT	Operate (9)	T	R
Op10	ACT	Operate (10)	T	R
Op11	ACT	Operate (11)	T	R
Op12	ACT	Operate (12)	T	R
Settings				
StrVal	ASG	Start Value		O

NOTES:

Common Logical Node Information→ OpCntRs: to count and store the number of events occurred

Status Information→ Str1: for issuing the sum of 51.S1 and 67.S1 Starts without directional information (base and accelerated)

Status Information→ Op1: for issuing the Operate combination of 51.S1 and 67.S1 Op (base and accelerated)

Status Information→ Str2: for issuing the sum of 51.S2 and 67.S2 Starts without directional information (base and accelerated)

Status Information→ Op2: for issuing the Operate combination of 51.S2 and 67.S2 Op (base and accelerated)

Status Information→ Str3: for issuing the sum of 51.S3 and 67.S3 Starts without directional information (base and accelerated)

Status Information→ Op3: for issuing the Operate combination of 51.S3 and 67.S3 Op (base and accelerated)

Status Information→ Str4: for issuing the sum of 51.S4 and 67.S4 Starts without directional information (base and accelerated)

Status Information→ Op4: for issuing the Operate combination of 51.S4 and 67.S4 Op (base and accelerated)

Status Information→ Str5: for issuing the combination of 46N Start and (87A+87B) digital signal status without directional information (base and accelerated)

Status Information→ Op5: for issuing the Operate combination of 46N Op and (87A+87B) digital signal status (base and accelerated).

Status Information→ Op6: for issuing the Operate combination of 67N.S1 Op (base and accelerated).

Status Information→ Op7: for issuing the Operate combination of 67N.S2a Op (base and accelerated).

Status Information→ Op8: for issuing the Operate combination of 67N.S2b Op (base and accelerated).

Status Information→ Op9: for issuing the Operate combination of 67N.S3 Op (base and accelerated).

Status Information→ Op10: for issuing the Operate combination of 67N.Sb Op (base and accelerated).

Status Information→ Op11: for issuing the Operate combination of 46N.S1 Op (base and accelerated).

Status Information→ Op12: for issuing the Operate combination of 45N.S4 Op (base and accelerated).

7.2.24 Summarizer of the MFP protections operations affecting the Circuit Breaker status

This LN is used to connect the “operate” outputs of one or more protections stages to a common “operate” that will trip the MV Circuit Breaker.

Table 93 – LNInstance: 1- prefix: P_Sum – PTRC2 type

Attribute Name	Attribute Type	Explanation	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
OpCntRs	INC	Resetable operation counter		R
Status Information				
Tr	ACT	Trip		(C) O
Op	ACT	Operate (combination of subscribed Op from protection functions)		(C) R
Str	ACD	Sum of all starts of all connected Logical Nodes		R
Settings				
TrMod	ING	Trip Mode		O
TrPlsTmms	ING	Trip Pulse Time		O

Condition C: At least one of the two status information (Tr, Op) shall be used.

NOTES:

Common Logical Node Information→ OpCntRs: to count and store the number of operations of the MFP protections due to a fault detection

Status Information→ Op: for notifying the trip to the Circuit Breaker triggered by one or more protection stages

Status Information→ Str: for notifying the start triggered by one or more protection stages

7.3 Logical Device Recloser: details of the LN

The LD Recloser (LD_Rec) includes all the Logical Nodes which data is used in the communication supporting the Automatic Reclosing function. This function, enabled for specific installations of the IED in the substation (ref. GSTP101), performs the reclosing procedure of the MV Circuit Breaker after it has been opened due to a fault.

The behaviour of this function (reclosing sequences) depends on the type of Protection that operated (ref. GSTP101). Therefore, tailored settings per single protection stage shall be modelled.

Table 94 – LLN01 type

Attribute Name	Attribute Type	Explanation	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
Loc	SPS	Local operation for complete logical device		O
OpTmh	INS	Operation Time		O
Controls				
Diag	SPC	Run Diagnostic		O
LEDRs	SPC	LED reset	T	O

Table 95 – LNInstance: 1 – LPHD2 type

Attribute Name	Attribute Type	Explanation	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				

PhyNam	DPL	Physical device name plate		M
PhyHealth	INS	Physical device health		M
OutOv	SPS	Output communications buffer overflow		O
Proxy	SPS	Indicates if this LN is a proxy		M
InOv	SPS	Input communications buffer overflow		O
NumPwrUp	INS	Number of Power ups		O
WrmStr	INS	Number of Warm Starts		O
WacTrg	INS	Number of watchdog device resets detected		O
PwrUp	SPS	Power Up detected		O
PwrDn	SPS	Power Down detected		O
PwrSupAlm	SPS	External power supply alarm		O
RsStat	SPC	Reset device statistics	T	O

7.3.1 Auto-Reclosing function management

The following LN is dedicated to the recloser notifications and settings, including the enabling/disabling.

Table 96 – LNInstance: 1 - prefix: R79Mng – RREC1 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
OpCntRs	INC	Resetable operation counter		R
Controls				
BlkRec	SPC	Block Reclosing		R
ChkRec	SPC	Check Reclosing		O
Status Information				
Auto	SPS	Automatic Operation (external switch status)		R
Op	ACT	Operate (used here to provide close to XCBR)	T	M
AutoRecSt	INS	Auto Reclosing Status		M
Settings				
Rec1Tmms	ING	First Reclose Time		O
Rec2Tmms	ING	Second Reclose Time		O
Rec3Tmms	ING	Third Reclose Time		O
PlsTmms	ING	Close Pulse Time		O
RclTmms	ING	Reclaim Time		O

NOTES:

Common Logical Node Information→ Mod: for handling the Enabling/Disabling command (1/5) of the automatic reclosing function (default: Disabled)

Common Logical Node Information→ OpCntRs: to count and store the number of events occurred

Controls → BlkRec: for the remote setting of the reclosing function block (volatile info, not retained in long-term memory storage in the absence of power supply):

a. 0 = Recloser unblocked (R)

b. 1 = Recloser blocked (E)

Status Information → Auto: for notifying the state of the automatic reclosing function. It is the logic AND among an external command (as per IEC 61850) from the RTU, the position of the dedicated selector on the front panel of the IED and the settings via configuration SW:

c. 0 = De-activated

d. 1 = Active

Status Information → Op: for notifying the 79**X** signal, that means that closing command has been issued to the Circuit Breaker

Status Information → AutoRecSt: for notifying 79**X_CRC** signal, that means that the reclosing sequence is in progress (=2).

The following LN represents the AutoRecSt values of the RREC through the status of four Boolean Dos (For legacy communication with the ENEL RTU).

Table 97 –LNInstance: 1 - prefix: CRCNtf – GGIO9 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
EEHealth	INS	External equipment health (external sensor)		O
EEName	DPL	External equipment name plate		O
Loc	SPS	Local operation		O
OpCntRs	INC	Resetable operation counter		R
Measured values				
AnIn	MV	Analogue input		O
Controls				
SPCSO	SPC	Single point controllable status output		O
DPCSO	DPC	Double point controllable status output		O
ISCSO	INC	Integer status controllable status output		O
Status Information				
IntIn	INS	Integer status input		O
Alm	SPS	General single alarm		O
Ind1	SPS	General indication (binary input) (1)		R
Ind2	SPS	General indication (binary input) (2)		R
Ind3	SPS	General indication (binary input) (3)		R
Ind4	SPS	General indication (binary input) (4)		R

NOTES:

Common Logical Node Information→ OpCntRs: to count and store the number of events occurred

Status Information → Ind1: for notifying the recloser **Ready** status (1 means AutoRecSt=1)

Status Information → Ind2: for notifying the recloser **In Progress** status (1 means AutoRecSt=2)

Status Information → Ind3: for notifying the recloser **Successful** status (1 means AutoRecSt=3)

Status Information → Ind4: for notifying the recloser **Unsuccessful** status (1 means AutoRecSt=4).

7.3.2 Additional automatic reclosing function settings

The following LN includes typical settings of the automatic reclosing function in the MFP, in particular its operation according to the type of protection that opened the Circuit Breaker.

Table 98 – LNInstance: 1 - prefix: R79TsP – GGIO10 type

Attribute Name	Attribute Type	Explanation	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
EEHealth	INS	External equipment health (external sensor)		O
EEName	DPL	External equipment name plate		O
Loc	SPS	Local operation		O
OpCntRs	INC	Resetable operation counter		R
Measured values				
AnIn	MV	Analogue input		O
Controls				
SPCSO1	SPC	Single point controllable status output (1)		R
SPCSO2	SPC	Single point controllable status output (2)		R
SPCSO3	SPC	Single point controllable status output (3)		R
SPCSO4	SPC	Single point controllable status output (4)		R
SPCSO5	SPC	Single point controllable status output (5)		R
SPCSO6	SPC	Single point controllable status output (6)		R
SPCSO7	SPC	Single point controllable status output (7)		R
SPCSO8	SPC	Single point controllable status output (8)		R
SPCSO9	SPC	Single point controllable status output (9)		R
SPCSO10	SPC	Single point controllable status output (10)		R
SPCSO11	SPC	Single point controllable status output (11)		R
SPCSO12	SPC	Single point controllable status output (12)		R
SPCSO13	SPC	Single point controllable status output (13)		R
SPCSO14	SPC	Single point controllable status output (14)		R
SPCSO15	SPC	Single point controllable status output (15)		R
SPCSO16	SPC	Single point controllable status output (16)		R
SPCSO17	SPC	Single point controllable status output (17)		R
SPCSO18	SPC	Single point controllable status output (18)		R
SPCSO19	SPC	Single point controllable status output (19)		R
SPCSO20	SPC	Single point controllable status output (20)		R
SPCSO21	SPC	Single point controllable status output (21)		R
DPCSO	DPC	Double point controllable status output		O
ISCSO1	INC	Integer status controllable status output (1)		R
ISCSO2	INC	Integer status controllable status output (2)		R
ISCSO3	INC	Integer status controllable status output (3)		R
ISCSO4	INC	Integer status controllable status output (4)		R

ISCSO5	INC	Integer status controllable status output (5)		R
ISCSO6	INC	Integer status controllable status output (6)		R
ISCSO7	INC	Integer status controllable status output (7)		R
ISCSO8	INC	Integer status controllable status output (8)		R
ISCSO9	INC	Integer status controllable status output (9)		R
ISCSO10	INC	Integer status controllable status output (10)		R
Status Information				
IntIn	INS	Integer status input		O
Alm	SPS	General single alarm		O
Ind	SPS	General indication (binary input)		O

NOTES:

Common Logical Node Information→ OpCntRs: to count and store the number of events occurred (configurations)

Controls → SPCSO1: for selecting the reclosing sequence:

a. 0 = RR

b. 1 = RR + RL (Default)

Controls → SPCSO2: for setting the acceleration of the Protection stages (if with dual time calibration) in case of disabled 79 (1 = acceleration)

Controls → SPCSO3: for setting the Enabling/Disabling of the TD in case of manual closing:

c. 0 = Disabled

d. 1 = Enabled

Controls → SPCSO4: for setting the Enabling/Disabling of the 79 in case of 51.S1 operation:

e. 0 = Disabled

f. 1 = Enabled (Default)

Controls → SPCSO5: for setting the Enabling/Disabling of the 79 in case of 51.S2 operation:

g. 0 = Disabled

h. 1 = Enabled (Default)

Controls → SPCSO6: for setting the Enabling/Disabling of the 79 in case of 51.S3 operation:

i. 0 = Disabled

j. 1 = Enabled (Default)

Controls → SPCSO7: for setting the Enabling/Disabling of the 79 in case of 51.S4 operation

k. 0 = Disabled (Default)

l. 1 = Enabled

Controls → SPCSO8: for setting the Enabling/Disabling of the 79 in case of 67.S1 operation:

m. 0 = Disabled (Default)

n. 1 = Enabled

Controls → SPCSO9: for setting the Enabling/Disabling of the 79 in case of 67.S2 operation

o. 0 = Disabled (Default)

p. 1 = Enabled

Controls → SPCSO10: for setting the Enabling/Disabling of the 79 in case of 67.S3 operation:

q. 0 = Disabled (Default)

r. 1 = Enabled

Controls → SPCSO11: for setting the Enabling/Disabling of the 79 in case of 67.S4 operation:

s. 0 = Disabled (Default)

t. 1 = Enabled

Controls → SPCSO12: for setting the Enabling/Disabling of the 79 in case of 51N.S1 operation:

u. 0 = Disabled (Default)

v. 1 = Enabled

Controls → SPCSO13: for setting the Enabling/Disabling of the 79 in case of 51N.S2 operation:

w. 0 = Disabled (Default)

x. 1 = Enabled

Controls → SPCSO14: for setting the Enabling/Disabling of the 79 in case of 51N.S3 operation:

y. 0 = Disabled (Default)

z. 1 = Enabled

Controls → SPCSO15: for setting the Enabling/Disabling of the 79 in case of 51N.SE operation:

a. 0 = Disabled (Default)

b. 1 = Enabled

Controls → SPCSO16: for setting the Enabling/Disabling of the 79 in case of 67N.S1 operation:

c. 0 = Disabled

d. 1 = Enabled (Default)

Controls → SPCSO17: for setting the Enabling/Disabling of the 79 in case of 67N.S2a operation:

e. 0 = Disabled

f. 1 = Enabled (Default)

Controls → SPCSO18: for setting the Enabling/Disabling of the 79 in case of 67N.S2b operation:

g. 0 = Disabled

h. 1 = Enabled (Default)

Controls → SPCSO19: for setting the Enabling/Disabling of the 79 in case of 67N.S3 operation:

i. 0 = Disabled

j. 1 = Enabled (Default)

Controls → SPCSO20: for setting the Enabling/Disabling of the 79 in case of 67N.S4 operation:

k. 0 = Disabled

l. 1 = Enabled (Default)

Controls → SPCSO21: for setting the Enabling/Disabling of the 79 in case of 67N.S5 operation:

m. 0 = Disabled

n. 1 = Enabled (Default)

Controls → ISCSO1: for setting the RM - number of “Memorized Closings” (0..5; min 0, max 5 , step 1 default 3)

Controls → ISCSO2: for setting the TRR - interruption/isolation Time of the RR (100..1000ms; 10ms; default 600ms)

Controls → ISCSO3: for setting the TRL - interruption/isolation Time of the RL (1..200s; 1s; default 30s)

Controls → ISCSO4: for setting the TNf - Neutralization Timer in case of phase fault trip (1..200s; 1s; default 70s)

Controls → ISCSO5: for setting the TNt - Neutralization Timer in case of earth fault trip (1..200s; 1s; default 70s)

Controls → ISCSO6: for setting the TDrr - Discrimination Timer for the RR (0..10s; 1s; default 5s)

Controls → ISCSO7: for setting the TDrl - Discrimination Timer for the RL (0..10s; 1s; 5s)

Controls → ISCSO8: for setting the TDrm - Discrimination Timer for the RM (0..10s; 1s; 5s)

Controls → ISCSO9: for setting the TDi - Discrimination Timer for the manual closing (1..10s; 1s; 5s)

Controls → ISCSO10: for setting the TMrp - Max. reset time of the protections (0.. 10min; 50ms; 0.5s).

7.3.3 Failed Reclosing alarm (FR)

Table 99 – LNInstance: 1 - prefix: R79FR – a CALH1 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
Status Information				
GrAlm	SPS	Group alarm		M
GrWrn	SPS	Group warning		O
AllmLstOv	SPS	Alarm list overflow		O

NOTES:

Status Information→ GrAlm: for notifying the FR - Failed Reclosing alarm.

7.4 Logical Device Medium voltage Feeder Automations: details of the LN

If the MFP is used as an MT Feeder Control and Protection IED (ref. GSTP101), the LNs of the Logical Device MV Feeder Automations (LD_MFA) are used to communicate with the RGDM ST installed in the MT feeder managed by the MFP in order to support the Logical Selectivity (based on the BLIND messages) and Remote Disconnection functions.

Table 100 – LLN01 type				
Attribute Name	**Attribute Type**	**Explanation**	**T**	**M/O**
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
Loc	SPS	Local operation for complete logical device		O
OpTmh	INS	Operation Time		O
Controls				
Diag	SPC	Run Diagnostic		O
LEDRs	SPC	LED reset	T	O

Table 101 –LNInstance: 1 – LPHD2 type				
Attribute Name	**Attribute Type**	**Explanation**	**T**	**M/O**
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
PhyNam	DPL	Physical device name plate		M
PhyHealth	INS	Physical device health		M
OutOv	SPS	Output communications buffer overflow		O
Proxy	SPS	Indicates if this LN is a proxy		M
InOv	SPS	Input communications buffer overflow		O
NumPwrUp	INS	Number of Power ups		O

WrmStr	INS	Number of Warm Starts		O
WacTrg	INS	Number of watchdog device resets detected		O
PwrUp	SPS	Power Up detected		O
PwrDn	SPS	Power Down detected		O
PwrSupAlm	SPS	External power supply alarm		O
RsStat	SPC	Reset device statistics	T	O

7.4.1 MFP Topological Address (TAG)

The following LN models the TAG (topological address, consisting of twelve integers) of the MFP, used to identify the role (predecessor/successor) of the IEDs that participate in the Logic Selectivity (FSL) and Remote Disconnection (TDLP) by comparing own TAG with those received from the other IEDs in the same MV feeder.

Only the stVal of the $Taddr_n$ is sent to optimize the message size and the resulting network traffic.

Table 102 – LNInstance: 1 - prefix: TAG – AETA1 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
EEHealth	INS	External equipment health (external sensor)		O
EEName	DPL	External equipment name plate		O
Loc	SPS	Local operation		O
OpCntRs	INC	Resetable operation counter		R
Controls				
AdrLevBN	INC	Address Level - Bit Number of the TAG		R
TAddr1	INC	Topological Address (1)		R
TAddr2	INC	Topological Address (2)		R
TAddr3	INC	Topological Address (3)		R
TAddr4	INC	Topological Address (4)		R
TAddr5	INC	Topological Address (5)		R
TAddr6	INC	Topological Address (6)		R
TAddr7	INC	Topological Address (7)		R
TAddr8	INC	Topological Address (8)		R
TAddr9	INC	Topological Address (9)		R
TAddr10	INC	Topological Address (10)		R
TAddr11	INC	Topological Address (11)		R
TAddr12	INC	Topological Address (12)		R
AdrLevBN	INC	Address Level - Bit Number of the TAG		R

NOTES:

Common Logical Node Information→ OpCntRs: to count and store the number of configurations

Controls → AdrLevBN: for setting the length (number of bits) of each addressing level of the TAG_n DO, contained in the BLIND and / or Remote Disconnection signal

Controls → TAddr1: for setting the IED's **TAG_1** (used/meaningful if >0)

Controls → TAddr2: for setting the IED's **TAG_2** (used/meaningful if >0)

Controls → TAddr3: for setting the IED's **TAG_3** (used/meaningful if >0)

Controls → TAddr4: for setting the IED's **TAG_4** (used/meaningful if >0)

Controls → TAddr5: for setting the IED's **TAG_5** (used/meaningful if >0)

Controls → TAddr6: for setting the IED's **TAG_6** (used/meaningful if >0)

Controls → TAddr7: for setting the IED's **TAG_7** (used/meaningful if >0)

Controls → TAddr8: for setting the IED's **TAG_8** (used/meaningful if >0)

Controls → TAddr9: for setting the IED's **TAG_9** (used/meaningful if >0)

Controls → TAdrr10: for setting the IED's **TAG_10** (used/meaningful if >0)

Controls → TAddr11: for setting the IED's **TAG_11** (used/meaningful if >0)

Controls → TAddr12: for setting the IED's **TAG_12** (used/meaningful if >0).

7.4.2 Logic Selectivity Function (FSL)

The Data Model and communication for the FSL (used to select and isolate the Faulty MT line trunk) is divided into two parts:

a. Configuration/management of characteristic data (timers, GOOSE payload type, function reset, etc.),

b. Monitoring of the BLIND from downstream RGDM ST IEDs.

7.4.2.1. Configuration of characteristic data

Table 103 – LNInstance: 1 - prefix: STGMng – GGIO11 type

Attribute Name	Attribute Type	Explanation	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
EEHealth	INS	External equipment health (external sensor)		O
EEName	DPL	External equipment name plate		O
Loc	SPS	Local operation		O
OpCntRs	INC	Resetable operation counter		R
Measured values				
AnIn	MV	Analogue input		O
Controls				
SPCSO	SPC	Single point controllable status output		O
DPCSO	DPC	Double point controllable status output		O
ISCSO1	INC	Integer status controllable status output (1)		R
ISCSO2	INC	Integer status controllable status output (2)		R
Status Information				
IntIn	INS	Integer status input		O

Alm	SPS	General single alarm		O
Ind	SPS	General indication (binary input)		O

NOTES:

Common Logical Node Information→ Mod: for handling the Enabling/Disabling command (1/5) of the (FSL) Logic Selectivity function (default: Disabled)

Common Logical Node Information→ OpCntRs: to count and store the number of events occurred

Controls → ISCSO1: for setting the logic type:

a. 0 = FRT

b. 1 = FSL

c. 2 = DBR

d. 3 = SFS

e. 4 = DSR

Controls → ISCSO2: for setting the Tadd timer.

7.4.2.2. FSL – BLIND monitoring

The following LN type is instantiated thirty times (only two instances are documented for the sake of conciseness) in order to map the BLIND (GOOSE messages) coming from maximum of thirty RGDM ST electrically downstream of the MFP.

Table 104 – LNInstance: 1 - prefix: SLMon – GGIO12 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
EEHealth	INS	External equipment health (external sensor)		O
EEName	DPL	External equipment name plate		O
Loc	SPS	Local operation		O
OpCntRs	INC	Resetable operation counter		R
Measured values				
AnIn	MV	Analogue input		O
Controls				
SPCSO	SPC	Single point controllable status output		R
DPCSO	DPC	Double point controllable status output		O
ISCSO1	INC	Integer status controllable status output (1)		R
ISCSO2	INC	Integer status controllable status output (2)		R
ISCSO3	INC	Integer status controllable status output (3)		R
ISCSO4	INC	Integer status controllable status output (4)		R
ISCSO5	INC	Integer status controllable status output (5)		R
ISCSO6	INC	Integer status controllable status output (6)		R
ISCSO7	INC	Integer status controllable status output (7)		R
ISCSO8	INC	Integer status controllable status output (8)		R
ISCSO9	INC	Integer status controllable status output (9)		R

ISCSO10	INC	Integer status controllable status output (10)		R
ISCSO11	INC	Integer status controllable status output (11)		R
ISCSO12	INC	Integer status controllable status output (12)		R
Status Information				
IntIn	INS	Integer status input		O
Alm	SPS	General single alarm		O
Ind	SPS	General indication (binary input)		O

LNInstance: 2..29 - prefix: SLMon

Table 105 – LNInstance: 30 - prefix: SLMon – GGIO12 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
EEHealth	INS	External equipment health (external sensor)		O
EEName	DPL	External equipment name plate		O
Loc	SPS	Local operation		O
OpCntRs	INC	Resetable operation counter		R
Measured values				
AnIn	MV	Analogue input		O
Controls				
SPCSO	SPC	Single point controllable status output		R
DPCSO	DPC	Double point controllable status output		O
ISCSO1	INC	Integer status controllable status output (1)		R
ISCSO2	INC	Integer status controllable status output (2)		R
ISCSO3	INC	Integer status controllable status output (3)		R
ISCSO4	INC	Integer status controllable status output (4)		R
ISCSO5	INC	Integer status controllable status output (5)		R
ISCSO6	INC	Integer status controllable status output (6)		R
ISCSO7	INC	Integer status controllable status output (7)		R
ISCSO8	INC	Integer status controllable status output (8)		R
ISCSO9	INC	Integer status controllable status output (9)		R
ISCSO10	INC	Integer status controllable status output (10)		R
ISCSO11	INC	Integer status controllable status output (11)		R
ISCSO12	INC	Integer status controllable status output (12)		R
Status Information				
IntIn	INS	Integer status input		O
Alm	SPS	General single alarm		O
Ind	SPS	General indication (binary input)		O

NOTES:

Common Logical Node Information→ OpCntRs: to count and store the number of events occurred

Controls → SPCSO: for mapping the BLIND signal from the downstream RGDM ST

a. 0 = no BLIND (no blocking to the internal protections operation)

b. 1 = BLIND (internal protections operation blocked)

Controls → ISCSO1: for mapping the TAG_1 of the electrically downstream RGDM ST (used/meaningful if >0)

Controls → ISCSO2: for mapping the TAG_2 of the electrically downstream RGDM ST (used/meaningful if >0)

Controls → ISCSO3: for mapping the TAG_3 of the electrically downstream RGDM ST (used/meaningful if >0)

Controls → ISCSO4: for mapping the TAG_4 of the electrically downstream RGDM ST (used/meaningful if >0)

Controls → ISCSO5: for mapping the TAG_5 of the electrically downstream RGDM ST (used/meaningful if >0)

Controls → ISCSO6: for mapping the TAG_6 of the electrically downstream RGDM ST (used/meaningful if >0)

Controls → ISCSO7: for mapping the TAG_7 of the electrically downstream RGDM ST (used/meaningful if >0)

Controls → ISCSO8: for mapping the TAG_8 of the electrically downstream RGDM ST (used/meaningful if >0)

Controls → ISCSO9: for mapping the TAG_9 of the electrically downstream RGDM ST (used/meaningful if >0)

Controls→ISCSO10: for mapping the TAG_10 of the electrically downstream RGDM ST (used/meaningful if >0)

Controls→ISCSO11: for mapping the TAG_11 of the electrically downstream RGDM ST (used/meaningful if >0)

Controls→ISCSO12: for mapping the TAG_12 of the electrically downstream RGDM ST (used/meaningful if >0).

This LN is ready to receive via GOOSE the “BLIND command” with the TAG_n (only the stVal to optimize the message size and the resulting network traffic) issued by one or more electrically downstream RGDM ST and used to avoid that the MFP trips the controlled Circuit Breaker in case of a fault that has to be isolated in a different trunk of the feeder.

7.4.3 Remote Disconnection Function (TDLP)

The MFP implements two different remote Disconnection modes:

a. when one (or more) protection inside the MFP trips the controlled Circuit Breaker at the head of the MV feeder, the IED publishes the “Remote Disconnection” GOOSE, including its own TAG, to all the downstream RGDM ST. As a consequence, each downstream RGDM ST publishes the “Open PI” GOOSE towards its actuator;

b. the RTU (GSTR1XX series, TPT2020), via MMS, controls the Remote Disconnection trigger in the MFP that propagates it via GOOSE towards all the downstream RGDM ST.

7.4.3.1. Remote Disconnection management

Table 106 –LNInstance: 1 - prefix: TDMng – GGIO13 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
EEHealth	INS	External equipment health (external sensor)		O
EEName	DPL	External equipment name plate		O
Loc	SPS	Local operation		O
OpCntRs	INC	Resetable operation counter		R
Measured values				
AnIn	MV	Analogue input		O
Controls				
SPCSO	SPC	Single point controllable status output		R
DPCSO	DPC	Double point controllable status output		O
ISCSO	INC	Integer status controllable status output		O
Status Information				
IntIn	INS	Integer status input		O
Alm	SPS	General single alarm		O
Ind	SPS	General indication (binary input)		O

NOTES:

Common Logical Node Information→ Mod: for handling the Enabling/Disabling command (1/5) of the (TDLP) Remote Disconnection function (default: Disabled)

Common Logical Node Information→ OpCntRs: to count and store the number of events occurred

Controls→ SPCSO: for issuing the Remote Disconnection command (internally triggered or requested by the RTU) TDLP to the downstream RGDM ST:

a. 0 = No TDLP

b. 1 = TDLP.

The MFP is ready to issue via GOOSE the TDLP command to the downstream RGDM ST including its own TAG_n

c. MFP/LD_MFA/GGIO13/TDMngGGIO1/SPCSO.

7.5 Logical Device Remote Input/Output: details of the Logical Nodes

The Logical Device Remote Input/Output (LD_RIO) includes all the Logical Nodes which data is used in the communication with the Remote Input/Output modules (RIO, that expand the connection to the field devices) and with the RTU for the dedicated reporting.

Table 107 – LLN01 type				
Attribute Name	**Attribute Type**	**Explanation**	**T**	**M/O**
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		

Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
Loc	SPS	Local operation for complete logical device		O
OpTmh	INS	Operation Time		O
Controls				
Diag	SPC	Run Diagnostic		O
LEDRs	SPC	LED reset	T	O

Table 108 – LLN01 type LNInstance: 1 – LPHD2 type				
Attribute Name	**Attribute Type**	**Explanation**	**T**	**M/O**
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
PhyNam	DPL	Physical device name plate		M
PhyHealth	INS	Physical device health		M
OutOv	SPS	Output communications buffer overflow		O
Proxy	SPS	Indicates if this LN is a proxy		M
InOv	SPS	Input communications buffer overflow		O
NumPwrUp	INS	Number of Power ups		O
WrmStr	INS	Number of Warm Starts		O
WacTrg	INS	Number of watchdog device resets detected		O
PwrUp	SPS	Power Up detected		O
PwrDn	SPS	Power Down detected		O
PwrSupAlm	SPS	External power supply alarm		O
RsStat	SPC	Reset device statistics	T	O

7.5.1 Configuration of the interface to the RIO Modules and state of the communication RIO-MFP (Default configuration only for the MODBUS communication between the MFP and the RIOs)

This LN allows to:

a. Enable the Remote Input/Output modules connected to the MFP and configure the communication protocol between these IEDs;

b. There are two types of Input/Output Remote modules (RIO):
- ***52 MT*** (following defined **RIO N°1** or **RIO1**),
- ***BM*** (following defined **RIO N°2** or **RIO2**);

c. According to GSTP101, max. two RIO can be connected to a MFP and in this case they shall be of different type
- one ***52 MT,***
- one ***BM;***

d. (ready to) monitor the state of the communication between the RIO(s) and the MFP.

Table 109 – LNInstance: 1 - prefix: RIOMng – GGIO14 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				

Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
EEHealth	INS	External equipment health (external sensor)		O
EEName	DPL	External equipment name plate		O
Loc	SPS	Local operation		O
OpCntRs	INC	Resetable operation counter		R
Measured values				
AnIn	MV	Analogue input		O
Controls				
SPCSO1	SPC	Single point controllable status output (1)		R
SPCSO2	SPC	Single point controllable status output (2)		R
SPCSO3	SPC	Single point controllable status output (3)		R
SPCSO4	SPC	Single point controllable status output (4)		R
DPCSO	DPC	Double point controllable status output		O
ISCSO	INC	Integer status controllable status output		O
Status Information				
IntIn1	INS	Integer status input (1)		R
IntIn2	INS	Integer status input (2)		R
Alm	SPS	General single alarm		O
Ind	SPS	General indication (binary input)		O

NOTES:

Common Logical Node Information→ OpCntRs: to count and store the number of events occurred

Controls→ SPCSO1: for Enabling/Disabling the RIO1:

a. 0 = Off

b. 1 = On

Controls→ SPCSO2: for selecting the protocol type for the communication with the RIO1

c. 0 = ModBus

d. 1 = IEC 61850

Controls→ SPCSO3: for Enabling/Disabling the RIO2:

e. 0 = Off

f. 1 = On

Controls→ SPCSO4: for selecting the protocol type for the communication with the RIO2

g. 0 = ModBus

h. 1 = IEC 61850

Status Information→ IntIn1: (ready) for mapping the **KA-RIO1** (via GOOSE) used to check, at Application Layer, the availability of the link between the MFP and the RIO1: a cyclic counter that the RIO1 periodically increments and issues

Status Information→ IntIn2: (ready) for mapping the **KA-RIO2** (via GOOSE) used to check, at Application Layer, the availability of the link between the MFP and the RIO1: a cyclic counter that the RIO2 periodically increments and issues.

This LN is ready to receive via GOOSE the "**KA-RIO1**" and "**KA-RIO2**" used to monitor the availability of the links between MFP and the RIO1 and RIO2.

7.5.2 Input/Output Remote module N°1 – 52 MT (in case of MODBUS communication profile)

7.5.2.1. Data exchange with the RIO n°1 (subscriptions and commands) and with the RTU (reports)

The following LN models:

a. the information that the MFP receives from the RIO N°1 (52 MT type) via GOOSE messages and the related reporting that the MFP issues to the RTU via MMS;

b. the commands that the MFP issues to the RIO N°1 (52 MT type) via GOOSE messages.

Table 110 – LNInstance: 1 - prefix: RIO1 – GGIO15 type

Attribute Name	Attribute Type	Explanation	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
EEHealth	INS	External equipment health (external sensor)		O
EEName	DPL	External equipment name plate		O
Loc	SPS	Local operation		O
OpCntRs	INC	Resetable operation counter		R
Measured values				
AnIn	MV	Analogue input		O
Controls				
SPCSO1	SPC	Single point controllable status output (1)		R
SPCSO2	SPC	Single point controllable status output (2)		R
SPCSO3	SPC	Single point controllable status output (3)		R
SPCSO4	SPC	Single point controllable status output (4)		R
SPCSO5	SPC	Single point controllable status output (5)		R
SPCSO6	SPC	Single point controllable status output (6)		R
SPCSO7	SPC	Single point controllable status output (7)		R
SPCSO8	SPC	Single point controllable status output (8)		R
SPCSO9	SPC	Single point controllable status output (9)		R
SPCSO10	SPC	Single point controllable status output (10)		R
SPCSO11	SPC	Single point controllable status output (11)		R
SPCSO12	SPC	Single point controllable status output (12)		R
SPCSO13	SPC	Single point controllable status output (13)		R
SPCSO14	SPC	Single point controllable status output (14)		R
DPCSO	DPC	Double point controllable status output		O
ISCSO	INC	Integer status controllable status output		O
Status Information				
IntIn	INS	Integer status input		O
Alm	SPS	General single alarm		O
Ind1	SPS	General indication (binary input) (1)		R
Ind2	SPS	General indication (binary input) (2)		R

Ind3	SPS	General indication (binary input) (3)		R
Ind4	SPS	General indication (binary input) (4)		R

NOTES:

Common Logical Node Information→ OpCntRs: to count and store the number of events occurred

Controls→ SPCSO1: for mapping the info Closed Earthing Switch (89TccX) issued by the RIO1 and internally correlated to the MFP/LD_RIO/XSWI1/R1_89TXSWI1.Pos

Controls→ SPCSO2: for mapping the info Opened Earthing Switch (89TcaX) issued by the RIO1 and internally correlated to the MFP/LD_RIO/XSWI1/R1_89TXSWI1.Pos

Controls→ SPCSO3: for mapping the info 52MT Closed Circuit Breaker issued by the RIO1 and internally correlated to the MFP/LD_Gen/XCBR1/St52XCBR1.Pos

Controls→ SPCSO4: for mapping the info 52MT Opened Circuit Breaker issued by the RIO1 and internally correlated to the MFP/LD_Gen/XCBR1/St52XCBR1.Pos

Controls→ SPCSO5: for mapping the info Closing Block – Live line with opened circuit-breaker (BLP) issued by the RIO1 and internally correlated to the MFP/LD_Gen/CILO1/IB52CILO1.EnaCls

Controls→ SPCSO6: for mapping the info MT Circuit Breaker - Line Voltage Absence (27X) issued by the RIO1 and internally correlated to the LD_Gen/GGIO1/EEDiagGGIO1.Alm1

Controls→ SPCSO7: for mapping the info Spring Charging Motor - Breaker Tripping (6L) issued by the RIO1 and internally correlated to the MFP/LD_Gen/GGIO1/EEDiagGGIO1.Alm1

Controls→ SPCSO8: for mapping the info Discharged springs (X33) issued by the RIO1 and internally correlated to the MFP/LD_Gen/GGIO1/EEDiagGGIO1.Alm1

Controls→ SPCSO9: for mapping the info 63G All issued by the RIO1 and internally correlated to the MFP/LD_RIO/SIMG1/R1Gs63SIMG1.InsAlm

Controls→ SPCSO10: for mapping the info 63G Tr. issued by the RIO1 and internally correlated to the LD_RIO/SIMG1/R1Gs63SIMG1.InsTr

Controls→ SPCSO11: for mapping the info S27 issued by the RIO1 and reported to the RTU (0 = Ok, 1 = Alarm)

Controls→ SPCSO12: (ready) for mapping additional info issued by the RIO1

Controls→ SPCSO13: (ready) for mapping additional info issued by the RIO1

Controls→ SPCSO14: (ready) for mapping additional info issued by the RIO1

Status Information→ Ind1: for issuing the Command 1 (generated by internal MFP logics) to the field devices via the RIO1

Status Information→ Ind2: for issuing the Command 2 (generated by internal MFP logics) to the field devices via the RIO1.

Status Information→ Ind3: for issuing the Command 3 (generated by internal MFP logics) to the field devices via the RIO1

Status Information→ Ind4: for issuing the Command 4 (generated by internal MFP logics) to the field devices via the RIO1.

The following table shows the:

c. The functional correlation between the variables (Generic LN) used to subscribe the signals coming from the RIO1 via GOOSE messages and the variables (Specific LNs) used to forward this information to the RTU via Report messages ;

d. The meaning of their values on the two interfaces.

Table 111 – Remote I/O module N°1 – 52 MT type					
Signal	**Input GOOSE from RIO**	**Output Reporting to the RTU**	**Variable values on the two interfaces**		**Meaning of the value**
			Input	**Output**	
Closed Earthing Switch (89TccX))	LD_RIO/GGIO15/RIO1GGIO1.SPCSO1	LD_RIO/XSWI1/R1_89TXSWI1.Pos	0	1 = Off	Opened switch
			1	2 = On	Closed switch
Opened Earthing Switch (89caX)	LD_RIO/GGIO15/RIO1GGIO1.SPCSO2		0	2 = On	Closed switch
			1	1 = Off	Opened switch
52MT Closed Circuit Breaker	LD_RIO/GGIO15/RIO1GGIO1.SPCSO3	LD_Gen/XCBR1/St52XCBR1.Pos	0	1 = Off	Opened Circuit Breaker
			1	2 = On	Closed Circuit Breaker
52MT Opened Circuit Breaker	LD_RIO/GGIO15/RIO1GGIO1.SPCSO4		0	2 = On	Closed Circuit Breaker
			1	1 = Off	Opened Circuit Breaker
Closing Block – Live line with opened circuit-breaker (BLP)	LD_RIO/GGIO15/RIO1GGIO1.SPCSO5	LD_Gen/CILO1/IB52CILO1.EnaCls	0	0	Closing enabled
			1	1	Closing inhibited
MT Circuit Breaker - Line Voltage Absence (27X)	LD_RIO/GGIO15/RIO1GGIO1.SPCSO6	LD_Gen/GGIO1/EEDiagGGIO1.Alm1	0	0	Ok
			1	1	Circuit Breaker anomaly
Powe supply tripping of Motor	LD_RIO/GGIO15/RIO1GGIO1.SPCSO7	LD_Gen/GGIO1/EEDiagGGIO1.Alm1	0	0	Ok
			1	1	Circuit Breaker anomaly
Discharged springs (X33)	LD_RIO/GGIO15/RIO1GGIO1.SPCSO8	LD_Gen/GGIO1/EEDiagGGIO1.Alm1	0	0	Ok
			1	1	Circuit Breaker anomaly
SF6 Alm signal low pressure	LD_RIO/GGIO15/RIO1GGIO1.SPCSO9	LD_RIO/SIMG1/R1Gs63SIMG1.InsAlm	0	0	Ok
			1	1	Circuit Breaker SF6 Alarming Pressure Level
SF6 Lockout signal (second stage)	LD_RIO/GGIO15/RIO1GGIO1.SPCSO10	LD_RIO/SIMG1/R1Gs63SIMG1.InsTr	0	0	Ok
			1	1	Circuit Breaker SF6 Tripping Pressure Level
S27	LD_RIO/GGIO15/RIO1GGIO1.SPCSO11	LD_RIO/GGIO16/RIO1GGIO1.SPCSO11	0	0	Ok
			1	1	S27
Additional I/O	LD_RIO/GGIO15/RIO1GGIO1.SPCSO12	…	0	…	…
			1	…	…
Additional I/O	LD_RIO/GGIO15/RIO1GGIO1.SPCSO13	…	0	…	…
			1	…	…
Additional I/O	LD_RIO/GGIO15/RIO1GGIO1.SPCSO14	…	0	…	…
			1	…	…

7.5.2.2. Reporting to the RTU related to the RIO1 (52 MT type) communication

The information coming from the RIO1 (subscribed in the LN RIO1GGIO1) whose semantics is defined in IEC61850-7-4:

a. Partly are already present (and therefore shall be re-used) in some LN of other LDs of MFP,

b. The remaining is modelled with the LNs introduced hereafter.

All these data is Reported to the RTU

Switch State (89

Table 112 – LNInstance: 1 - prefix: R1_89T – XSWI1 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
Loc	SPS	Local operation		M
EEHealth	INS	External equipment health		O
EEName	DPL	External equipment name plate		O
OpCnt	INS	Operator counter		M
Controls				
Pos	DPC	Switch position		M
BlkOpn	SPC	Block opening		M
BlkCls	SPC	Block closing		M
ChaMotEna	SPC	Charger motor enabled		O
Status Information				
SwTyp	INS	Switch type		M
SwOpCap	INS	Switch operating capability		M
MaxOpCap	INS	Circuit switch operating capability when fully charged		O

NOTES:

Controls → Pos: for reporting the state of the circuit switch, ref. IEC61850-7-3 defines four states (intermediate-state | off | on | bad-state), but only the off and on are handled, according to the information transmitted by the RIO1.

Circuit Breaker SF6 supervision

Table 113 –LNInstance: 1 – prefix: R1Gs63 – SIMG1 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
EEHealth	INS	External equipment health		O
EEName	DPL	External equipment name plate		O
Measured values				
Pres	MV	Isolation gas pressure		O
Den	MV	Isolation gas density		O
Tmp	MV	Isolation gas temperature		O
Status Information				
InsAlm	SPS	Insulation gas critical (refill isolation medium)		M
InsBlk	SPS	Insulation gas not safe (block device operation)		O
InsTr	SPS	Insulation gas dangerous (trip for device isolation)		R
PresAlm	SPS	Isolation gas pressure alarm		(C) R
DenAlm	SPS	Isolation gas density alarm		(C)

TmpAlm	SPS	Isolation gas temperature alarm		(C)
InsLevMax	SPS	Isolation gas level maximum (relates to predefined filling value)		O
InsLevMin	SPS	Isolation gas level minimum (relates to predefined filling value		O

Condition C: depending on the supervised properties of the insulation gas, at least one status information shall be used.

NOTES:

Status Information → InsAlm: for reporting to the RTU the 63G Alm. - Circuit Breaker SF6 Alarming Pressure Level according to the information issued by the RIO1 (0 = Ok, 1 = Alarm)

Status Information → InsTr: for reporting to the RTU the 63G Tr. - Circuit Breaker SF6 Tripping Pressure Level according to the information issued by the RIO1 (0 = Ok, 1 = Alarm)

Status Information → PresAlm: (ready) for reporting to the RTU the Circuit Breaker Anomaly SF6 low Pressure. This info isn't currently reported to the RTU but is modelled to comply with the [4] and to support the interoperability with other IEDs in the substation interfacing a SF6 insulated Circuit Breaker (0 = Ok, 1 = Alarm).

7.5.3 Input/Output Remote module N°2 – BM (in case of MODBUS communication profile)

7.5.3.1. Data exchange with the RIO n°2 (subscriptions and commands) and with the RTU (reports)

The following LN models:

a. the information that the MFP receives from the RIO N°2 (BM type) via GOOSE messages and the related reporting that the MFP issues to the RTU via MMS;

b. the commands that the MFP issues to the RIO N°2 (BM type) via GOOSE messages.

Table 114 – LNInstance: 1 - prefix: RIO2 – GGIO15 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
EEHealth	INS	External equipment health (external sensor)		O
EEName	DPL	External equipment name plate		O
Loc	SPS	Local operation		O
OpCntRs	INC	Resetable operation counter		R
Measured values				
AnIn	MV	Analogue input		O
Controls				
SPCSO1	SPC	Single point controllable status output (1)		R
SPCSO2	SPC	Single point controllable status output (2)		R
SPCSO3	SPC	Single point controllable status output (3)		R
SPCSO4	SPC	Single point controllable status output (4)		R
SPCSO5	SPC	Single point controllable status output (5)		R
SPCSO6	SPC	Single point controllable status output (6)		R
SPCSO7	SPC	Single point controllable status output (7)		R
SPCSO8	SPC	Single point controllable status output (8)		R

SPCSO9	SPC	Single point controllable status output (9)		R
SPCSO10	SPC	Single point controllable status output (10)		R
SPCSO11	SPC	Single point controllable status output (11)		R
SPCSO12	SPC	Single point controllable status output (12)		R
SPCSO13	SPC	Single point controllable status output (13)		R
SPCSO14	SPC	Single point controllable status output (14)		R
DPCSO	DPC	Double point controllable status output		O
ISCSO	INC	Integer status controllable status output		O
Status Information				
IntIn	INS	Integer status input		O
Alm	SPS	General single alarm		O
Ind1	SPS	General indication (binary input) (1)		R
Ind2	SPS	General indication (binary input) (2)		R
Ind3	SPS	General indication (binary input) (3)		R
Ind4	SPS	General indication (binary input) (4)		R

NOTES:

Common Logical Node Information→ OpCntRs: to count and store the number of events occurred

Controls→ SPCSO1: for mapping the info 26 Alm. Series / Parallel Resistors issued by the RIO2 and reported to the RTU (0 = Ok, 1 = Alarm)

Controls→ SPCSO2: for mapping the info 26 Alm. Fixed / Mobile Coil issued by the RIO2 and reported to the RTU (0 = Ok, 1 = Alarm)

Controls→ SPCSO3: for mapping the info 97 Alm. Fixed / Mobile Coil issued by the RIO2 and reported to the RTU (0 = Ok, 1 = Alarm)

Controls→ SPCSO4: for mapping the info 99 Alm. Fixed / Mobile Coil issued by the RIO2 and reported to the RTU (0 = Ok, 1 = Alarm)

Controls→ SPCSO5: for mapping the info Anomaly anti-condensation resistance Mobile Coil / ATV tripping issued by the RIO2 and reported to the RTU (0 = Ok, 1 = Alarm)

Controls→ SPCSO6: for mapping the info 26 Tr. Series / Parallel Resistors issued by the RIO2 and reported to the RTU (0 = Ok, 1 = Alarm)

Controls→ SPCSO7: for mapping the info Coil Severe Alarm issued by the RIO2 and reported to the RTU (0 = Ok, 1 = Alarm)

Controls→ SPCSO8: for mapping the info 26 Alm. TFN issued by the RIO2 and internally correlated to the MFP/LD_RIO/YPTR1/R2TN26YPTR1.HPTmpAlm

Controls→ SPCSO9: for mapping the info 97 Alm. TFN issued by the RIO2 and internally correlated to the MFP/LD_RIO/YPTR1/R2TN97YPTR1.HPTmpTr

Controls→ SPCSO10: for mapping the info 26 Tr. TFN issued by the RIO2 and internally correlated to the MFP/LD_RIO/YPTR1/R2TN26YPTR1.HPTmpTr

Controls→ SPCSO11: for mapping the info 97 Tr. TFN issued by the RIO2 and internally correlated to the MFP/LD_RIO/YPTR1/R2TN97YPTR1.HPTmpTr

Controls→ SPCSO12: for mapping the info MT Circuit Breaker - Line Voltage Absence (27X) issued by the RIO2 and reported to the RTU (0 = Ok, 1 = Alarm)

Controls→ SPCSO13: (reserved) for mapping other info issued by the RIO2

Controls→ SPCSO14: (reserved) for mapping other info issued by the RIO2

Status Information→ Ind1: for issuing the Command 1 (generated by internal MFP logics) to the field devices via the RIO2

Status Information→ Ind2: for issuing the Command 2 (generated by internal MFP logics) to the field devices via the RIO2.

Status Information→ Ind3: for issuing the Command 3 (generated by internal MFP logics) to the field devices via the RIO2

Status Information→ Ind4: for issuing the Command 4 (generated by internal MFP logics) to the field devices via the RIO2.

The following table shows the:

a. The functional correlation between the variables (Generic LN) used to subscribe the signals coming from the RIO2 via GOOSE messages and the variables (Specific LNs) used to forward this information to the RTU via Report messages;

b. The meaning of their values on the two interfaces.

Table 115 – Remote I/O module N°2 – BM type

Signal	Input GOOSE from RIO	Output Reporting to the RTU	Variable values on the two interfaces		Meaning of the value
			Input	Output	
26 Alm. Series / Parallel Resistors	LD_RIO/GGIO15/RIO2GGIO1.SPCSO1	LD_RIO/GGIO16/RIO2GGIO1.SPCSO1	0	0	Ok
			1	1	Alarm on
26 Alm. Fixed / Mobile Coil	LD_RIO/GGIO15/RIO2GGIO1.SPCSO2	LD_RIO/GGIO16/RIO2GGIO1.SPCSO2	0	0	Ok
			1	1	Alarm on
97 Alm. Fixed / Mobile Coil	LD_RIO/GGIO15/RIO2GGIO1.SPCSO3	LD_RIO/GGIO16/RIO2GGIO1.SPCSO3	0	0	Ok
			1	1	Alarm on
99 Alm. Fixed / Mobile Coil	LD_RIO/GGIO15/RIO2GGIO1.SPCSO4	LD_RIO/GGIO16/RIO2GGIO1.SPCSO4	0	0	Ok
			1	1	Alarm on
Anomaly anti-condensation resistance Mobile Coil / ATV trip	LD_RIO/GGIO15/RIO2GGIO1.SPCSO5	LD_RIO/GGIO16/RIO2GGIO1.SPCSO5	0	0	Ok
			1	1	Alarm on
26 Tr. Series / Parallel Resistors	LD_RIO/GGIO15/RIO2GGIO1.SPCSO6	LD_RIO/GGIO16/RIO2GGIO1.SPCSO6	0	0	Ok
			1	1	Alarm on
Coil Severe Alarm	LD_RIO/GGIO15/RIO2GGIO1.SPCSO7	LD_RIO/GGIO16/RIO2GGIO1.SPCSO7	0	0	Ok
			1	1	Coil Severe Alarm
26 Alm. TFN	LD_RIO/GGIO15/RIO2GGIO1.SPCSO8	LD_RIO/YPTR1/R2TN26YPTR1.HPTmpAlm	0	0	Normal Temperature
			1	1	Alm. 26 High Temperature
97 Alm. TFN	LD_RIO/GGIO15/RIO2GGIO1.SPCSO9	LD_RIO/YPTR1/R2TN97YPTR1.HPTmpAlm	0	0	Normal Temperature
			1	1	Alm. 97 High Temperature
26 Tripping TFN	LD_RIO/GGIO15/RIO2GGIO1.SPCSO10	LD_RIO/YPTR1/R2TN26YPTR1.HPTmpTr	0	0	Ok
			1	1	26 Tripping TFN – High Temperature
97 Tripping TFN	LD_RIO/GGIO15/RIO1GGIO1.SPCSO11	LD_RIO/YPTR1/R2TN97YPTR1.HPTmpTr	0	0	Ok
			1	1	97 Tripping TFN – High Temperature
MT Circuit Breaker - Line Voltage Absence	LD_RIO/GGIO15/RIO2GGIO1.SPCSO12	LD_RIO/GGIO16/RIO2GGIO1.SPCSO12	0	TBD	OK
			1	TBD	Alarm on

Additional I/O	LD_RIO/GGIO15/RIO2GGIO1.SPCSO13	…	0	…	…
			1	…	…
Additional I/O	LD_RIO/GGIO15/RIO2GGIO1.SPCSO14	…	0	…	…
			1	…	…

7.5.3.2. Reporting to the RTU related to the RIO 2 (BM type) communication

The information coming from the RIO2 (subscribed in the LN RIO2GGIO1) whose semantics is defined in IEC61850-7-4:

a. Partly are already present (and therefore shall be re-used) in some LN of other LDs of MFP;

b. The remaining is modelled with the LNs introduced hereafter.

26 TFN Alarm/Tripping (Temperature)

Table 116 – LNInstance: 1 - prefix: R2TN26 – YPTR1 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
EEHealth	INS	External equipment health (external sensor)		O
EEName	DPL	External equipment name plate		O
OpTmh	INS	Operation time		O
Measured values				
HPTmp	MV	Winding hotspot temperature (in °C)		O
Status Information				
HPTmpAlm	SPS	Winding hot point temperature alarm		R
HPTmpTr	SPS	Winding hot point temperature trip	T	R
OANL	SPS	Operation at no load		O
OpOvA	SPS	Operation at overcurrent		O
OpOvV	SPS	Operation at overvoltage		O
OpUnV	SPS	Operation at undervoltage		O
CGAlm	SPS	Core ground alarm		O
Settings				
HiVRtg	ASG	Rated Voltage (High voltage level)		O
LoVRtg	ASG	Rated Voltage (Low voltage level)		O
PwrRtg	ASG	Rated power		O

NOTES:

Status Information→ HPTmpAlm: for reporting the 26 Alm. TFN (Temperature) according to the information issued by the RIO2

Status Information→ HPTmpTr: for reporting the 26 Tripping TFN (Temperature) according to the information issued by the RIO2.

97 Alarm/Tripping TFN (Buchholz)

Table 117 – LNInstance: 1 - prefix: R2TN97 – YPTR1 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
EEHealth	INS	External equipment health (external sensor)		O
EEName	DPL	External equipment name plate		O
OpTmh	INS	Operation time		O
Measured values				
HPTmp	MV	Winding hotspot temperature (in °C)		O
Status Information				
HPTmpAlm	SPS	Winding hot point temperature alarm		R
HPTmpTr	SPS	Winding hot point temperature trip	T	R
OANL	SPS	Operation at no load		O
OpOvA	SPS	Operation at overcurrent		O
OpOvV	SPS	Operation at overvoltage		O
OpUnV	SPS	Operation at undervoltage		O
CGAlm	SPS	Core ground alarm		O
Settings				
HiVRtg	ASG	Rated Voltage (High voltage level)		O
LoVRtg	ASG	Rated Voltage (Low voltage level)		O
PwrRtg	ASG	Rated power		O

NOTES:

Status Information→ HPTmpAlm: for reporting the info 97 Alm. TFN (Buchholz) according to the information issued by the RIO2

Status Information→ HPTmpTr: for reporting the info 97 Tripping TFN (Buchholz) according to the information issued by the RIO2.

7.6 Virtual Input/Output Logical Device: Detail of LN

The Virtual Input/Output Logical Device (LD_VIO) contains all the LNs needed to model experimental inputs and outputs ready for any future use/development.

Table 118 – LLN01 type				
Attribute Name	**Attribute Type**	**Explanation**	**T**	**M/O**
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
Loc	SPS	Local operation for complete logical device		O
OpTmh	INS	Operation Time		O
Controls				

Diag	SPC	Run Diagnostic		O
LEDRs	SPC	LED reset	T	O

Table 119 – LNInstance: 1 – LPHD2 type				
Attribute Name	**Attribute Type**	**Explanation**	**T**	**M/O**
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
PhyNam	DPL	Physical device name plate		M
PhyHealth	INS	Physical device health		M
OutOv	SPS	Output communications buffer overflow		O
Proxy	SPS	Indicates if this LN is a proxy		M
InOv	SPS	Input communications buffer overflow		O
NumPwrUp	INS	Number of Power ups		O
WrmStr	INS	Number of Warm Starts		O
WacTrg	INS	Number of watchdog device resets detected		O
PwrUp	SPS	Power Up detected		O
PwrDn	SPS	Power Down detected		O
PwrSupAlm	SPS	External power supply alarm		O
RsStat	SPC	Reset device statistics	T	O

7.6.1 Virtual Input

Table 120 – LNInstance: 1 - prefix: VIn01 – GGIO16 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
EEHealth	INS	External equipment health (external sensor)		O
EEName	DPL	External equipment name plate		O
Loc	SPS	Local operation		O
OpCntRs	INC	Resetable operation counter		R
Measured values				
AnIn	MV	Analogue input		O
Controls				
SPCSO	SPC	Single point controllable status output		R
DPCSO	DPC	Double point controllable status output		O
ISCSO	INC	Integer status controllable status output		O
Status Information				
IntIn	INS	Integer status input		O
Alm	SPS	General single alarm		R
Ind	SPS	General indication (binary input)		O

LNInstance: 1 - prefix: VIn02..VIn31

Table 121 – LNInstance: 1 - prefix: VIn32 – GGIO16 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
EEHealth	INS	External equipment health (external sensor)		O
EEName	DPL	External equipment name plate		O
Loc	SPS	Local operation		O
OpCntRs	INC	Resetable operation counter		R
Measured values				
AnIn	MV	Analogue input		O
Controls				
SPCSO	SPC	Single point controllable status output		R
DPCSO	DPC	Double point controllable status output		O
ISCSO	INC	Integer status controllable status output		O
Status Information				
IntIn	INS	Integer status input		O
Alm	SPS	General single alarm		R
Ind	SPS	General indication (binary input)		O

NOTES:

Common Logical Node Information→ OpCntRs: to count and store the number of State variations

Controls→ SPCSO: available/ready Input n (n = 1..32)

Controls→ Alm: available/ready signalling n (n = 1..32).

7.6.2 Virtual Output

Table 122 – LNInstance: 1 - prefix: VOut – GGIO17 type				
Attribute Name	**Attribute Type**	**Explanation**	T	M/O
LNName		Shall be inherited from Logical Node Class (IEC 61850-7-2)		
Data				
Common Logical Node Information				
		LN shall inherit all Mandatory Data from Common Logical Node Class		M
EEHealth	INS	External equipment health (external sensor)		O
EEName	DPL	External equipment name plate		O
Loc	SPS	Local operation		O
OpCntRs	INC	Resetable operation counter		O
Measured values				
AnIn	MV	Analogue input		O

Controls				
SPCSO	SPC	Single point controllable status output		O
DPCSO	DPC	Double point controllable status output		O
ISCSO	INC	Integer status controllable status output		O
Status Information				
IntIn	INS	Integer status input		O
Alm	SPS	General single alarm		O
Ind1	SPS	General indication (binary input)		R
Ind2	SPS	General indication (binary input)		R
Ind3	SPS	General indication (binary input)		R
Ind4	SPS	General indication (binary input)		R
Ind5	SPS	General indication (binary input)		R
Ind6	SPS	General indication (binary input)		R
Ind7	SPS	General indication (binary input)		R
Ind8	SPS	General indication (binary input)		R
Ind9	SPS	General indication (binary input)		R
Ind10	SPS	General indication (binary input)		R
Ind11	SPS	General indication (binary input)		R
Ind12	SPS	General indication (binary input)		R
Ind13	SPS	General indication (binary input)		R
Ind14	SPS	General indication (binary input)		R
Ind15	SPS	General indication (binary input)		R
Ind16	SPS	General indication (binary input)		R

NOTES:

Controls→ Ind1: available/ready Output 1

Controls→ Ind2: available/ready Output 2

Controls→ Ind3: available/ready Output 3

Controls→ Ind4: available/ready Output 4

Controls→ Ind5: available/ready Output 5

Controls→ Ind6: available/ready Output 6

Controls→ Ind7: available/ready Output 7

Controls→ Ind8: available/ready Output 8

Controls→ Ind9: available/ready Output 9

Controls→ Ind10: available/ready Output 10

Controls→ Ind11: available/ready Output 11

Controls→ Ind12: available/ready Output 12

Controls→ Ind13: available/ready Output 13

Controls→ Ind14: available/ready Output 14

Controls→ Ind15: available/ready Output 15

Controls→ Ind16: available/ready Output 16.

8 ASPECTS OF DATA COMMUNICATION MODELED UNDER IEC61850

Figure 3 describes the set of protocol stacks, ref. IEEE 802.1Q, and communication services (ref. IEC61850-5) defined in the IEC61850 standard and used to communicate with the IEDs of the DS (RGDM ST other MFP, the MTP and the client (TPT2020 and/or other for testing or temporary operations):

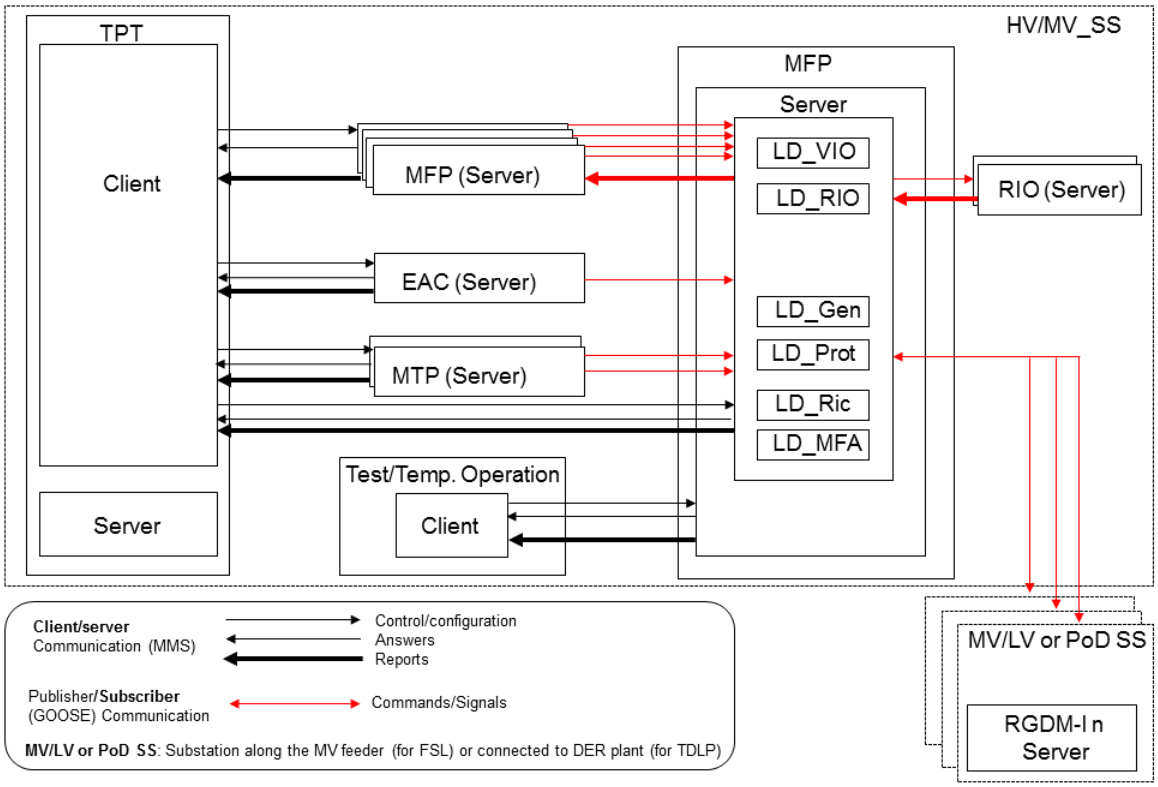

Figure 3 – IE61850 Communication Streams and Services

The MFP uses Client/Server messaging to communicate with the RTU (GSTR1XX series, TPT2020) in the DS, according to the following architecture and protocols IEE.802.1Q:

a. 7 OSI Layers,

b. ACSI via MMS via TCP/IP via ISO/IEC 8802-3,

c. Unicast

for commands/controls, configurations, periodic spontaneous reporting or events.

The IED will also interoperate with other Servers in the DS via GOOSE, ref. to IEEE.802.1Q:

d. 3 OSI Layers,

e. GOOSE via ISO/IEC 8802-3 via IEEE 802.1Q (Virtual LAN),

f. Multicast

for bay/field automation.

The spreadsheet file will be provided by ENEL during the procurement process (ref. Par.9.1)

9 MISCELLANEOUS

This chapter include further requirements, recommendations and additional information.

9.1 Clarification during the procuremen process

By summarizing, during the procurement process the following clarification will be provided to the supplier:

a. The spreadsheet file that modelled the input/output required inGSTP101 according to IEC61850 as described in chapter 7 and 8;

b. The ICD file that implement the formal description of the IED in chapter 7 and 8.

9.2 ICD file revision control

Owing to the changes affecting the information model or the communication of the IED, the following rules are adopted to ensure that the version numbering clearly identifies each variation or iteration of the ICD file.

<Header id = "IEDxxx ENEL" version = "v" revision = "rrr" toolID = "" nameStructure = "IEDName" />

a. version is an integer increased by one unit for major releases (e.g. during the prototyping it will be 1, in operation it will be 2 or more),

b. revision is an integer increased by one unit for minor releases due to some new feature (affecting the Data Model or the Communication) or bug fix. It is reset to zero when the version changes.

*<ReportControl … confRev="**c**" datSet="xxx"…/>*

*<GSEControl … confRev="**c**" datSet="xxx" …/>*

The confRev, by IEC 61850 standard, is an integer starting from “1” that increments

c. when the referenced datSet is changed ,ref IEC 61850-5,

d. when the Report or the GOOSE control block itself is modified IEC 61850-6,

e. the counter is never reset.

For example, the attached ICD file may have

Header

f. version = "2" (for operation)

g. revision = "0" (no minor revisions since the last major version)

h. <GSEControl name = "gcb_TDLP"

i. confRev = "3" (due to modified Data Set or Control Block since the prototyping).