MOTOROLA

DUAL DECADE COUNTER; DUAL 4-STAGE BINARY COUNTER

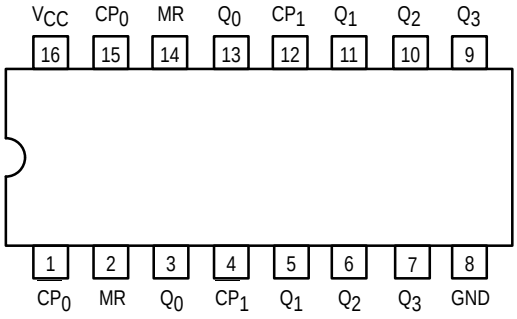
The SN54/74LS390 and SN54/74LS393 each contain a pair of high-speed 4-stage ripple counters. Each half of the LS390 is partitioned into a divide-by-two section and a divide-by five section, with a separate clock input for each section. The two sections can be connected to count in the 8.4.2.1 BCD code or they can count in a biquinary sequence to provide a square wave (50% duty cycle) at the final output.

Each half of the LS393 operates as a Modulo-16 binary divider, with the last three stages triggered in a ripple fashion. In both the LS390 and the LS393, the flip-flops are triggered by a HIGH-to-LOW transition of their CP inputs. Each half of each circuit type has a Master Reset input which responds to a HIGH signal by forcing all four outputs to the LOW state.

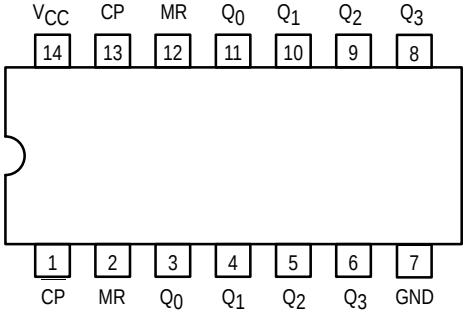
- Dual Versions of LS290 and LS293
- LS390 has Separate Clocks Allowing ÷2, ÷2.5, ÷5
- Individual Asynchronous Clear for Each Counter
- Typical Max Count Frequency of 50 MHz
- Input Clamp Diodes Minimize High Speed Termination Effects

CONNECTION DIAGRAM DIP (TOP VIEW)

SN54/74LS390



SN54/74LS393

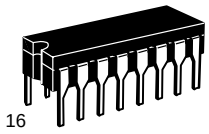


NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

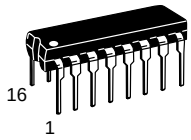
SN54/74LS390
SN54/74LS393

DUAL DECADE COUNTER; DUAL 4-STAGE BINARY COUNTER

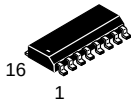
LOW POWER SCHOTTKY



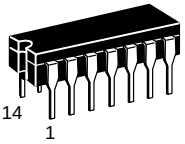
J SUFFIX
CERAMIC
CASE 620-09



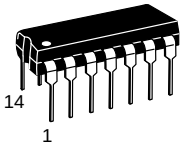
N SUFFIX
PLASTIC
CASE 648-08



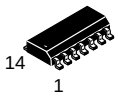
D SUFFIX
SOIC
CASE 751B-03



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06



D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

PIN NAMES		LOADING (Note a) HIGH	LOW
$\overline{CP}$	Clock (Active LOW going edge) Input to +16 (LS393)	0.5 U.L.	1.0 U.L.
$\overline{CP}_0$	Clock (Active LOW going edge) Input to ÷2 (LS390)	0.5 U.L.	1.0 U.L.
$\overline{CP}_1$	Clock (Active LOW going edge) Input to ÷5 (LS390)	0.5 U.L.	1.5 U.L.
MR	Master Reset (Active HIGH) Input	0.5 U.L.	0.25 U.L.
$Q_0 - Q_3$	Flip-Flop outputs (Note b)	10 U.L.	5 (2.5) U.L.

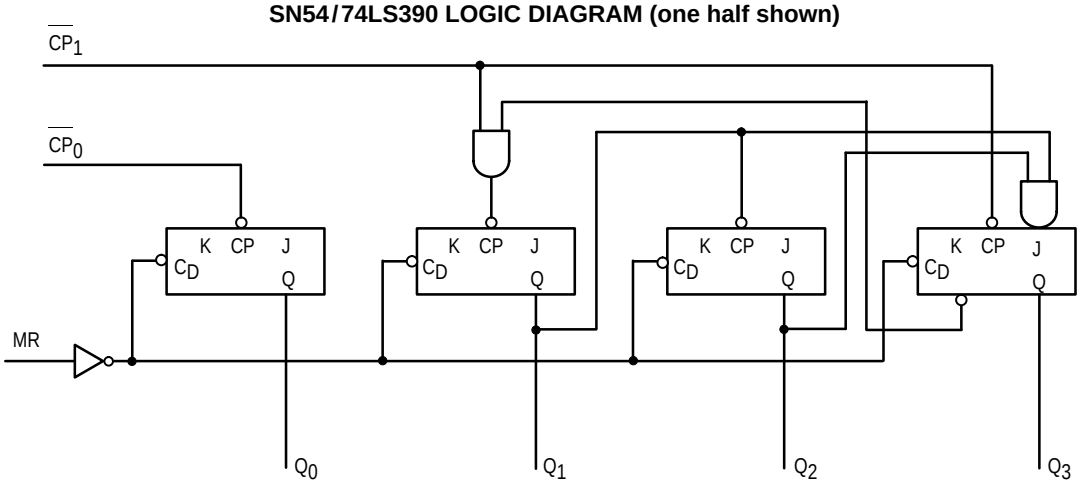
NOTES:
a) 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

FUNCTIONAL DESCRIPTION

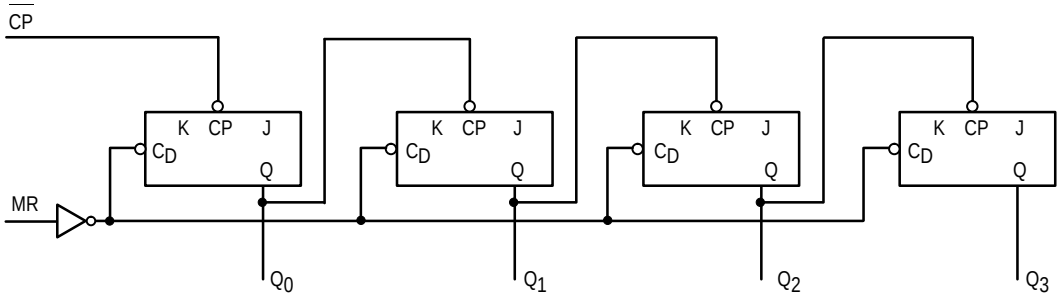
Each half of the SN54/74LS393 operates in the Modulo 16 binary sequence, as indicated in the ÷16 Truth Table. The first flip-flop is triggered by HIGH-to-LOW transitions of the CP input signal. Each of the other flip-flops is triggered by a HIGH-to-LOW transition of the Q output of the preceding flip-flop. Thus state changes of the Q outputs do not occur simultaneously. This means that logic signals derived from combinations of these outputs will be subject to decoding spikes and, therefore, should not be used as clocks for other counters, registers or flip-flops. A HIGH signal on MR forces all outputs to the LOW state and prevents counting.

Each half of the LS390 contains a ÷5 section that is independent except for the common MR function. The ÷5 section operates in 4.2.1 binary sequence, as shown in the ÷5 Truth Table, with the third stage output exhibiting a 20% duty cycle when the input frequency is constant. To obtain a ÷10 function having a 50% duty cycle output, connect the input signal to CP_1 and connect the Q_3 output to the CP_0 input; the Q_0 output provides the desired 50% duty cycle output. If the input frequency is connected to CP_0 and the Q_0 output is connected to CP_1, a decade divider operating in the 8.4.2.1 BCD code is obtained, as shown in the BCD Truth Table. Since the flip-flops change state asynchronously, logic signals derived from combinations of LS390 outputs are also subject to decoding spikes. A HIGH signal on MR forces all outputs LOW and prevents counting.

SN54/74LS390 LOGIC DIAGRAM (one half shown)



SN54/74LS393 LOGIC DIAGRAM (one half shown)



SN54/74LS390 BCD TRUTH TABLE (Input on CP_0; Q_0 CP_1)

COUNT	OUTPUTS			
	Q_3	Q_2	Q_1	Q_0
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

SN54/74LS390 ÷5 TRUTH TABLE (Input on CP_1)

COUNT	OUTPUTS		
	Q_3	Q_2	Q_1
0	L	L	L
1	L	L	H
2	L	H	L
3	L	H	H
4	H	L	L

SN54/74LS390 ÷10 (50% @ Q_0) TRUTH TABLE (Input on CP_1, Q_3 to CP_0)

COUNT	OUTPUTS			
	Q_3	Q_2	Q_1	Q_0
0	L	L	L	L
1	L	L	H	L
2	L	H	L	L
3	L	H	H	L
4	H	L	L	L
5	L	L	L	H
6	L	L	H	H
7	L	H	L	H
8	L	H	H	H
9	H	L	L	H

SN54/74LS393 TRUTH TABLE

COUNT	OUTPUTS			
	Q_3	Q_2	Q_1	Q_0
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	–55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			–0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Typ	Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current	MR			−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
		$\overline{CP}$, $\overline{CP_0}$			−1.6	mA		
		$\overline{CP_1}$			−2.4	mA		
I_{OS}	Short Circuit Current (Note 1)		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				26	mA	V_{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter		Limits Min	Typ	Max	Unit	Test Conditions
f_{MAX}	Maximum Clock Frequency CP_0 to Q_0		25	35		MHz	C_L = 15 pF
f_{MAX}	Maximum Clock Frequency CP_1 to Q_1		20			MHz	
t_{PLH} t_{PHL}	Propagation Delay, CP to Q_0	LS393		12 13	20 20	ns	
t_{PLH} t_{PHL}	$\overline{CP_0}$ to Q_0	LS390		12 13	20 20	ns	
t_{PLH} t_{PHL}	$\overline{CP}$ to Q_3	LS393		40 40	60 60	ns	
t_{PLH} t_{PHL}	$\overline{CP_0}$ to Q_2	LS390		37 39	60 60	ns	
t_{PLH} t_{PHL}	$\overline{CP_1}$ to Q_1	LS390		13 14	21 21	ns	
t_{PLH} t_{PHL}	$\overline{CP_1}$ to Q_2	LS390		24 26	39 39	ns	
t_{PLH} t_{PHL}	$\overline{CP_1}$ to Q_3	LS390		13 14	21 21	ns	
t_{PHL}	MR to Any Output	LS390/393		24	39	ns	

AC SETUP REQUIREMENTS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter		Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
t_W	Clock Pulse Width	LS393	20			ns	V_{CC} = 5.0 V
t_W	$\overline{CP}_0$ Pulse Width	LS390	20			ns	
t_W	$\overline{CP}_1$ Pulse Width	LS390	40			ns	
t_W	MR Pulse Width	LS390/393	20			ns	
t_{rec}	Recovery Time	LS390/393	25			ns	

AC WAVEFORMS

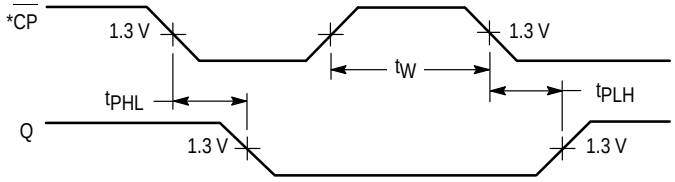


Figure 1

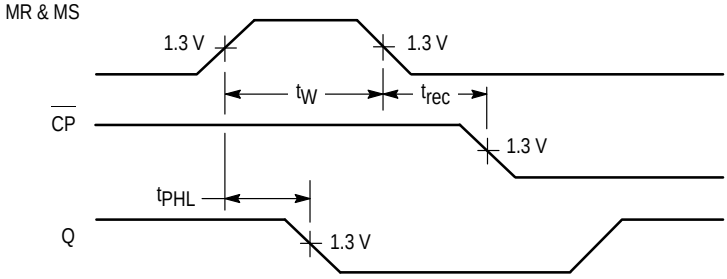


Figure 2

*The number of Clock Pulses required between t_{PHL} and t_{PLH} measurements can be determined from the appropriate Truth Table.