Fairchild Semiconductor
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High-Speed CMOS (MM74HC) Processing

The MM74HC logic family achieves its high speed by utilizing microCMOS Technology. This is a 3.5 silicon gate P-well CMOS process single layer poly, single layer metal, P-well process with oxide-isolated transistors. Why do silicon-gate transistors (polycrystalline) switch faster than metal-gate transistors? The reason is related both to the parasitic capacitances inherent in integrated circuits and the gain of the transistors. The speed at which an MOS transistor can switch depends on how fast its internal parasitic capacitance, as well as its external load capacitance, can be charged and discharged. Capacitance takes time to be charged and discharged, and hence degrades a transistor's performance. The gain of a transistor is a measure of how well a transistor can charge and discharge a capacitor. Therefore, to increase speed, it is desirable to both decrease parasitic capacitance and increase transistor gain. These advantages are achieved with Fairchild's silicon-gate CMOS process. To understand exactly how these improvements occur in silicon-gate CMOS, it is helpful to compare the process to the metal-gate CMOS process.

Metal-Gate CMOS Processing

Figure 1 through Figure 12 are cross sections of a metal-gate CMOS pair of P- and N-channel transistors with associated guard rings. Guard rings are necessary in metal-gate processing to prevent leakage currents between the sources and drains of separate transistors. The starting material is an N-type silicon substrate covered by a thin layer of thermally grown silicon dioxide (SiO_2) (Figure 1). Silicon dioxide, also called oxide acts as both a mask for certain processing steps and a dielectric insulator. Figure 2 shows the addition of a lightly doped P−well in which the N-channel transistors and P+ guard rings will later be located. The P−well is ion implanted into the substrate. A thin layer of oxide allows ions to be implanted through it, while a thicker oxide will block ion implantation.

Next, the oxide over the P−well is stripped, and a new layer of oxide is grown. Following this, holes are etched into the oxide where the P+ source, drain, and guard ring diffusions shall occur. The P+ regions are diffused, and then additional oxide is grown to fill the holes created for diffusion (Figures 3, 4, 5). The following step is to cut holes in the oxide to diffuse the N-channel sources, drains and guard bands. The oxide is again thermally grown (Figures 6, 7).

In the following step, the composite mask is created by again cutting holes in the oxide. This defines the areas where contacts and transistor gates will occur (Figure 8). A thin layer of gate oxide is grown over these regions (Figure 9), and alignment of this to the source and drain regions is a critical step. If the gate oxide overlaps the source or drain, this will cause additional parasitic capacitance.

Contacts to transistor sources and drains are cut into the thin oxide where appropriate (Figure 10), and then the interconnect metal is deposited (Figure 11). Depositing the metal over the gate areas is also a critical step, for a misalignment will cause extra unwanted overlap capacitance. Figure 12 illustrates the final step in processing, which is to deposit an insulating layer of silicon dioxide over the entire surface of the integrated circuit.

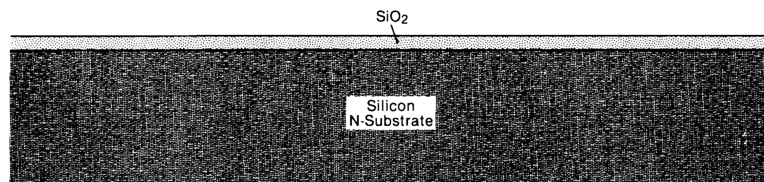

FIGURE 1.
Initial Oxidation, Thermally Grown Silicon Dioxide Layer on Silicon Substrate Surface

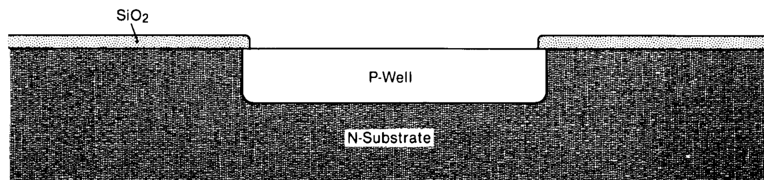

FIGURE 2.
Mask and Formation of P − Well Tub in which N-Channel Devices will be Located

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Metal-Gate CMOS Processing (Continued)

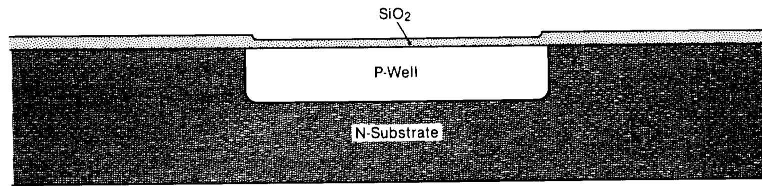

FIGURE 3.
Well Oxidation, Thermally Grown Silicon Dioxide Layer Over P − Well Area

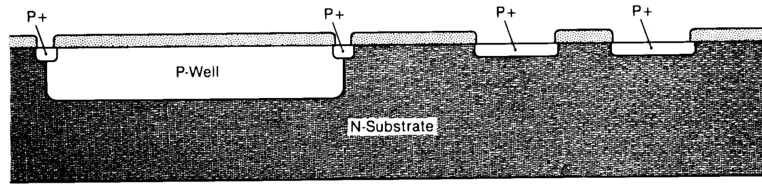

FIGURE 4.
P+ Mask and Formation of Low Resistance P + Type Pockets in − Well and N-Substrate

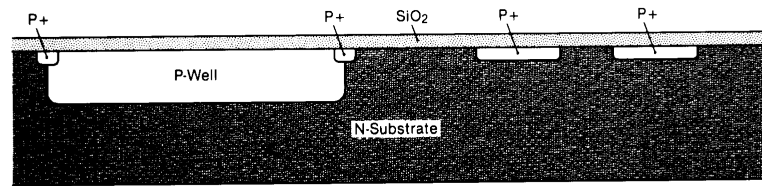

FIGURE 5.
P + Oxidation, Thermally Grown Silicon Dioxide Layer Over P + Type Pockets

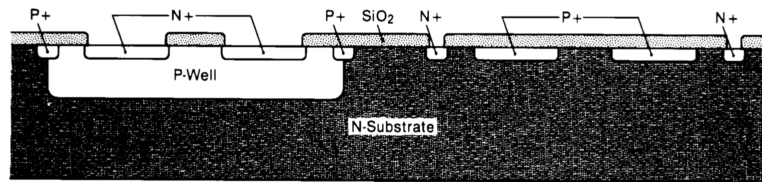

FIGURE 6.
N + Mask and Formation of Low Resistance N + Type Pockets in P− Well and N-Substrate

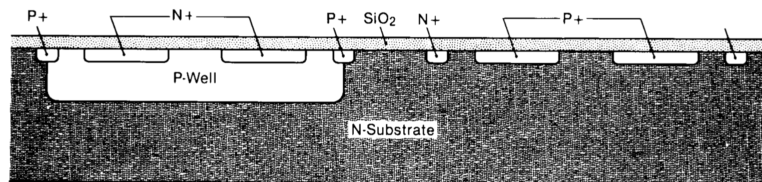

FIGURE 7.
N + Oxidation, Thermally Grown Silicon Dioxide Layer Over N + Type Pockets

Metal-Gate CMOS Processing (Continued)

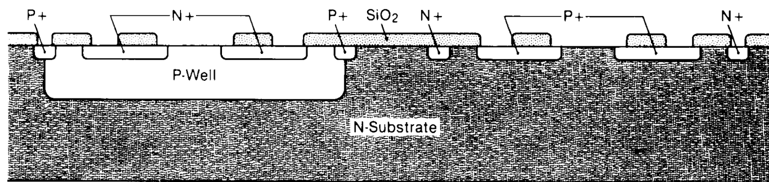

FIGURE 8.
Composite Mask and Openings to N- and P-Channel Devices

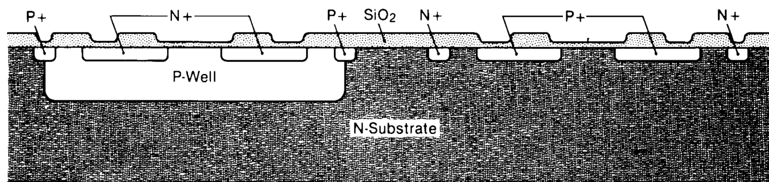

FIGURE 9.
Gate Oxidation, Thermally Grown Silicon Dioxide Layer Over N- and P-Channel Devices

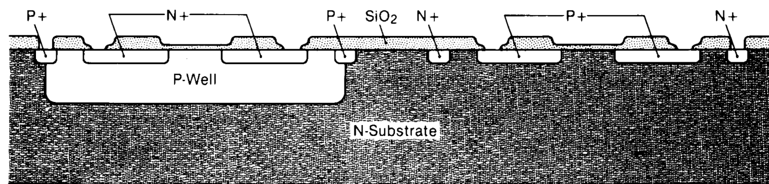

FIGURE 10.
Contact Mask and Openings to N- and P-Channel Devices

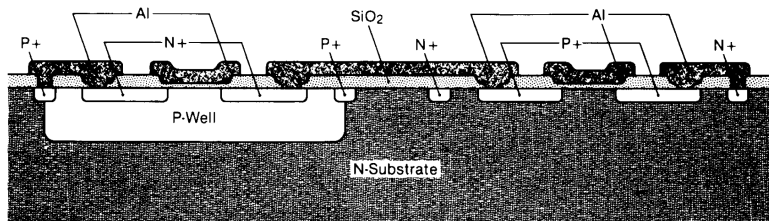

FIGURE 11.
Metallization, Metal Mask, Resulting in Gate Metal and Metal Interconnects

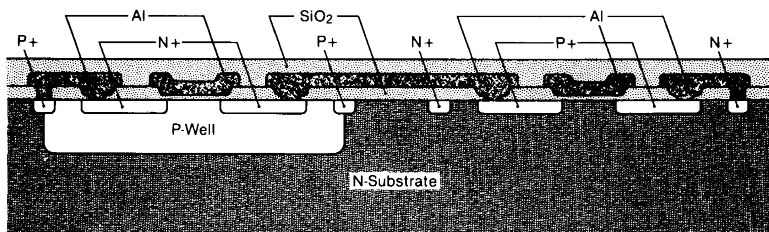

FIGURE 12.
Passivation Oxide, Deposited Silicon Dioxide Over Entire Die Surface

Silicon-Gate CMOS Processing

The silicon-gate CMOS process starts with the same two steps as the metal-gate process, yielding an N– substrate with an ion-implanted P– well (Figure 13 and Figure 14). That, however, is where the similarity ends. Next, the initial oxide is stripped, and another layer of oxide, called pad oxide, is thermally grown. Also, a layer of silicon nitride is deposited across the surface of the wafer (Figure 15). The nitride prevents oxide growth on the areas it covers. Thus, in Figure 16, the nitride is etched away wherever field oxide is to be grown. The field oxide is a very thick layer of exude, and it is grown everywhere except in the transistor regions (Figure 17). As an oxide grows in silicon, it consumes the silicon substrate beneath it and combines it with ambient oxygen to produce silicon dioxide. Growth of this very thick oxide causes the oxide to be recessed below the surface of the silicon substrate by a significant amount. A recessed field oxide eliminates the need for guard ring diffusions, because current cannot flow through the field oxide, which completely isolates each transistor from every other transistor.

The next step is to deposit a layer of polycrystalline silicon, also called poly, which will form both the gate areas and a second layer of interconnect (Figure 18). The poly is then etched, and any poly remaining becomes a gate if it is over gate oxide, and interconnect if it is over field oxide. A new layer of oxide is grown over the poly, which will act as an insulator between the poly and the metal interconnect (Figure 19). The poly over the transistor areas is not as wide as the gate oxide. This allows the source and drain diffusions to be ion implanted through the gate oxide. The poly gate itself, along with the field oxide, is used as a mask for implantation. Therefore, the source and drain implants will automatically be aligned to the gate poly, which is what makes this process a self-aligned gate process (Figure 20).

Figure 21 illustrates the steps of cutting contacts into the insulating layer of oxide, so the metal may be connected to gate and field poly, as well as to source and drain implants. A layer of metal is deposited across the entire wafer, and is etched to produce the desired interconnection. Finally, as in metal-gate processing, an insulating layer of oxide is deposited onto the wafer (Figure 22).

Advantages of Silicon-Gate Processing

There are three major ways in which silicon-gate processing reduces parasitic capacitance: recessed field oxide, lower gate overlap capacitance, and shallower junction depths. Figure 23 and Figure 24 are cross sections of metal gate and silicon gate CMOS circuits, respectively. These figures show the parasitic on-chip capacitances (C_1 through C_4) for each type of process.

The N+ and P+ source and drain regions, as well as guard ring regions, in the metal-gate process, have two capacitances associated with them: periphery and area capacitances (C_2 and C_1). These capacitances are associated with the diode junctions between the P+ regions and the N– substrate, as well as the N+ regions and P– well. The finer line widths of silicon-gate CMOS, coupled with the shallower junction depths, act to decrease the size of these parasitic diodes. Capacitance is proportional to diode area, hence the diode area reduction results in a significantly reduced parasitic capacitance in silicon-gate CMOS.

Another origin of unwanted capacitance is the area where the gate overlaps the source and drain regions (C_4). The overlap is much larger in metal-gate processing than in silicon-gate CMOS. This is due to the fact that the metal-gate must be made wider than the channel width to allow for alignment tolerances. In silicon-gate processing, since the gate acts as the mask for the ion implantation of the source and drain regions, there is no alignment error, which results in greatly reduced overlap.

How does the use of polysilicon gates increase the gain of a MOSFET? Polysilicon may be etched to finer line widths than metal, permitting the fabrication of transistors with shorter gate lengths. The equation that describes the gain of a MOSFET is shown below:

$$I = \frac{(\text{Beta})\ (\text{Width})}{2(\text{Length})} [(\text{Gate Voltage}) - (\text{Threshold Voltage})]^2$$

Thus, a decrease in gate length will cause an increase in current drive capability. This, in turn, will allow the transistor to charge a capacitance more rapidly, therefore increasing the gain of the transistor. Also, the gate oxide is thinner for the silicon-gate CMOS process. A thinner gate oxide increases the Beta term in the equation, which further increases gain. Finally, although it is not apparent from the processing cross sections, the transistor threshold (turn on) voltage is lower. This is accomplished by the use of ion implants to adjust the threshold.

There is one more advantage of silicon-gate processing that should be noted: the polysilicon provides for an additional layer of interconnect. This allows three levels of interconnect, which are metal, polysilicon, and the N+ and P+ ion-implanted regions. Having these three levels helps to keep the die area down, since much die area is usually taken up by interconnection.

When all these advantages are summed up, the result is a CMOS technology that produces devices as fast as the equivalent LSTTL device. Figure 25 illustrates a comparison between the MM74HC00 buffered NAND gate and the MM74C00, CD4011B, and DM74LS00 NAND gates. The MM74HC00 is about an order of magnitude faster than the CD4011B buffered NAND gate, and about 5 times faster than the unbuffered MM74C00, at 15 pF. As load capacitance increases, the speed differential between metal-gate and silicon-gate CMOS increases, with the MM74HC00 operating as fast as the DM74S00 at any load capacitance.

Summary

Polycrystalline silicon-gate CMOS has many advantages over metal-gate CMOS. It is faster because on-chip parasitic capacitances are reduced and transistor gains are increased. This is due mainly to a recessed field oxide and a self-aligned gate process. Transistor gains are increased by decreasing transistor lengths and threshold voltages, and increasing beta. Polysilicon also allows for an extra layer of interconnect, which helps to keep die area down.

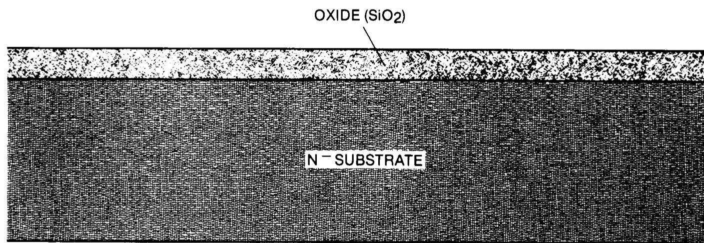

FIGURE 13.
Initial Oxidation, Thermally Grown Silicon Dioxide on N− Silicon Substrate

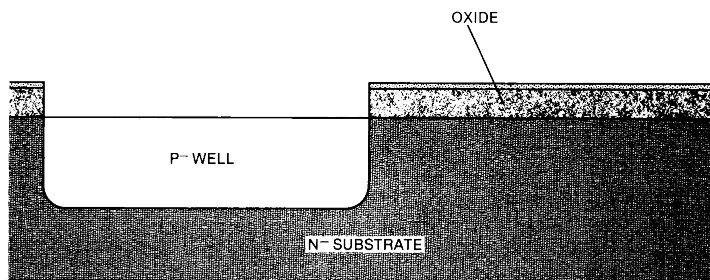

FIGURE 14.
Ion-Implanted P− Tub in which N-Channel Devices will be Located

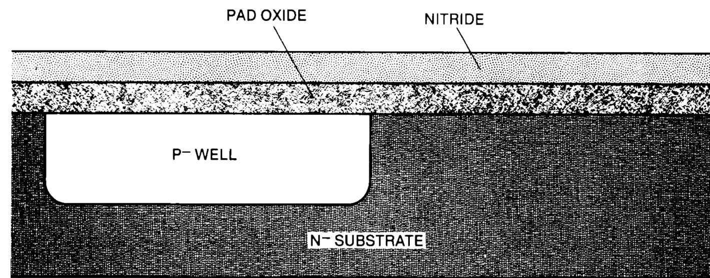

FIGURE 15.
Initial Oxide is Stripped, Pad Oxide is Thermally Grown, and a Layer of Silicon Nitride is Deposited across the Surface of the Wafer

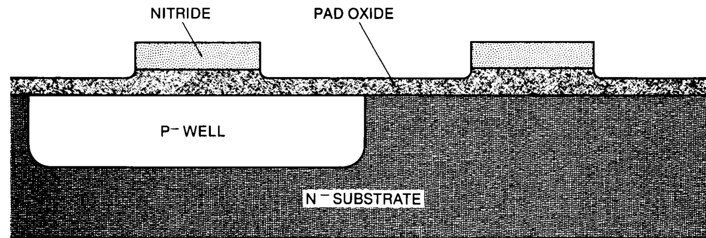

FIGURE 16.
Nitride is Stripped in Areas where Field Oxide is to be Grown.
Areas Covered by Nitride will become Transistor Area

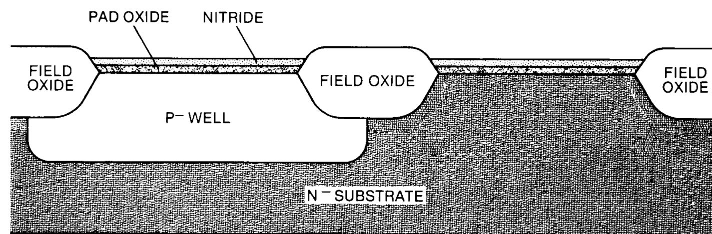

FIGURE 17.
Field Oxide is Thermally Grown. The Nitride Acts as a Barrier to Oxide Growth

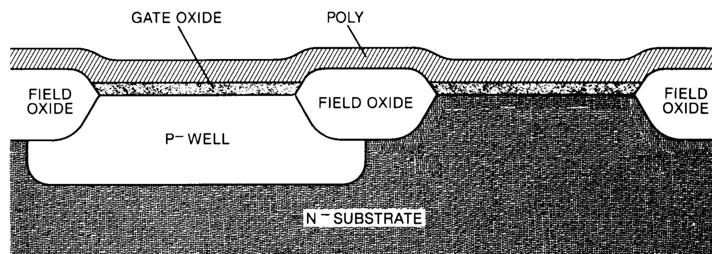

FIGURE 18.
Nitride is Stripped, Pad Oxide is Stripped Over Transistor Areas
and a Thin Gate Oxide is Grown Polycrystalline Silicon is Deposited

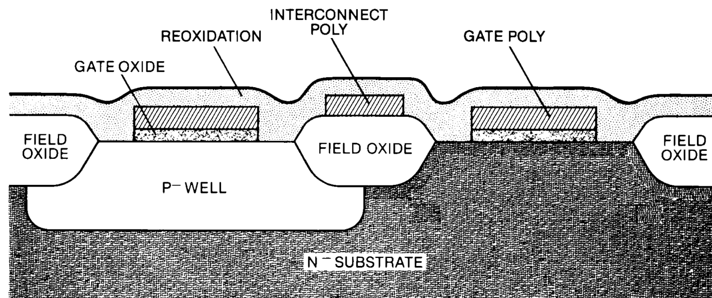

FIGURE 19.
Polysilicon Layer is Etched to Provide Gate and Interconnect Poly Areas. New layer of Oxidation is Grown.

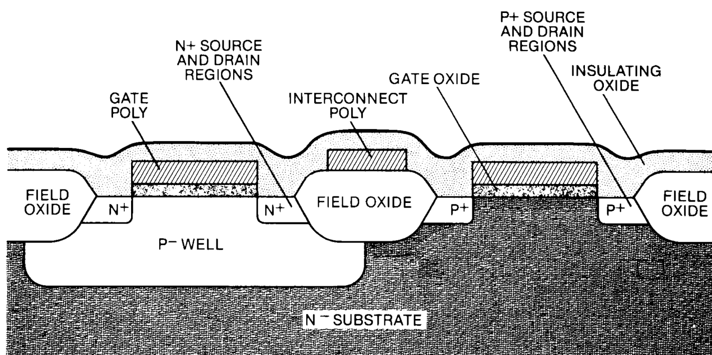

FIGURE 20.
N+ and P+ Source and Drain Regions are Ion Implanted,
and the Re-Oxidation is Grown Thicker to Form an Insulating Layer

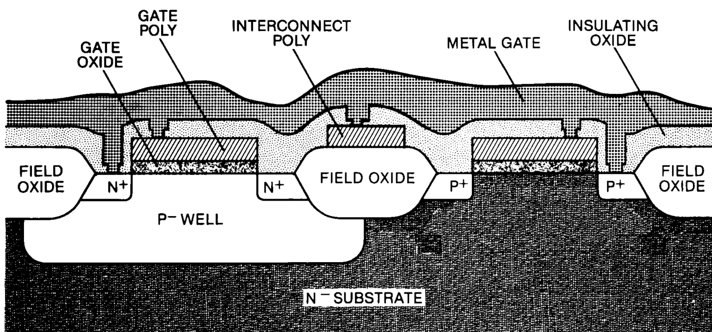

FIGURE 21.
Contact Openings are Cut in the Insulating Oxide,
and a Layer of Metallization is Deposited Across the Entire Wafer

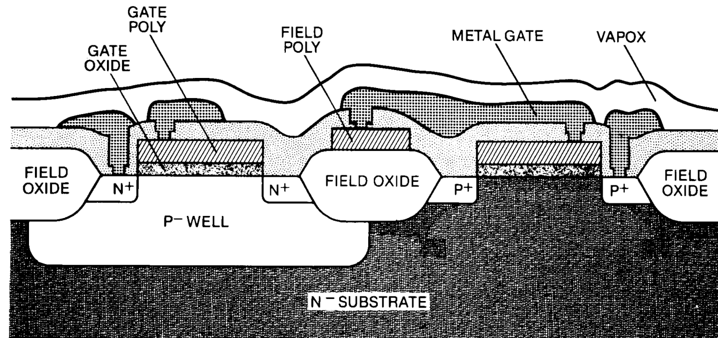

FIGURE 22.
Metal Mask is Etched to Provide Interconnect. Vapox (SiO_2) is Deposited over Entire Surface of Wafer

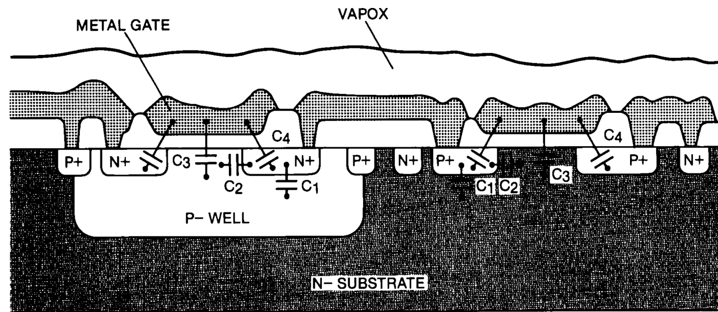

FIGURE 23.
Cross Section of Metal Gate CMOS Process Showing Parasitic On-Chip Capacitances

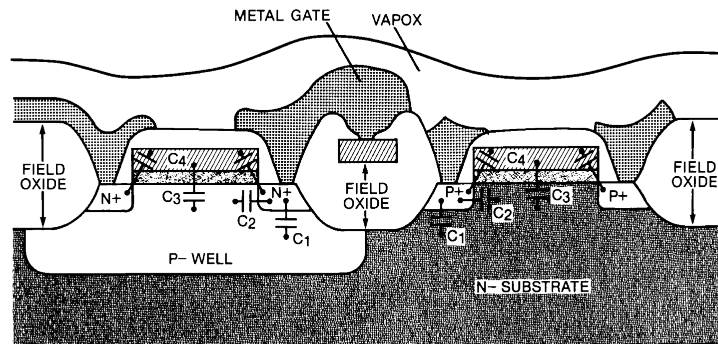

FIGURE 24.
Cross Section of Silicon Gate CMOS Process Showing Parasitic On-Chip Capacitances

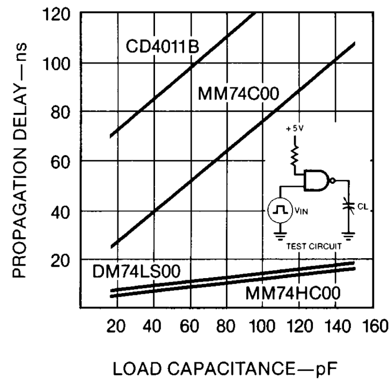

FIGURE 25.
Propagation Delay vs. Load Capacitance for 2-Input NAND Gate

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