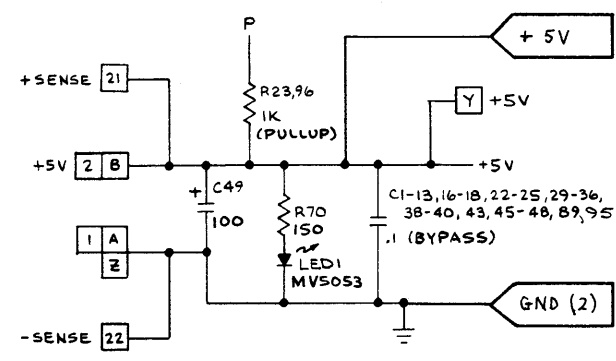
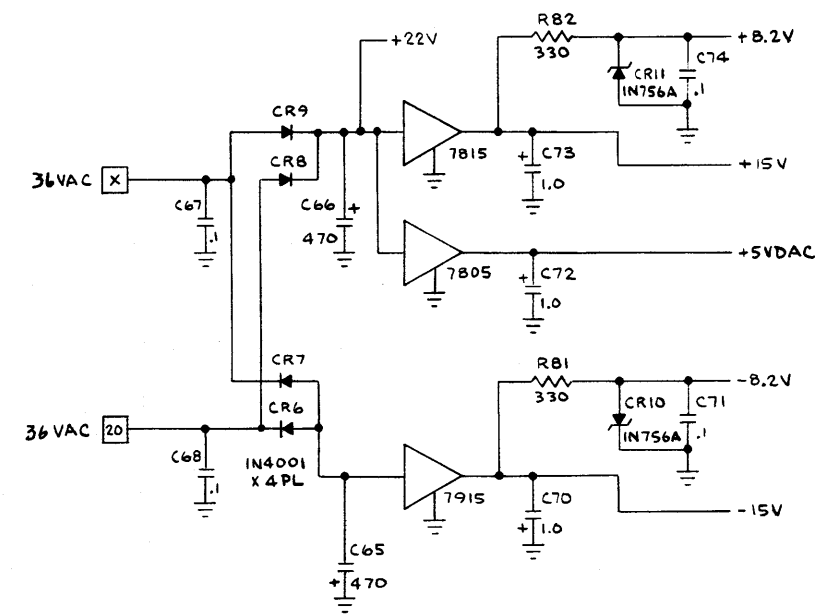


POWER INPUT

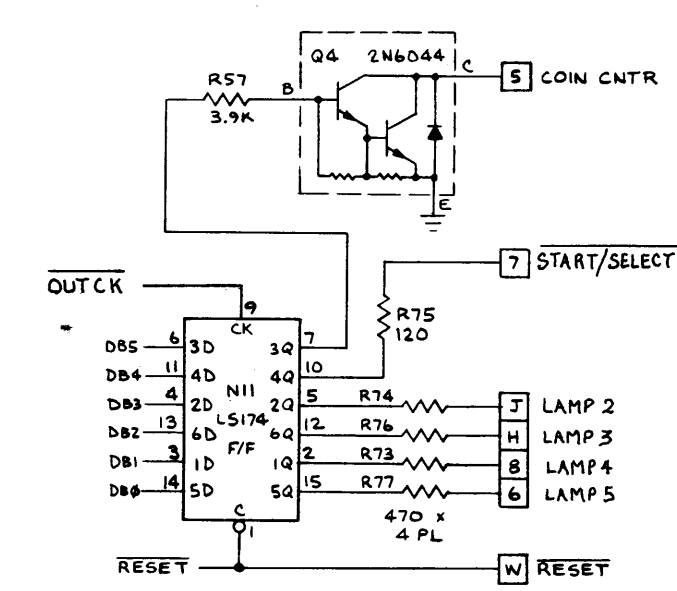


This circuitry consists of the PCB inputs and outputs for the +5 VDC logic power and 36 VAC input to the on board regulators. The +5 VDC inputs and outputs are discussed on the Sheet 1, Side A of this schematic set.

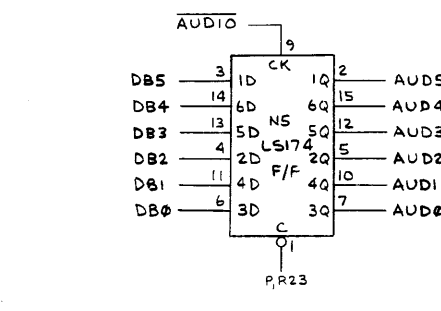
The 36 VAC inputs are received by two full wave rectifiers. Diodes CR6 and CR7 rectify the negative cycle of the input and the 7915 regulates the voltage at -15 VDC. Diodes CR8 and CR9 rectify the positive pulse of the 36 VAC input and the 7815 regulates the voltage at +15 VDC. The 7805 regulates an additional 5 VDC for the DACs. Zener diode CR11 supplies the +8.2 VDC for the sample and hold circuit. The +22V (unregulated) is used to power operational amplifier R7 in the audio output.

LAMP, LED, AND COIN COUNTER OUTPUT

This circuit consists of coin counter driver Q4 and data latch N11, clocked by the microcomputer's address decoder. When the input to Q4 is high, the collector goes low grounding the return of the coin counter in the coin door. When START/SELECT is clocked low, it grounds the START and SELECT LEDs in the control panel. When LAMP2, LAMP3, LAMP4, or LAMP5 is clocked high the appropriate lamp driver transistor is biased into conduction lighting the lamp. LAMP2 is TRAINING MISSION, LAMP3 is CADET MISSION, LAMP4 is PRIME MISSION, and LAMP5 is the COMMAND MISSION lamp.



AUDIO OUTPUT



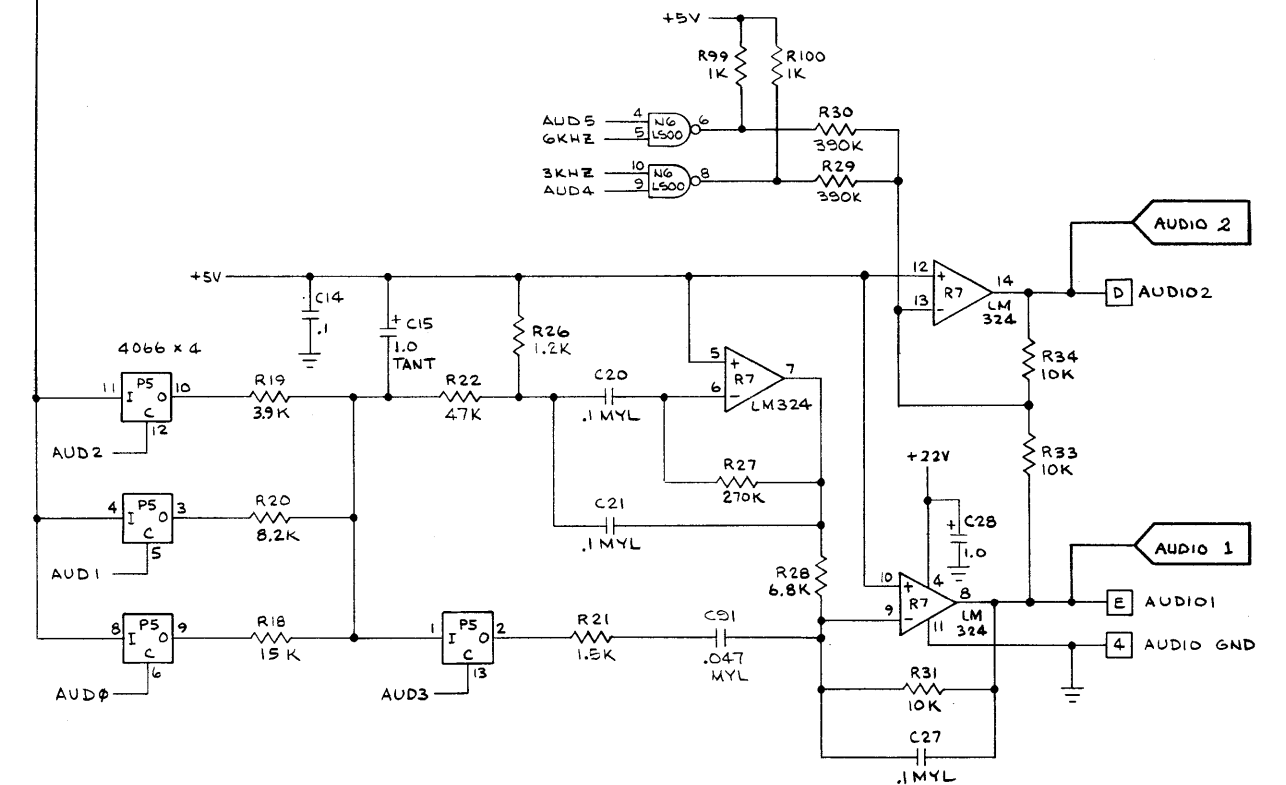
There are four sounds generated in the Lunar Lander game: thrust, explosion, 3 KHz and 6 KHz. All audio control lines are altered by the microcomputer when AUDIO0 from the address decoder, is low. The enabled audio depends on the state of AUDIO0 thru AUD5.

Thrust and explosion audio signals are both developed by random noise from noise generator M6 and M7. The resistive and capacitive network connected to the pin 6 input of operational amplifier R7 is a low pass filter that filters out the high frequencies for the thrust audio. The pins 8 and 14 outputs of op amp R7 develop two equal amplitude, opposite phase signals for the thrust and explosion signals only. Pin 14 of R7 is the output for the 3 KHz and 6 KHz signals.

Thrust passes through analog switches P5 when AUDIO0 and/or AUD1, and/or AUD2 is high. When AUDIO only is high, the thrust audio is at its lowest volume. When AUDIO thru AUD2 are all high, the thrust audio is at its highest volume.

The explosion audio is enabled by AUD3. The volume of this signal is also determined by the state of AUDIO0 thru AUD2.

The 3 KHz audio and 6 KHz audio are enabled by AUD4 and AUD5 respectively. The 3 KHz signal is used as an audio warning of low fuel and indicator of proper ROM and RAM operation during Self-Test. The 6 KHz signal is used as the coin door SLAM audio and during Self-Test to indicate proper operation of control panel and coin door switch inputs and improper operation of ROM and RAM.



OPTION SWITCH SETTINGS

Your game will contain either of two different sets of program ROM/PROMs. Check your game to see if it contains -01 or -02 program ROM/PROMs; then refer to the appropriate table below to determine your game's option switch settings.

Option Switch Settings with -01 ROMs on Printed Circuit Board

Switch settings of 8-Toggle DIP Switch (located at position P8 on the game PCB)								Results
8	7	6	5	4	3	2	1	
On	On							450 fuel units per coin
On	Off							600 fuel units per coin
On	On							750 fuel units per coin \$
Off	On							900 fuel units per coin
		TOGGLE						Free play
		On						Coined play as determined by toggles 7 & 8 \$
			Off	Off				* German instructions on screen
			Off	On				* Spanish instructions on screen
			On	Off				* French instructions on screen
			On	On				English instructions on screen \$
		UNUSED						Right coin mechanism (as you face the game) registers:
					On	On		1 credit per coin \$
					On	Off		4 credits per coin
					Off	On		5 credits per coin
					Off	Off		6 credits per coin
					On	On		Right coin mechanism (as you face the game) registers:
					On	Off		1 credit per coin \$
					On	On		4 credits per coin
					Off	On		5 credits per coin
					Off	Off		6 credits per coin
					On	On		Right coin mechanism always registers 1 credit per coin)

Option Switch Settings with -02 ROMs on Printed Circuit Board

Switch Settings of 8-Toggle DIP Switch (located at position P8 on the game PCB)								Results
8	7	6	5	4	3	2	1	
On	On							450 fuel units per coin
On	Off							600 fuel units per coin
On	On							750 fuel units per coin \$
Off	On							900 fuel units per coin
		TOGGLE						Free play
		On						Coined play as determined by toggles 7 & 8 \$
			Off	Off				* German instructions on screen
			Off	On				* Spanish instructions on screen
			On	Off				* French instructions on screen
			On	On				English instructions on screen \$
		UNUSED						Right coin mechanism (as you face the game) registers:
					Off	Off		1 credit per coin \$
					On	On		4 credits per coin
					On	Off		5 credits per coin
					Off	On		6 credits per coin
					On	On		Right coin mechanism always registers 1 credit per coin)

*Important: When changing any instruction language switches, do not worry if the six phrases at the top of the screen still remain in the previous language; and only the fuel units per coin phrase has immediately changed. Simply wait until the lunar lander "crashes" (in the attract mode), then the language will reset completely. In free play, the language will not reset until the game's start button is pressed.

\$ Indicates settings made at the factory and/or recommended settings.

The video output circuit consists of three individual circuits: X axis, Y axis, and Z axis video output circuits. The X axis and Y axis video output circuits consist of a digital-to-analog (DAC) converter, current-to-voltage converter, sample and hold, sample and hold control, and amplifier. The Z axis video output circuit consists of a shift register and a summer.

X and Y Outputs

The DACs (B11 and D11) each receive binary numbers from the vector generator's position counters outputs. These numbers represent the location of the beam on the monitor. For the X axis, the number is 0 to 1,023, where 0 is at the far left of the monitor screen, 512 at the center, and 1,023 is at the far right. For the Y axis, the number is from 0 to 768, where 0 is at the bottom of the monitor screen, 384 is the center, and 768 is the top.

The DACs convert these binary number inputs to current output. The DAC's current output is applied to the pin 6 inputs of current-to-voltage converters A12 and C12. The pin 5 inputs ensure that the null points (resting point on the monitor screen) of the pin 7 outputs are 512 for the X axis and 384 for the Y axis.

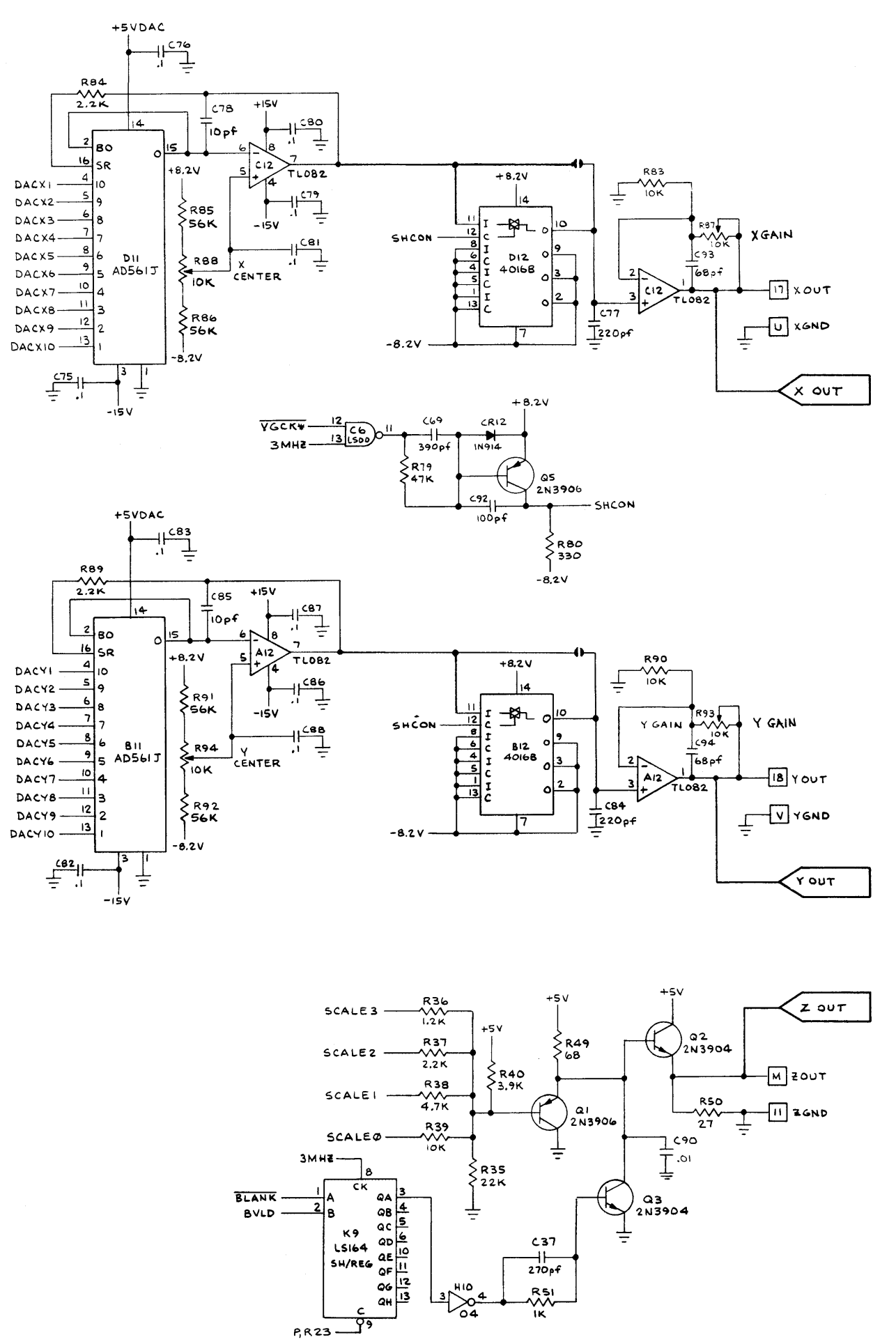
From the current-to-voltage converters, the signal is fed to the sample and hold circuits. Analog switches B12 and D12 pass the voltages to sample and hold capacitors C77 and C84. This is controlled by SHCON (sample and hold control). SHCON is derived by gating 3 MHz from the microcomputer clock circuitry and VGCK* from the vector generator's state generator. The result of these inputs ensure that the pin 7 outputs of voltage-to-current converters A12 and C12 have sufficiently stabilized before being applied to the sample and hold capacitors. The output swing of SHCON is -8 to +8 VDC. When SHCON is high, the voltage charges or discharges the sample and hold capacitor to the voltage value. The voltages are then applied to the second stages of A12 and C12 for an impedance matched output to the X and Y inputs of the monitor. Since the monitor doesn't have field adjustable X and Y gains, the gains are adjusted by variable resistors R87 and R93.

Z Output

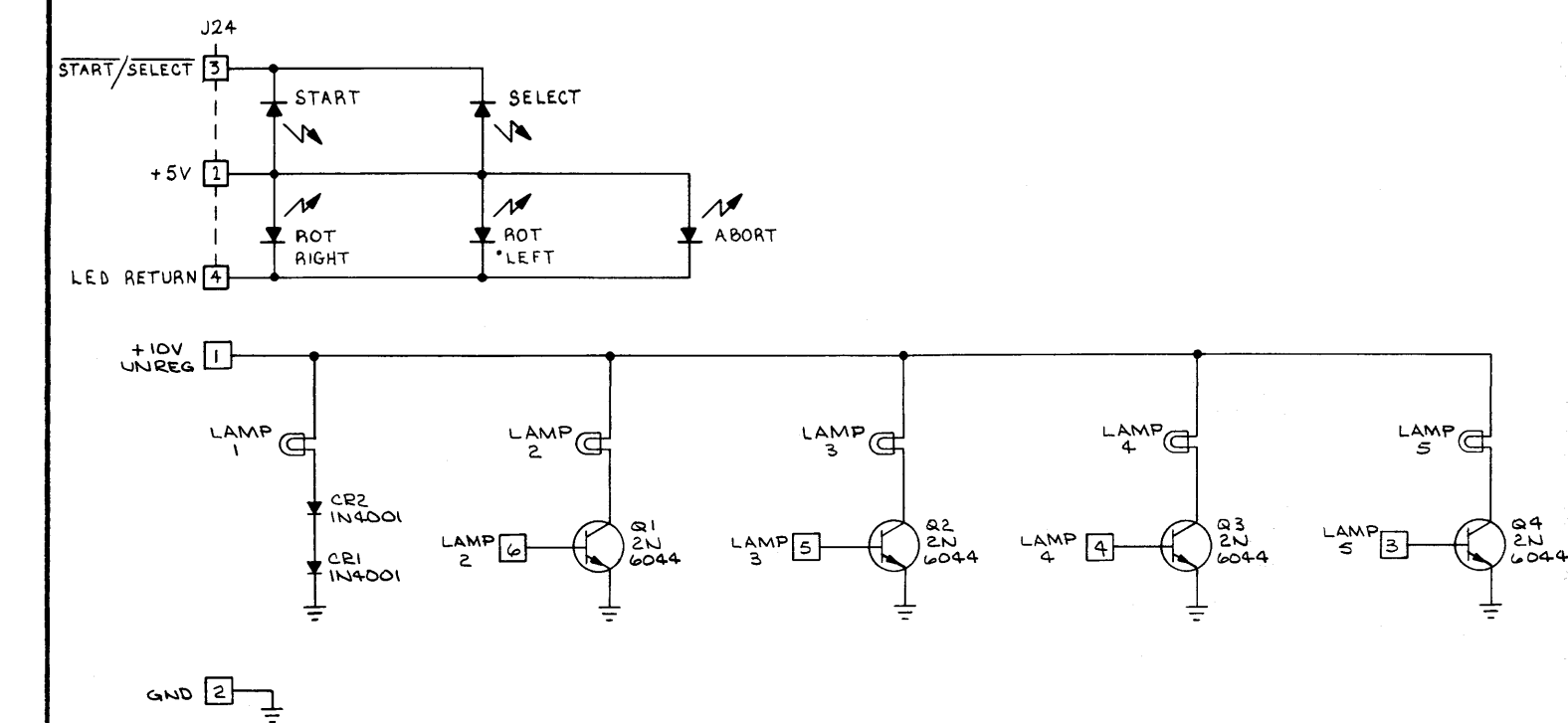
The Z axis video output receives six inputs. BVLD (beam valid), from the output of the vector generator's position counters, tells the Z axis to draw the line. BLANK (vector line blank), from the vector generator's state machine, tells the Z axis to stop drawing a line. SCALE0 thru SCALE3 (grey level shading scale), from the output of the vector generator's data latch, tells the Z axis the grey level shading of the line that is being drawn on the monitor.

When BVLD and BLANK are both high, a high is clocked through shift register K9 that turns transistor Q3 off. This allows the scale inputs to be passed through transistor Q2. When BLANK goes low, a low is clocked through K9, transistor Q3 turns on, and the signal is grounded at the base of transistor Q2.

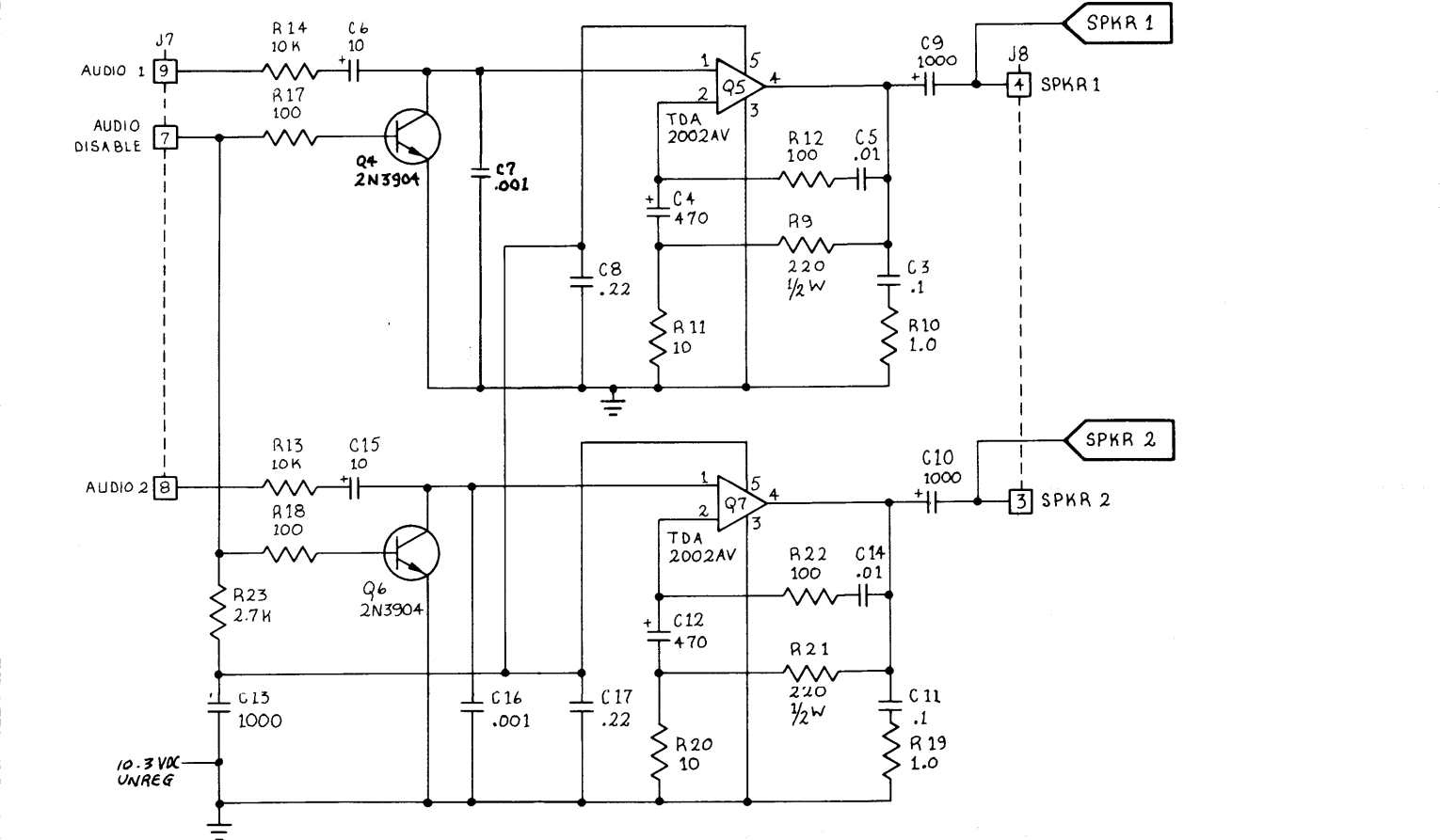
The scale inputs at the base of transistor Q1 determines Q1's emitter voltage, during the line draw period. The SCALE0 thru SCALE3 resistors R36 thru R39, resistor R35, and resistor R40 result in a range of about +1.0 VDC when all are low and +4.0 VDC when all are high. The emitter of Q1 follows at about +1.7 to 4.7 VDC, while the emitter of transistor Q2 follows at about +1.0 to 4.0 VDC. This output is applied to the Z input of the monitor. Since there are brightness and contrast controls in the monitor, there are no adjustments in this circuit.



PART OF CONTROL PANEL



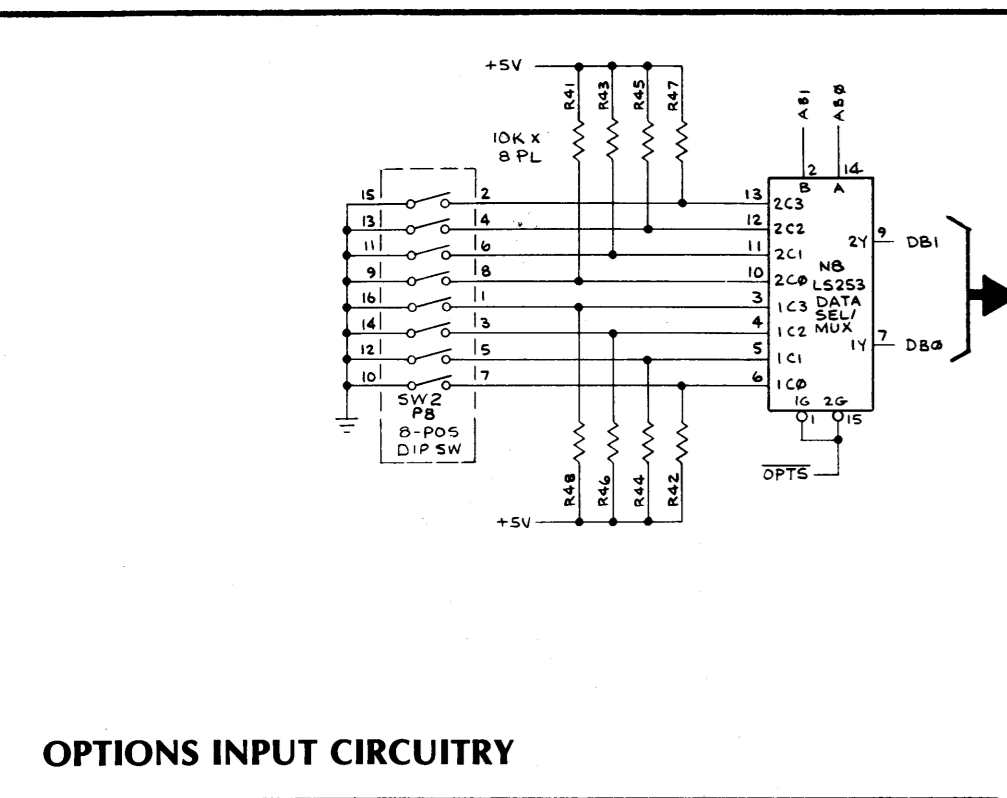
PART OF REGULATOR/AUDIO PCB



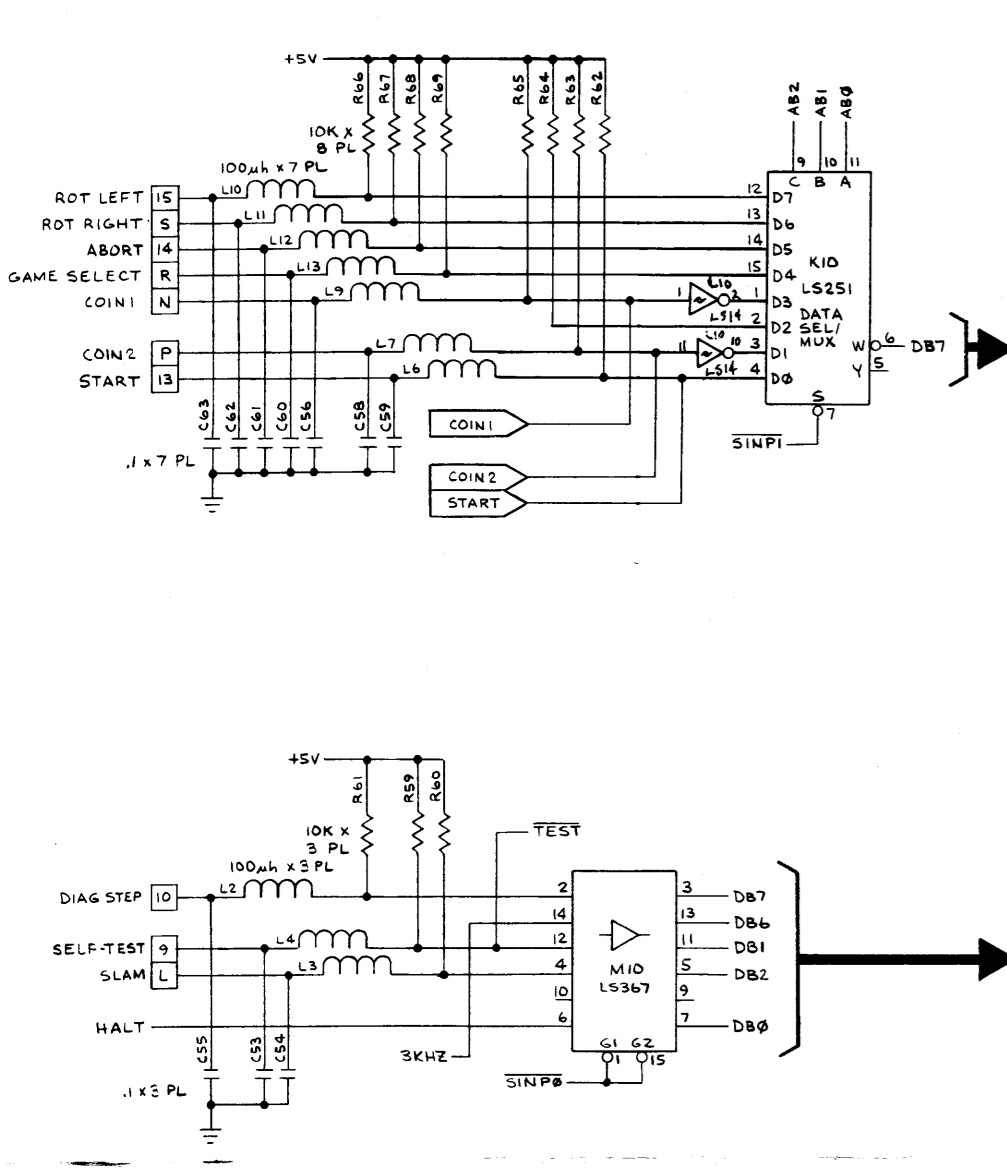
NOTE: AUDIO AMPLIFIER IS PART OF REGULATOR/AUDIO PCB AND IS REPEATED ON SHEET 1, SIDE A.

SEE MONITOR MANUAL FOR MONITOR SCHEMATIC DIAGRAM

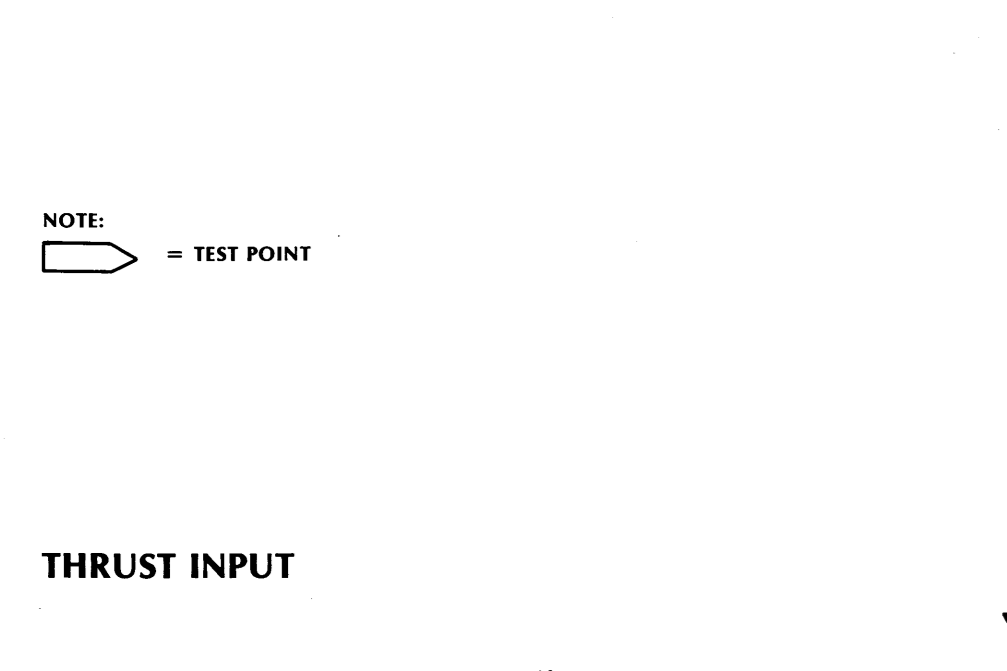
© 1979 Atari, Inc.



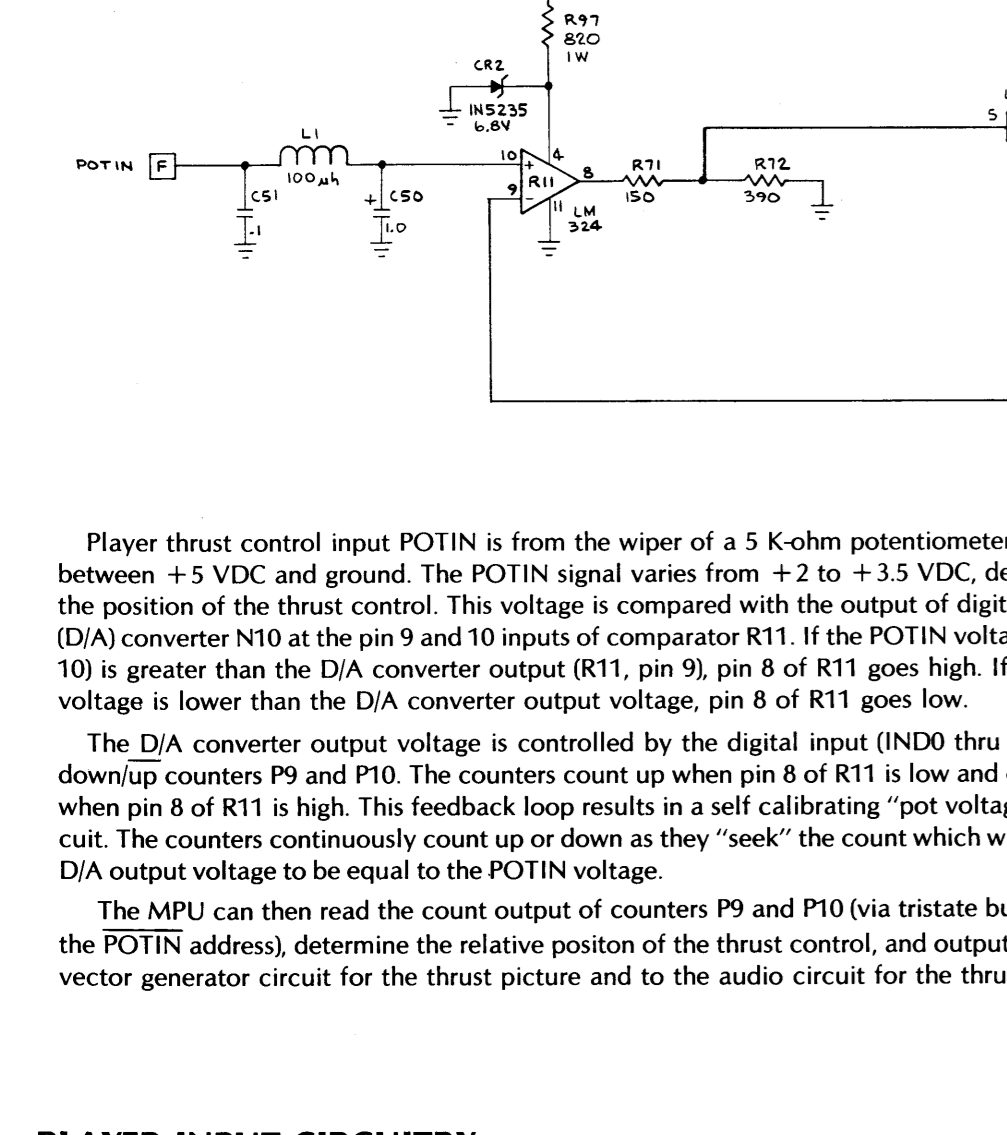
The game option switches are read by the MPU when OPTS (option switch enable) is low. Switch toggles to be read are selected by AB0 and AB1 from the MPU. Switch toggles 1, 3, 6, and 7 are read on data line DB0 and toggles 2, 4, 6 and 8 are read on DB1. Toggle inputs are "on" when pulled to ground.



The coin door and control panel switches are read by the MPU when SINPT (switch input one enable) is low. Switches to be read are selected by AB0 thru AB2 from the MPU. All inputs are read on data line DB7. Switch inputs are "on" when pulled to ground.



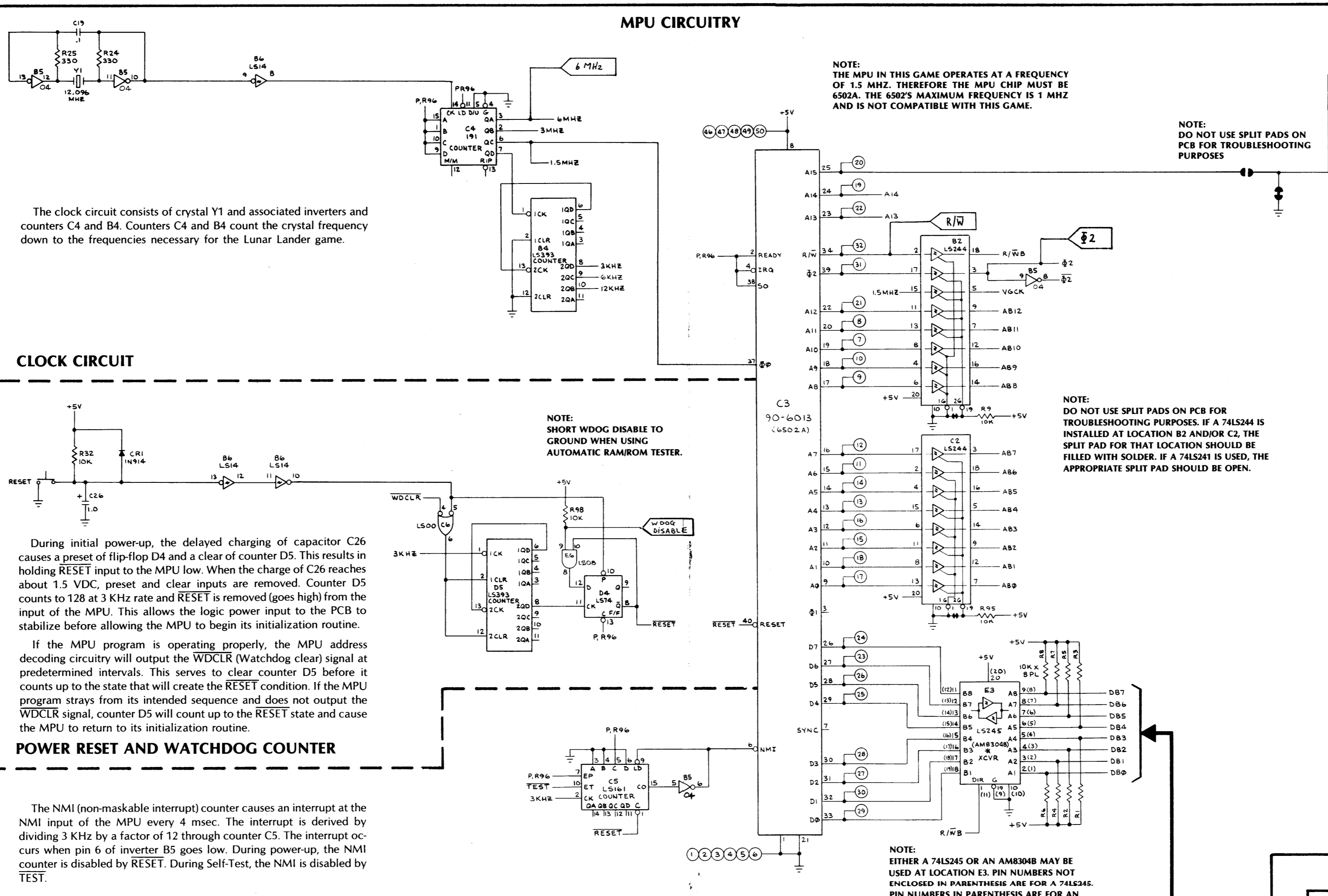
DIAG STEP (diagnostic step), 3 KHz, SELF-TEST, SLAM, and HALT inputs are read by the MPU when SINPT (switch input one enable) is low. Inputs are directly read by the MPU on data lines DB7, DB6, DB1, DB2, and DB0 respectively. Switch inputs are active when pulled to ground. DIAG, STEP, 3 KHz, and SELF-TEST are signals read by the MPU to initiate and control the game's self-test procedure. SLAM is a signal read by the MPU to indicate the status of the antismash switch mounted on the coin door. The MPU reads HALT to determine the state of the vector generator.



Player thrust control input POTIN is from the wiper of a 5 K-ohm potentiometer connected between +5 VDC and ground. The POTIN signal varies from +2 to +3.5 VDC, depending on the position of the thrust control. This voltage is compared with the output of digital-to-analog (D/A) converter N10 at the pin 9 and 10 inputs of comparator R11. If the POTIN voltage (R11, pin 10) is greater than the D/A converter output (R11, pin 9), pin 8 of R11 goes high. If the POTIN voltage is lower than the D/A converter output voltage, pin 8 of R11 goes low.

The D/A converter output voltage is controlled by the digital input (IND0 thru IND7) from down/up counters P9 and P10. The counters count up when pin 8 of R11 is low and count down when pin 8 of R11 is high. This feedback loop results in a self-calibrating "pot voltage seek" circuit. The counters continuously count up or down as they "seek" the count which will cause the D/A output voltage to be equal to the POTIN voltage.

The MPU can then read the count output of counters P9 and P10 (via tristate buffer N9) and the POTIN address, determine the relative position of the thrust control, and output data to the vector generator circuit for the thrust picture and to the audio circuit for the thrust sound.



The clock circuit consists of crystal Y1 and associated inverters and counters C4 and B4. Counters C4 and B4 count the crystal frequency down to the frequencies necessary for the Lunar Lander game.

CLOCK CIRCUIT

POWER RESET AND WATCHDOG COUNTER

The NMI (non-maskable interrupt) counter causes an interrupt at the NMI input of the MPU every 4 msec. The interrupt is derived by dividing 3 KHz by a factor of 12 through counter C5. The interrupt occurs when pin 6 of inverter B5 goes low. During power-up, the NMI counter is disabled by RESET. During Self-Test, the NMI is disabled by TEST.

NMI COUNTER

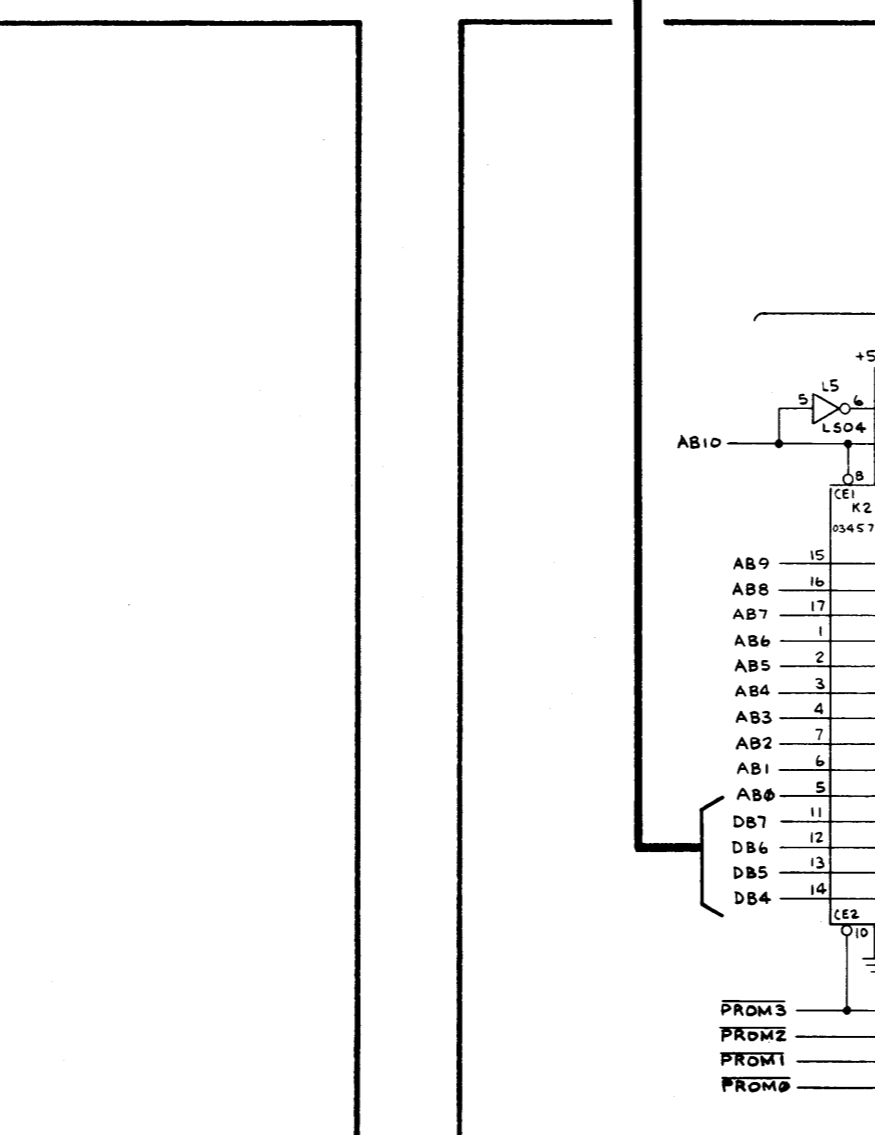
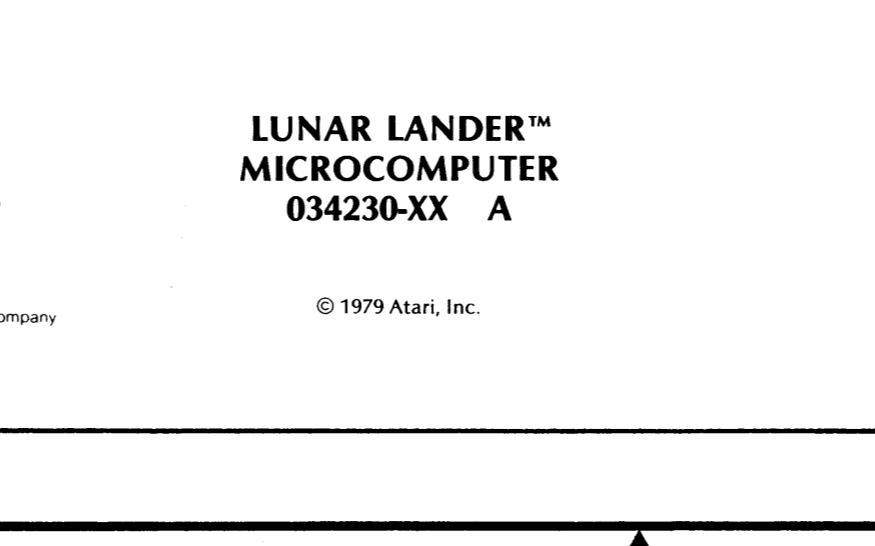
RAM CIRCUITRY

CLOCK CIRCUIT

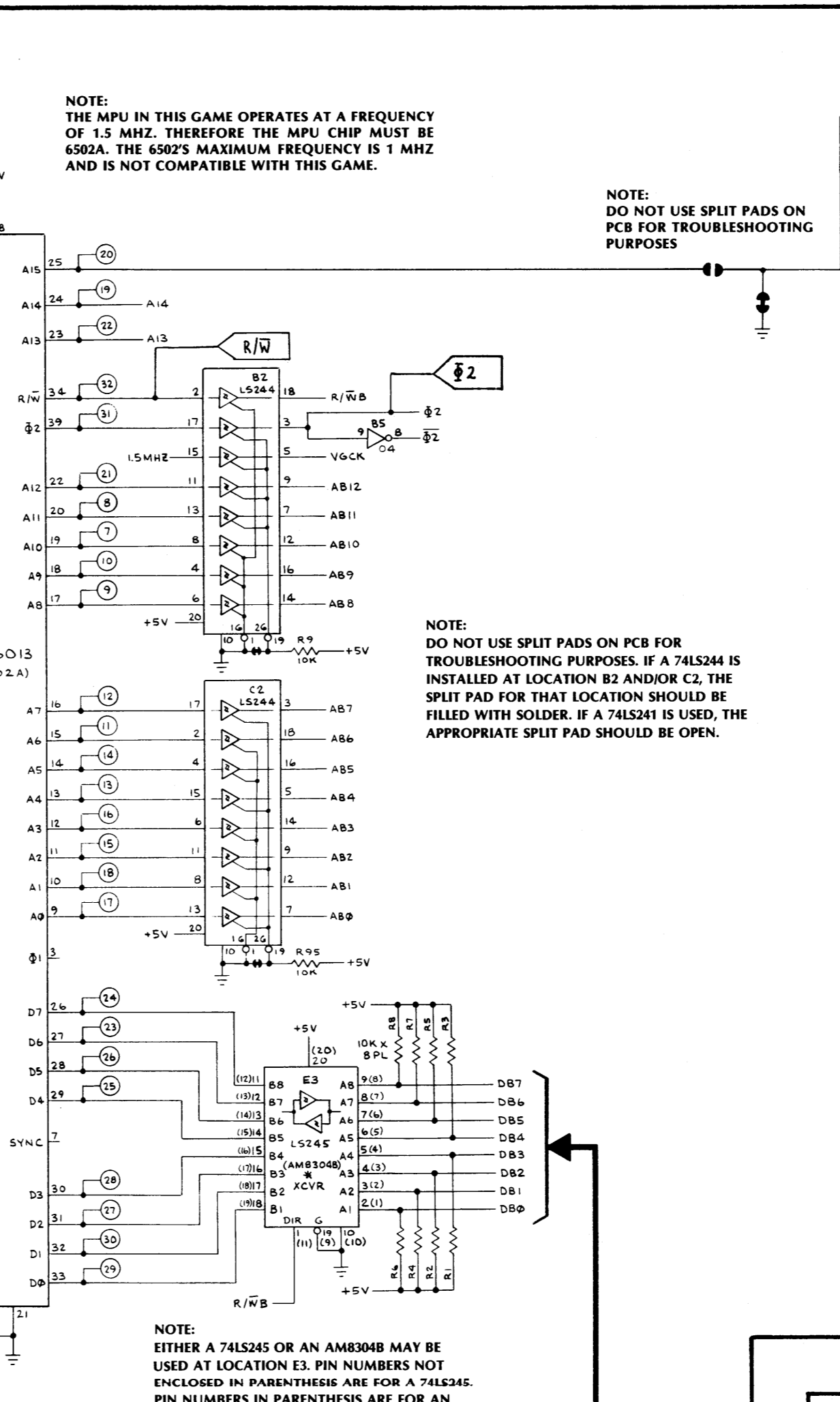
POWER RESET AND WATCHDOG COUNTER

NMI COUNTER

RAM CIRCUITRY



RAM CIRCUITRY



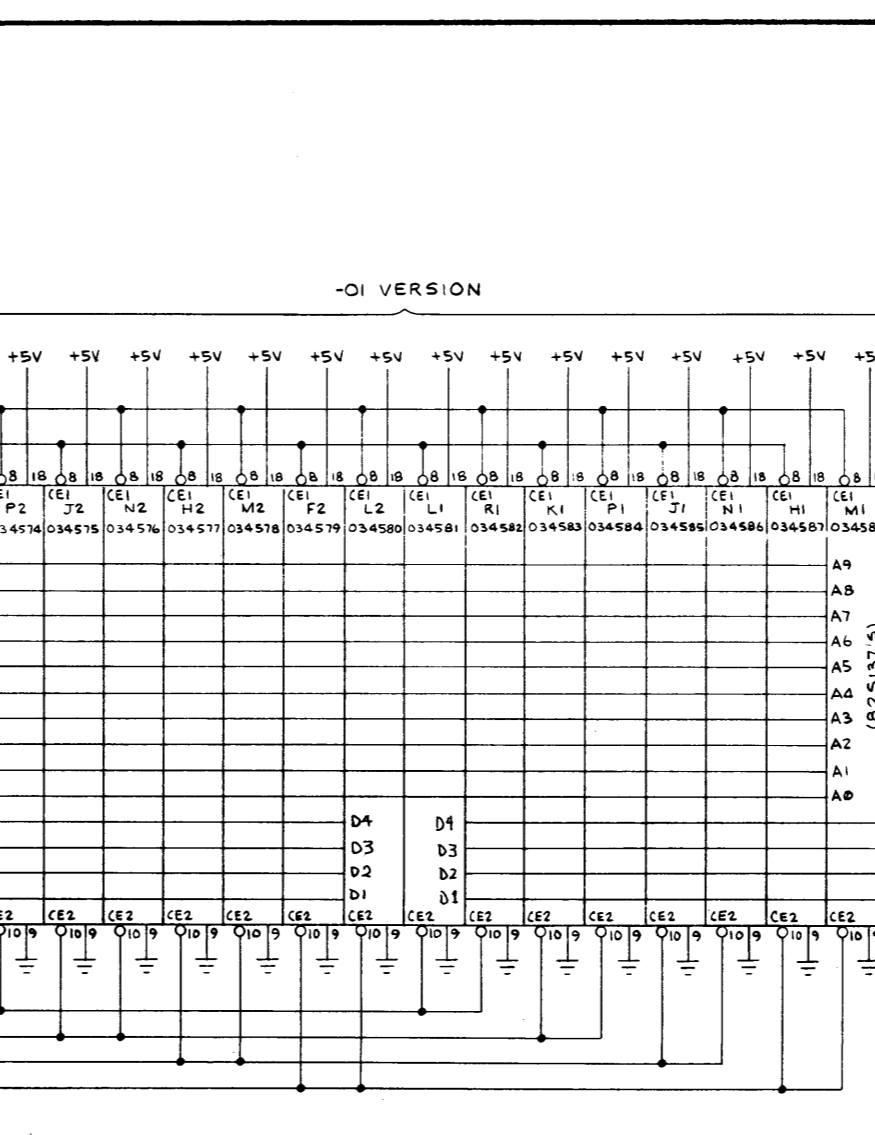
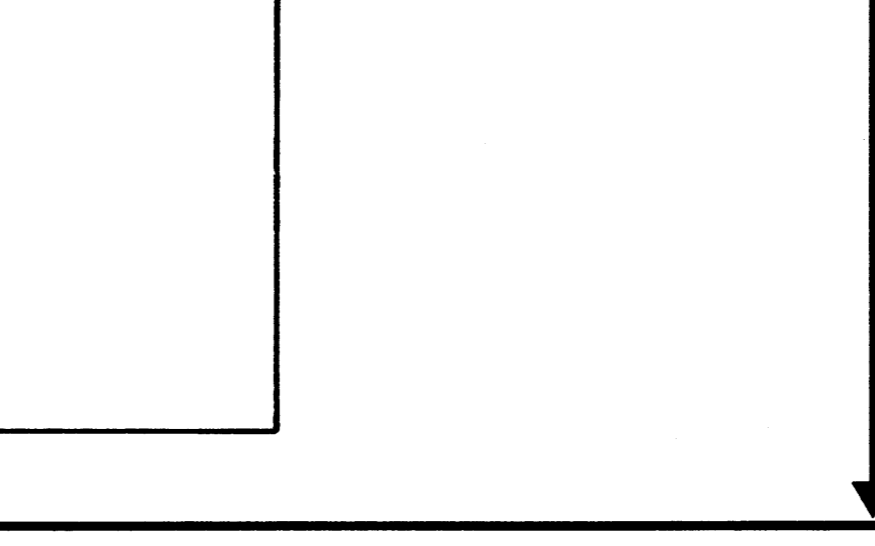
The address decoder performs the function of turning on or enabling the appropriate circuitry at the critical time, so that information can be transferred back and forth between the game circuitry and the MPU. The memory map below is for the Lunar Lander game.

ADDRESS DECODING CIRCUITRY

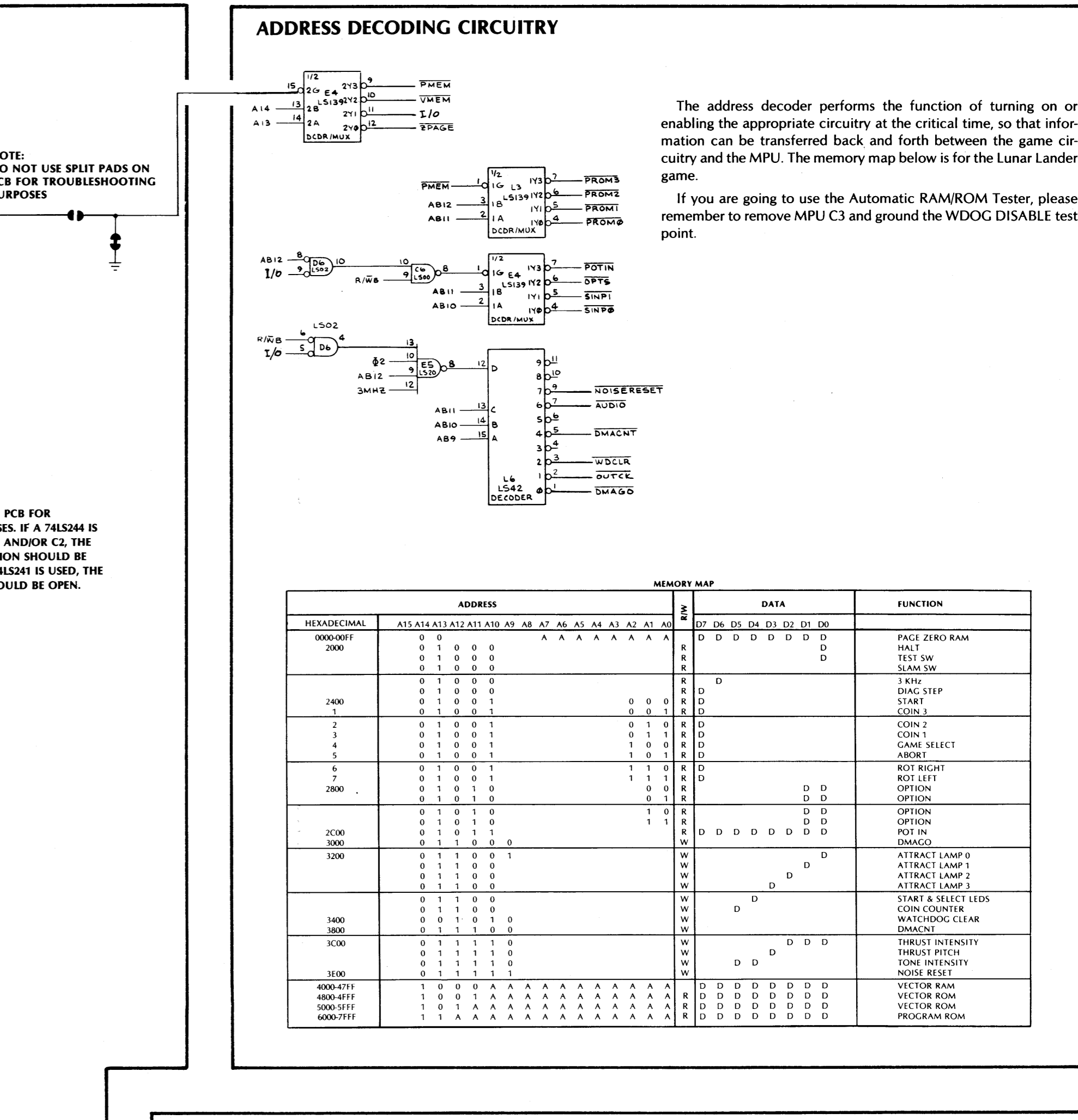
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MEMORY MAP

HEXADCEMAL	ADDRESS	DATA	FUNCTION
0000-000F	0 0 0 0 0 0 0 0	A A A A A A A A	PAGE ZERO RAM
0000	0 0 0 0 0 0 0 0	D D D D D D D D	HALT
0001	0 0 0 0 0 0 0 0	D D D D D D D D	TEST SW
0002	0 0 0 0 0 0 0 0	D D D D D D D D	SLAM SW
2400	0 1 0 0 0 0 0 0	R D	3 KHz
2	0 1 0 0 0 0 0 0	R D	DICK SWEEP
3	0 1 0 0 0 0 0 0	R D	START
4	0 1 0 0 0 0 0 0	R D	COIN-2
5	0 1 0 0 0 0 0 0	R D	COIN-1
6	0 1 0 0 0 0 0 0	R D	GAME SELECT
7	0 1 0 0 0 0 0 0	R D	ABORT
8	0 1 0 0 0 0 0 0	R D	ROT RIGHT
9	0 1 0 0 0 0 0 0	R D	ROT LEFT
2000	0 1 0 0 0 0 0 0	R D	OPTION
3000	0 1 0 0 0 0 0 0	R D	OPTION
4000-4FFF	0 1 0 0 0 0 0 0	R D	OPTION
4800-4FFF	0 1 0 0 0 0 0 0	R D	OPTION
5000-5FFF	0 1 0 0 0 0 0 0	R D	OPTION
6000-7FFF	0 1 0 0 0 0 0 0	R D	OPTION



RAM CIRCUITRY



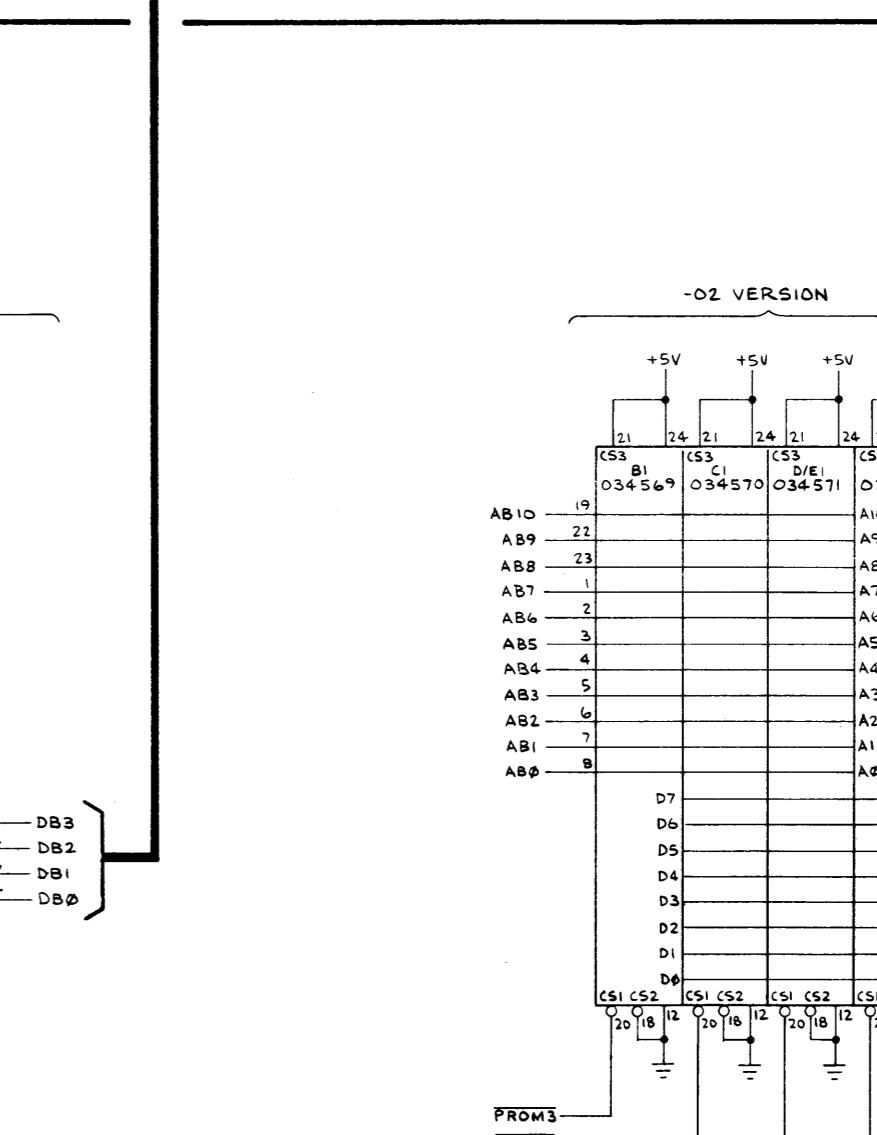
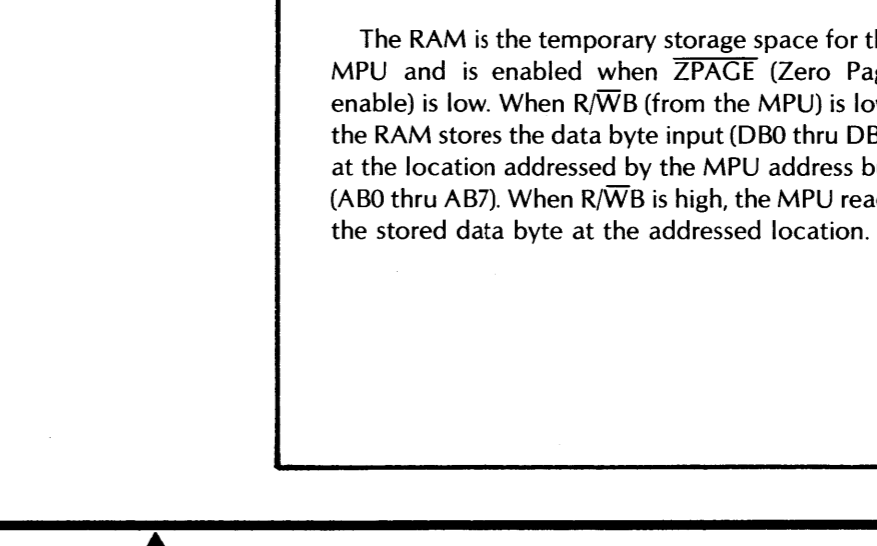
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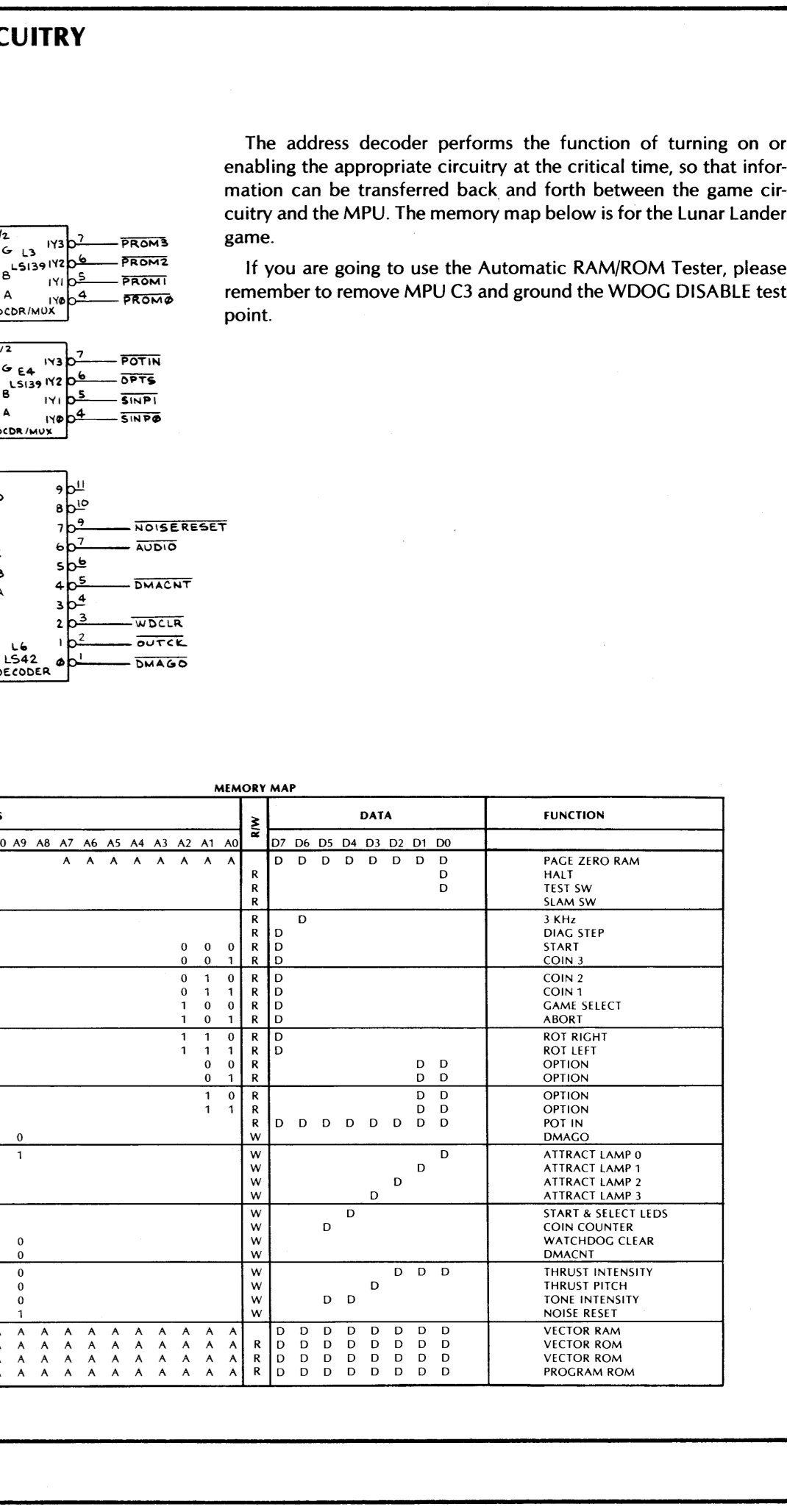
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0001	0 0 0 0 0 0 0 0	D D D D D D D D	TEST SW
0002	0 0 0 0 0 0 0 0	D D D D D D D D	SLAM SW
2400	0 1 0 0 0 0 0 0	R D	3 KHz
2	0 1 0 0 0 0 0 0	R D	DICK SWEEP
3	0 1 0 0 0 0 0 0	R D	START
4	0 1 0 0 0 0 0 0	R D	COIN-2
5	0 1 0 0 0 0 0 0	R D	COIN-1
6	0 1 0 0 0 0 0 0	R D	GAME SELECT
7	0 1 0 0 0 0 0 0	R D	ABORT
8	0 1 0 0 0 0 0 0	R D	ROT RIGHT
9	0 1 0 0 0 0 0 0	R D	ROT LEFT
2000	0 1 0 0 0 0 0 0	R D	OPTION
3000	0 1 0 0 0 0 0 0	R D	OPTION
4000-4FFF	0 1 0 0 0 0 0 0	R D	OPTION
4800-4FFF	0 1 0 0 0 0 0 0	R D	OPTION
5000-5FFF	0 1 0 0 0 0 0 0	R D	OPTION
6000-7FFF	0 1 0 0 0 0 0 0	R D	OPTION



RAM CIRCUITRY



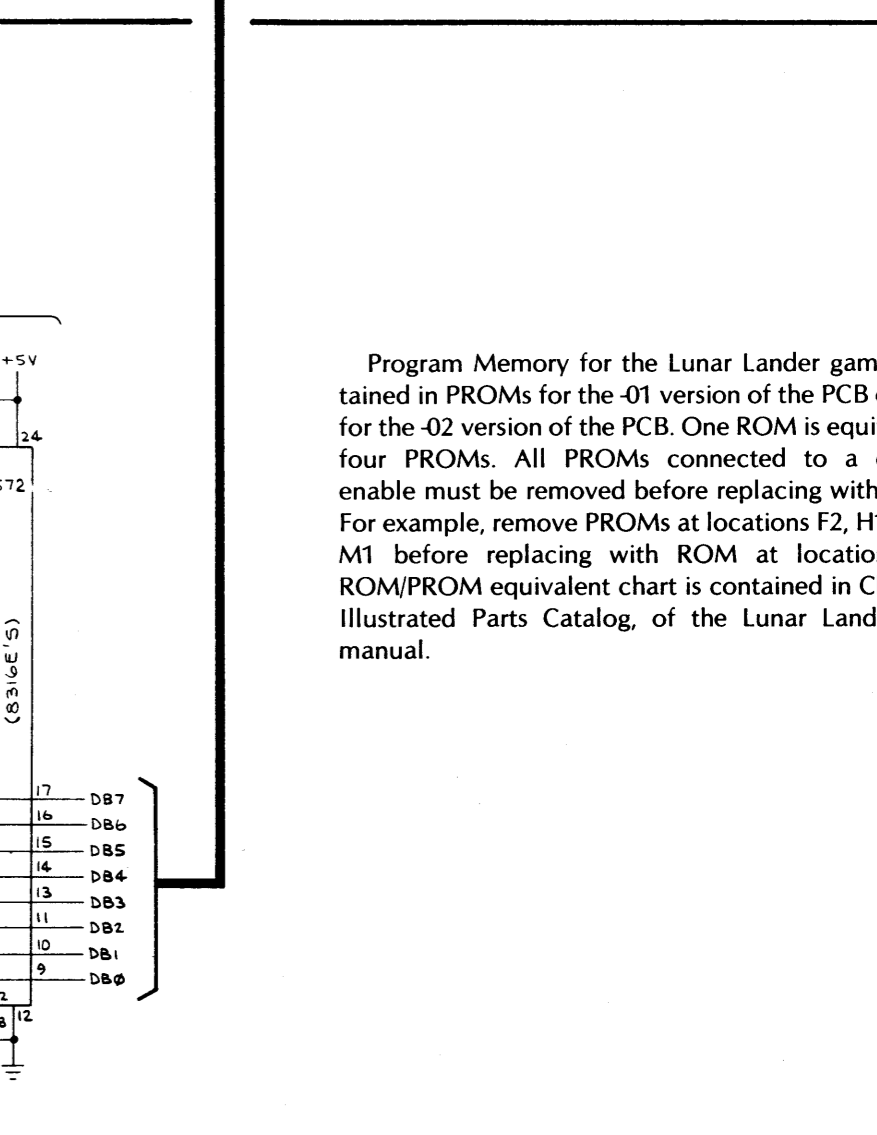
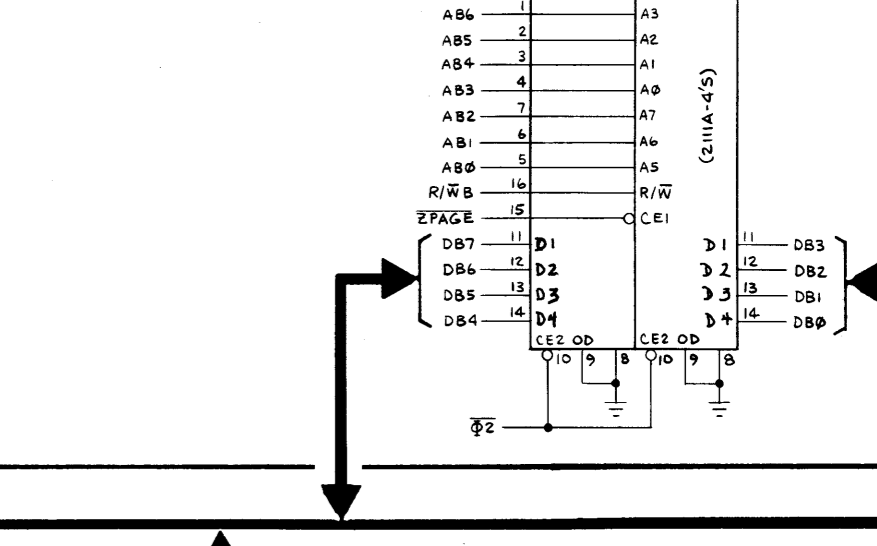
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ADDRESS DECODING CIRCUITRY

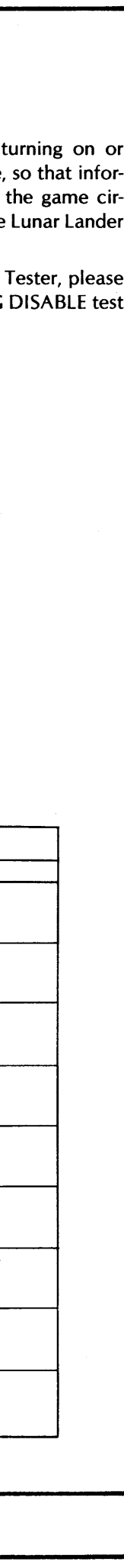
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2400	0 1 0 0 0 0 0 0	R D	3 KHz
2	0 1 0 0 0 0 0 0	R D	DICK SWEEP
3	0 1 0 0 0 0 0 0	R D	START
4	0 1 0 0 0 0 0 0	R D	COIN-2
5	0 1 0 0 0 0 0 0	R D	COIN-1
6	0 1 0 0 0 0 0 0	R D	GAME SELECT
7	0 1 0 0 0 0 0 0	R D	ABORT
8	0 1 0 0 0 0 0 0	R D	ROT RIGHT
9	0 1 0 0 0 0 0 0	R D	ROT LEFT
2000	0 1 0 0 0 0 0 0	R D	OPTION
3000	0 1 0 0 0 0 0 0	R D	OPTION
4000-4FFF	0 1 0 0 0 0 0 0	R D	OPTION
4800-4FFF	0 1 0 0 0 0 0 0	R D	OPTION
5000-5FFF	0 1 0 0 0 0 0 0	R D	OPTION
6000-7FFF	0 1 0 0 0 0 0 0	R D	OPTION



RAM CIRCUITRY



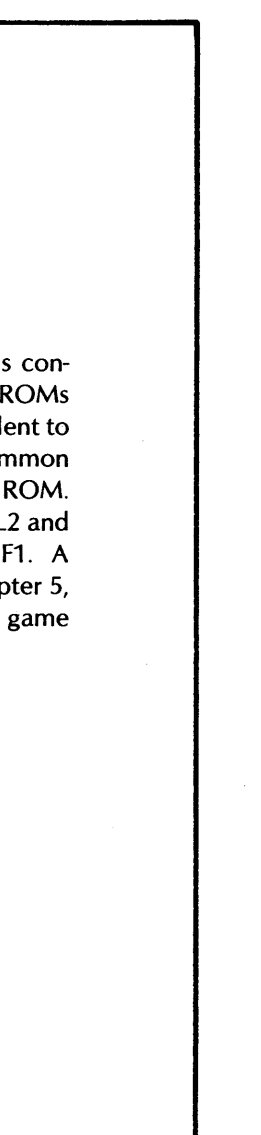
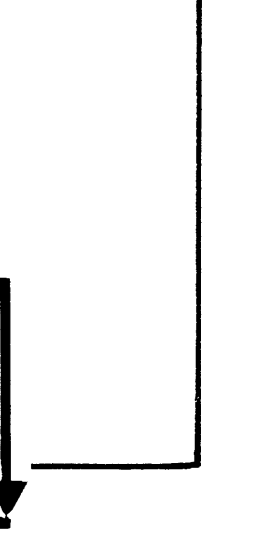
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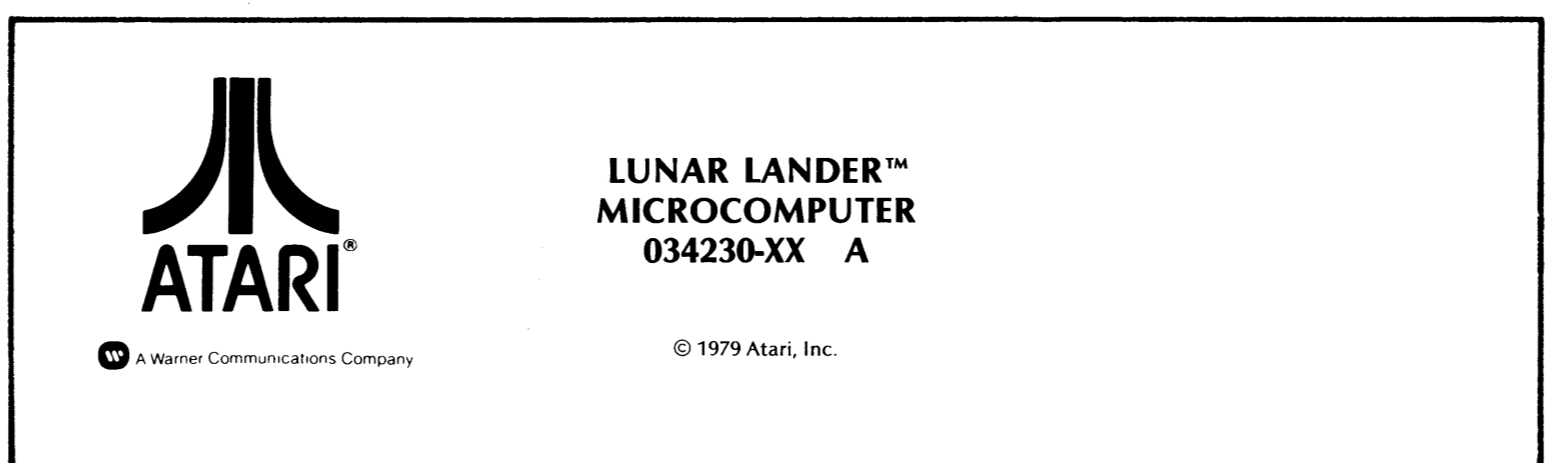
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0000	0 0 0 0 0 0 0 0	D D D D D D D D	HALT
0001	0 0 0 0 0 0 0 0	D D D D D D D D	TEST SW
0002	0 0 0 0 0 0 0 0	D D D D D D D D	SLAM SW
2400	0 1 0 0 0 0 0 0	R D	3 KHz
2	0 1 0 0 0 0 0 0	R D	DICK SWEEP
3	0 1 0 0 0 0 0 0	R D	START
4	0 1 0 0 0 0 0 0	R D	COIN-2
5	0 1 0 0 0 0 0 0	R D	COIN-1
6	0 1 0 0 0 0 0 0	R D	GAME SELECT
7	0 1 0 0 0 0 0 0	R D	ABORT
8	0 1 0 0 0 0 0 0	R D	ROT RIGHT
9	0 1 0 0 0 0 0 0	R D	ROT LEFT
2000	0 1 0 0 0 0 0 0	R D	OPTION
3000	0 1 0 0 0 0 0 0	R D	OPTION
4000-4FFF	0 1 0 0 0 0 0 0	R D	OPTION
4800-4FFF	0 1 0 0 0 0 0 0	R D	OPTION
5000-5FFF	0 1 0 0 0 0 0 0	R D	OPTION
6000-7FFF	0 1 0 0 0 0 0 0	R D	OPTION

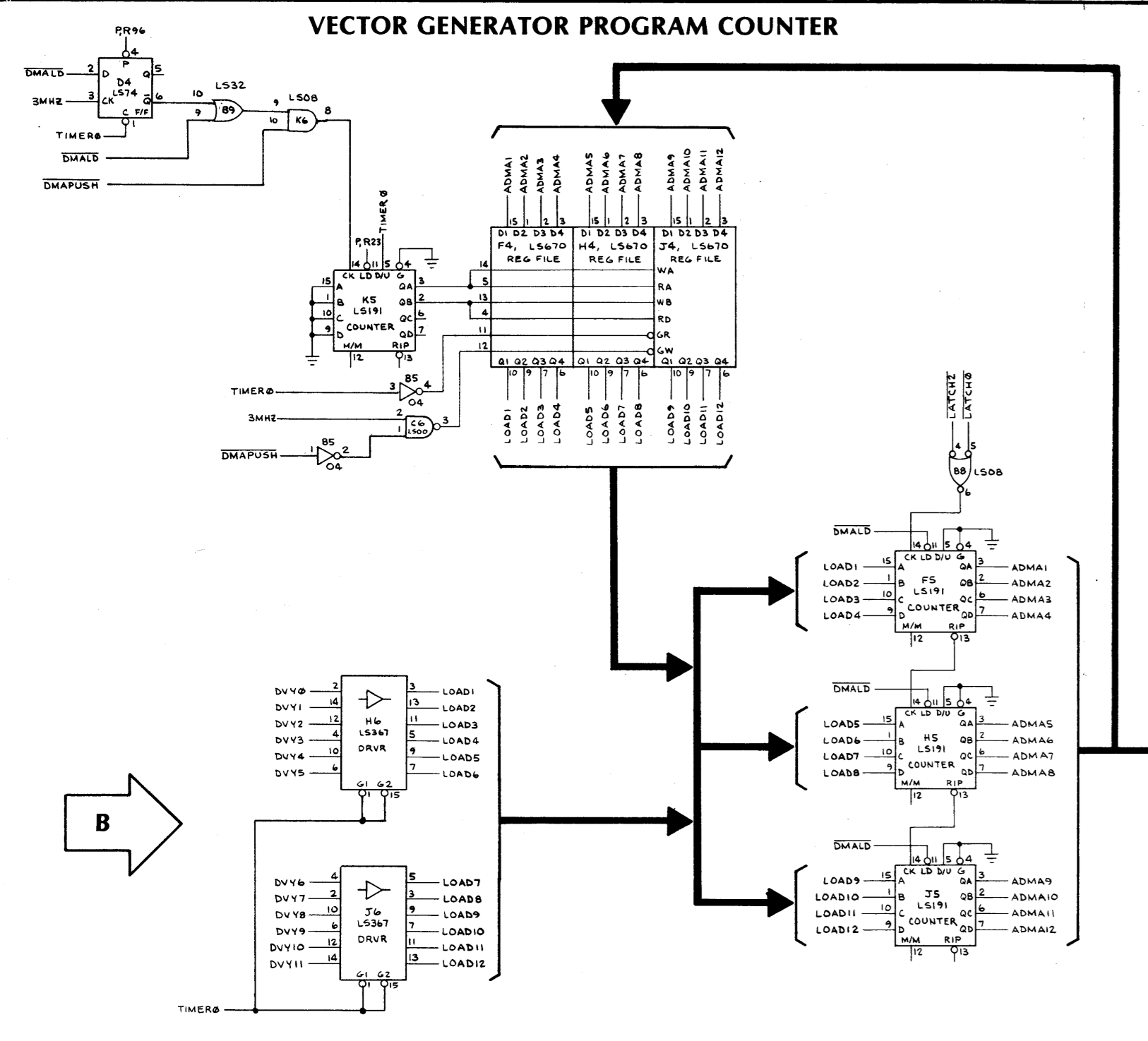


RAM CIRCUITRY



LUNAR LANDER™
MICROCOMPUTER
034230-XX A
© 1979 Atari, Inc.

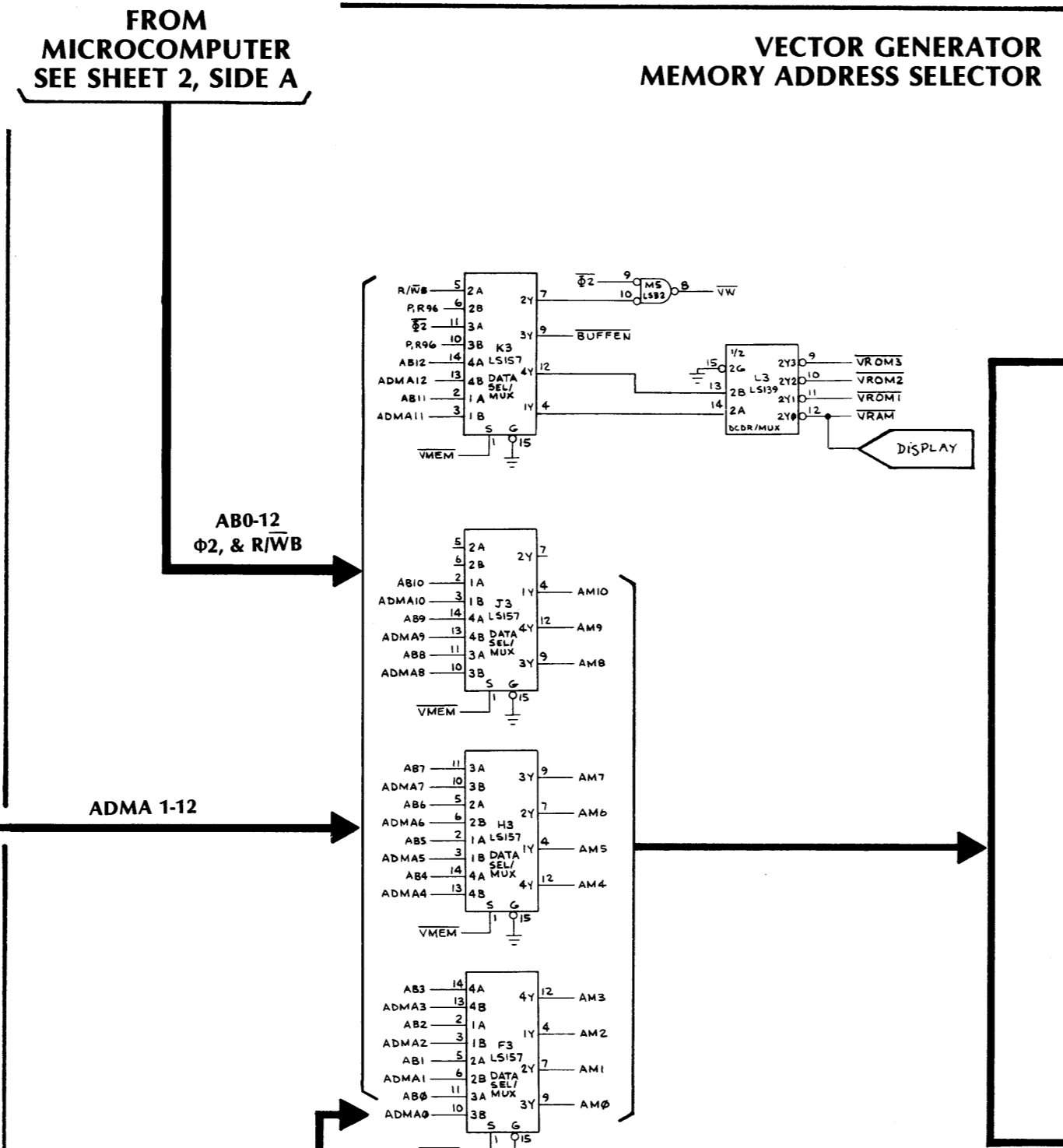
Program Memory for the Lunar Lander game is contained in PROMs for the -01 version of the PCB or ROMs for the -02 version of the PCB. One ROM is equivalent to four PROMs. All PROMs connected to a common enable must be removed before replacing with a ROM. For example, remove PROMs at locations F2, H1, L2 and M1 before replacing with ROM at location F1. A ROM/PROM equivalent chart is contained in Chapter 5, Illustrated Parts Catalog, of the Lunar Lander game manual.



Counters F5, H5 and J5 contain the address of the next data byte (instruction) to be fetched from the Vector Generator memory. Because these counters point to the next instruction in memory to be retrieved and performed, they are called the program counter. This program counter is incremented one count (to the next sequential address) each time the information at its current address is loaded into data latch 0 or data latch 2.

The program counter may also be preset to "jump" to a new address. This new address can be loaded into the program counter from the vector generator memory via data latches F7 & H7 and buffers H6 & J6.

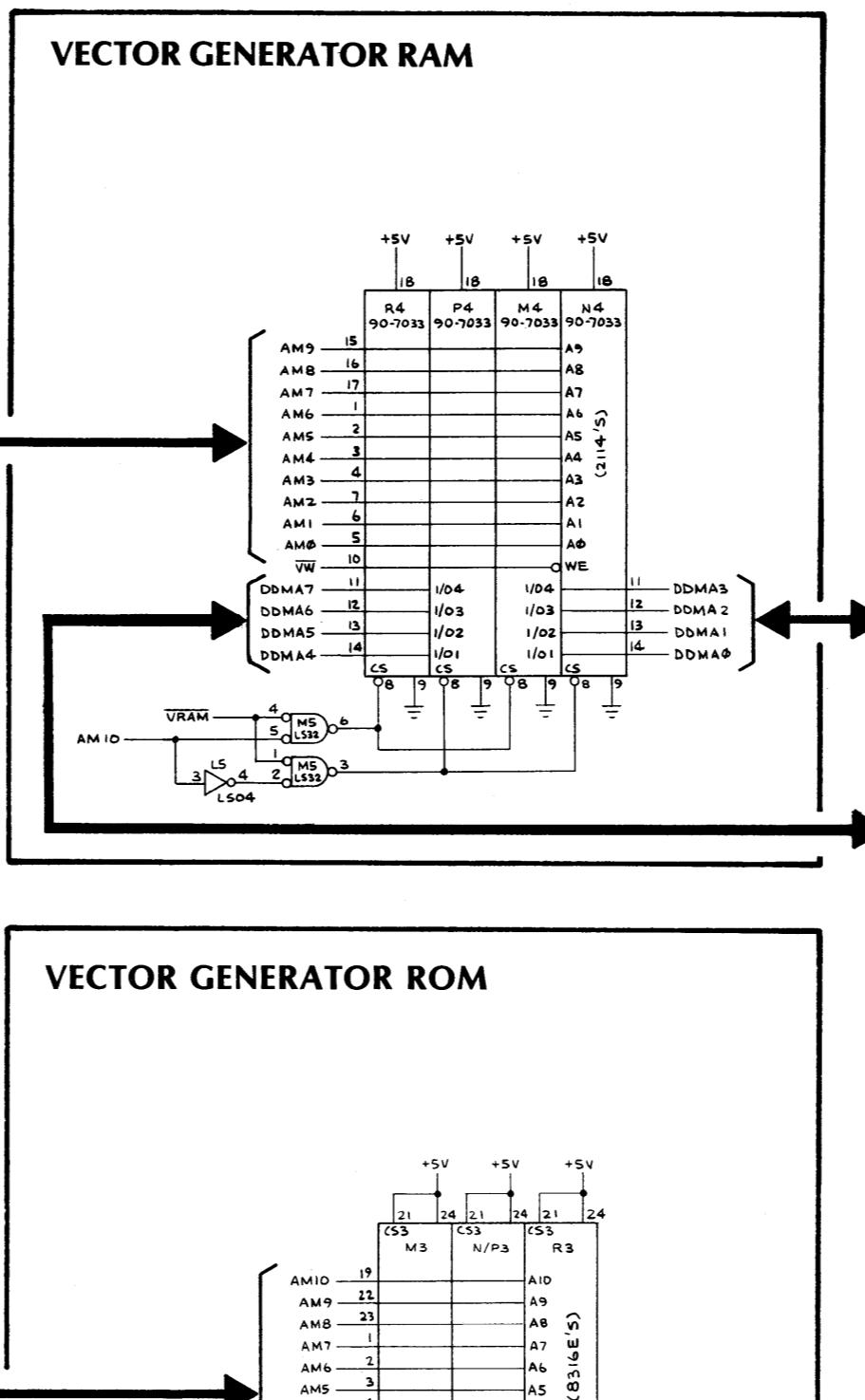
The program counter may also be preset to "return" to a previous address which it had stored in its "stack". The stack consists of register files F4, H4, & J4, and down/up counter K5. The stack is a 4-word 12-bit memory, used to save the contents of the program counter for future reference. It is loaded when DMAPUSH is low. Immediately after information is written into the stack, counter K5 increments one count. Immediately before loading the program counter from the stack, counter K5 decrements one count.



The address selector consists of multiplexers F3, H3, J3 and K3. When VMEM is low, the MPU of the microcomputer gains access to the address inputs of the vector generator memory. In this state, BUFFEN is from $\Phi 2$ and VW (vector generator write) is low when $\Phi 2$ and R/WB are both low. When VMEM is high, the address input to the vector generator memory is from the vector generator program counter and state machine. In this state, BUFFEN and VW are both held high by the pullup resistors connected to the 2B and 3B inputs of multiplexer K3.

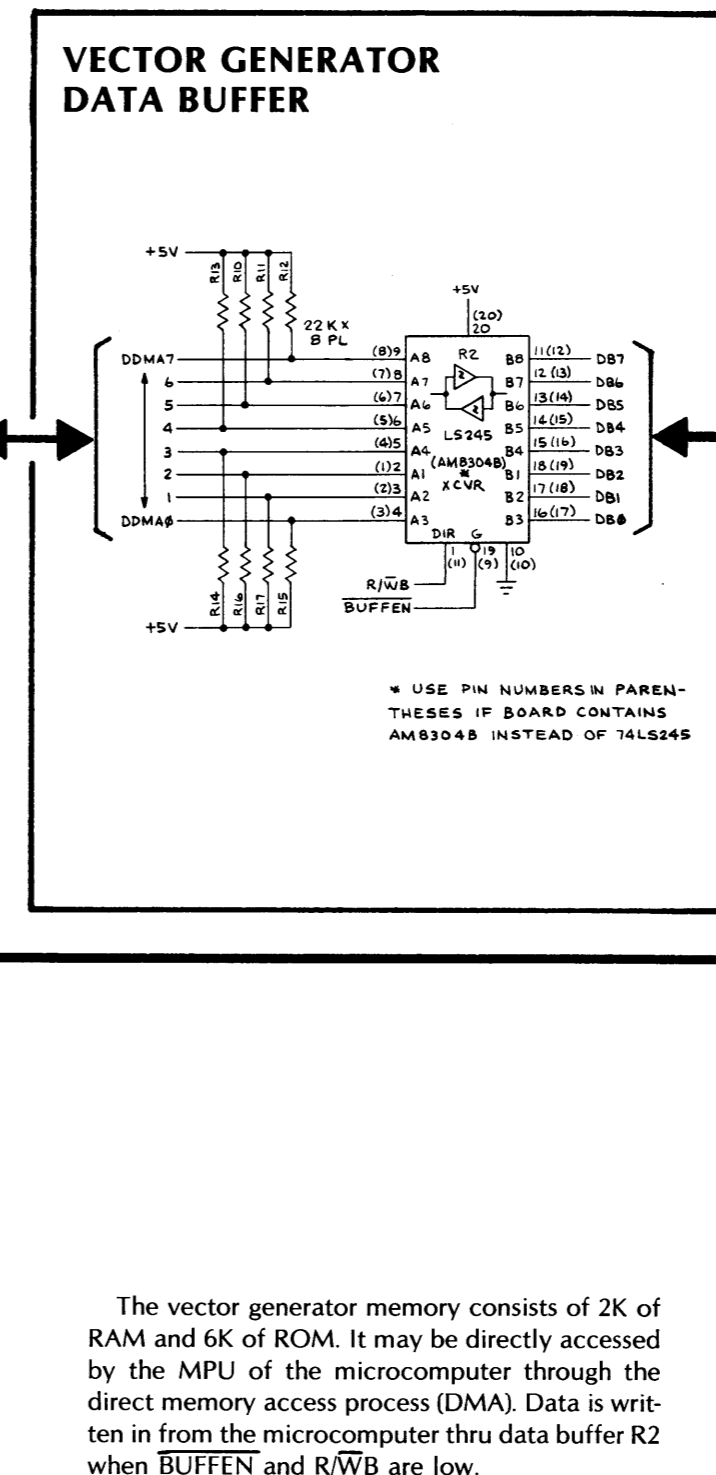
Address decoder L3 decodes address bits A11 and A12, and selects the RAM or one of three ROMs of the vector generator memory.

This address-selecting arrangement allows the game MPU to access the vector generator memory, i.e., write data into the vector generator RAM to instruct the vector generator what it should do next. The address selector can then allow the vector generator program counter and state machine to access this same area of RAM also, and read what instructions were sent to it by the game MPU.



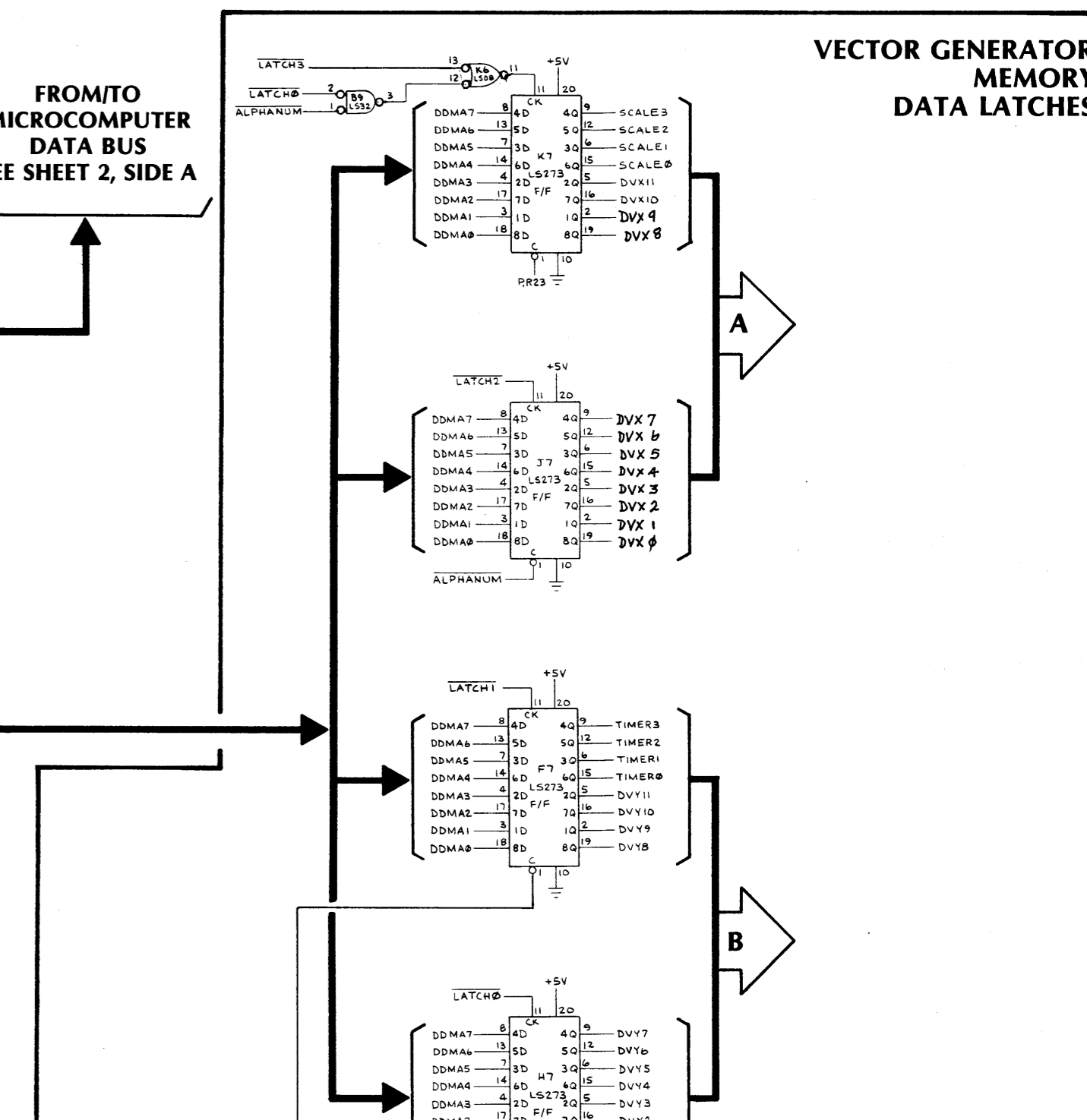
The vector generator memory consists of 2K of RAM and 6K of ROM. It may be directly accessed by the MPU of the microcomputer through the direct memory access process (DMA). Data is written in from the microcomputer thru data buffer R2 when BUFFEN and R/WB are low.

Any one of the three 2K x 8 vector generator program memory chips M3, N/P3, or R3 may be substituted with two equivalent 1K x 8 chips in locations K4 and L4. See the Illustrated Parts Catalog, Chapter 5, of the game manual for equivalent part numbers.



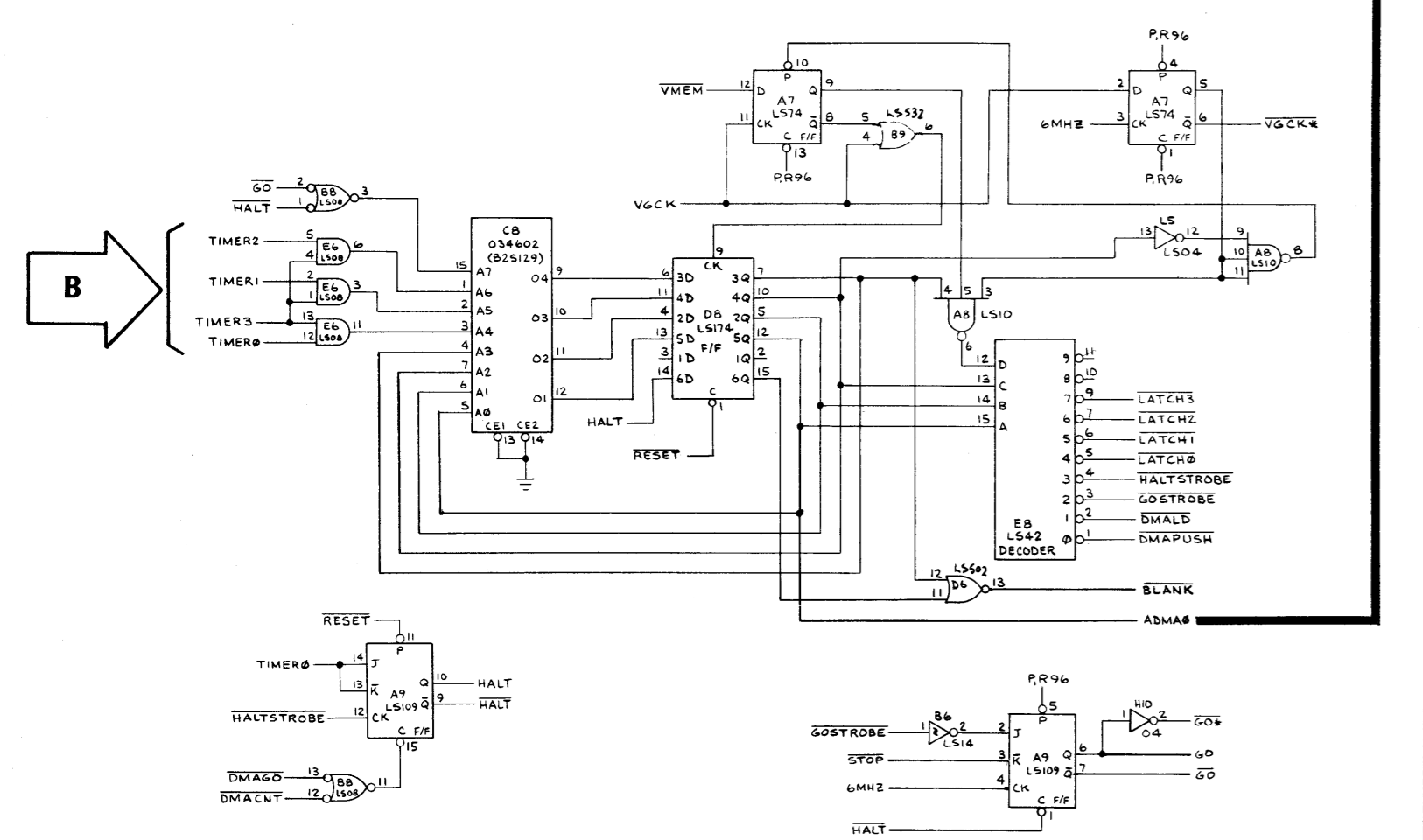
The data latches consist of latch 0 (H7), latch 1 (F7), latch 2 (J7), and latch 3 (K7). Inputs DDMA0 thru DDMA7 are the data outputs from the vector generator memory.

Latches 0 thru 2 are directly clocked by the rising edge of the LATCH0, LATCH1, and LATCH2 outputs from the vector generator's state machine. Latch 3 is clocked by LATCH3 or by LATCH0, if ALPHANUM is low. Latch 0 is cleared when RESET, DMAGO, or ALPHANUM goes low. Latch 3 is cleared by ALPHANUM.



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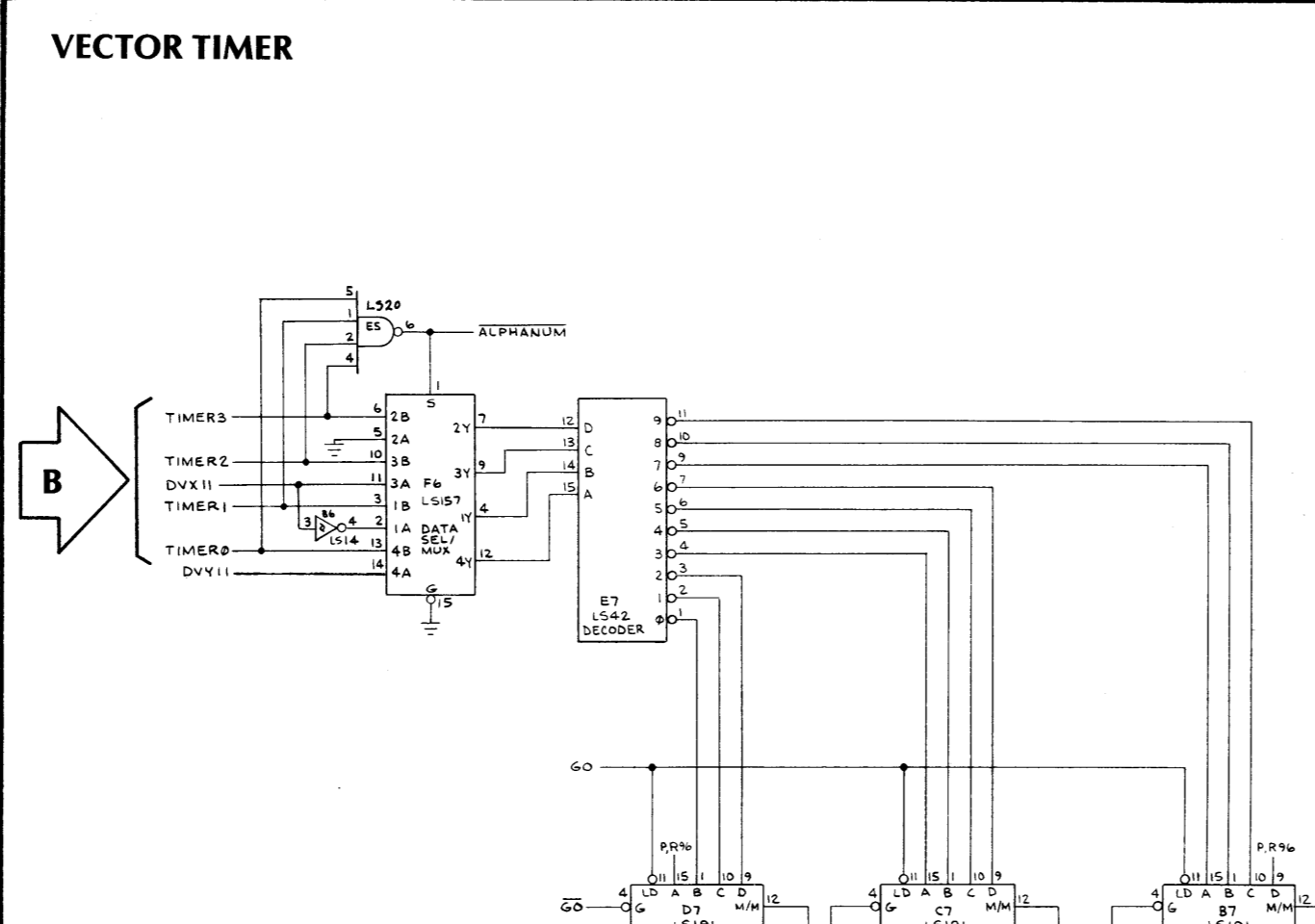
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The state machine is the "master controller" of the vector generator circuitry. It receives instructions from the game MPU, via the vector generator RAM. It carries out these instructions by accessing the appropriate sections of the vector generator ROM memory, using the vector generator program counter to do so. The state machine reads the vector generator ROM data (via Timer 0-3) and decodes this information to determine how it should use this data: 1) to draw a vector, 2) to move the monitor beam to a new position on the monitor display; 3) to "jump" to a new vector memory address; 4) to return to a previous vector memory address; or 5) to tell the game MPU that it has completed its current instructions, and is waiting for its next command.

The state machine consists of input gates B8 and E6, ROM C8, latch D8, clock circuitry A7, and decoder E8. Four bit input TIMER0 thru TIMER3 is the operation code input to the state machine. The A4 thru A6 address input to ROM C8 tells the ROM which instructions to perform. Address inputs A0 thru A3 from latch D8 tells the ROM which state was last performed. The address A7 input GO tells the ROM that the position counters are presently drawing a vector. The HALT input to A7 tells the ROM that the vector generator has completed its operations.

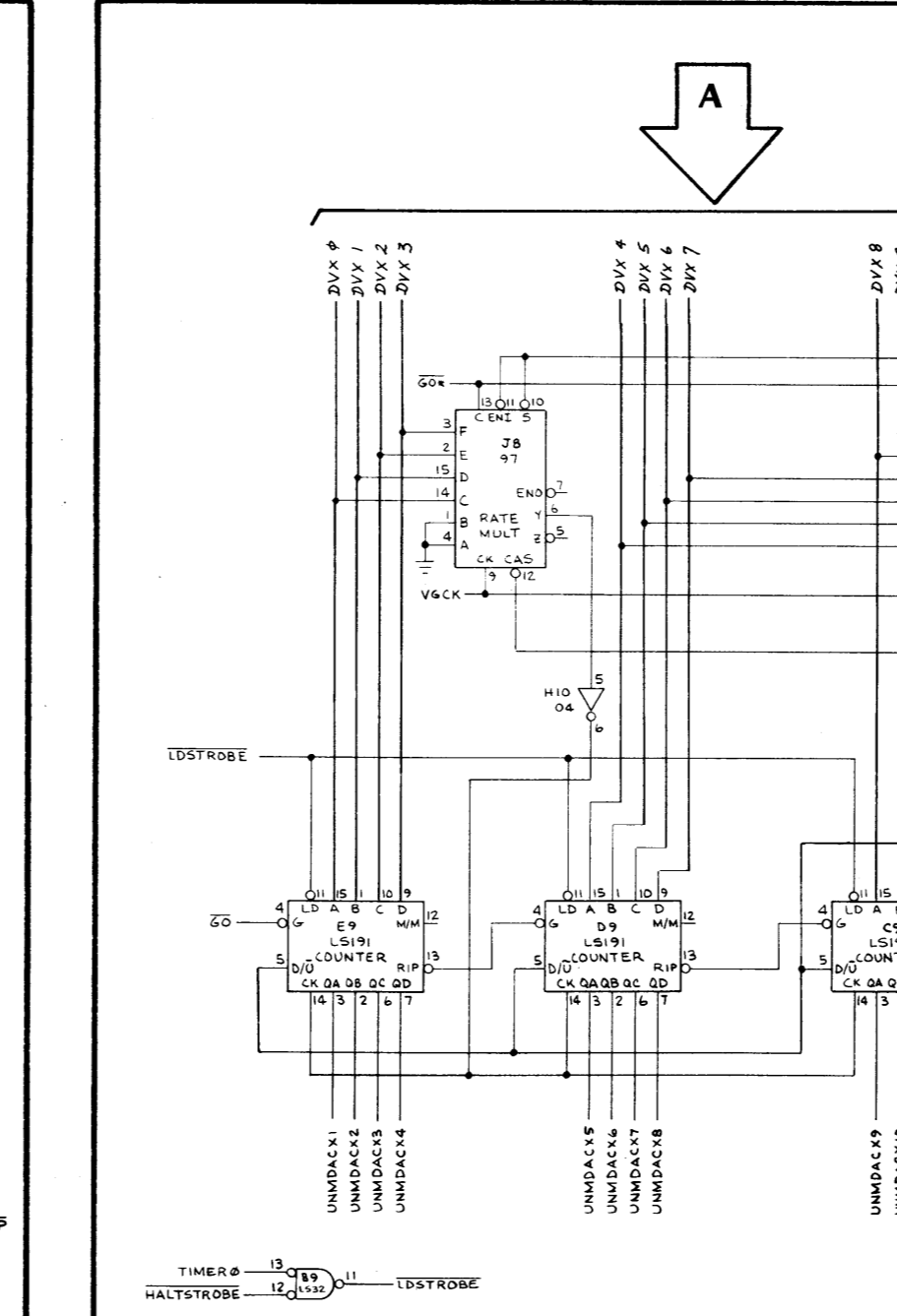
During initial power up of the game, the HALT signal is present low. The microcomputer reads the high HALT signal through its switch input port (buffer M10) on data line DB0. This tells the microcomputer that the vector generator is halted and waiting for an instruction. To ensure that the beam is off when the state



The purpose of the vector timer is to time out the length of time it takes to "draw" an actual vector on the monitor display. During the interval when the X and Y position counters are actually drawing the vector, STOP is high. This prevents the vector generator state machine from advancing to its next state until the vector currently being drawn is completed. As soon as the vector has been drawn, STOP goes low, allowing the state machine to advance to the next state in its intended sequence.

The vector timer consists of multiplexer F6, decoder E7, and counters B7, C7, and D7. If TIMER0 thru TIMER3 inputs are any state but all high, decoder E7 directly decodes the signals and loads the decoded low into one of the counters. When GO goes low, the counters count from the loaded count until the counters all reach their maximum count. This count is a maximum length of 1024. At this time STOP goes low and clears the GO flip-flop of the state machine.

If the TIMER signals are all high, ALPHANUM goes low and data signals DVX11 and DUY11 are decoded by decoder E7. With this input the counter's maximum length of count is 64.

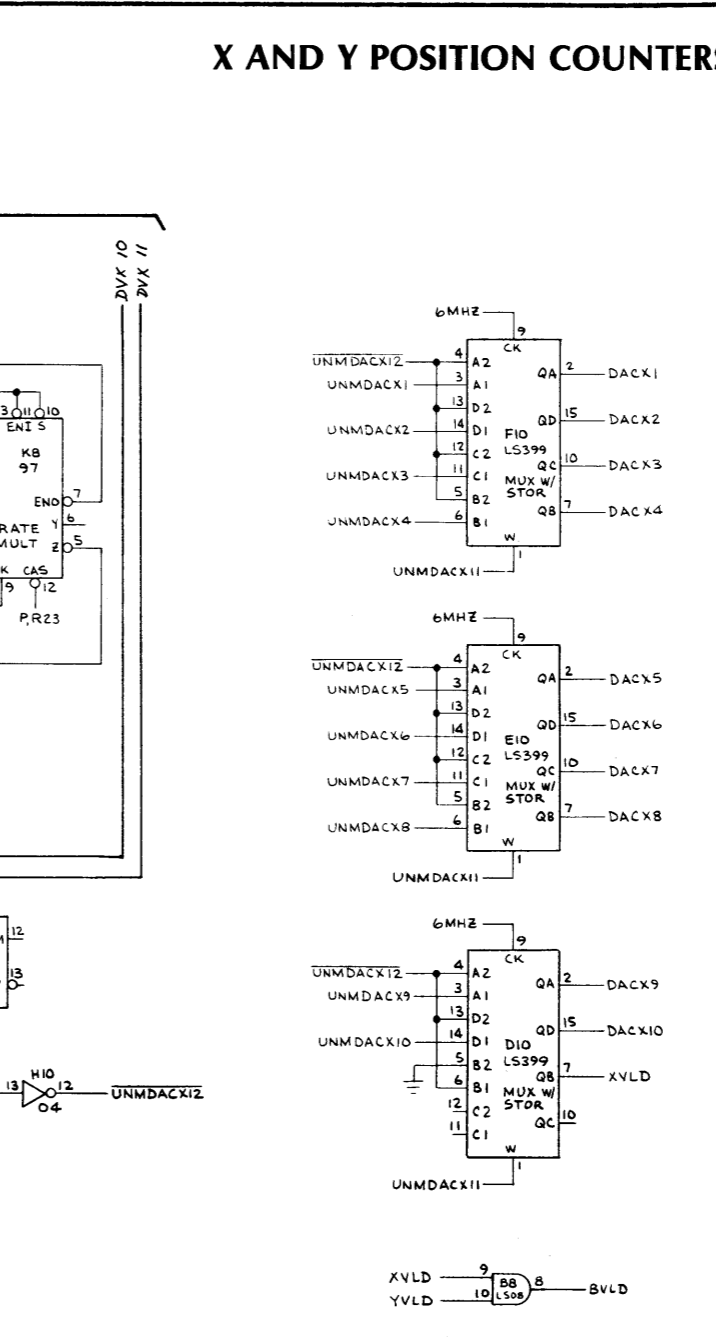


The X and Y position counters are two identical circuits. Therefore, the following description discusses only the X position counters.

The X position counters contain rate multipliers (J8 and K8), down/up counters (C9, D9, and E9), multiplexers (D10, E10, and F10), and associated gates (B8 and H10). The output of the down/up counters is a 12-bit binary number that represents the horizontal location of the beam on the monitor screen (or X axis), with 0 being the far left side of the screen and 1023 being the far right side of the screen. Increasing or decreasing this binary number output will cause the beam to move to the right or left, respectively. The vector generator state machine decodes instructions from its memory, and then is capable of using that data to alter the binary count of these counters in one of two ways.

The state machine can preset these counters to an entirely different number from their previous contents. This will cause the beam to "jump" to a new location on the monitor screen instantaneously, i.e., for drawing a new vector from a different starting position than where the previous vector ended. While the beam is "jumping" to this new position, the beam itself is turned off to prevent unwanted lines from appearing on the screen. To preset this new position into the counters, the state generator causes LDSTROBE to go low. At this time, a new 12-bit number (DVX0-11) is loaded into the counters from the vector generator memory data latches.

The state machine can also instruct these counters to count up or down any specific number of counts. This will cause the beam to move to the left or to the right a specific distance relative to where it was. During this beam movement, the beam is turned on with the desired intensity. This is the procedure used to draw a vector on the monitor screen. The direction (to the left or right) and length (0 to 1023) of the vector to be drawn relative to the beam's current position is determined by DVX0-11 (from the vector



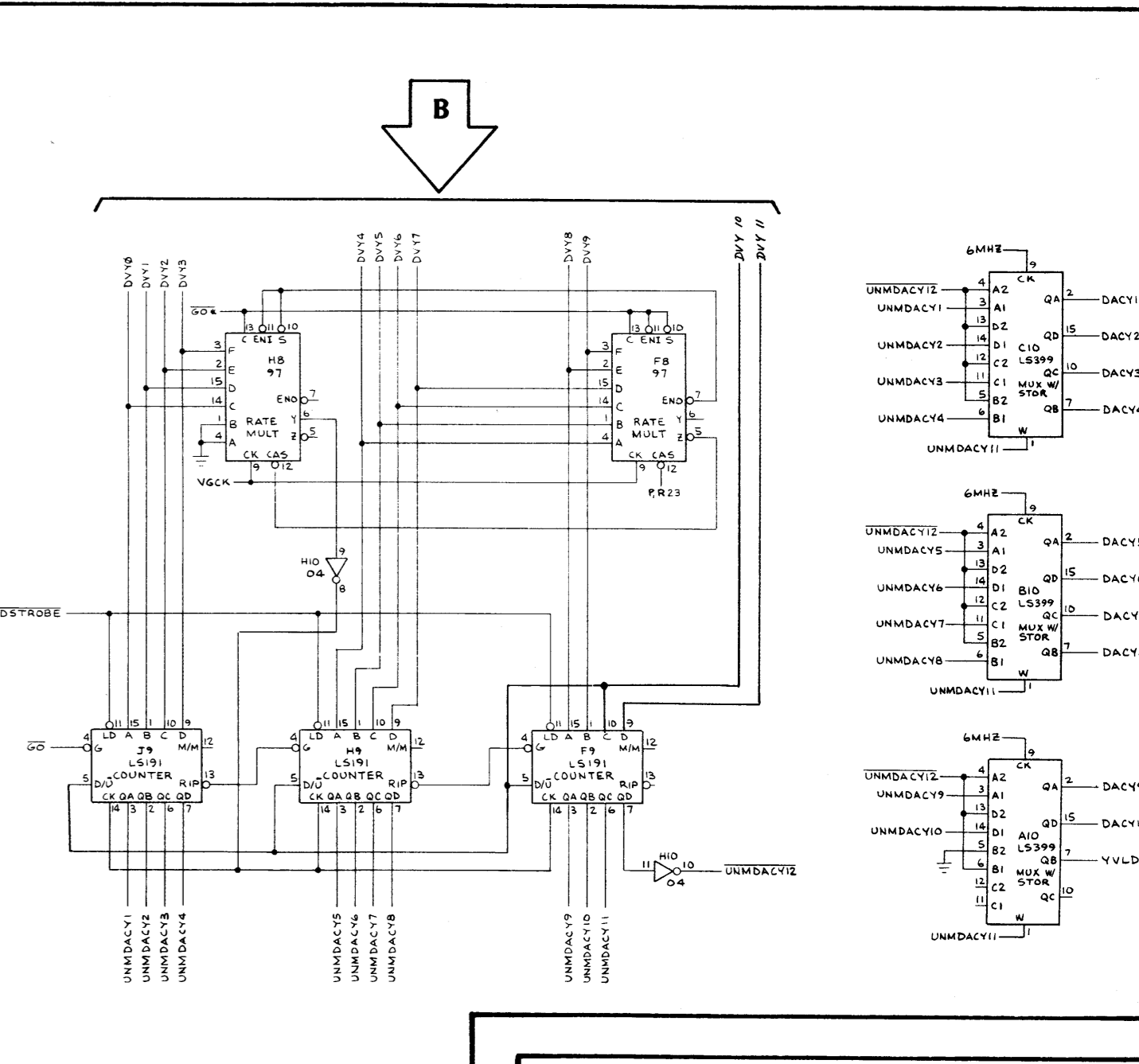
generator memory data latches). This data contains information that determines how many clock pulses the counters will receive and whether the counters will count up or down.

DVX0-9 memory data is loaded into rate multipliers J8 and K8. The function of these devices is to space the desired number of counter clock pulses at equal intervals over the time period that it will take to draw the desired vector. This insures that vectors of different length will still be displayed with the same relative beam intensity. DVX10 and 11 are loaded directly into the counters. DVX10 determines whether the counters count up or down. DVX11 is used to control the select input of multiplexers D10, E10, and F10.

The UNMDACX1 thru UNMDACX10 (X axis unmultiplexed digital-to-analog converter signals) are transferred and stored at the output of the multiplexers on each rising edge of the 6 MHz clock (from the microcomputer clock circuitry). The DACX1 thru DACX10 signals are sent to the digital-to-analog converters (DACs) in the X video output.

The DACX1 and DACX10 outputs represent the physical placement of the beam on the monitor. The far left of the monitor screen is 0, the center is 512, and the far right is 1023. Therefore, if the DACX1 thru DACX10 signal was greater than 1023, the monitor beam would go off the right side of the screen and start again on the left side of the screen, a "wraparound" condition. To prevent a wraparound, the multiplexers' select input from UNMDACX11 goes high when the count is greater than 1023 or less than 0. This selects UNMDACX12 to be output from the multiplexers to the DACs, forcing all zeroes or all ones, and thus keeping the beam on the appropriate side of the screen, instead of allowing it to wraparound.

The XVLDD and YVLDD (X and Y valid) outputs from the X and Y position counter multiplexers are gated together to enable the Z axis output, BVLD (beam valid).



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LUNAR LANDER™ VECTOR GENERATOR SCHEMATIC 034230-XX A

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