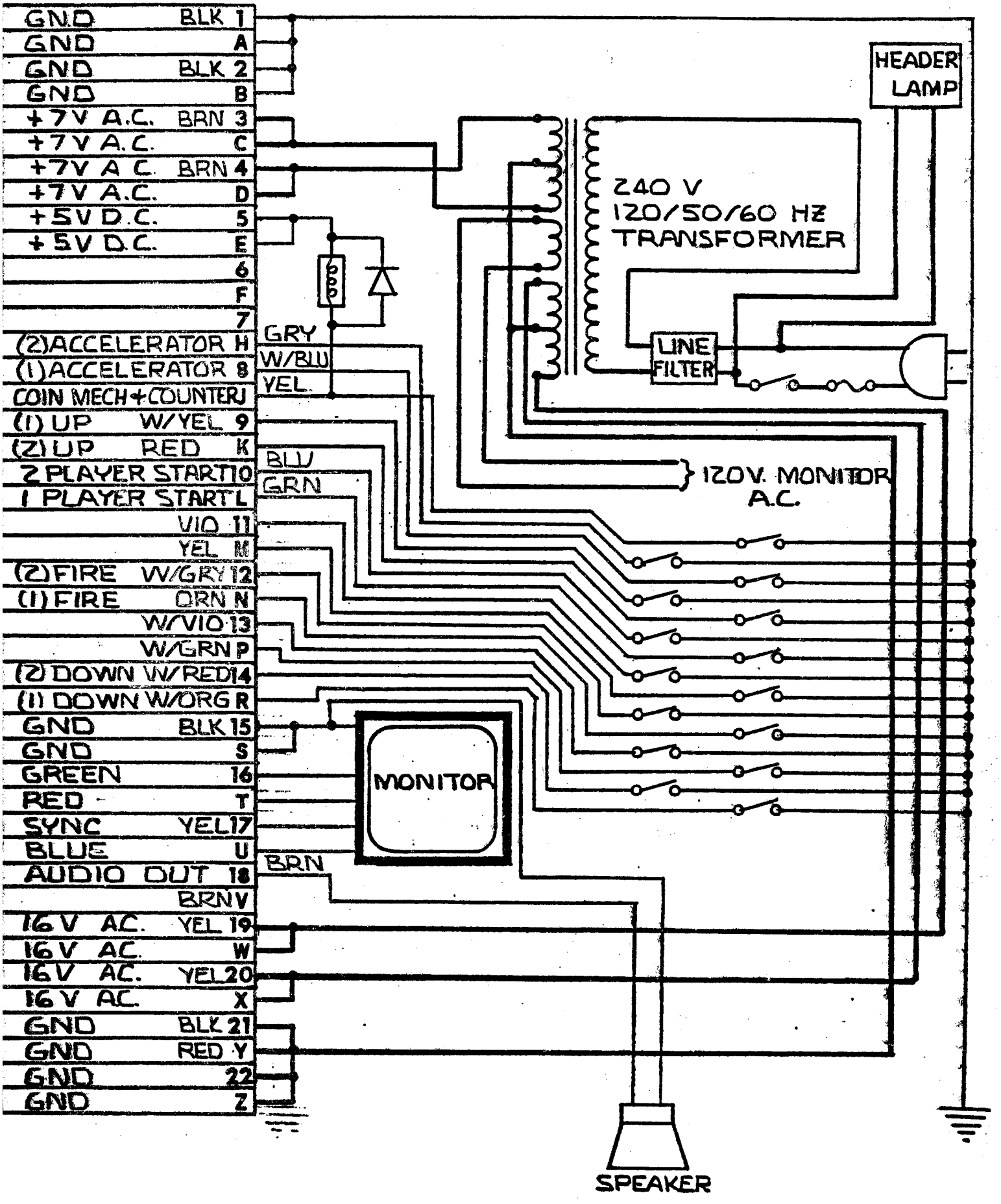
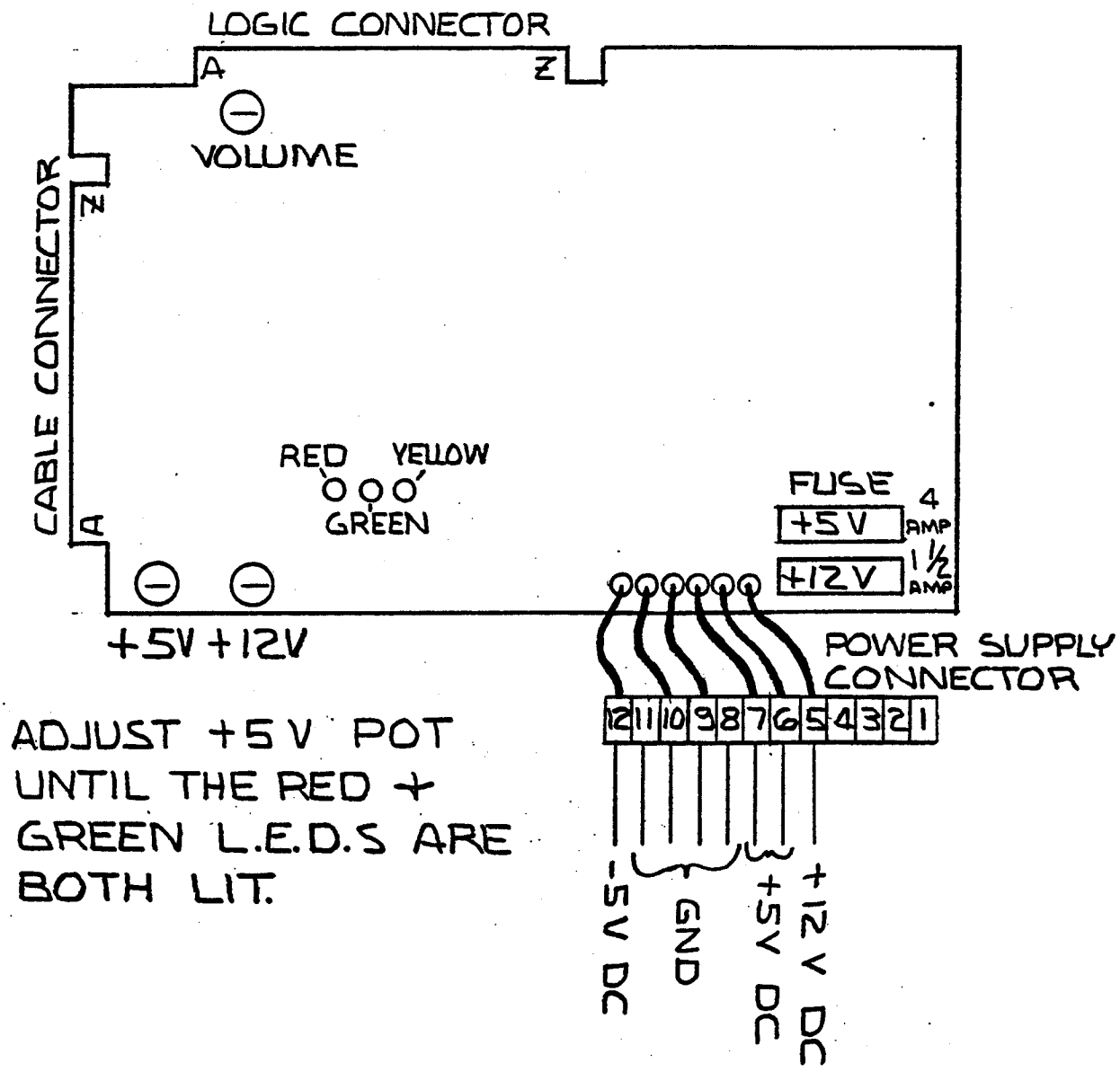
LOOPING
WIRING DIAGRAM



LOOPING POWER SUPPLY ADJUSTMENTS



ADJUST +5V POT UNTIL THE RED + GREEN L.E.D.S ARE BOTH LIT.

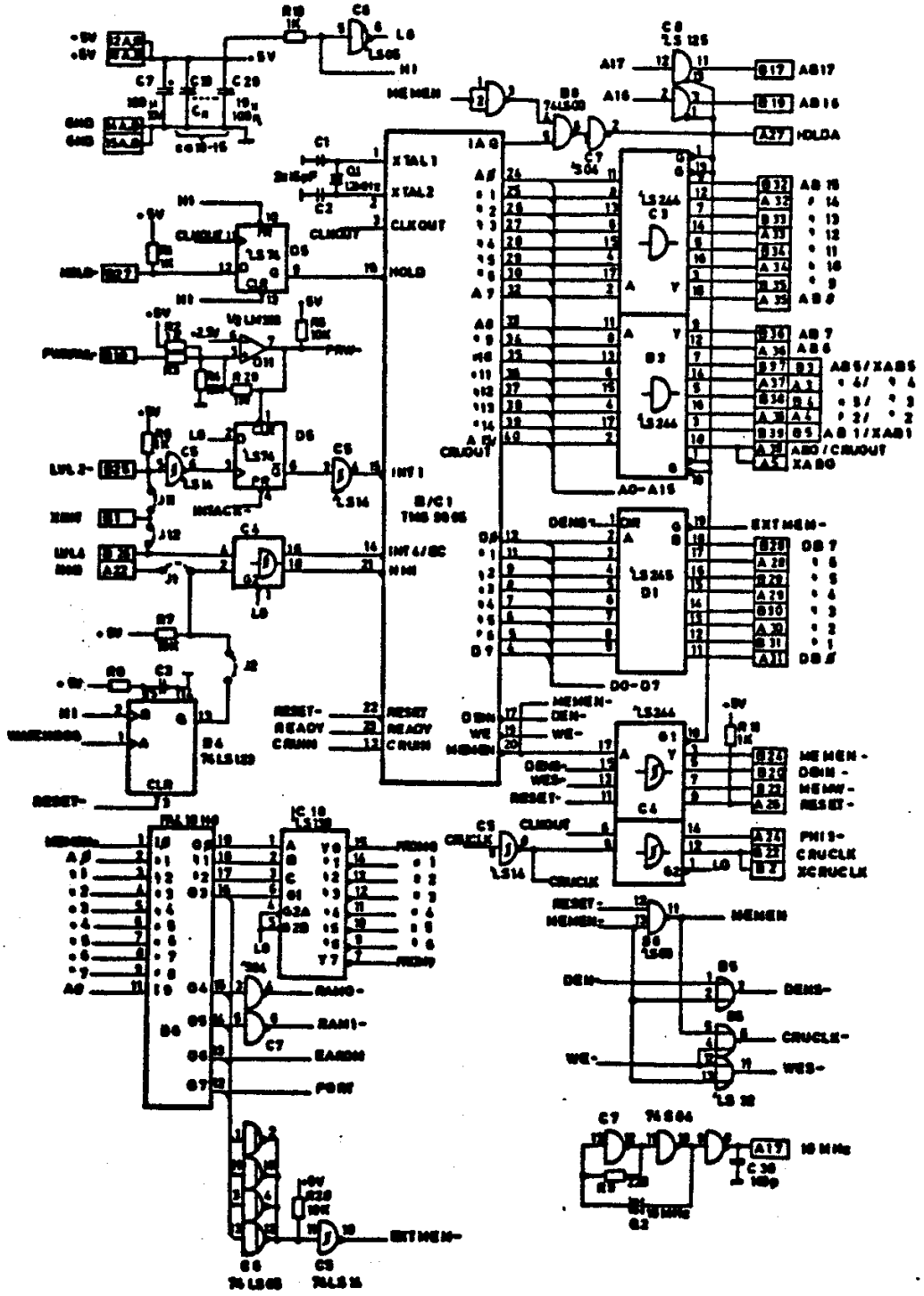
LOGIC BOARD CONNECTIONS

Components Side		Solder Side	
1	Red	1	Green
2	Sync.	2	Blue
3	Pot 1	3	Pot 2
4	GND Pot - Video GND	4	Audio 1
5	1 Player Fast	5	Two Player
6	Coin (programmable)	6	Coin 1/1
7	One Player	7	1 Player Fire
8	1 Player Up	8	1 Player Down
9		9	
10	2 Player Fast	10	
11		11	2 Player Fire
12	2 Player Down	12	2 Player Up
13		13	
14		14	
15		15	
16		16	
17	GND	17	GND
18		18	GND
19		19	
20	GND	20	Audio 2
21		21	
22		22	

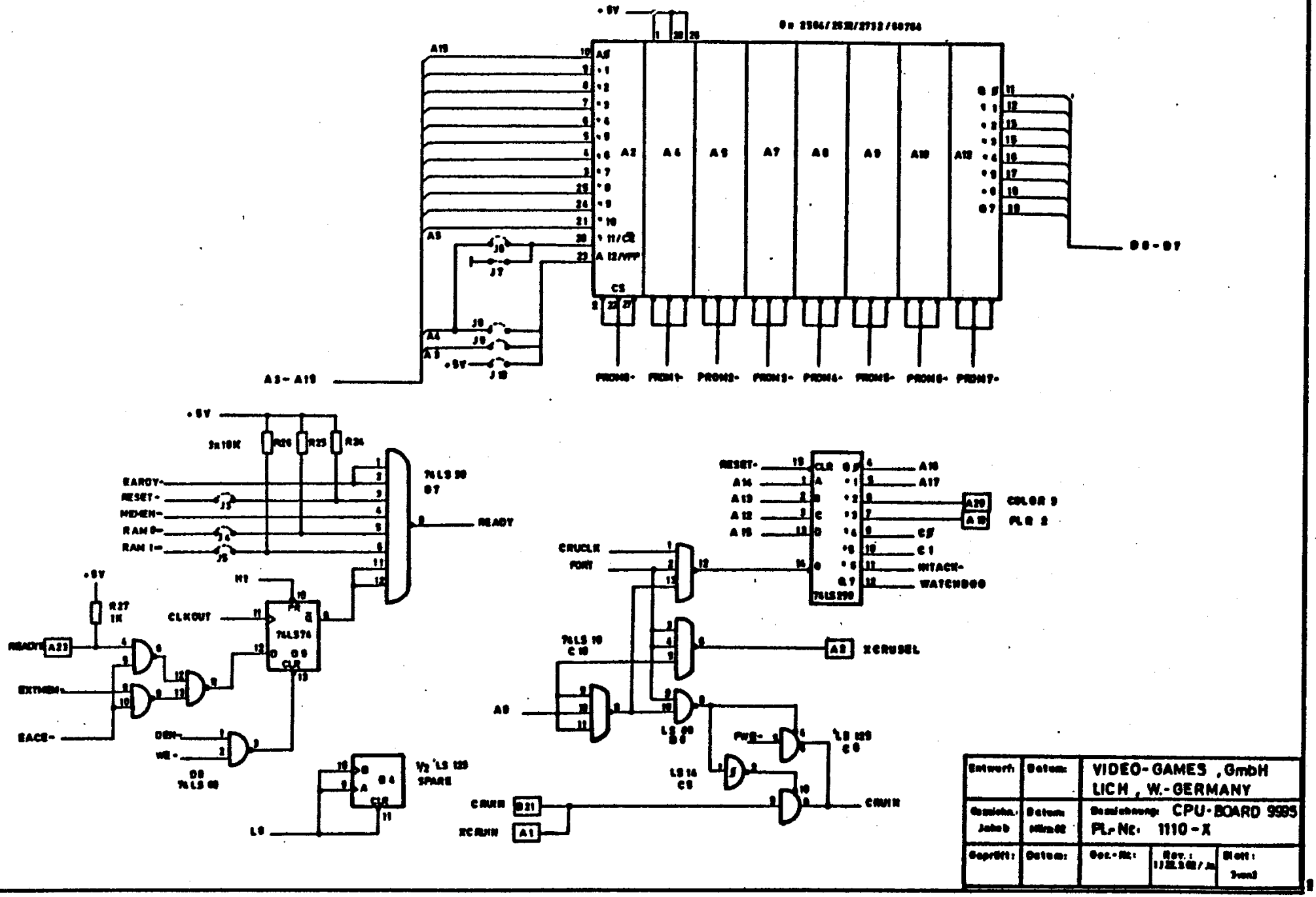
SWITCH SETTINGS

Coin 1 Coin 2

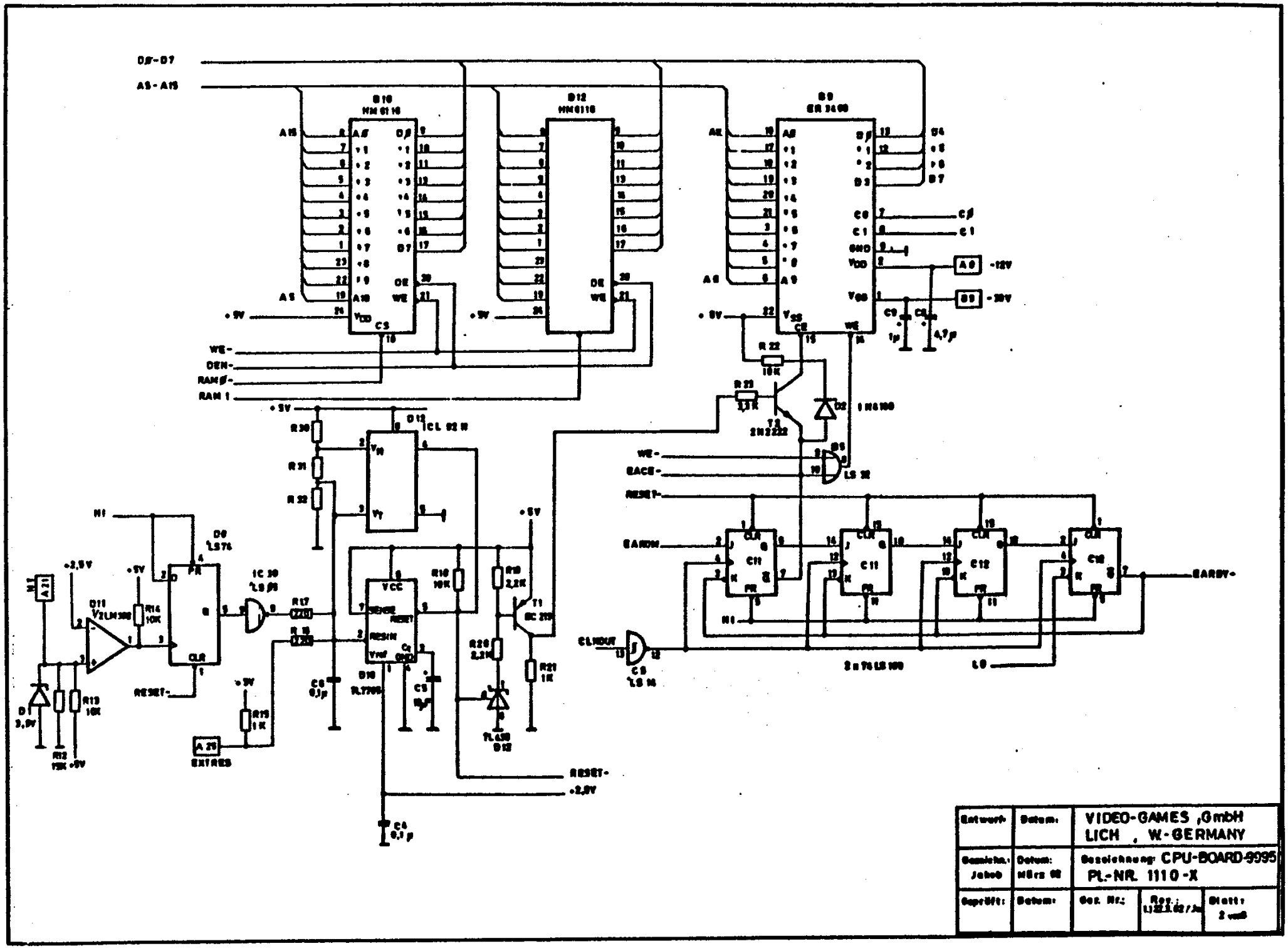
1	2	3	4	5	6	7	8	Functions
							OFF	1 Credit/Coin
							ON	2 Coins/Credit
				OFF	OFF	OFF		7 Credits/Coin
				OFF	OFF	ON		6 Credits/Coin
				OFF	ON	OFF		5 Credits/Coin
				OFF	ON	ON		4 Credits/Coin
				ON	OFF	OFF		3 Credits/Coin
				ON	OFF	ON		2 Credits/Coin
				ON	ON	OFF		1 Credit/Coin
				ON	ON	ON		10 Credits/Coin
		OFF						5 Jets/PLayer
		ON						3 Jets/Player



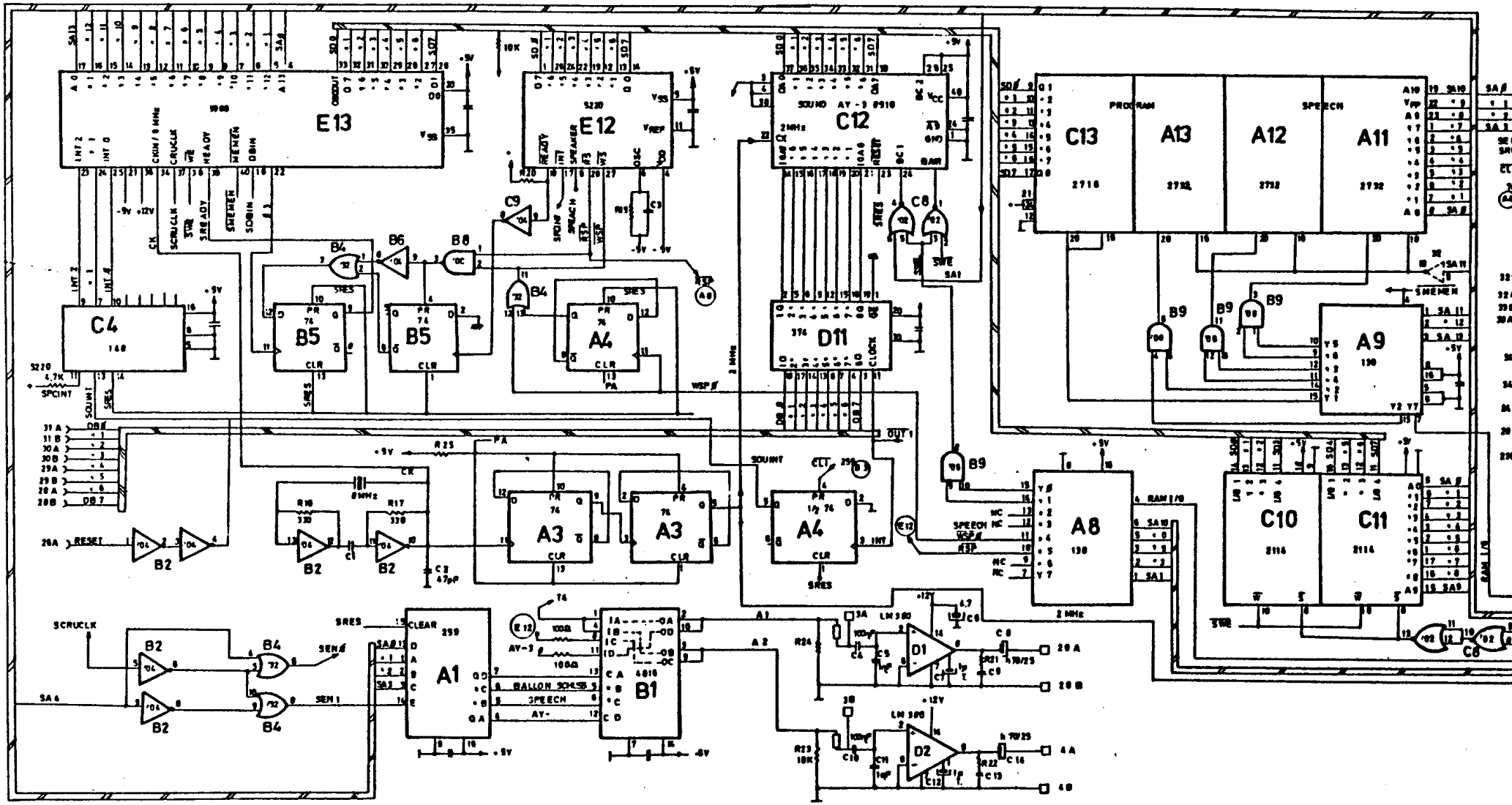
Datum:	Datum:	VIDEO-GAMES GmbH
Name:	Name:	LICH, W-GERMANY
Datum:	Bezeichnung:	PL-NR.: 1110-X
Name:	Zeichnungs-Nr.:	
Blatt: 1 von 2		

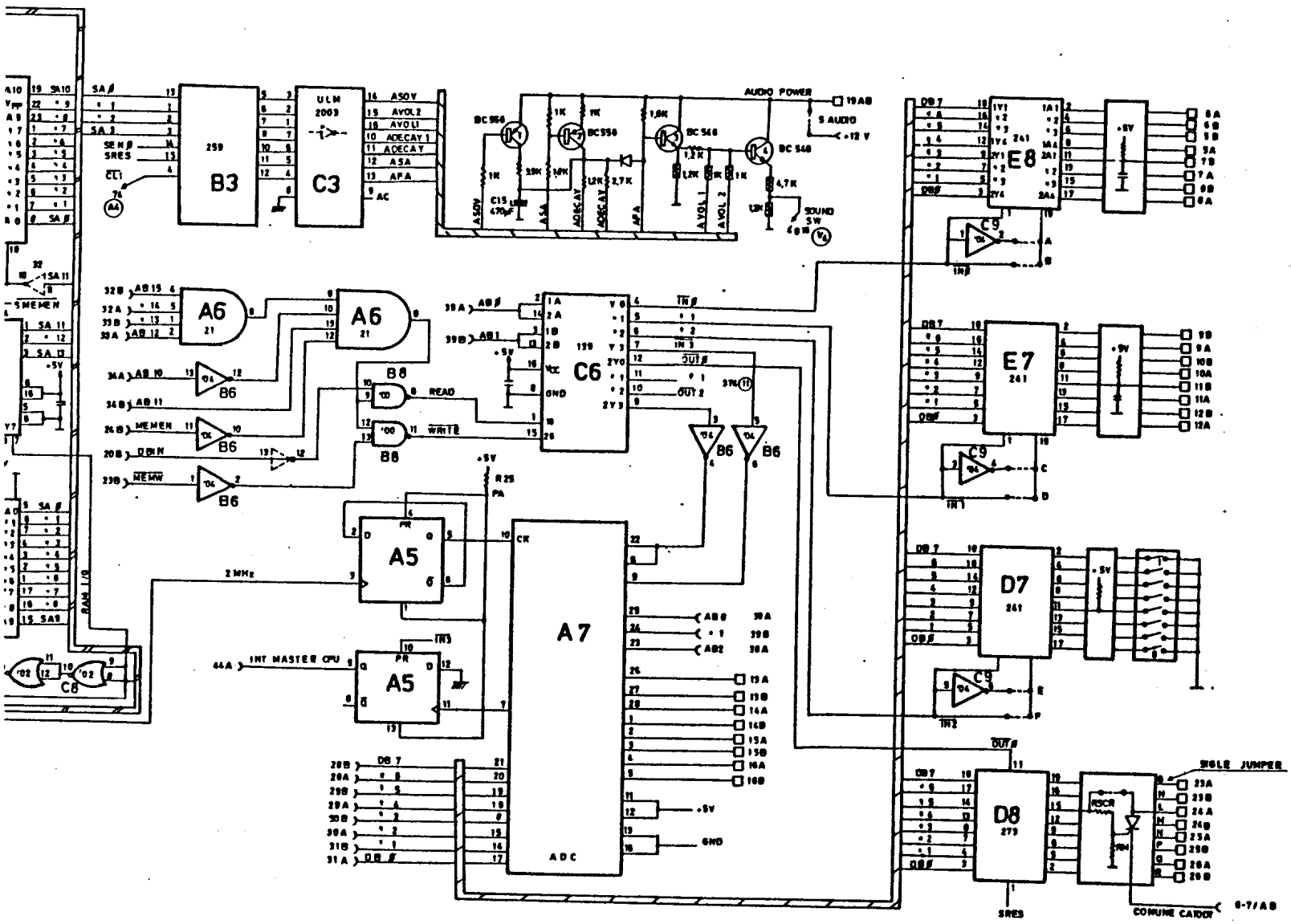


Entwurf:	Datum:	VIDEO-GAMES , GmbH LICH , W.-GERMANY		
Gezeichn.: Jakob	Datum: 08mai82	Bezeichnung: CPU-BOARD 9995 PL.-Nr.: 1110 - X		
Geprüft:	Datum:	Ser.-Nr.:	Rev.: 11.05.82/Ja	Blatt: 2von3

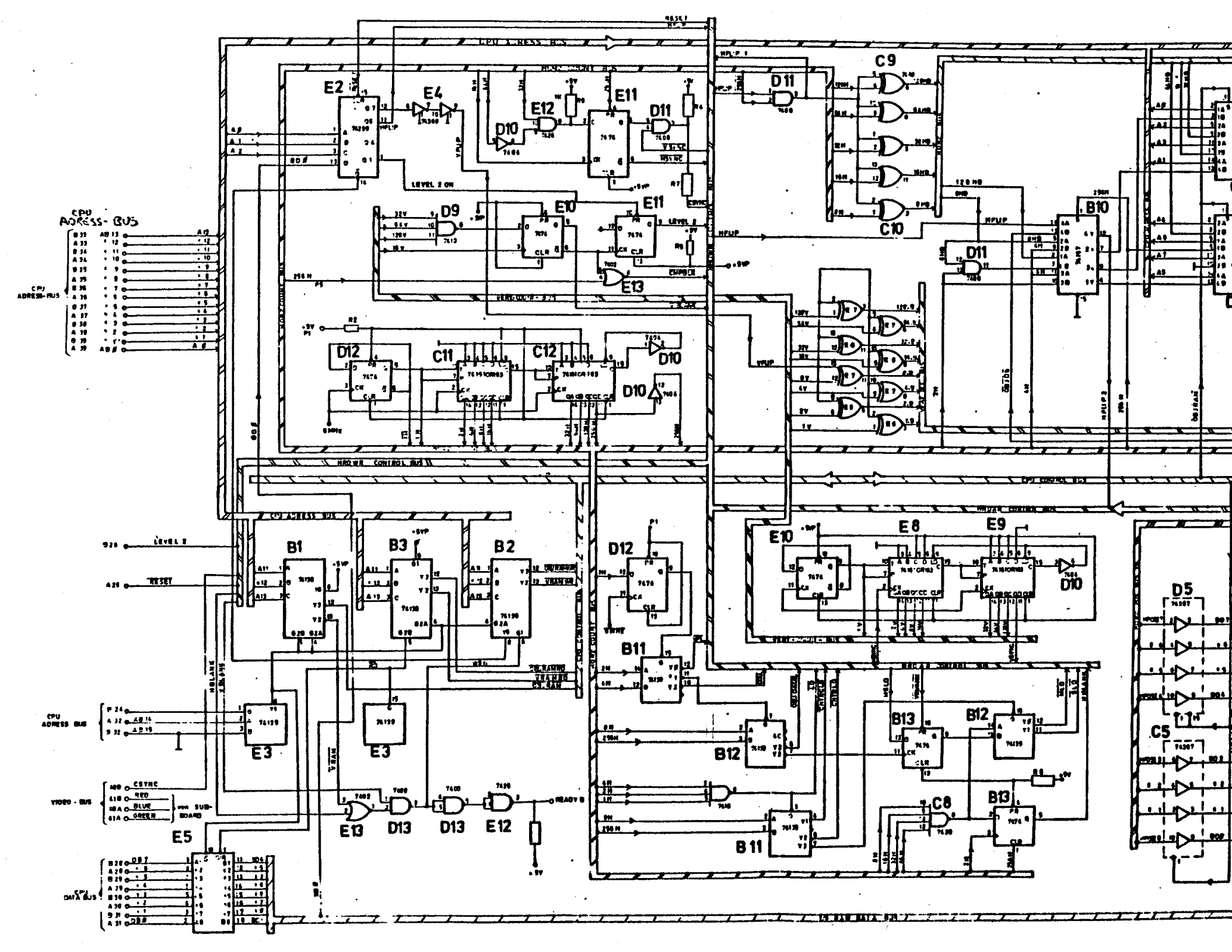


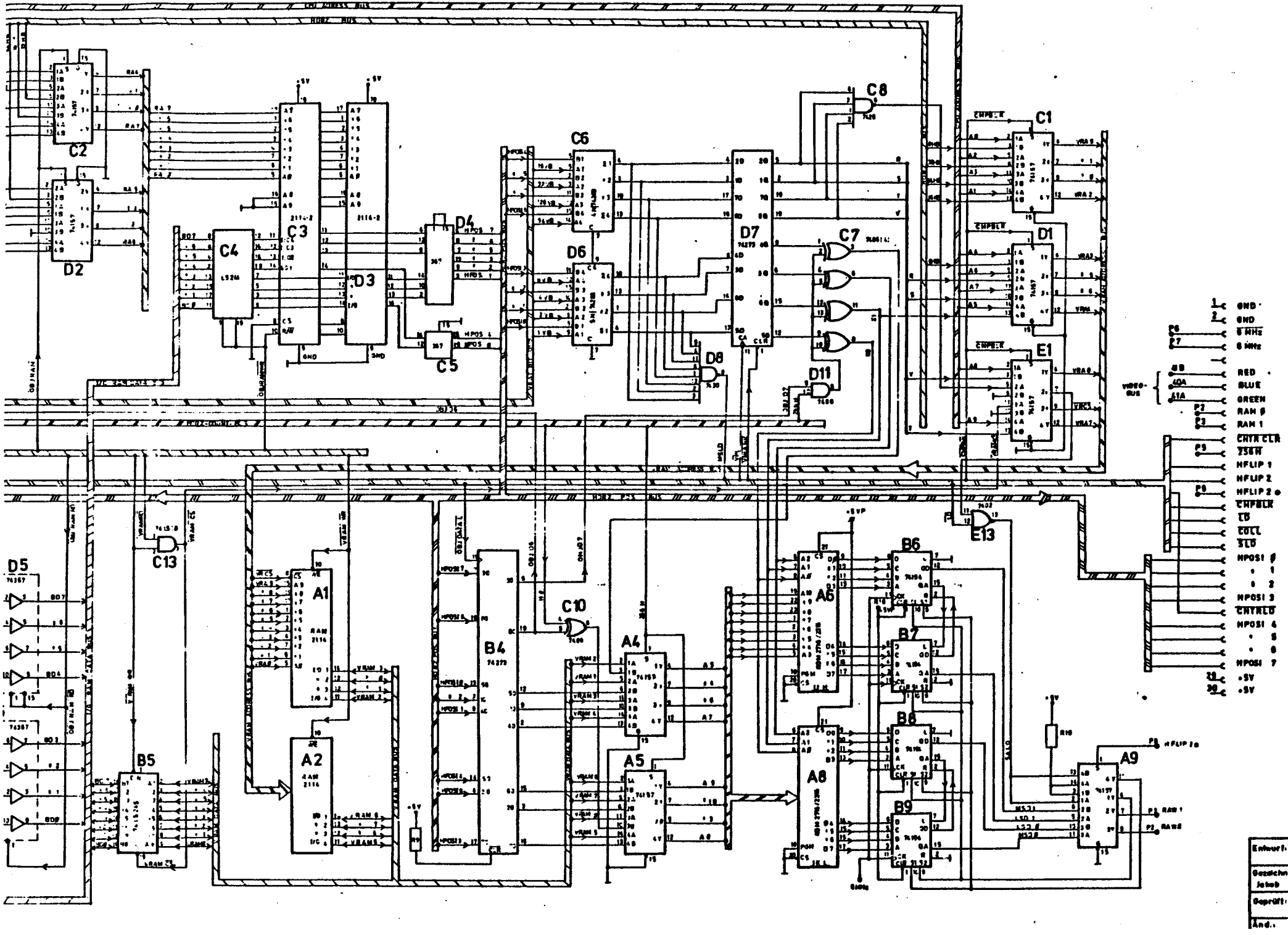
Entwurf:	Datum:	VIDEO-GAMES ,GmbH LICH , W-GERMANY		
Gezeichn.: Jakob	Datum: März 88	Bezeichnung: CPU-BOARD-9995 PL.-NR. 1110-X		
Geprüft:	Datum:	Ser. Nr.:	Rev.:	Blatt: 2 von 8

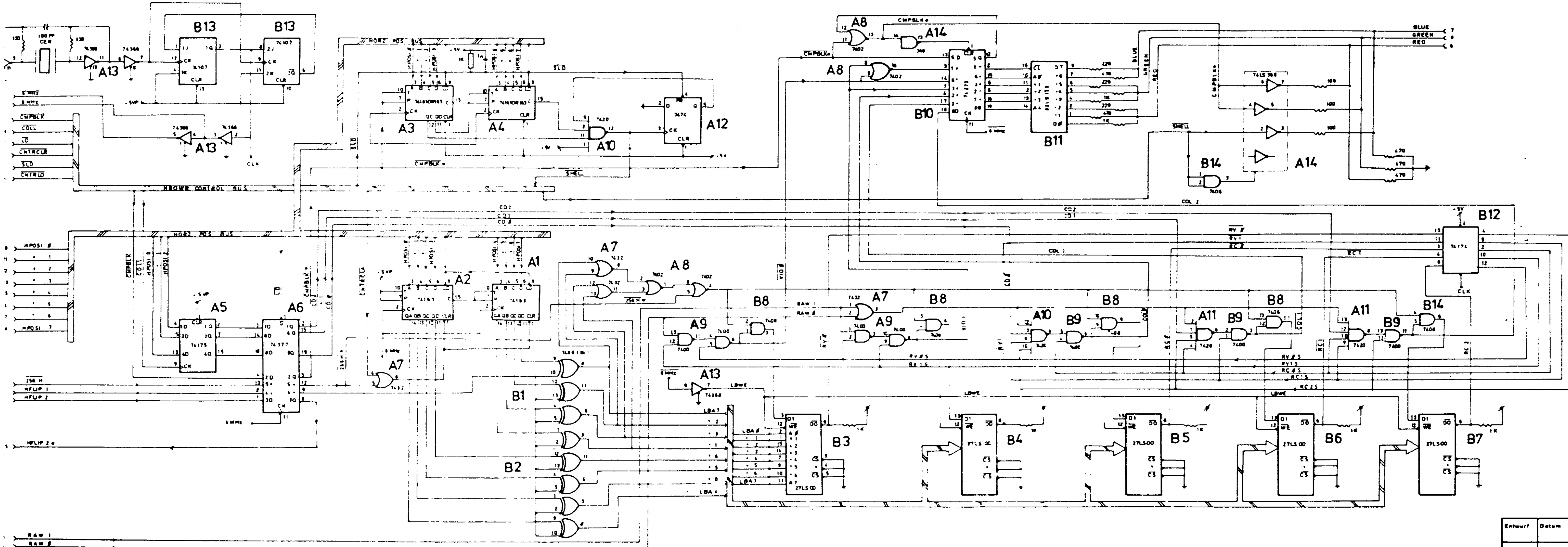

E13
E12
C12
C13
A13
A12
A11
C4
B5
B5
A4
D11
A9
A3
A3
A4
A8
C10
C11
B2
B4
B6
B8
B9
A1
B1
D1
D2
SCRCLK
SRES
SPEECH
AY-3
RESET



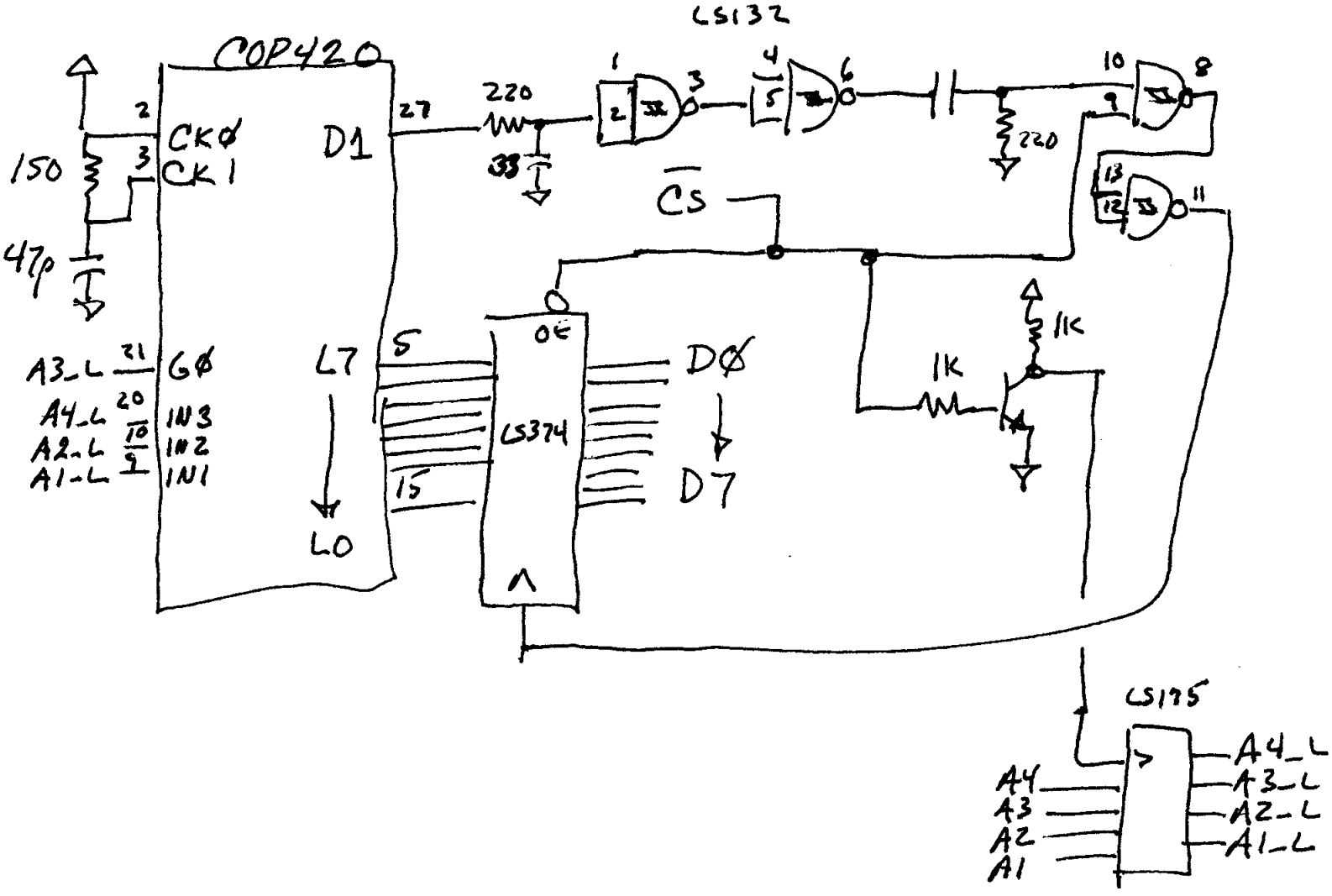
Entwurf:	Datum:	VIDEO-GAMES , GmbH LICH , W.-GERMANY	
Gezeichn.: Jakob	Datum März 82	Bezeichnung I/O-SPEECH-SOUND-BOARD	
Geprüft:	Datum:	Gez.-Nr.:	Rev.: 1.22.3.82/Ja. Blatt:


CPU ADRESS-BUS
CPU ADRESS BUS
HARDWR CONTROL BUS
CPU CONTROL BUS
CPU DATA BUS
VIDEO - BUS
LEVEL 2
RESET
CSYNC
RED
BLUE
GREEN
READY B
E2
E4
E11
E12
D10
D11
C9
C10
B10
D9
E10
E13
D12
C11
C12
B1
B3
B2
E3
E5
D13
B11
B12
B13
C8
E8
E9
D5
C5


C1
C2
C3
C4
C5
C6
C7
C8
D1
D2
D3
D4
D5
D6
D7
D8
D11
E1
E13
A1
A2
A4
A5
A6
A8
A9
B4
B5
B6
B7
B8
B9
C10
C13
GND
GND
8 MHz
8 MHz
RED
BLUE
GREEN
RAM 0
RAM 1
CNTRCLR
ZSEW
HFLIP 1
HFLIP 2
HFLIP 2
CMPBLK
LD
COLL
SLO
HPOSI 0
HPOSI 1
HPOSI 2
HPOSI 3
CNTRLD
HPOSI 4
HPOSI 7
+5V
+5V
VIDEO-BUS



Entwurf	Datum	VIDEO-GAMES . Gm UCH . W-GERMANY		
Gezeichn. Jakob	Datum Marz 82	Bezeichnung CRT-Board-B 119		
Geprüft.	Datum	Ger-Nr	Rev 1.22 3 82/	Blat


LS132
COP420
CKØ
CKI
D1
L7
LO
150
47p
220
33
220
CS
1K
11K
LS374
OE
DØ
D7
A3_L
A4_L
A2_L
A1_L
GØ
IN3
IN2
IN1
LS175
A4
A3
A2
A1
A4_L
A3_L
A2_L
A1_L