

GAUNTLET™

Schematic Package Supplement to the Gauntlet™ Operators Manual



NOTE

This staple temporarily holds the schematic package together. Remove the staple before using these schematics.



NOTE

In the schematics printed on Sheets 1-16 a slash (/) in front of a signal name indicates an active low signal. In the signal name glossary (printed at the end of this schematic package) these signals are over-scored, e.g., COMPSYNC.

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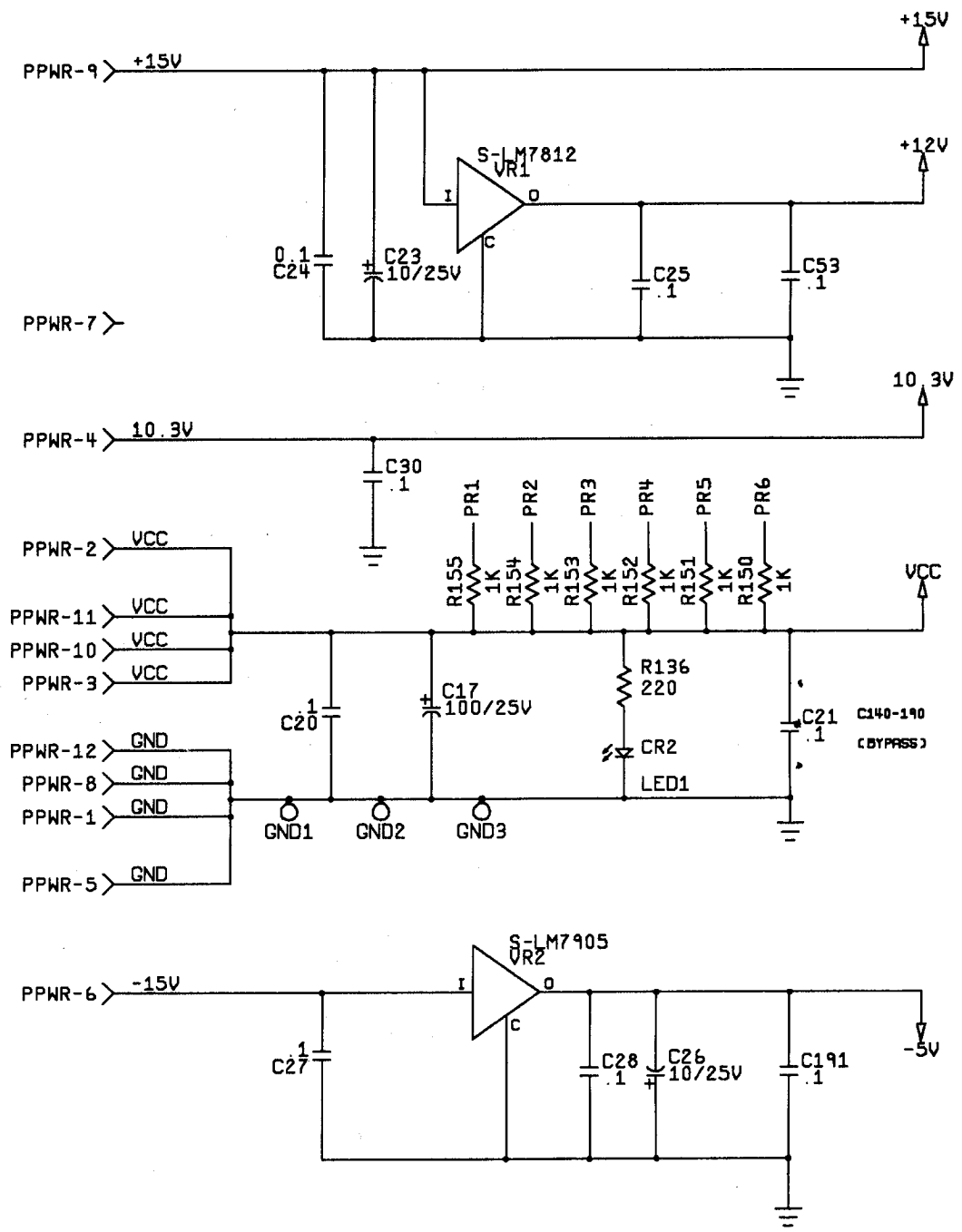
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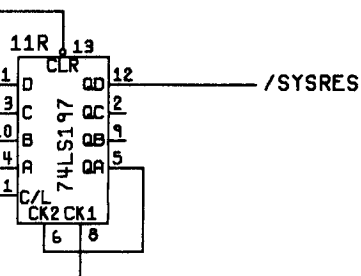
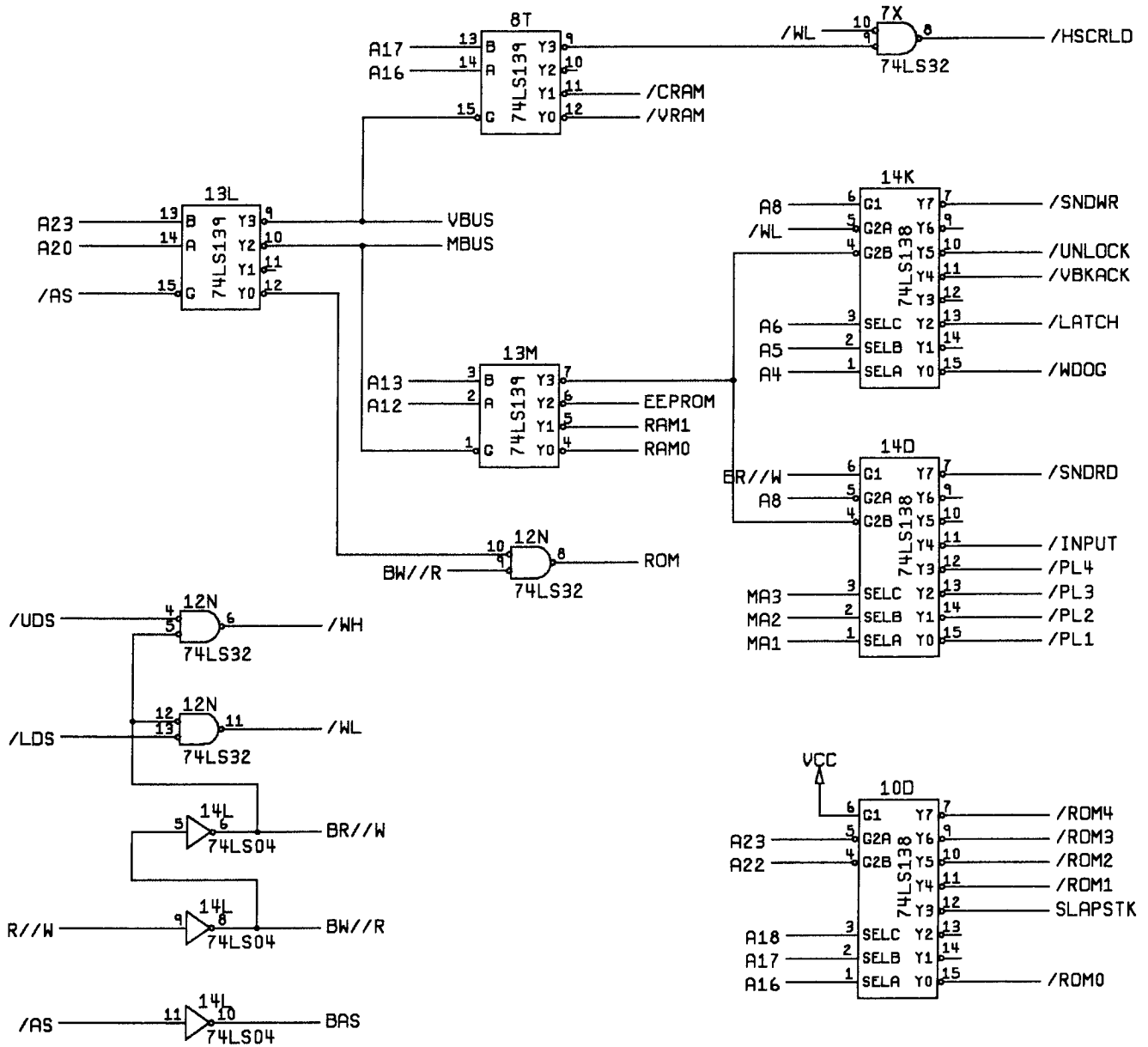


**Gauntlet™ Game PCB
Schematic Diagram**

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**SP-284 Sheet 1
1st printing**



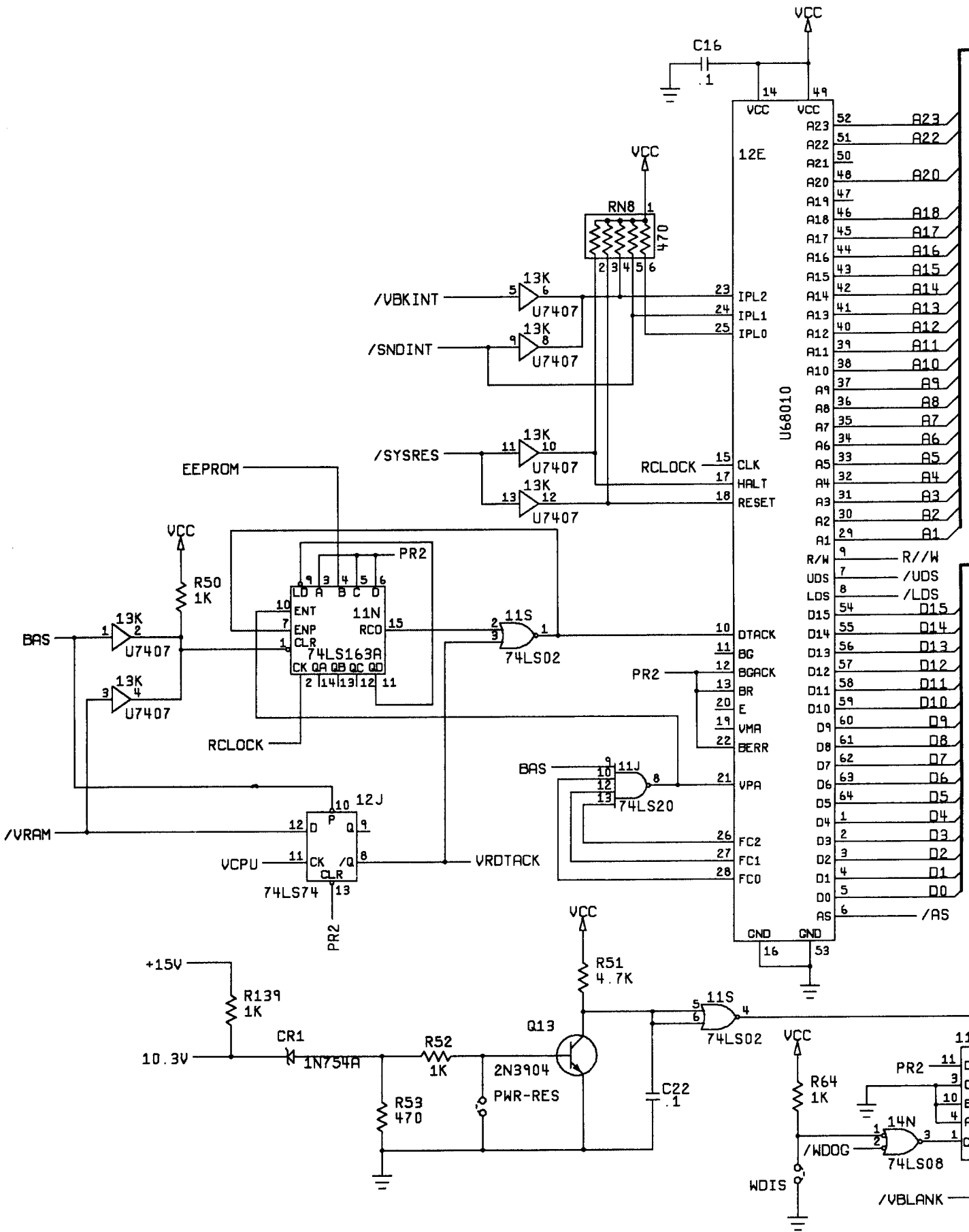


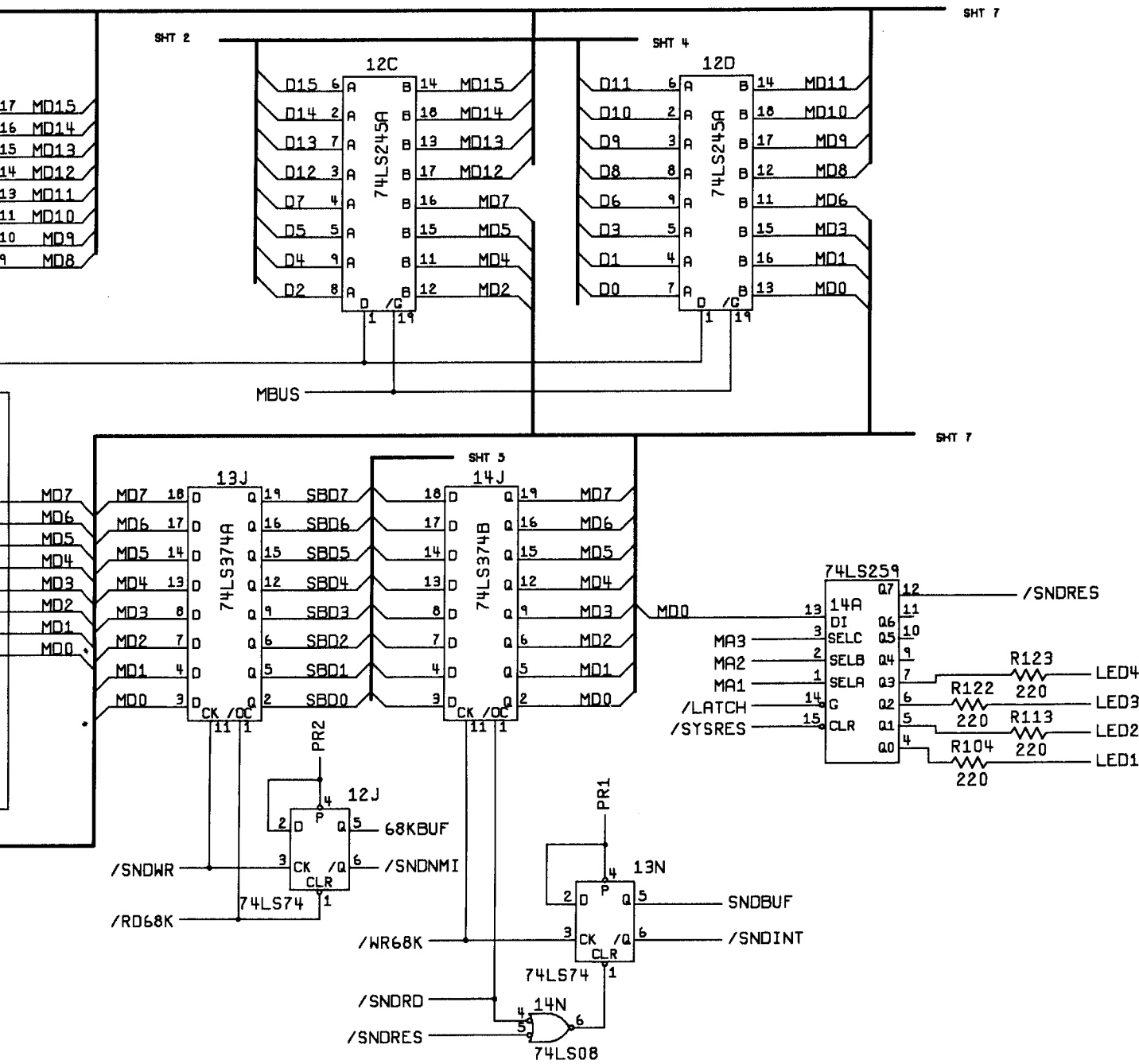
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Gauntlet™ Game PCB Schematic Diagram



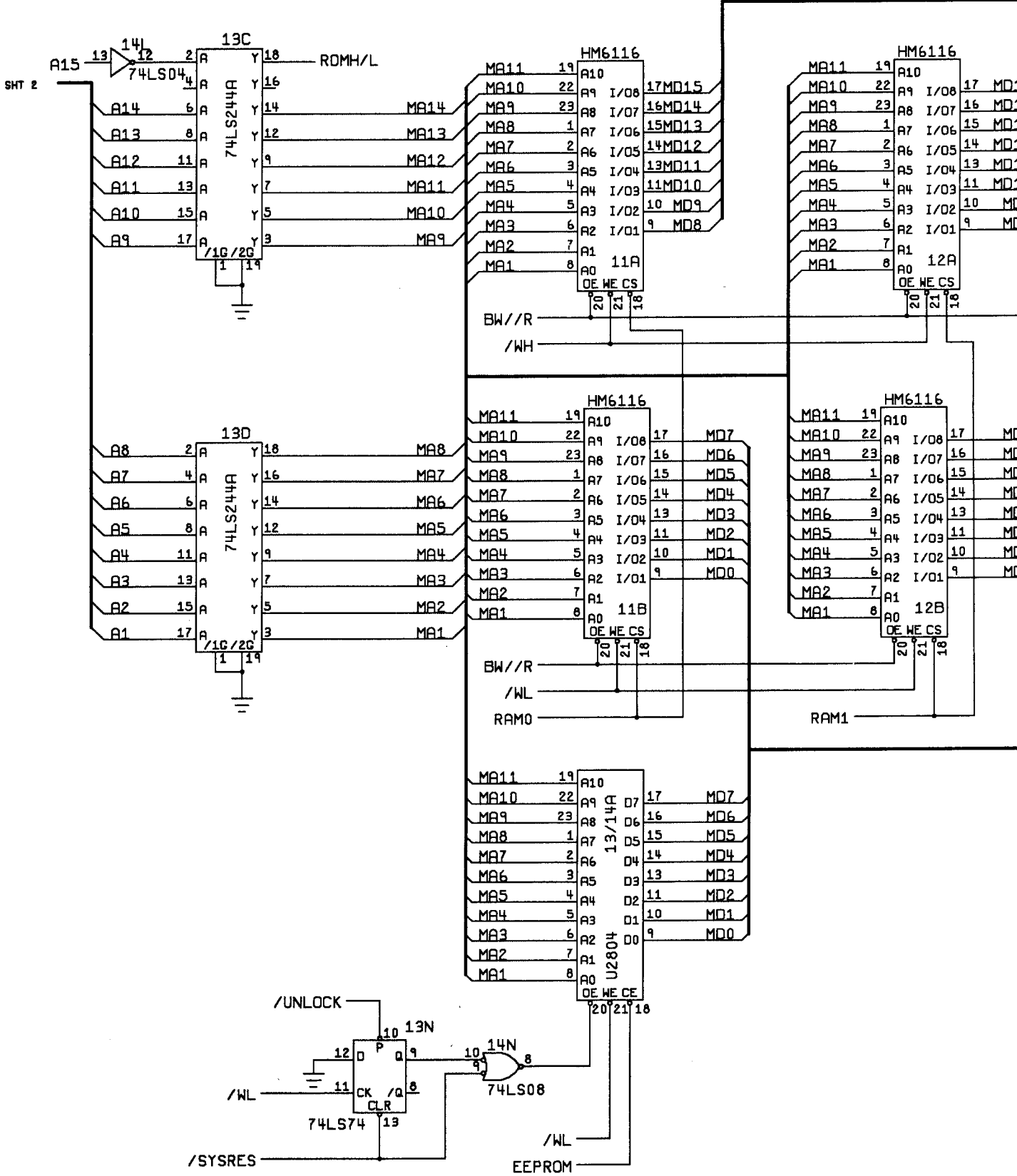


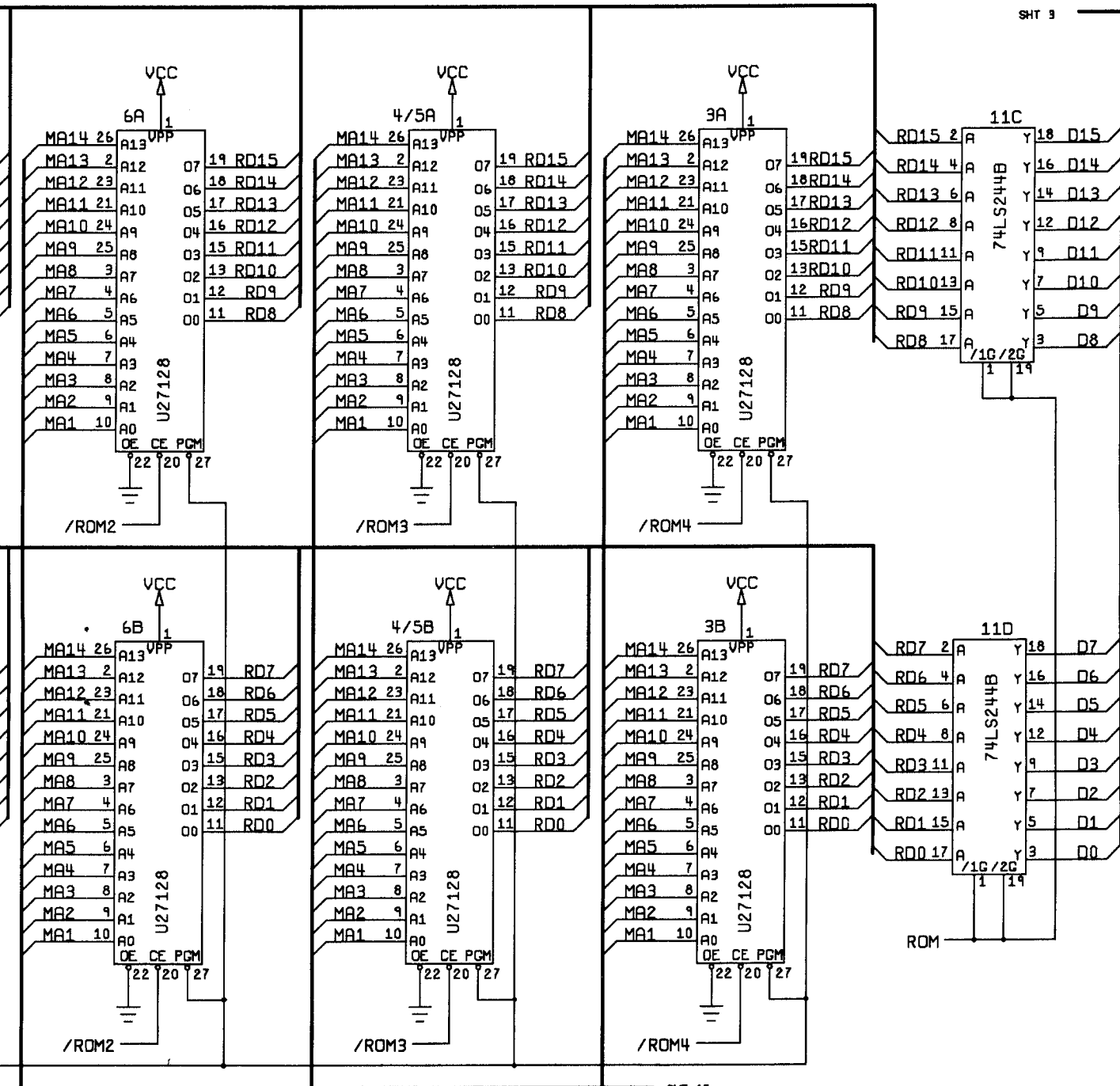
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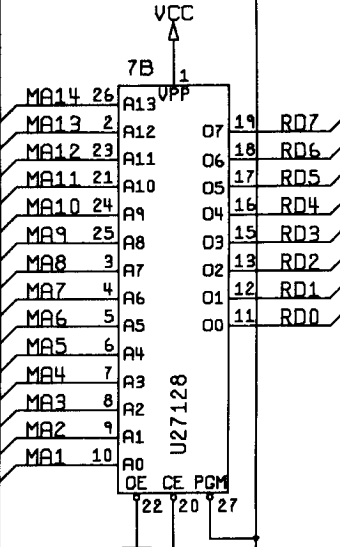
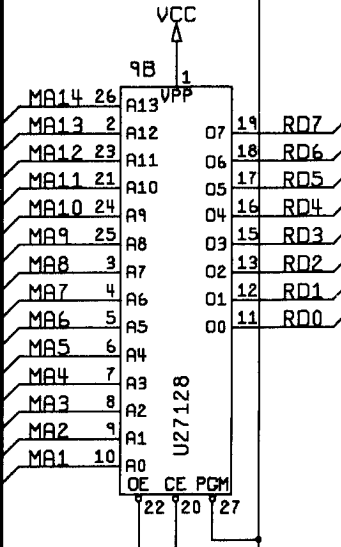
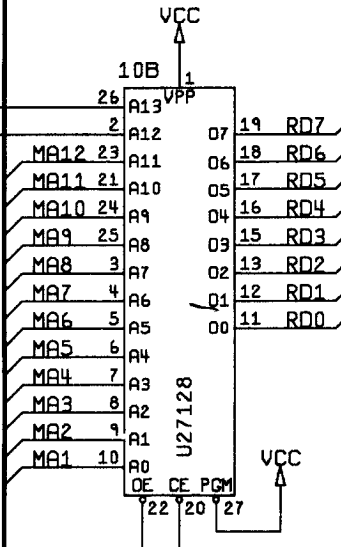
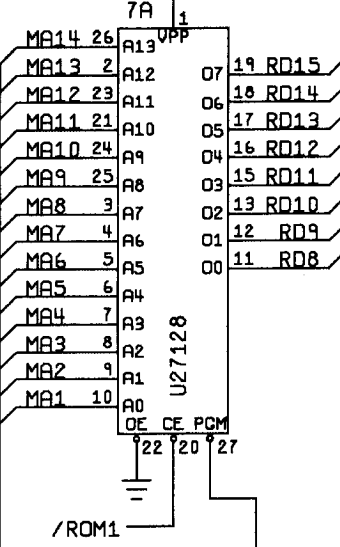
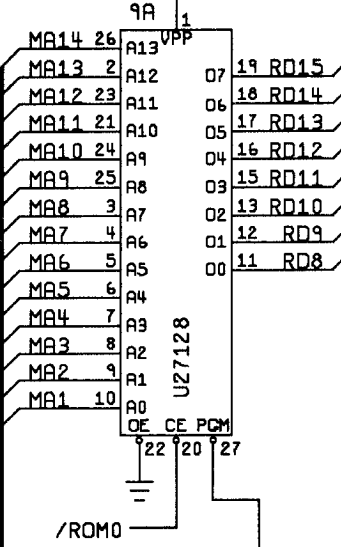
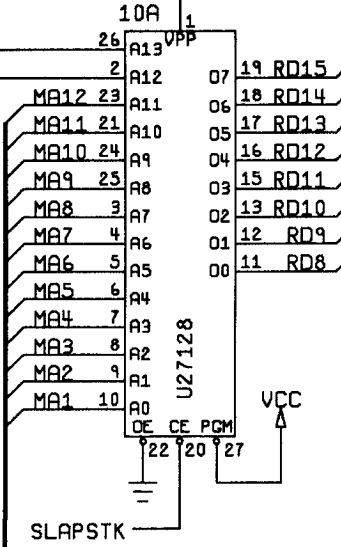
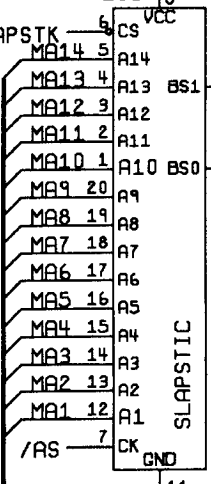
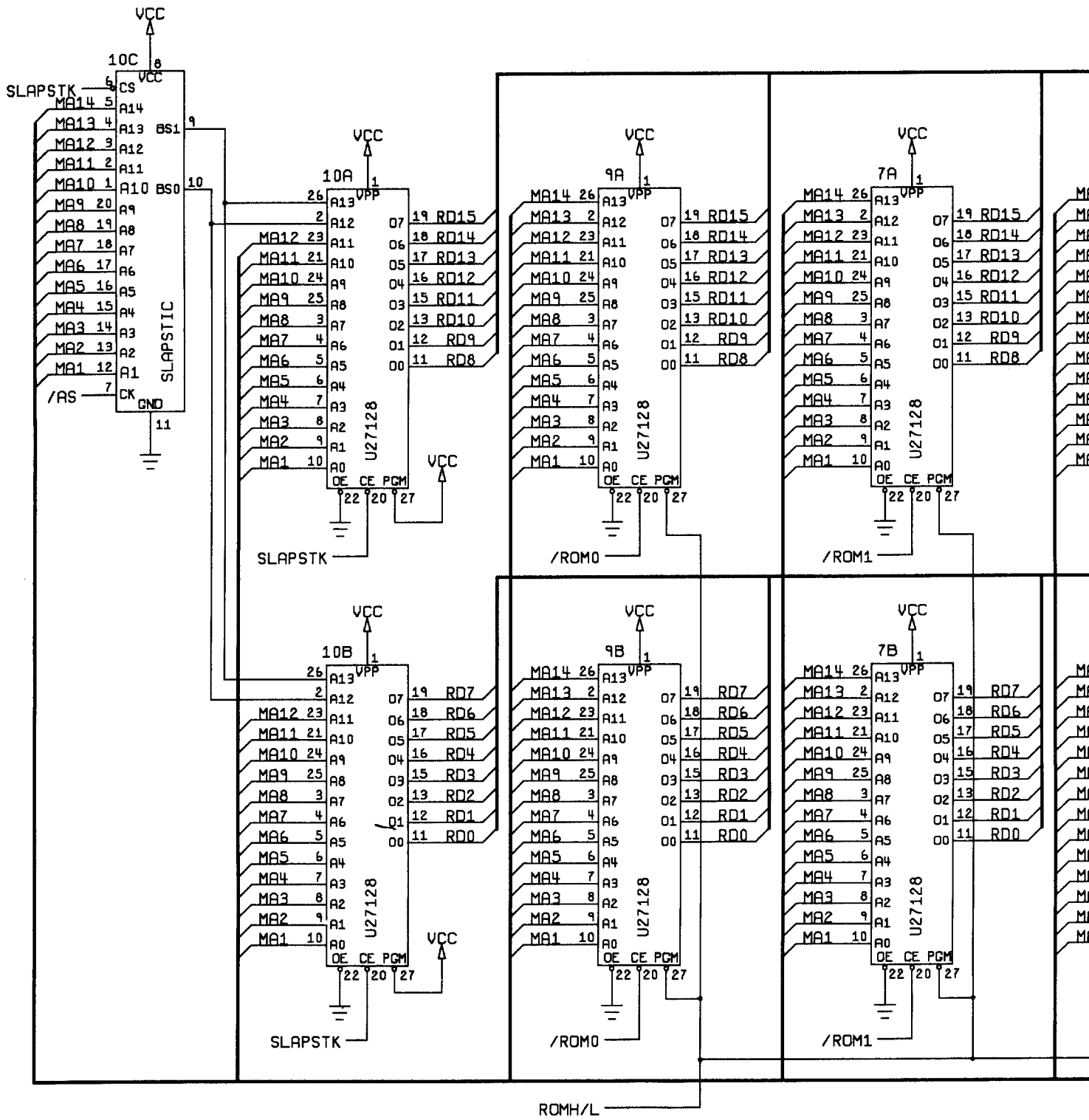


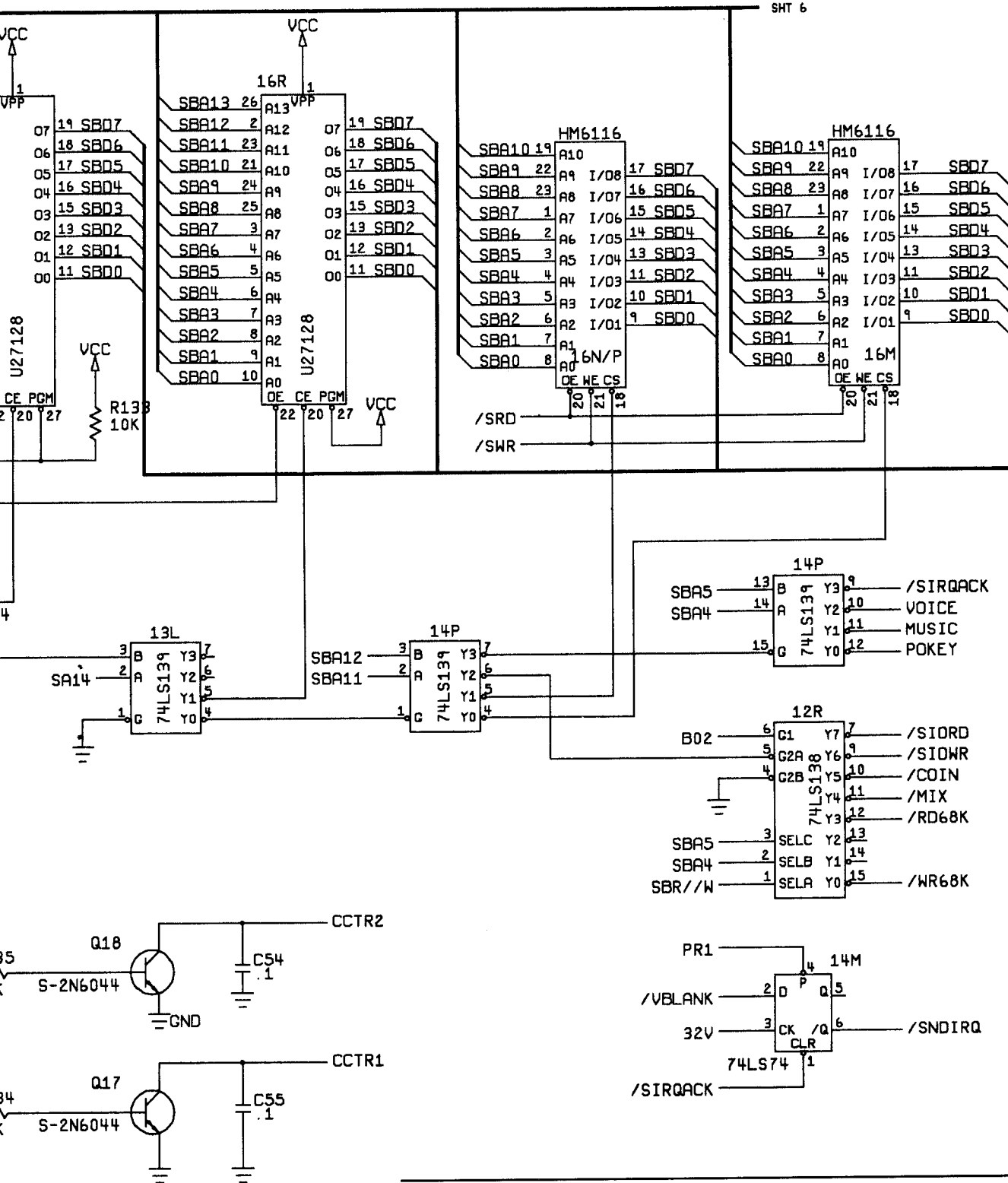
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Gauntlet™ Game PCB Schematic Diagram



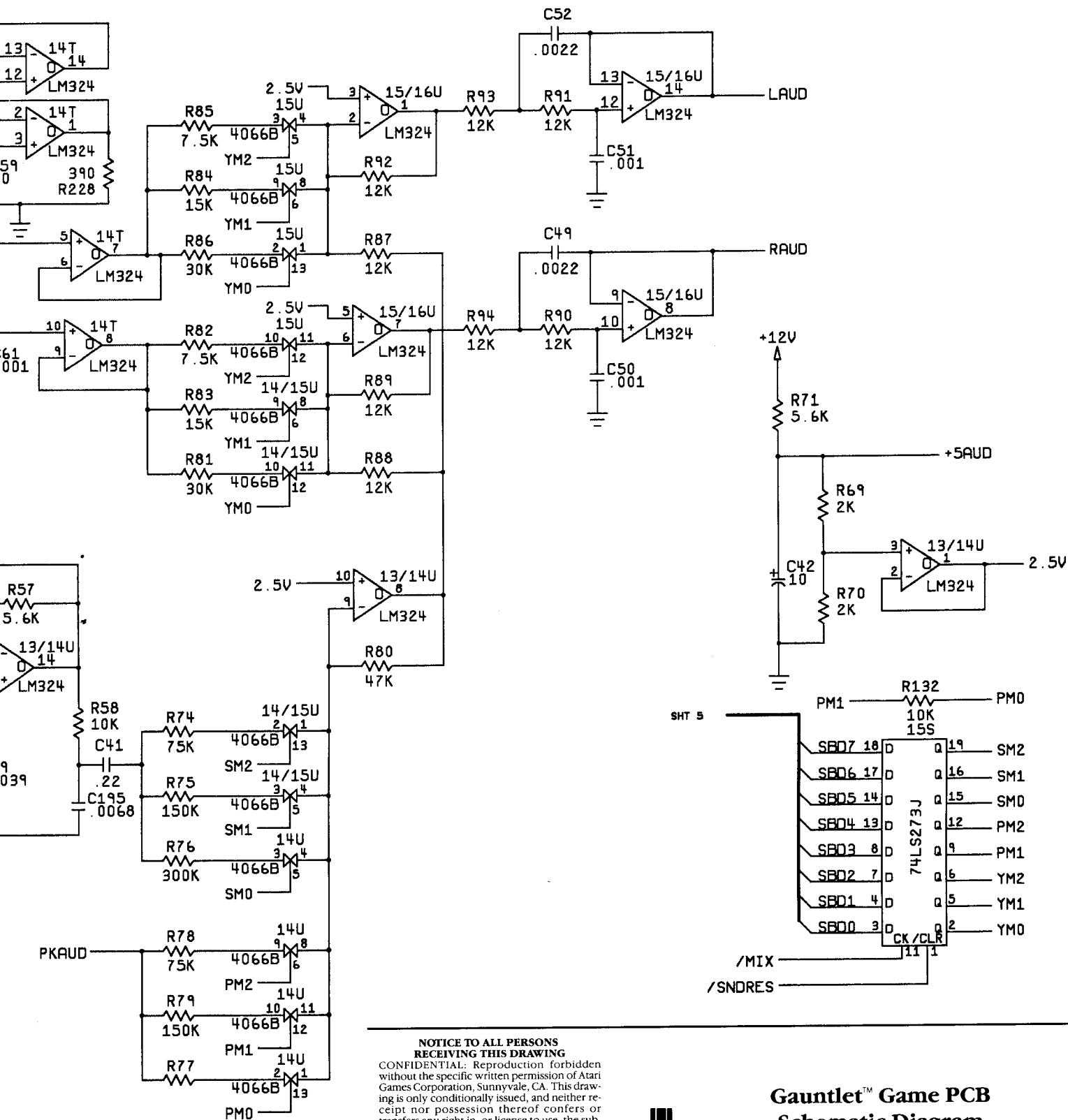


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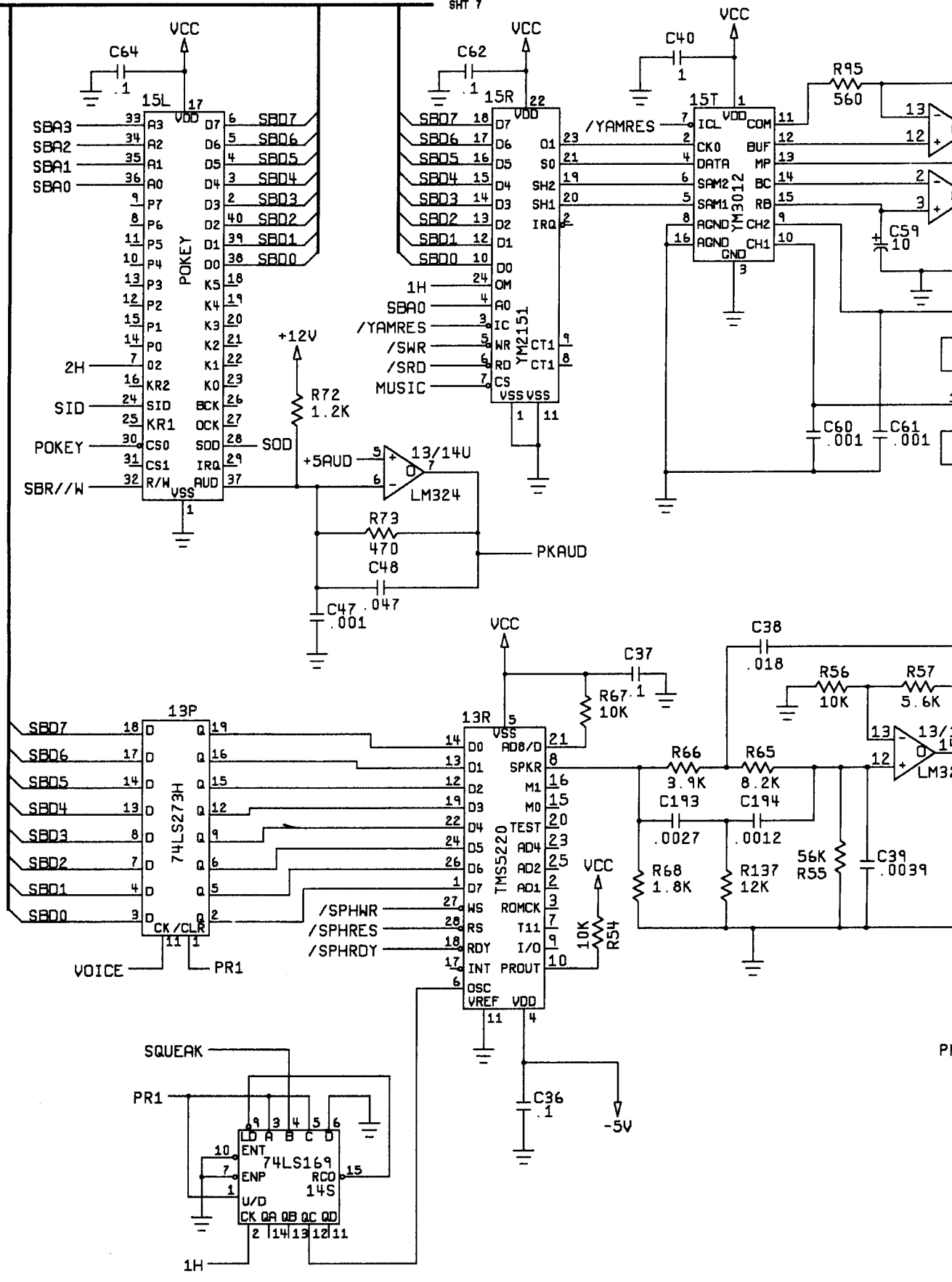


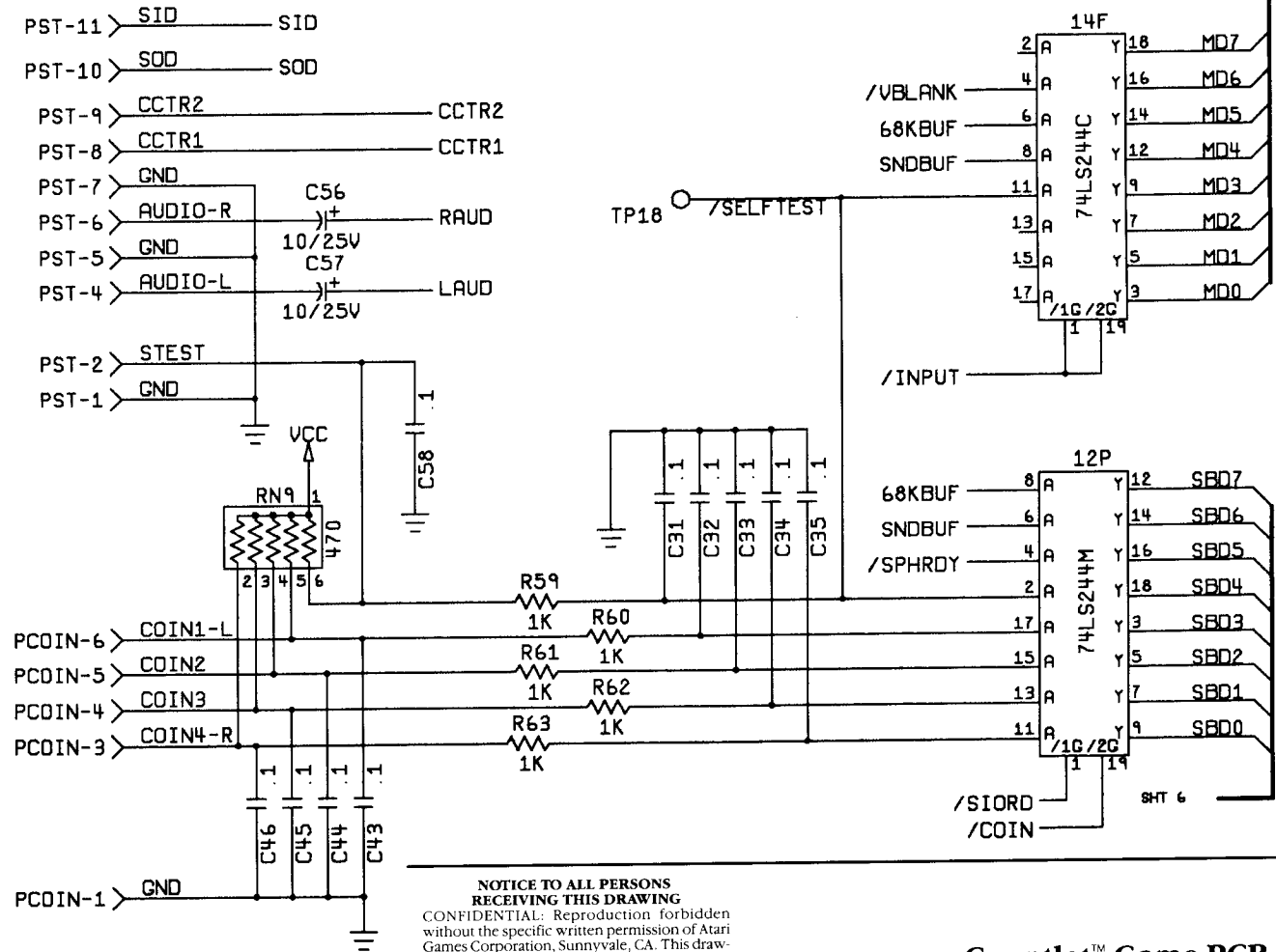
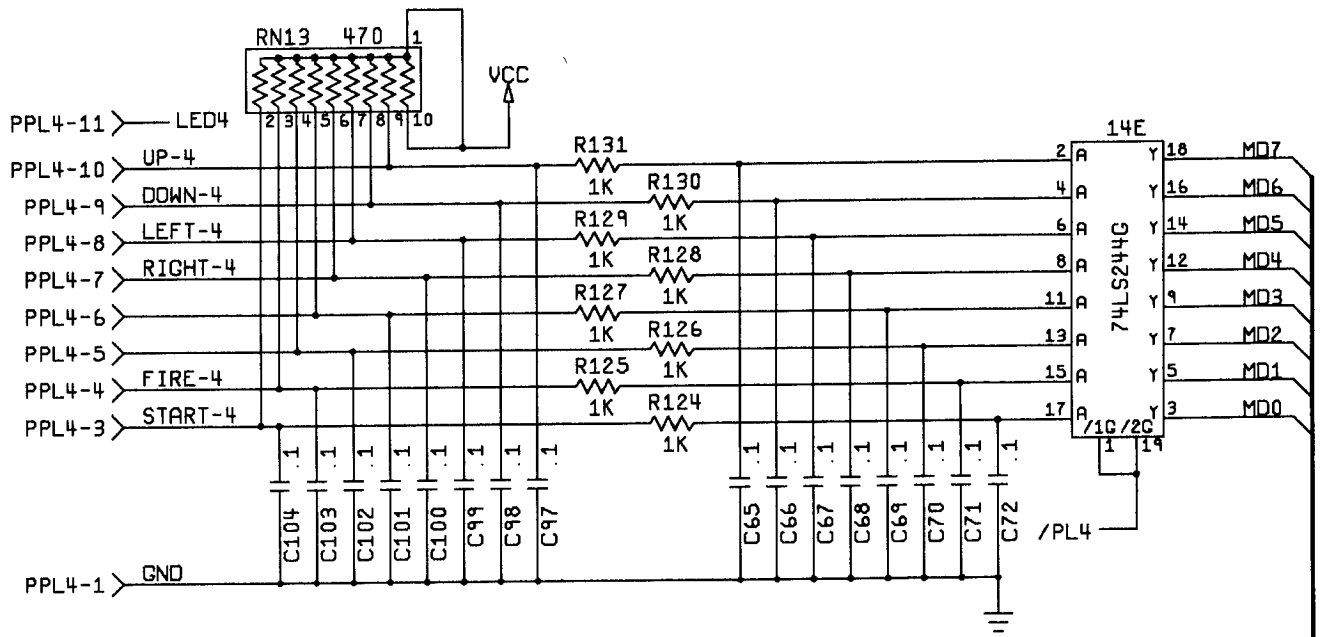
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Schematic Diagram**



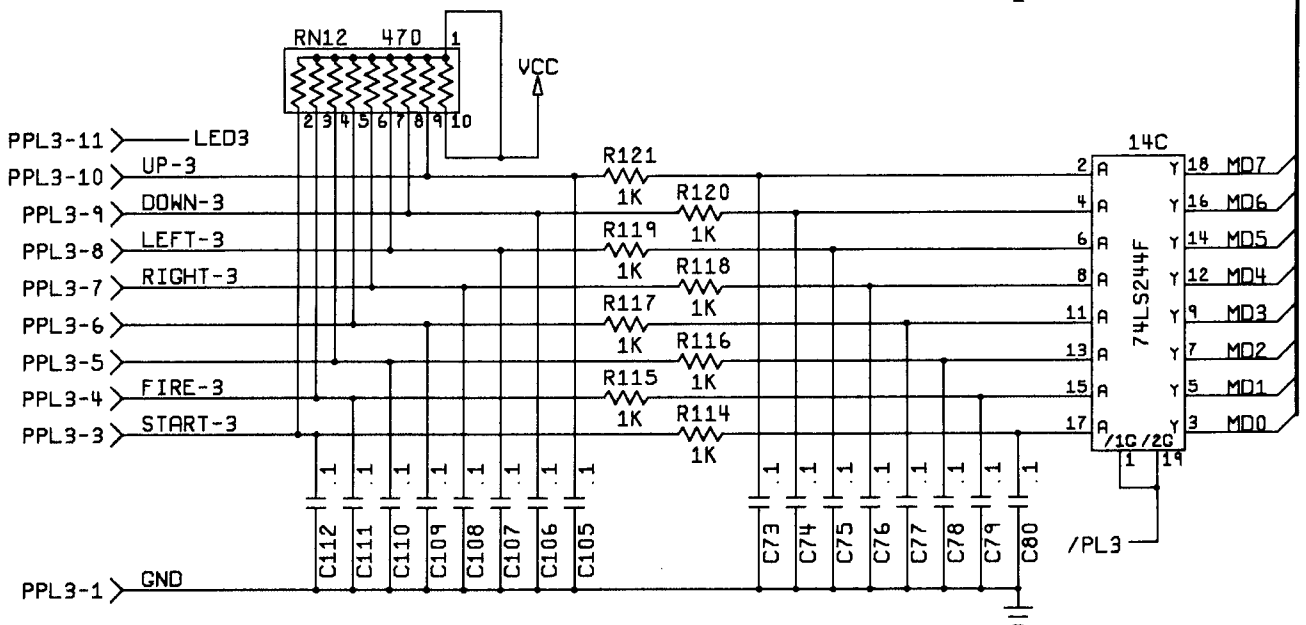
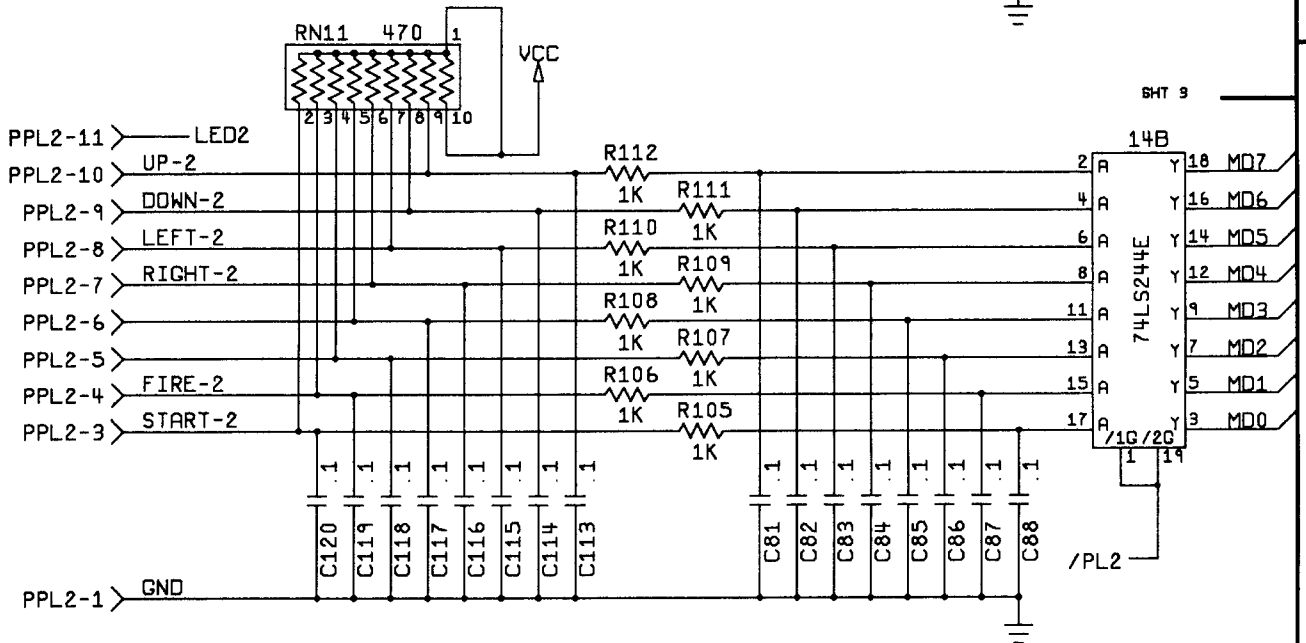
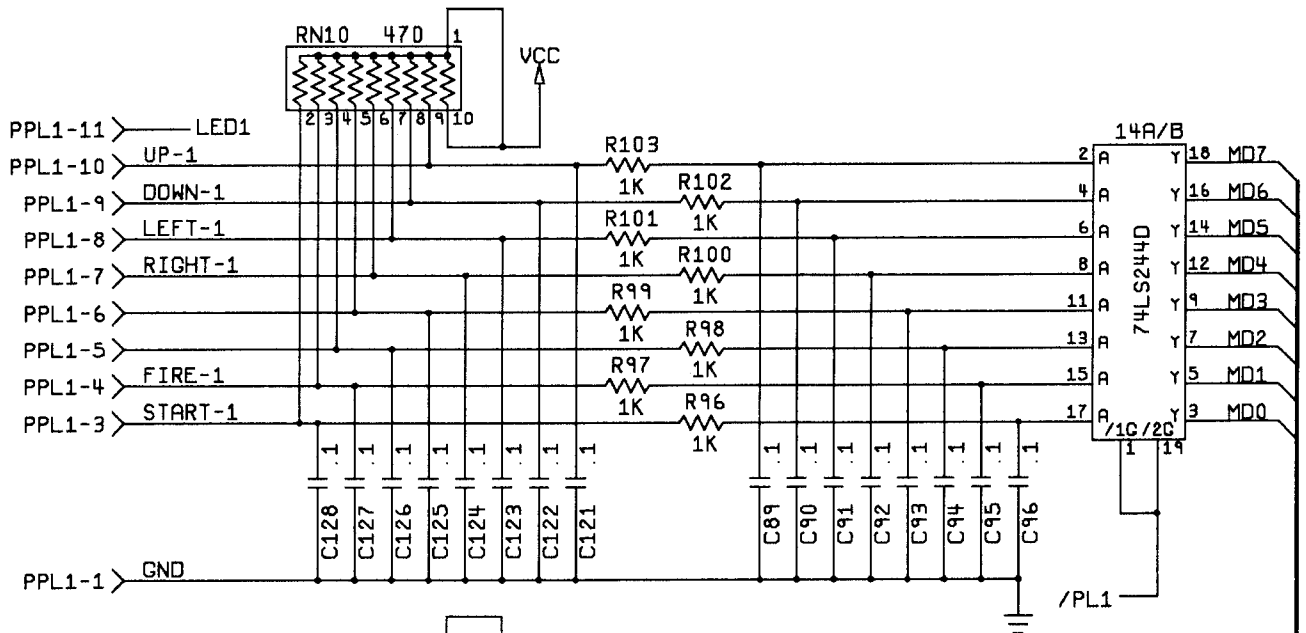


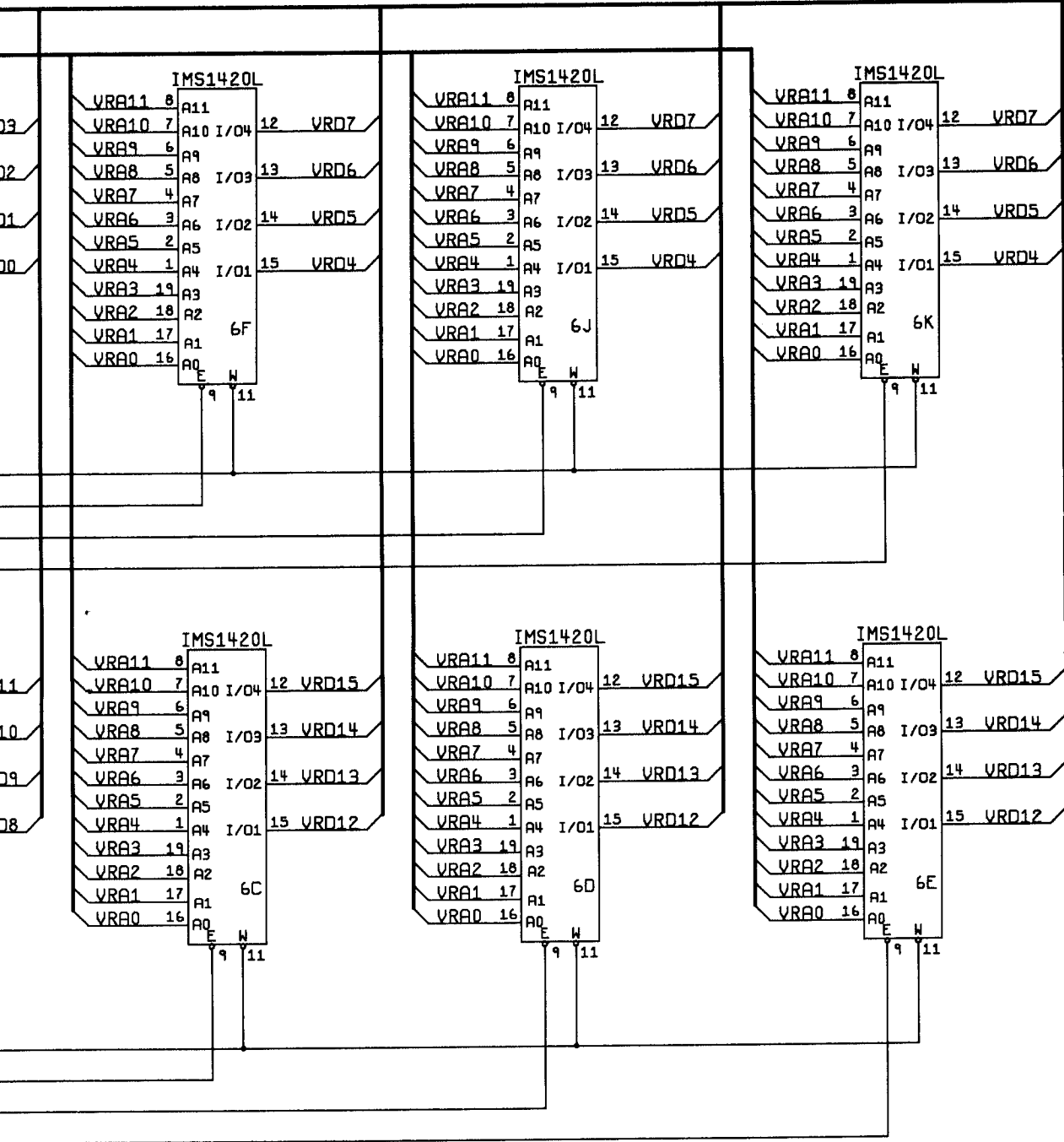
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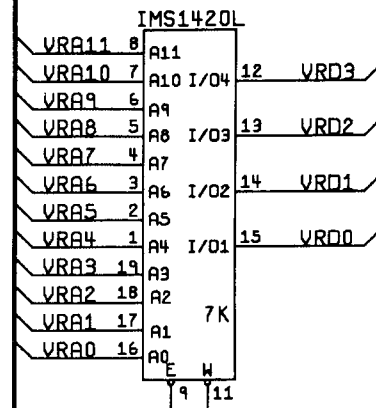
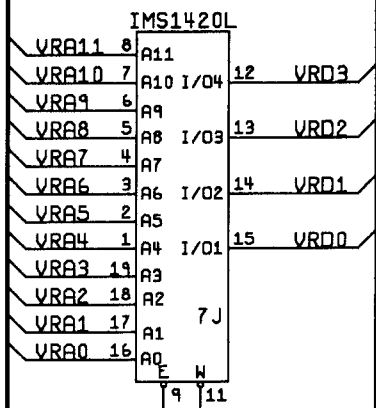
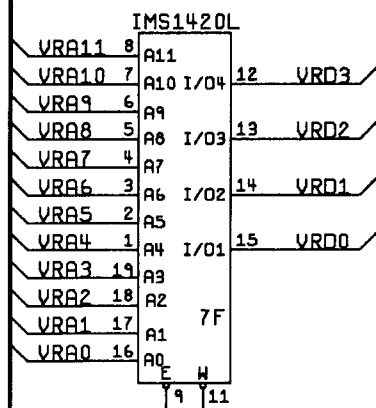
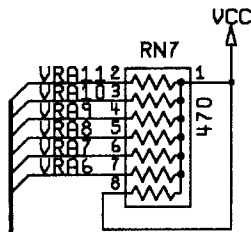


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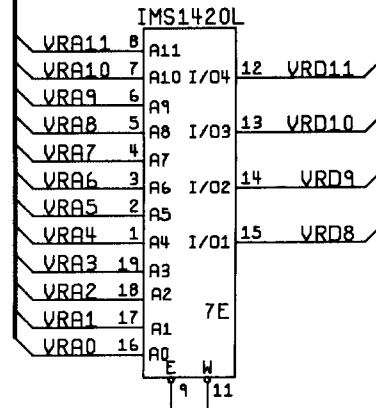
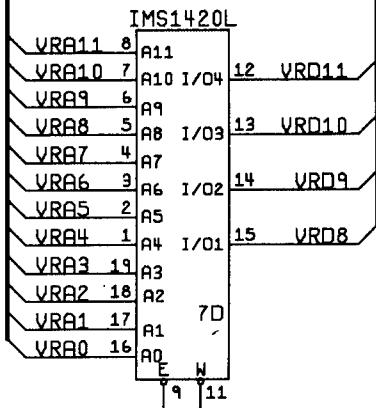
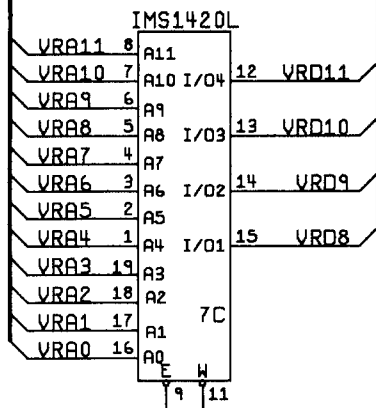
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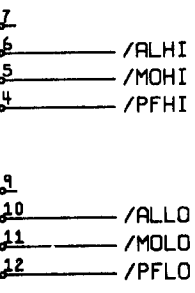
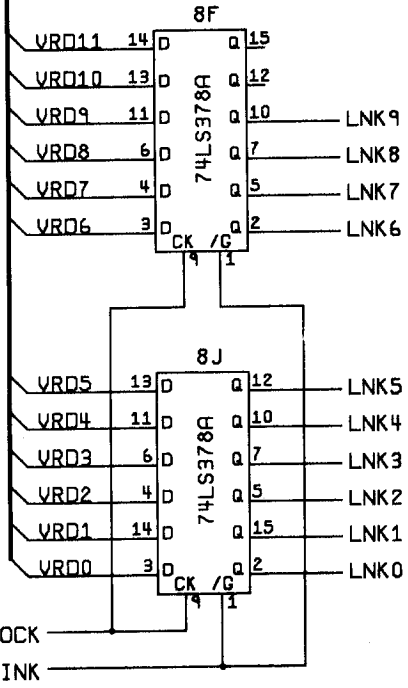
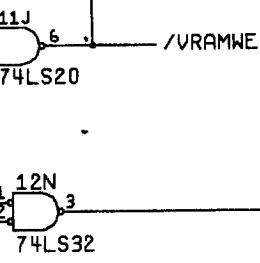
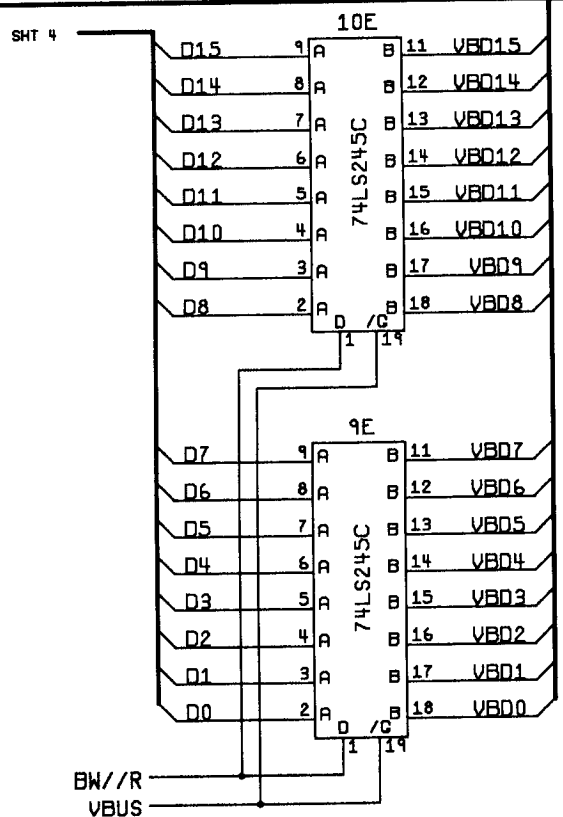
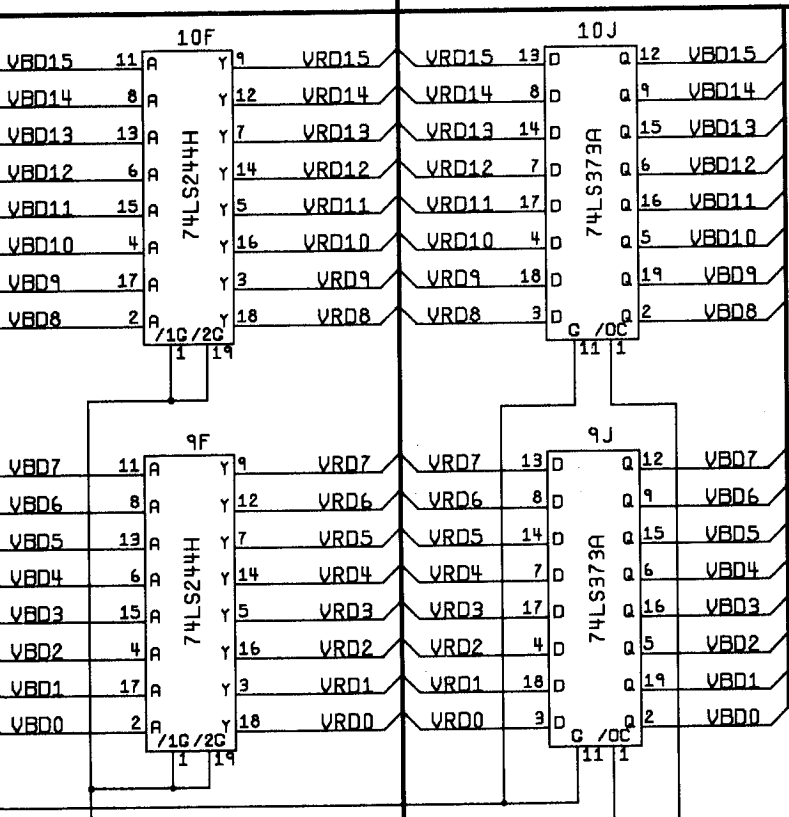
Gauntlet™ Game PCB Schematic Diagram



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/PFLO
/ALLO



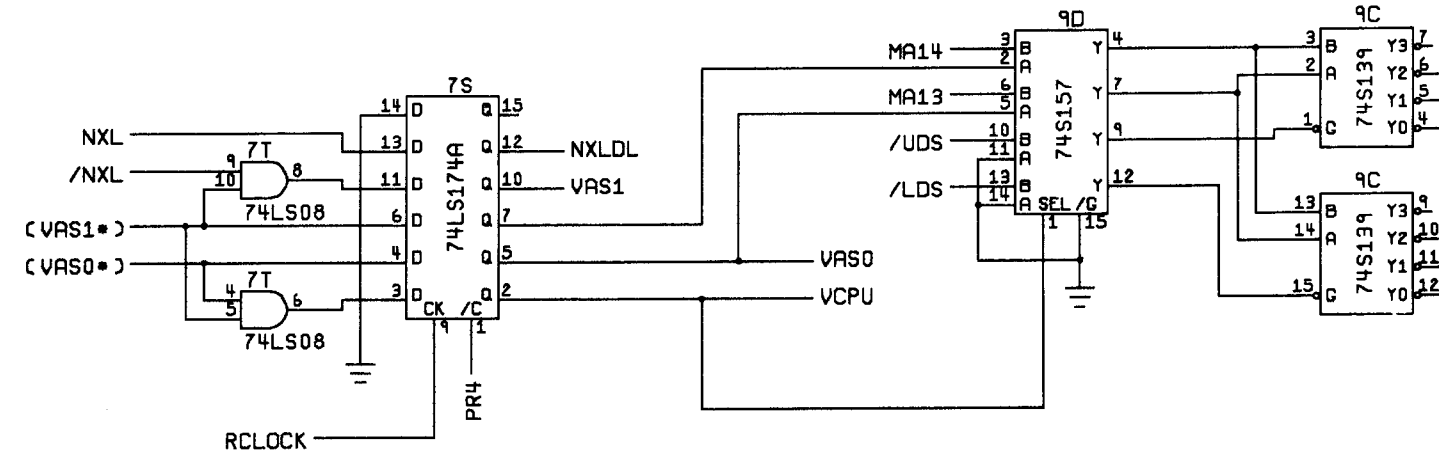
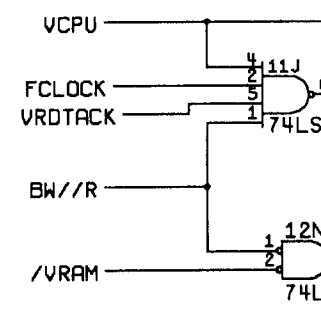
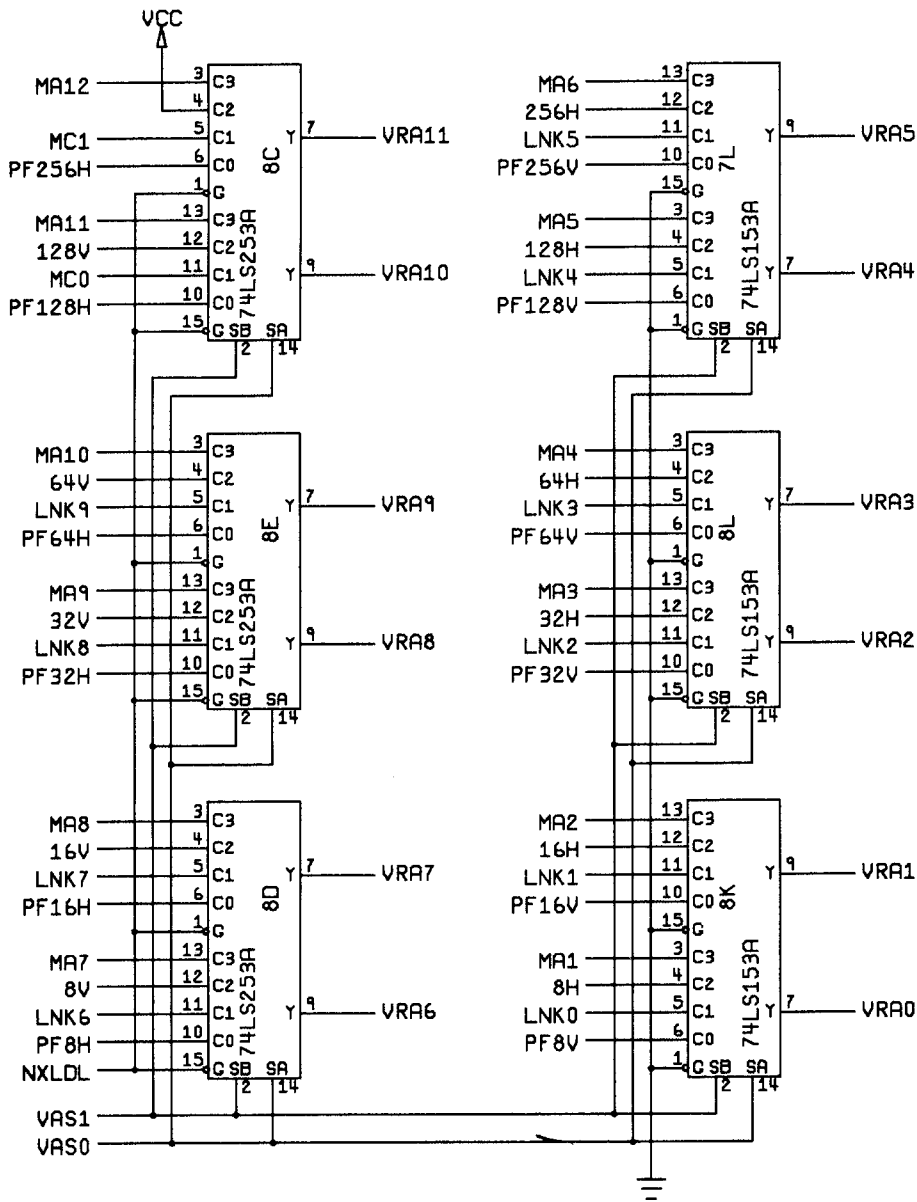
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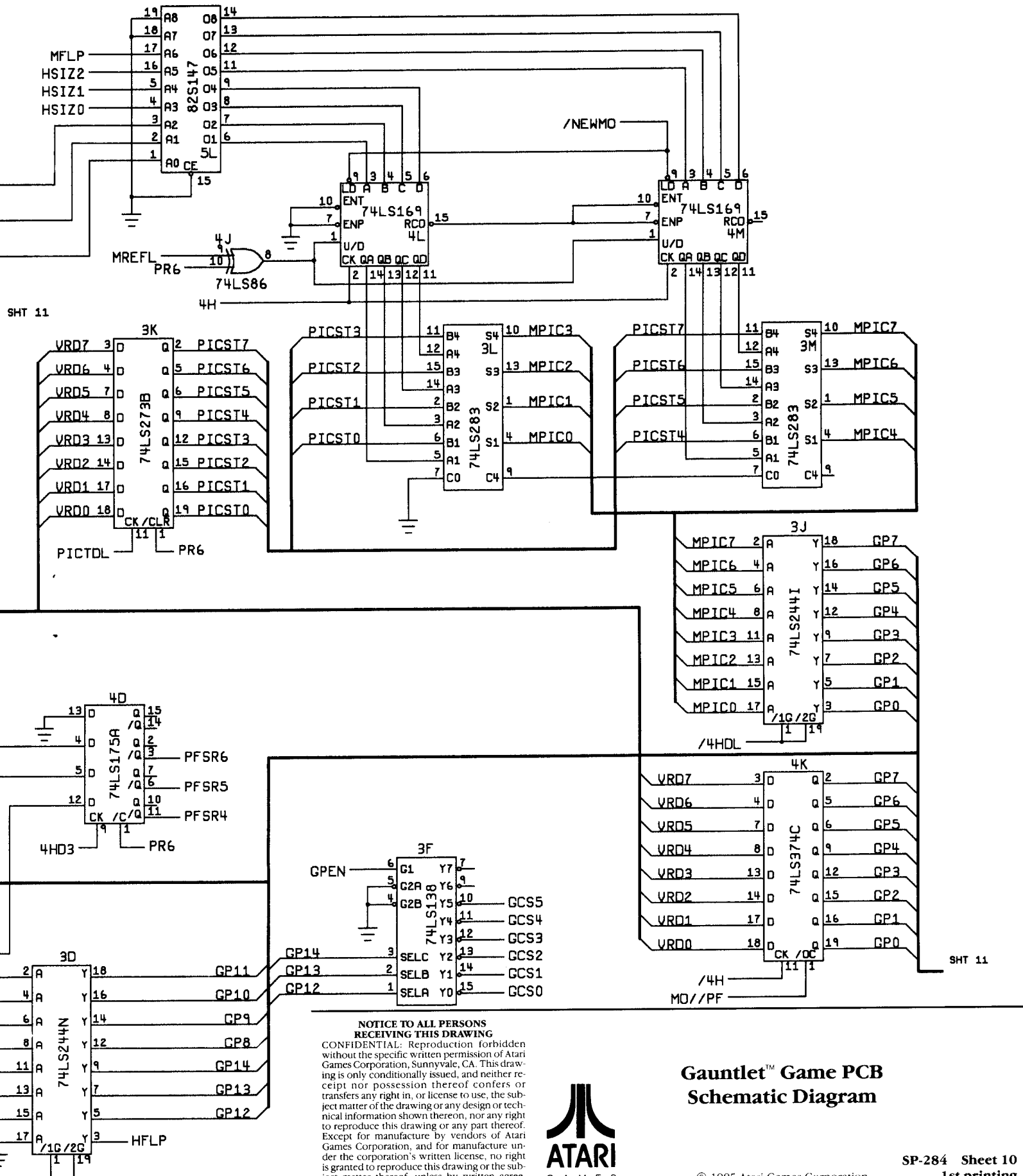


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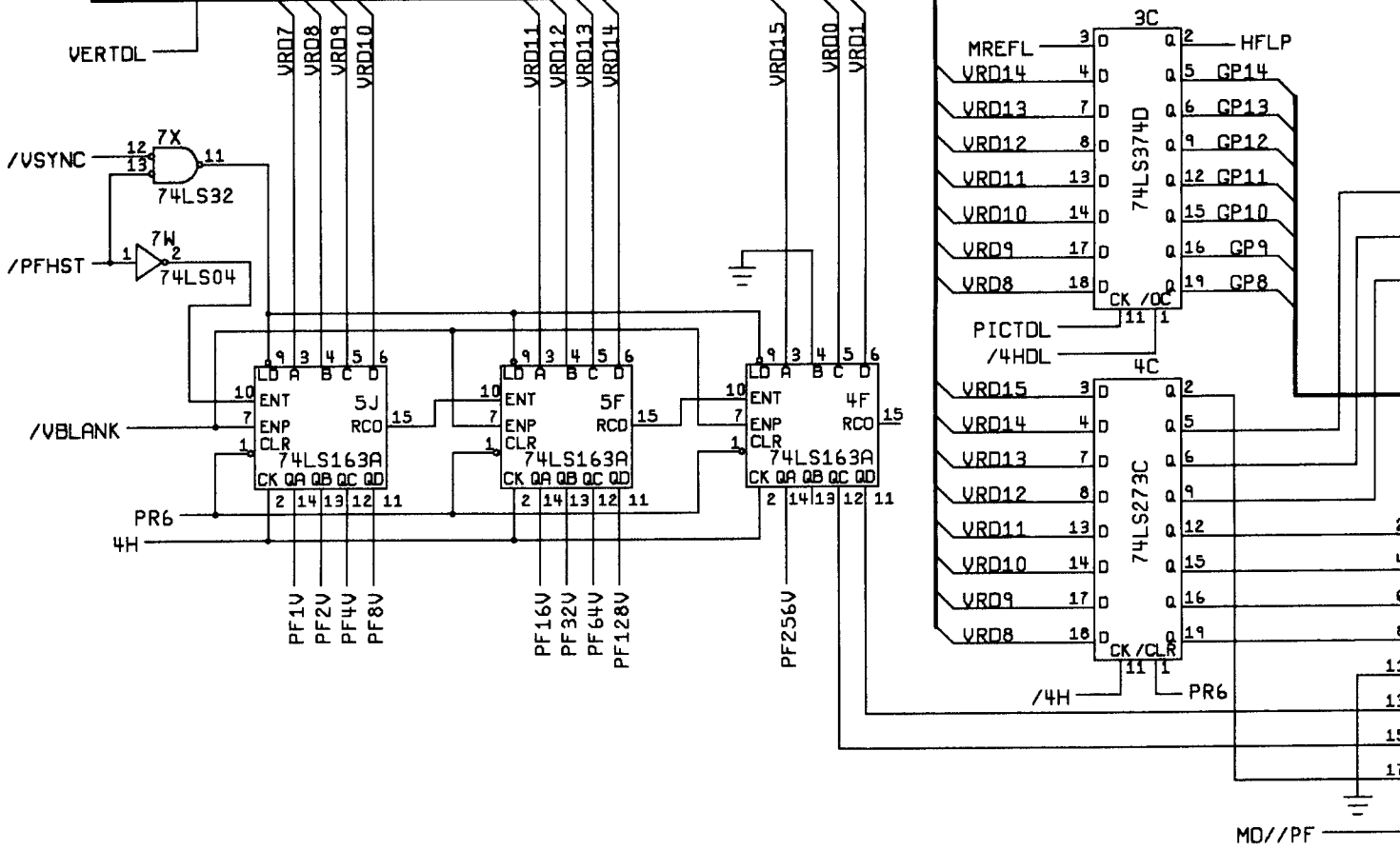
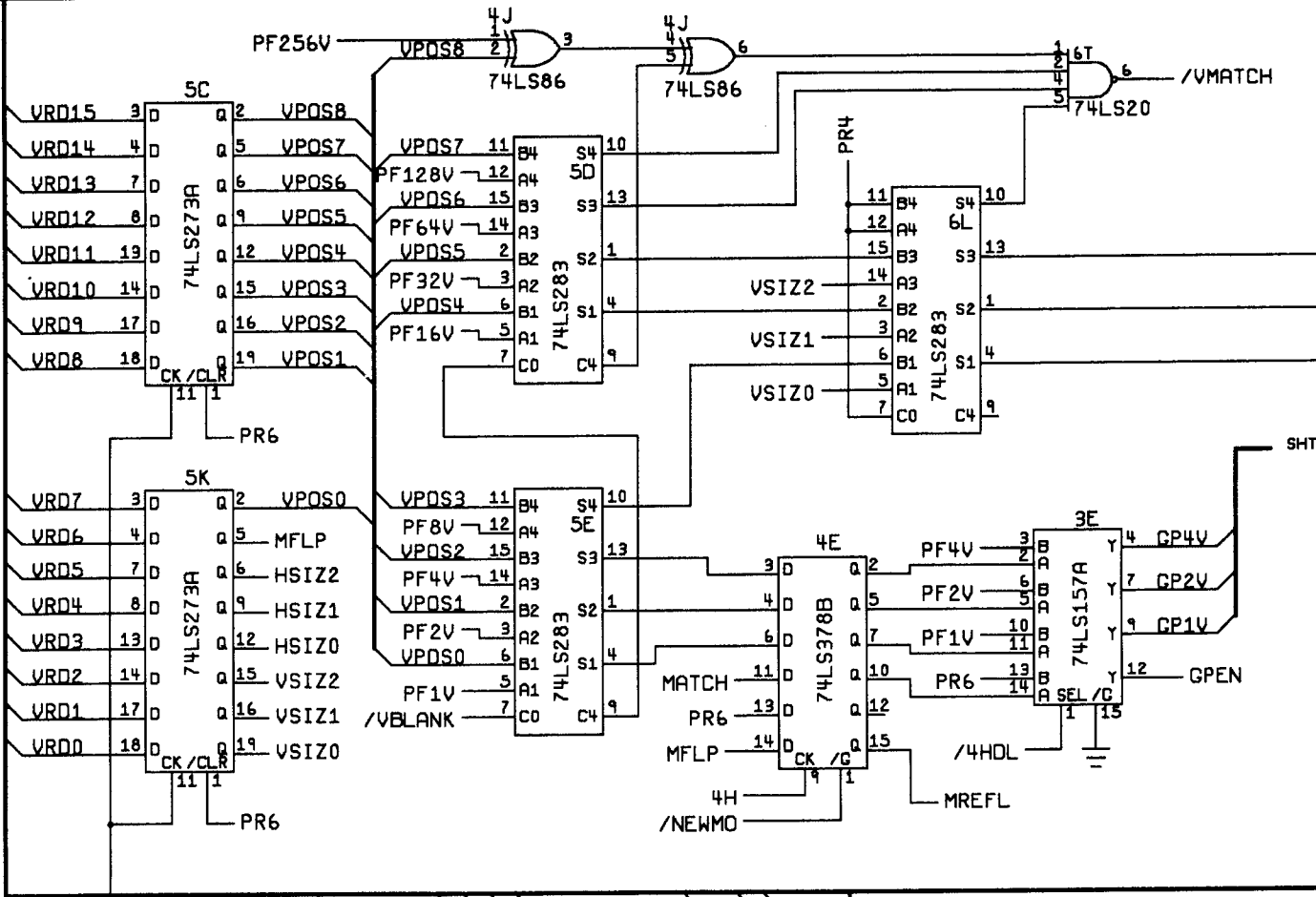


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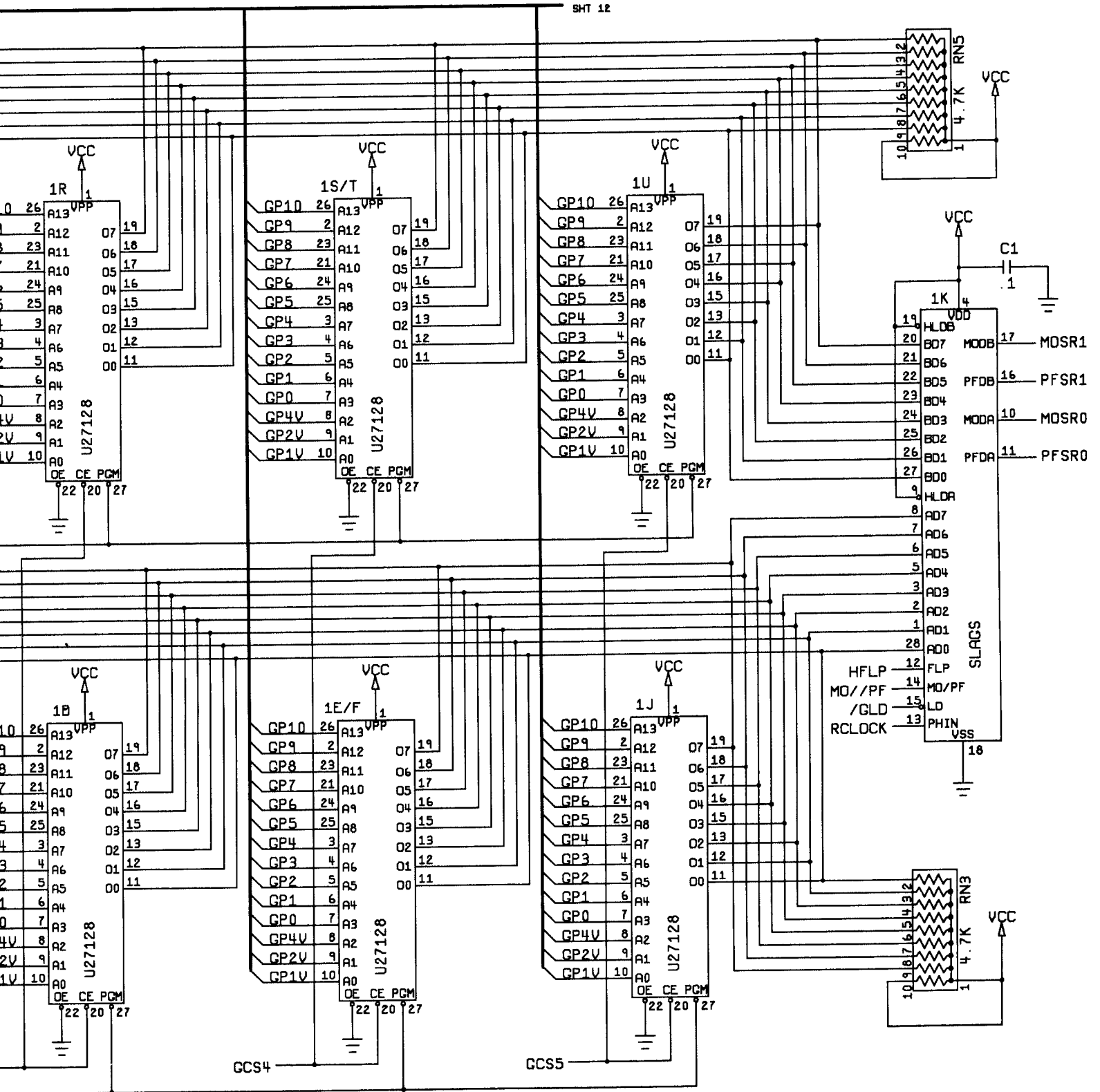


Gauntlet™ Game PCB Schematic Diagram

SHT 9 SHT 14



MD//PF



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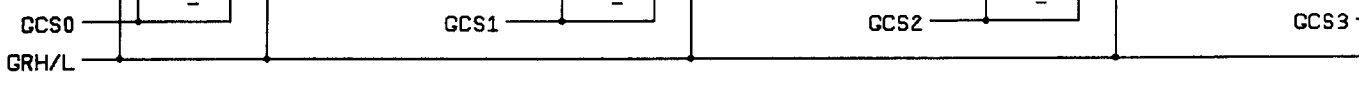
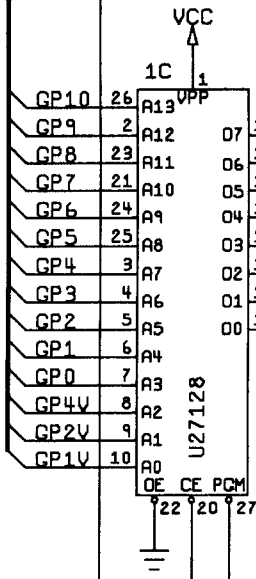
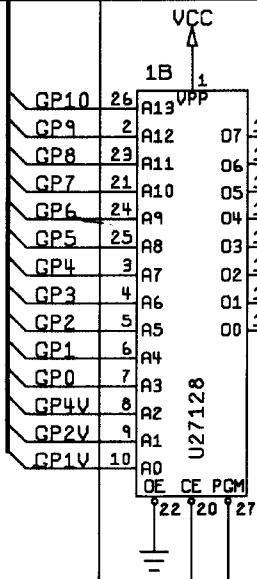
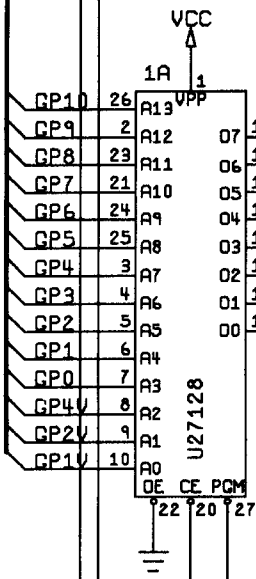
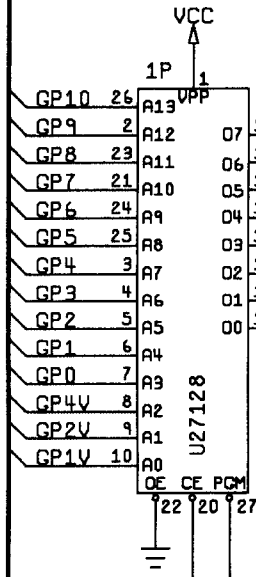
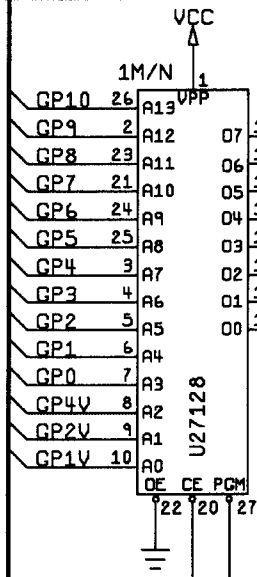
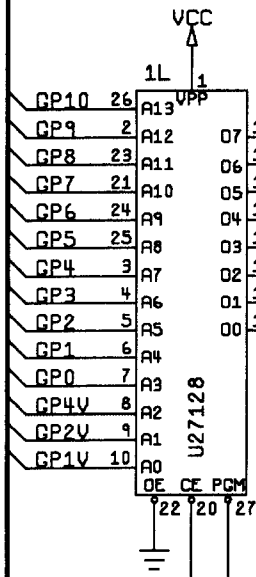
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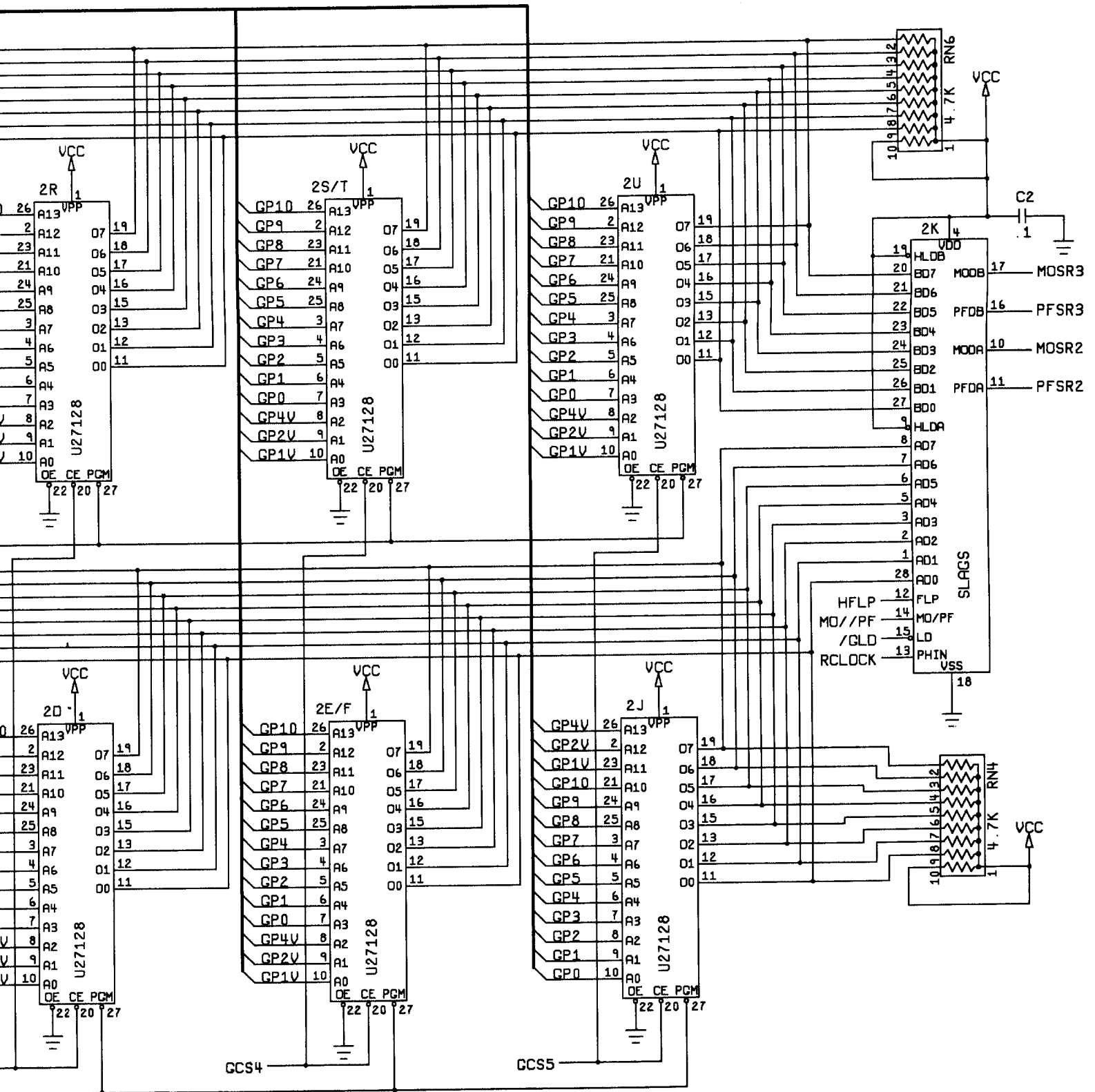


Gauntlet™ Game PCB Schematic Diagram

PLANE 1

PLANE 0





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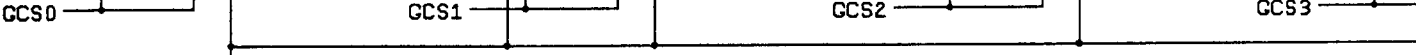
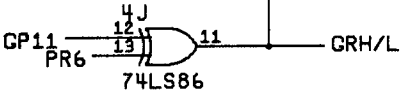
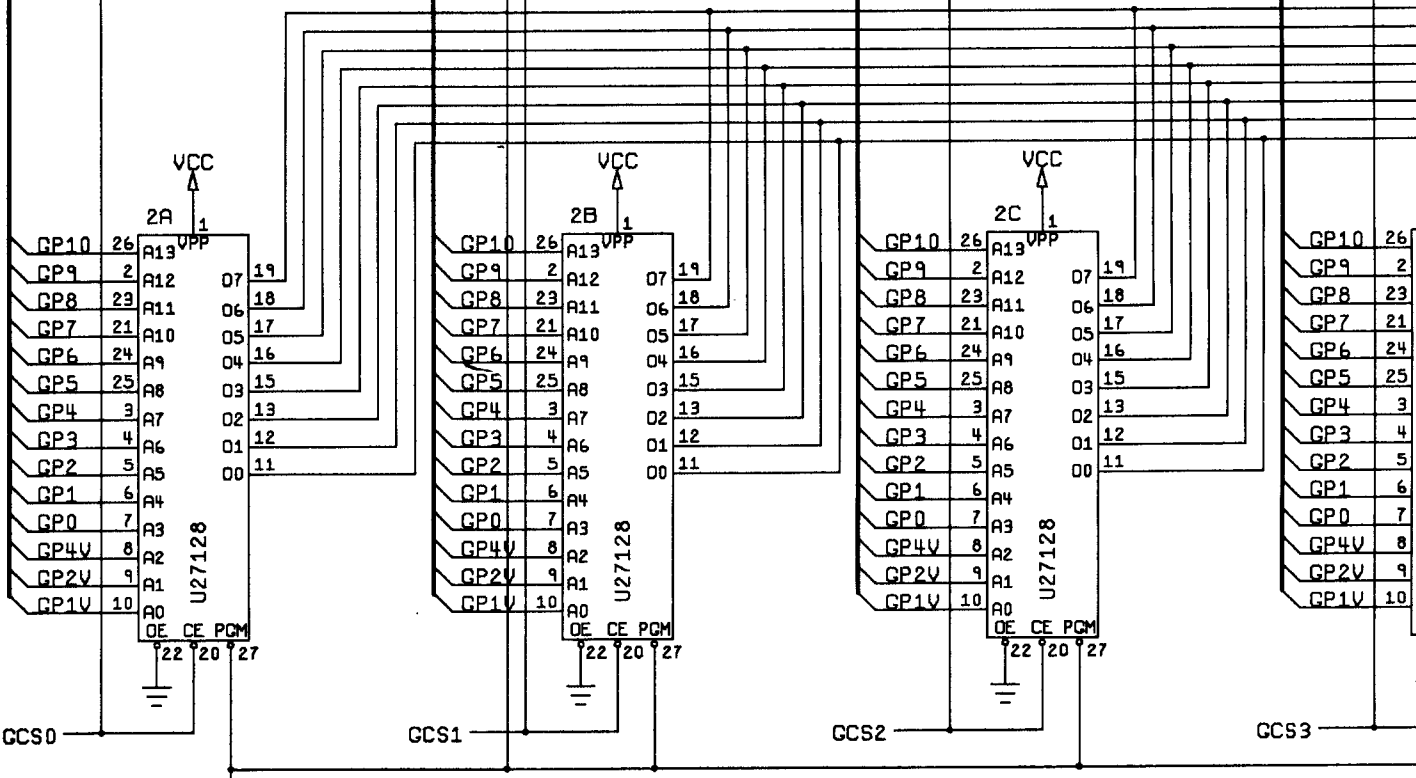
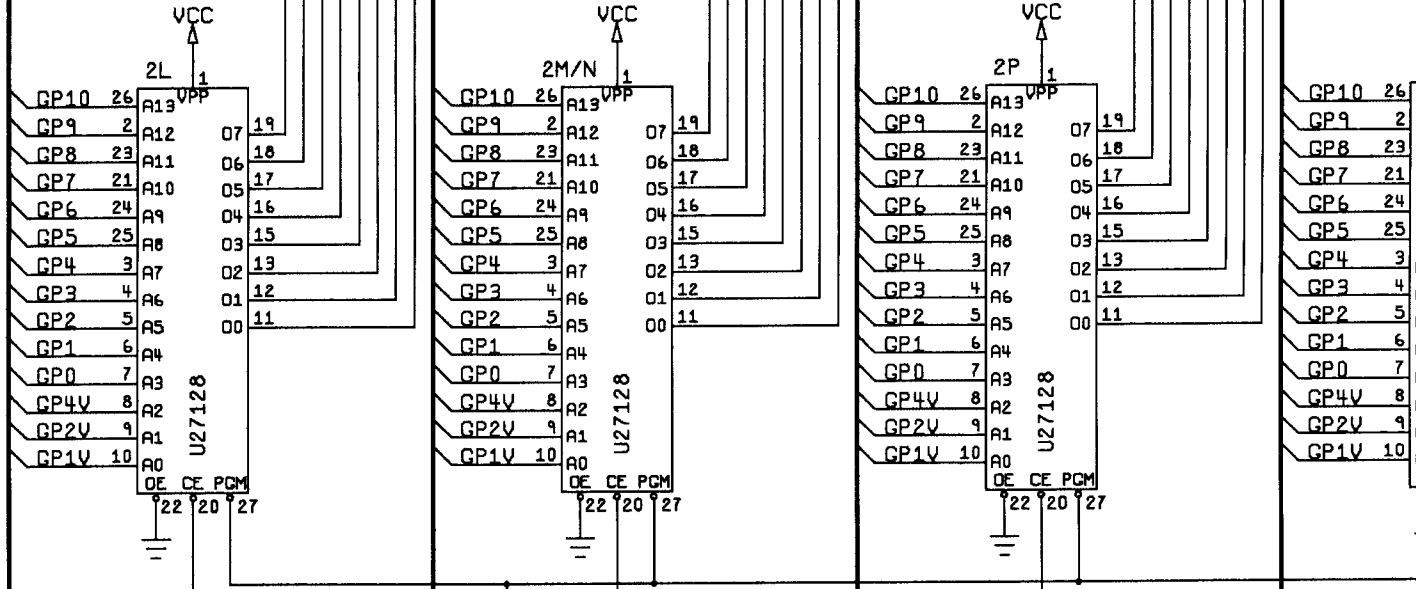
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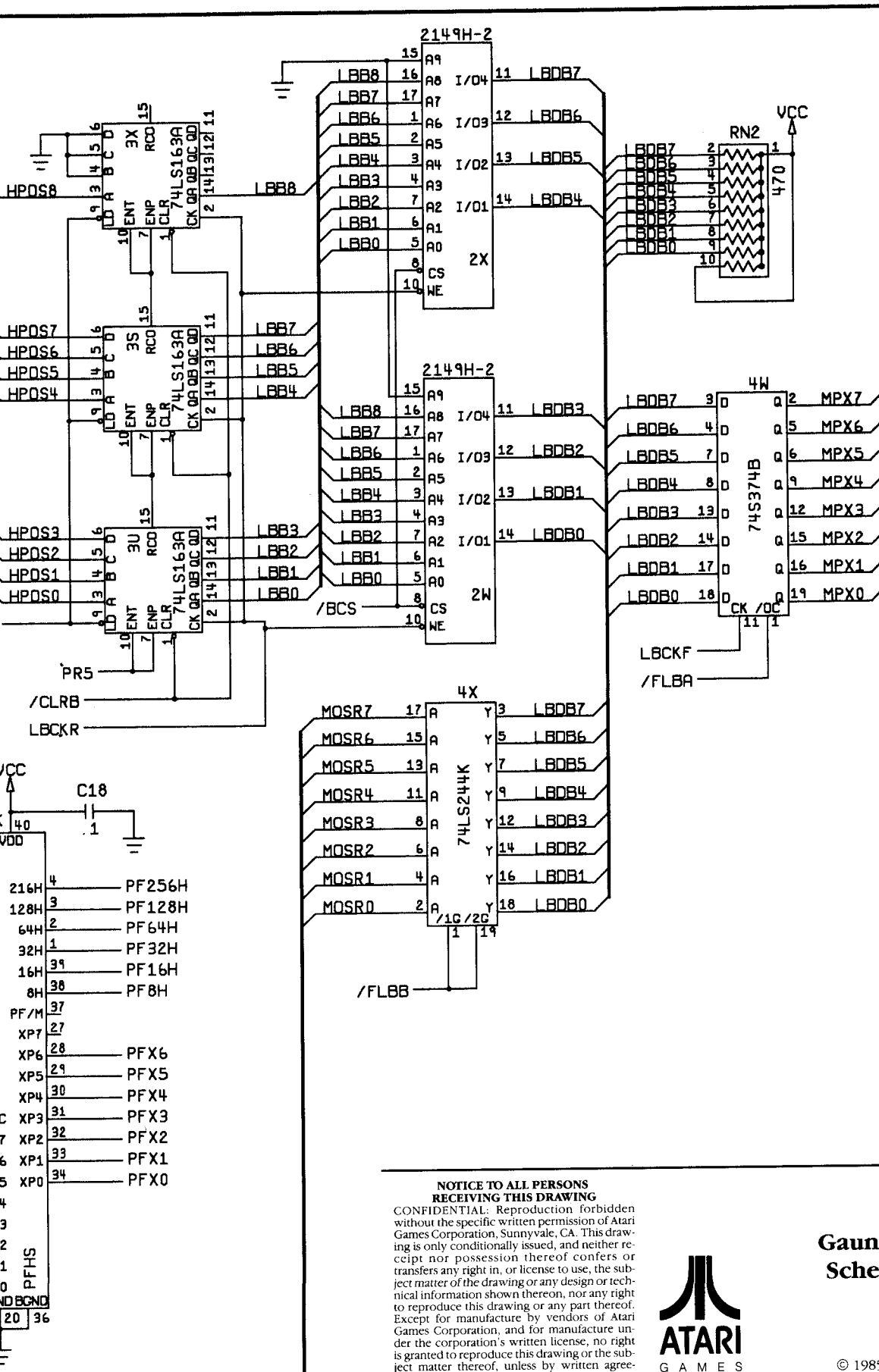


**Gauntlet™ Game PCB
Schematic Diagram**

PLANE 3

PLANE 2



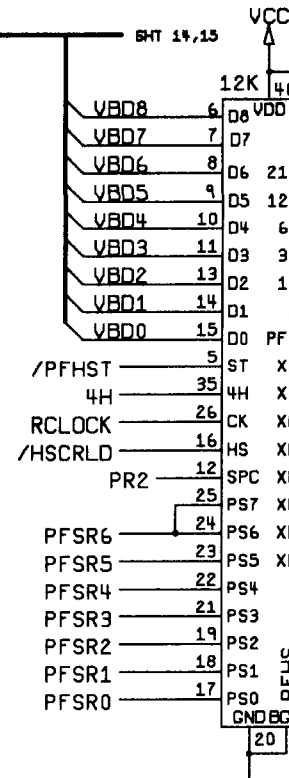
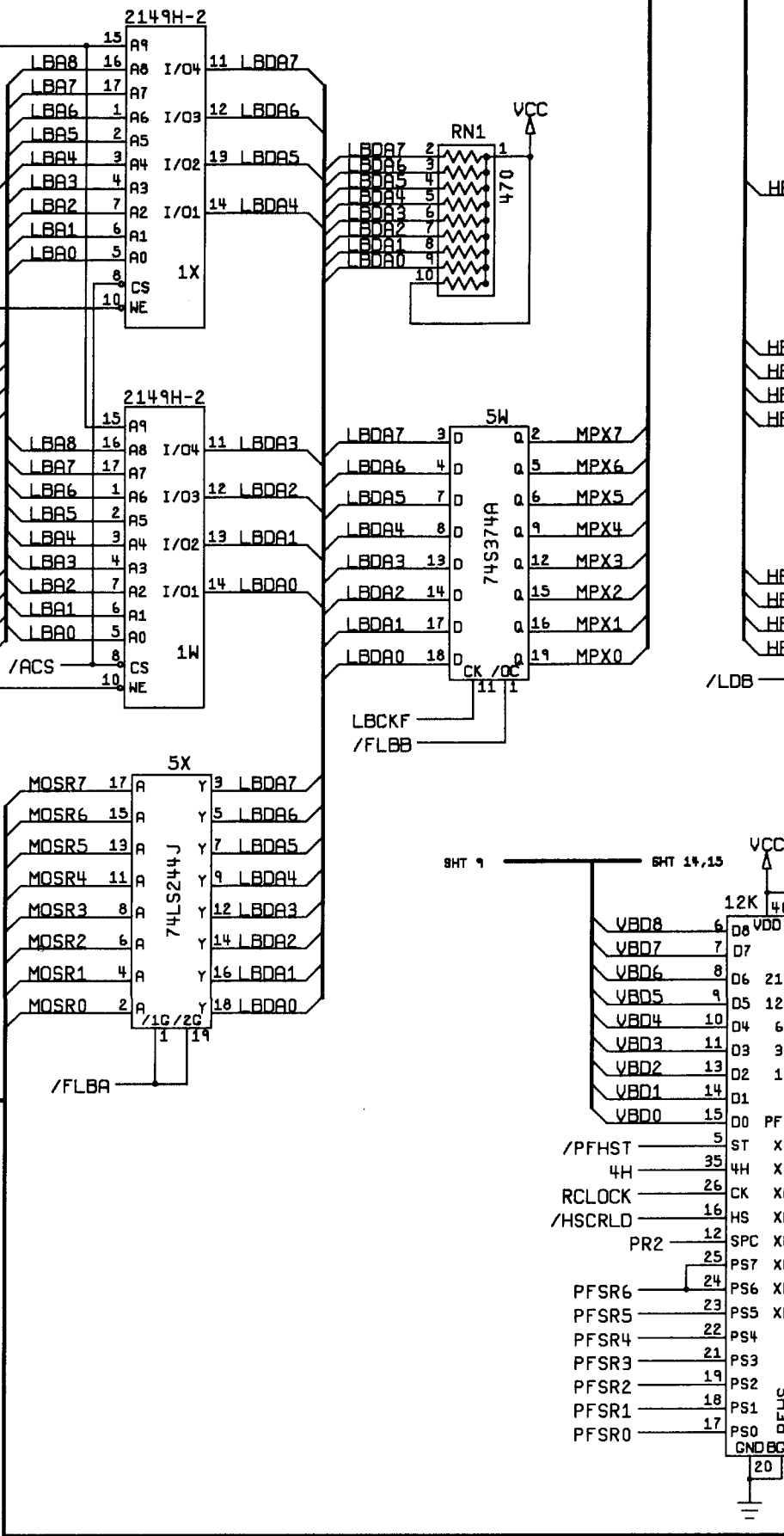
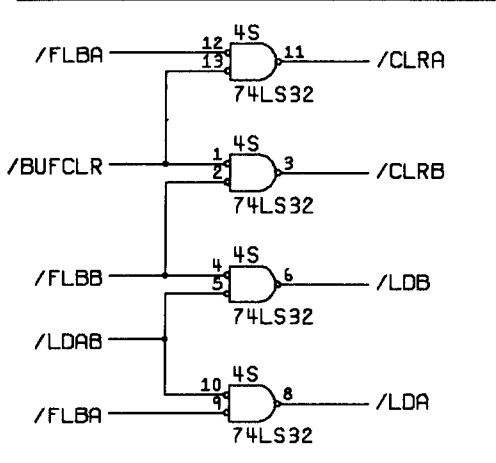
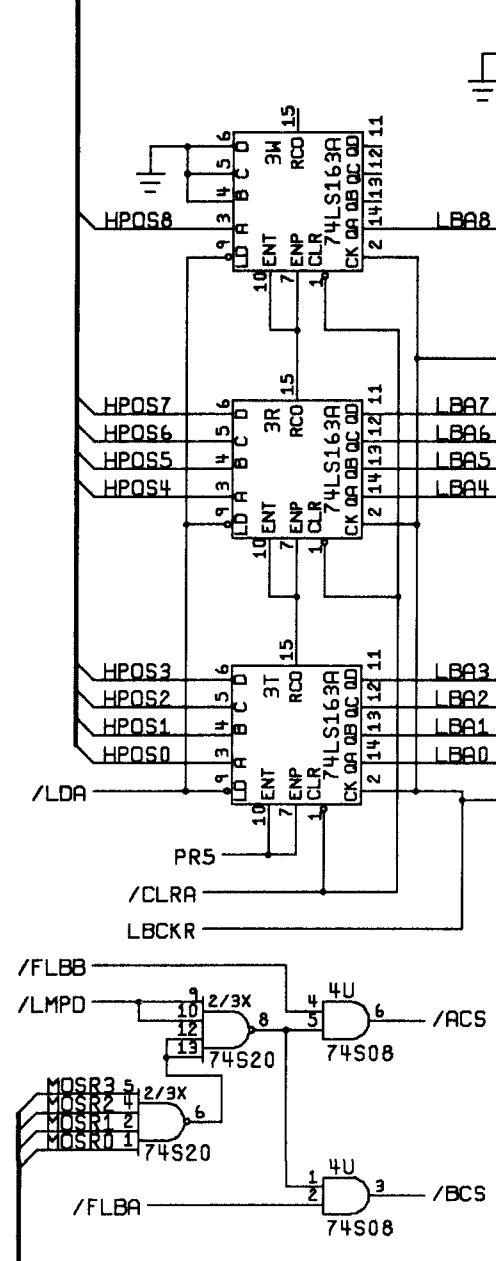
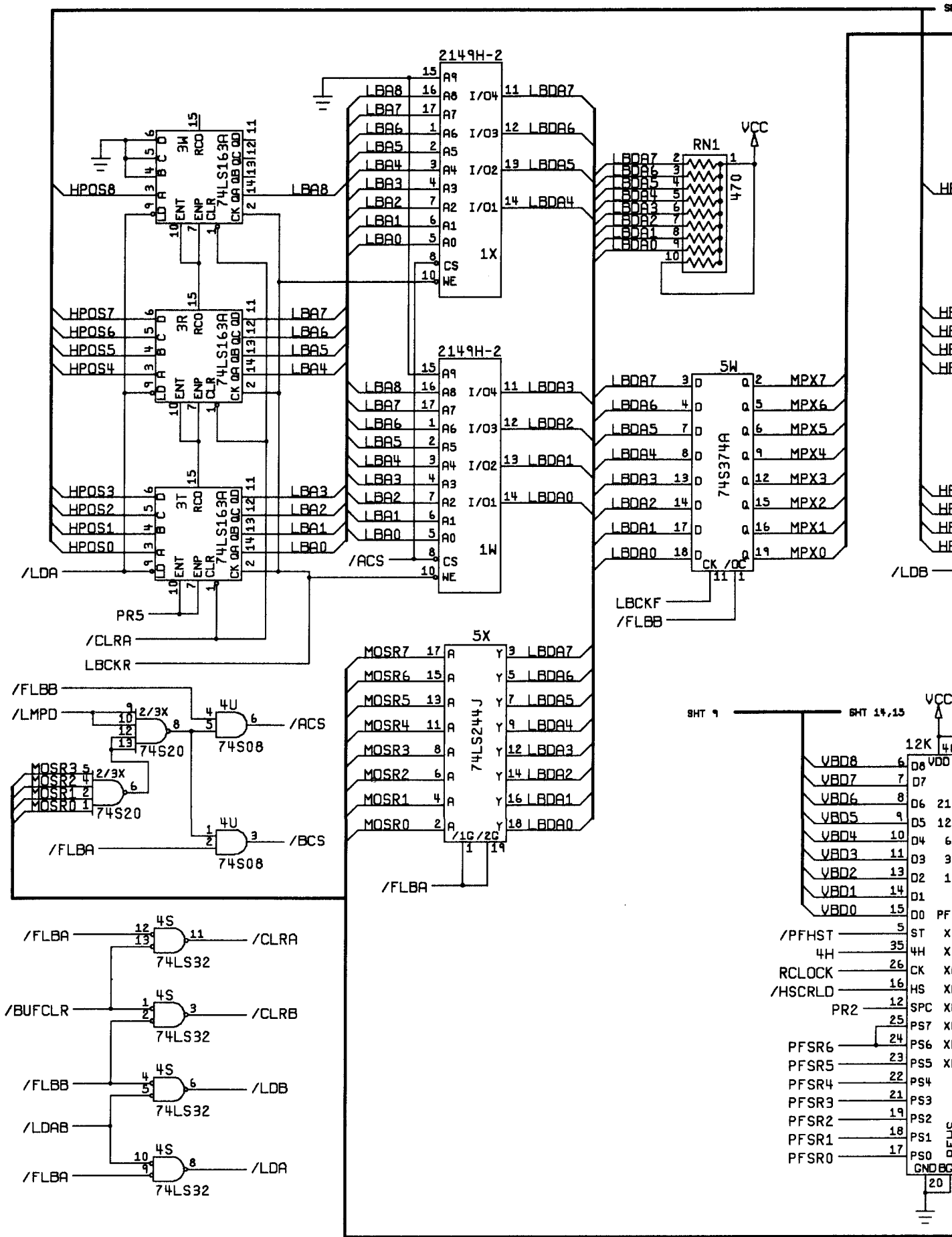


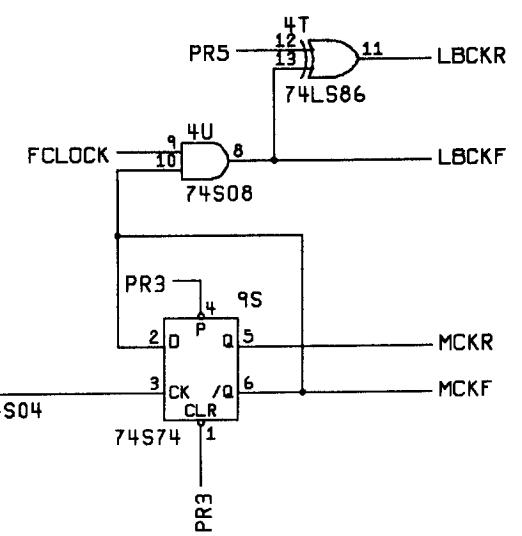
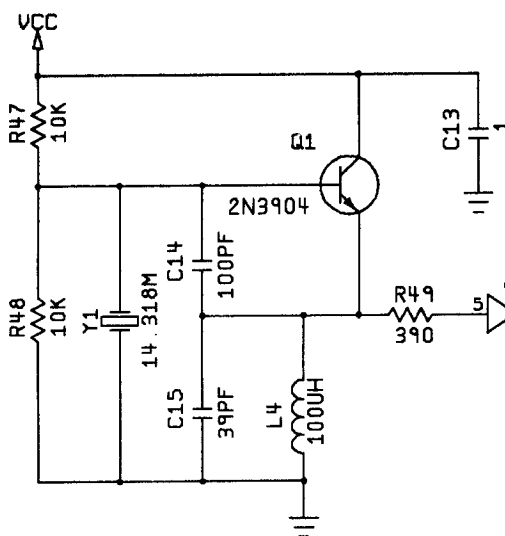
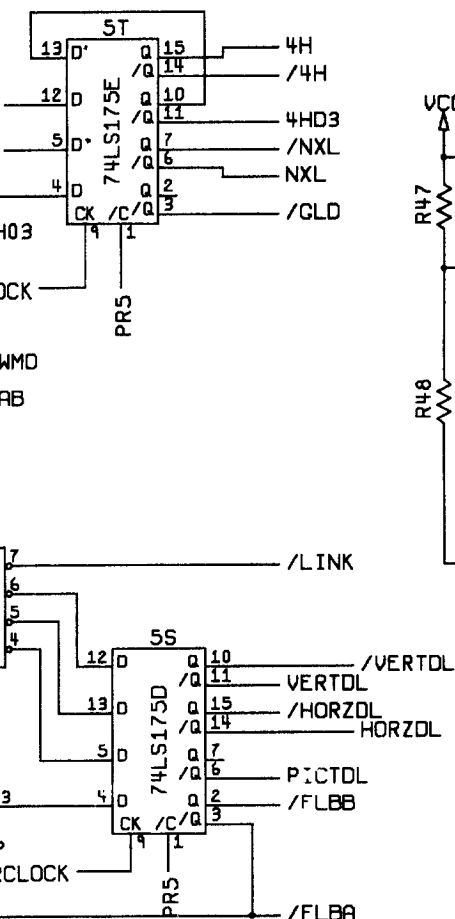
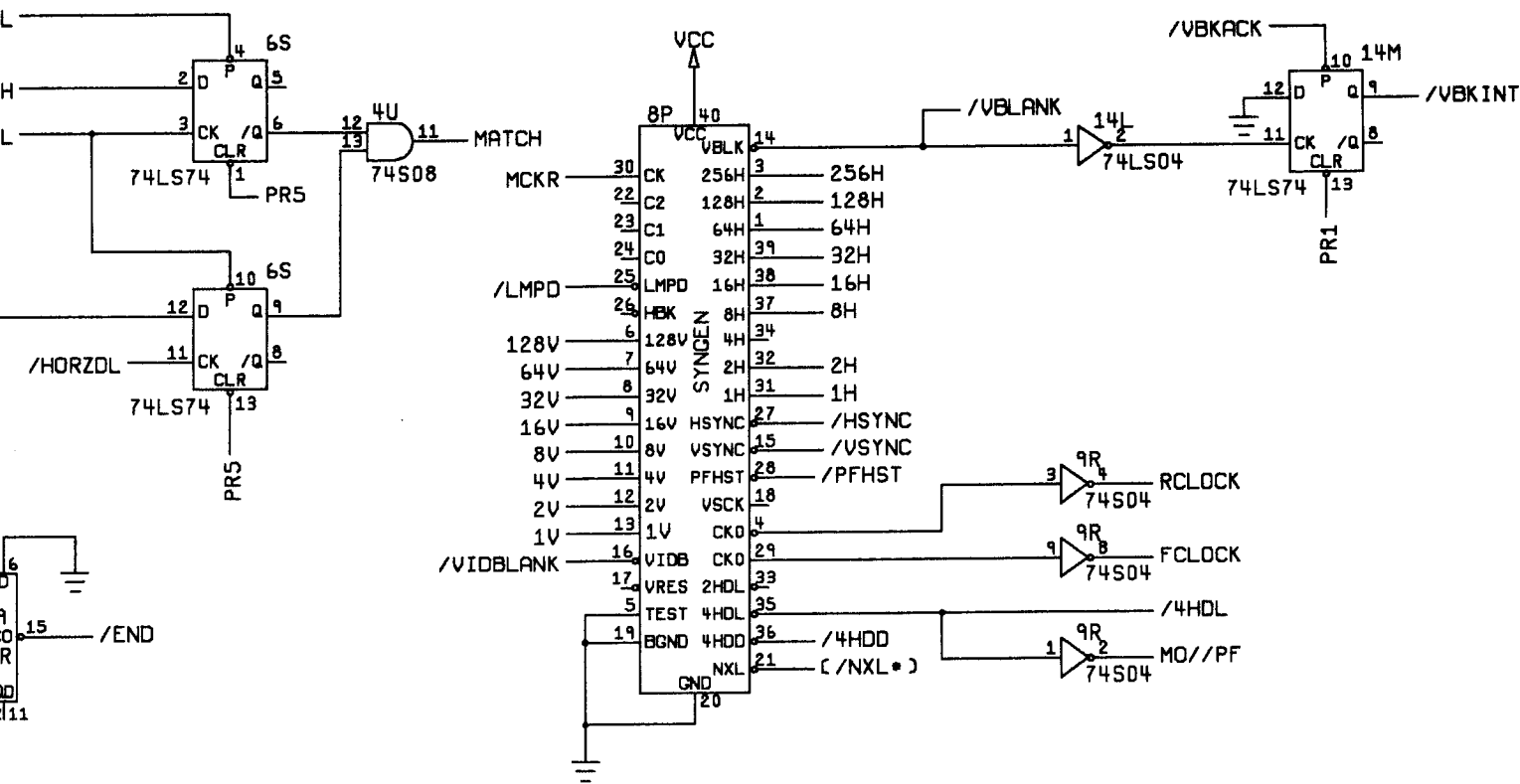
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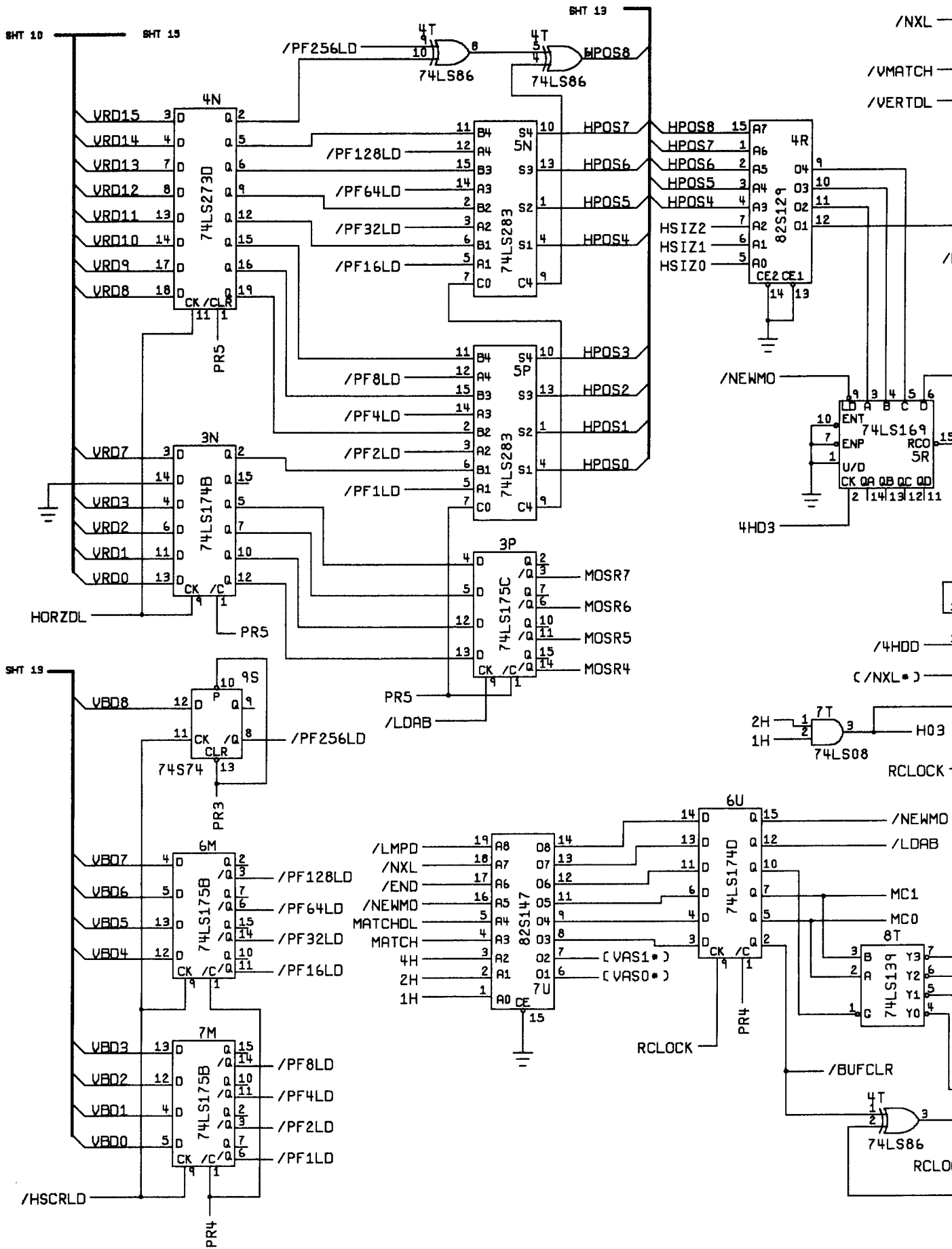


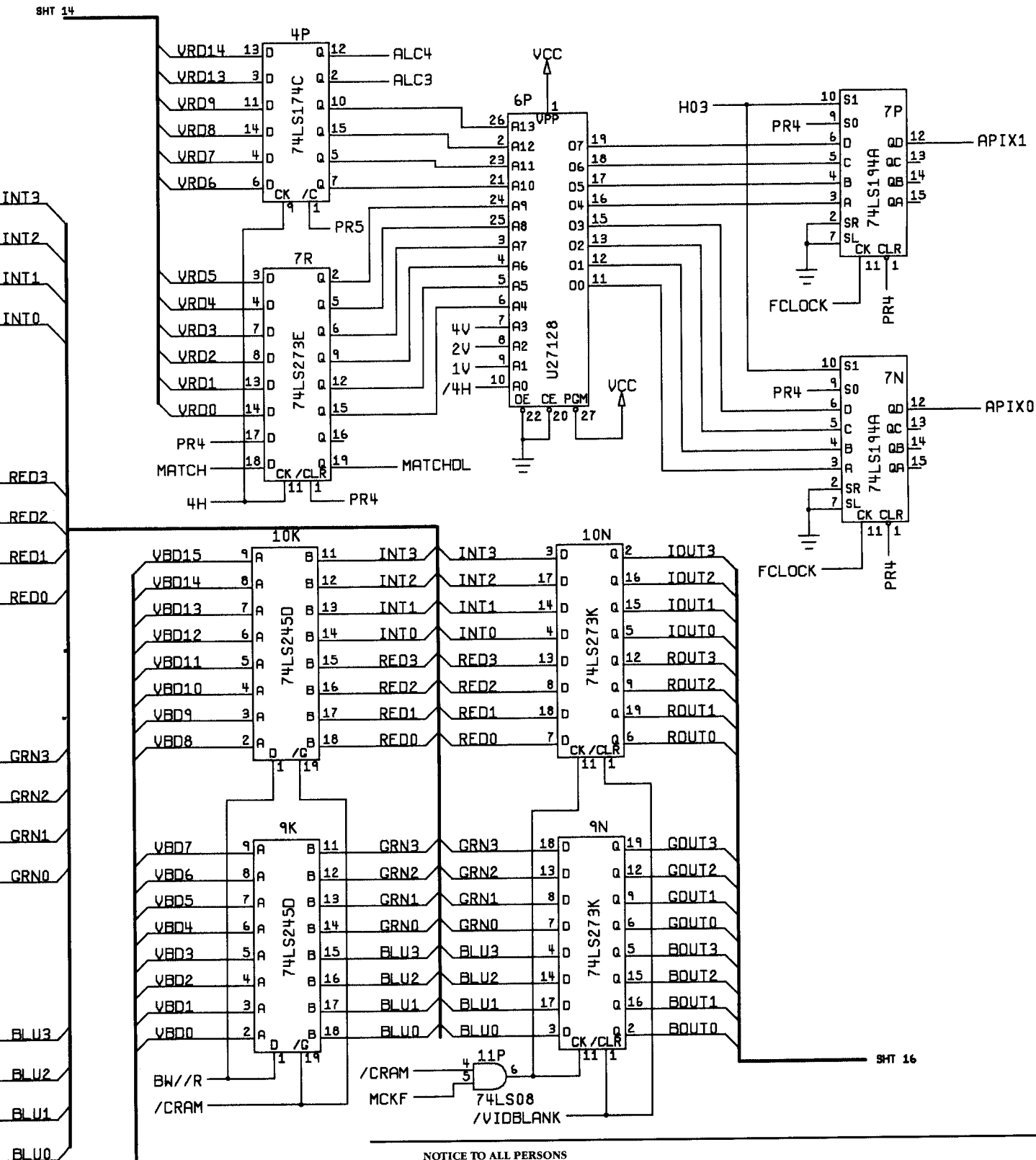


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Gauntlet™ Game PCB Schematic Diagram



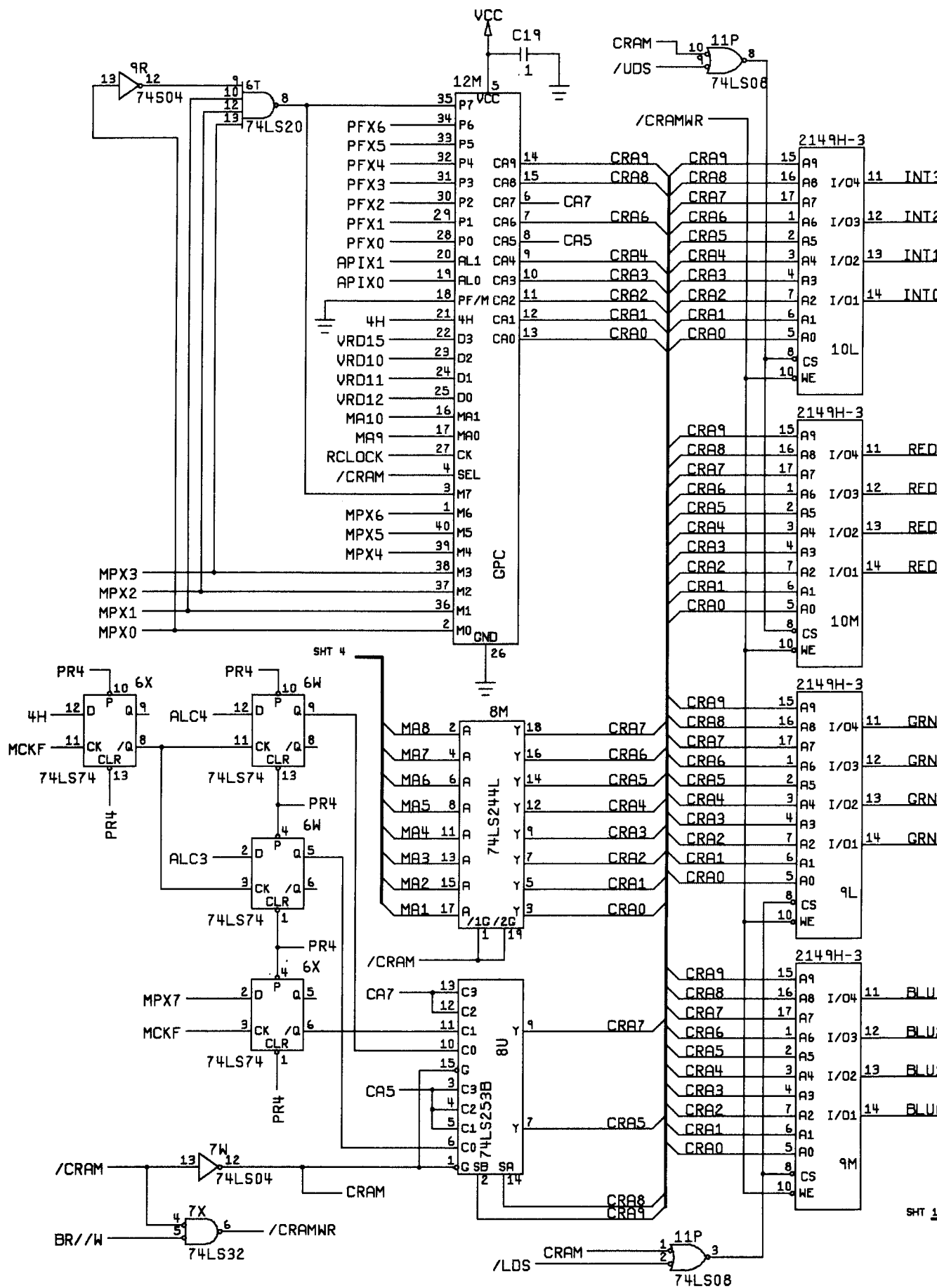


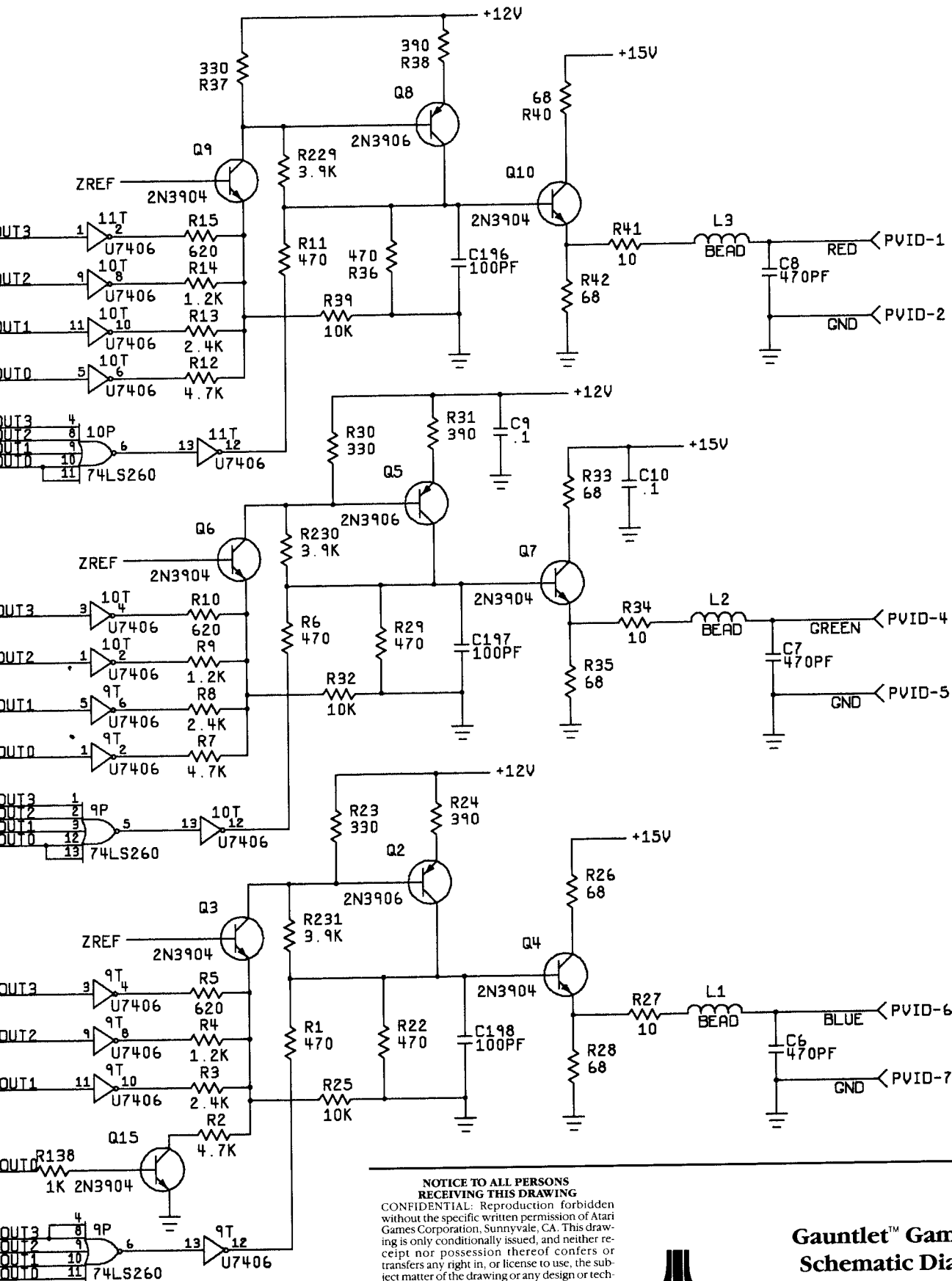
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Gauntlet™ Game PCB Schematic Diagram



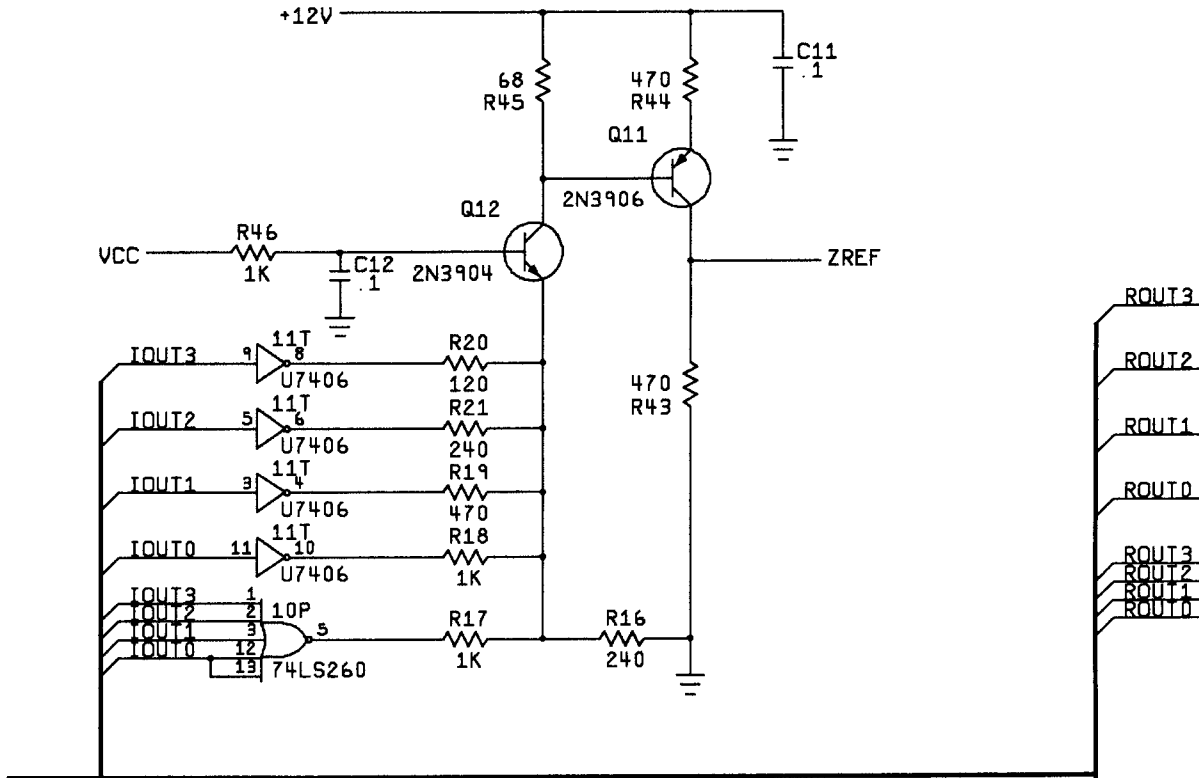


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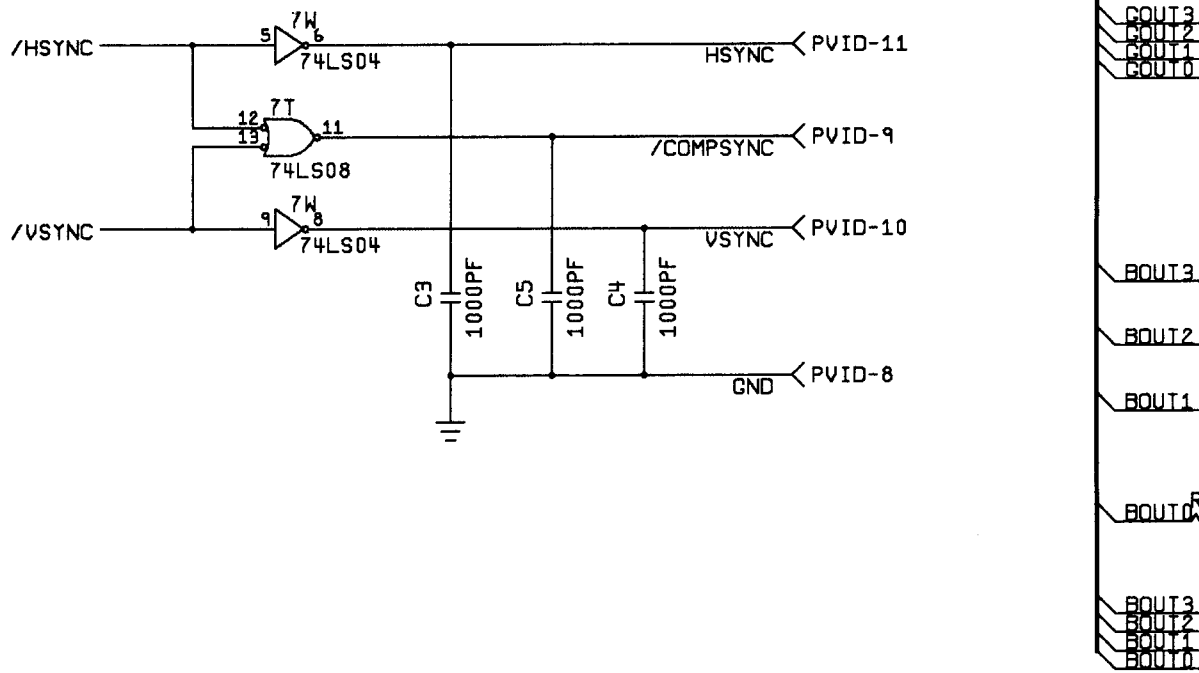
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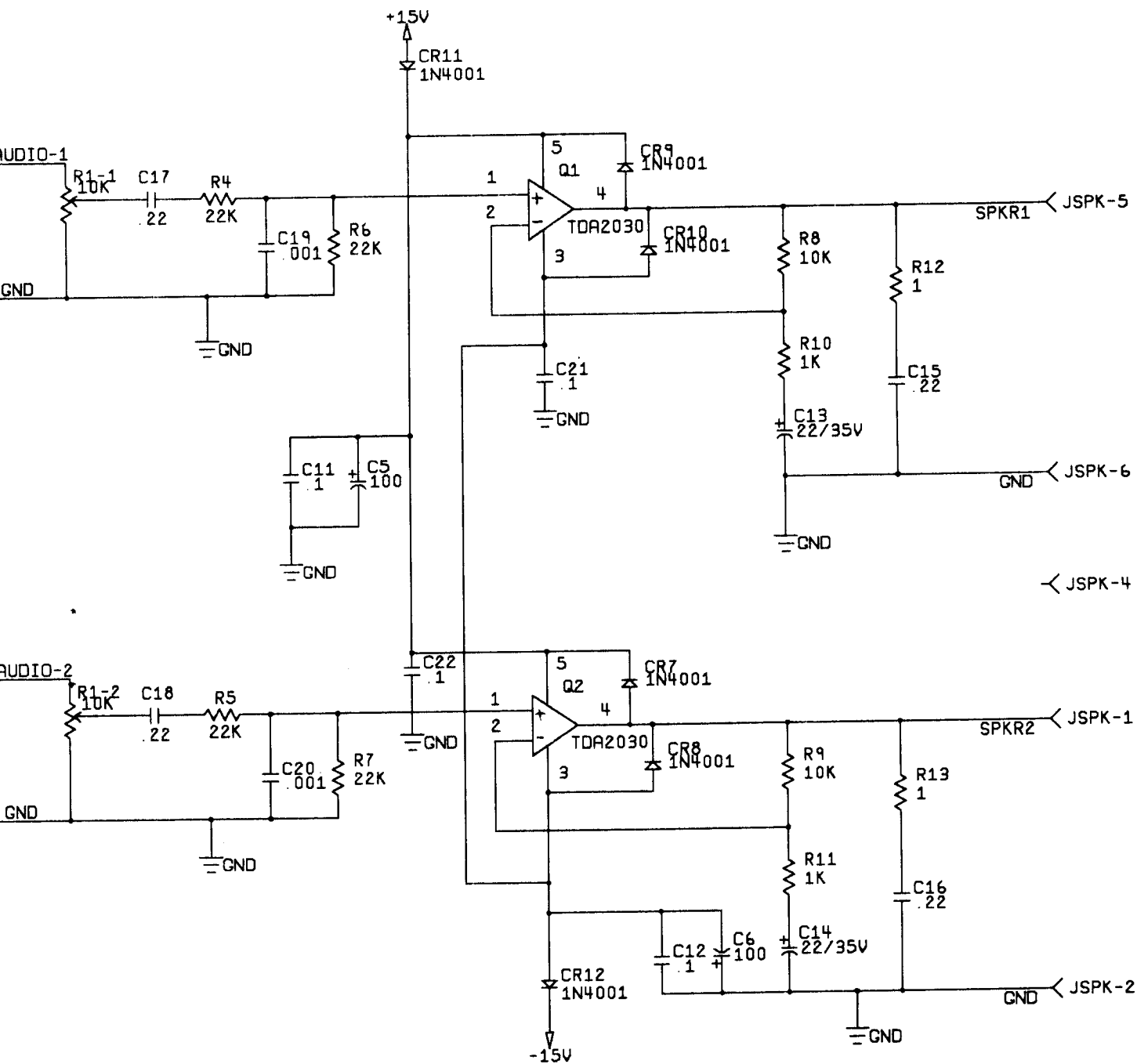


Gauntlet™ Game PCB Schematic Diagram



SHT 1.5



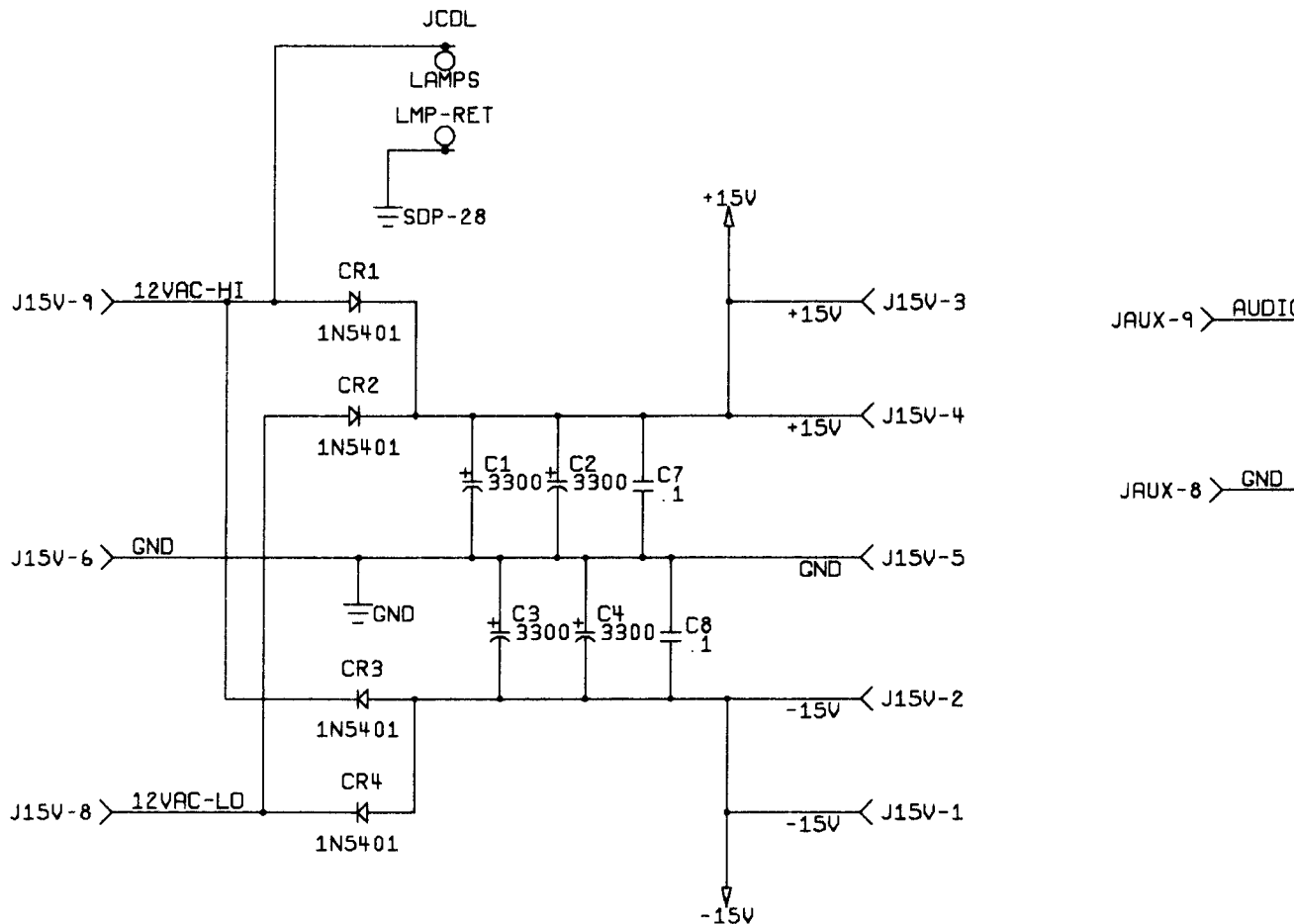


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**Audio PCB Assembly
Schematic Diagram (U.S.)**

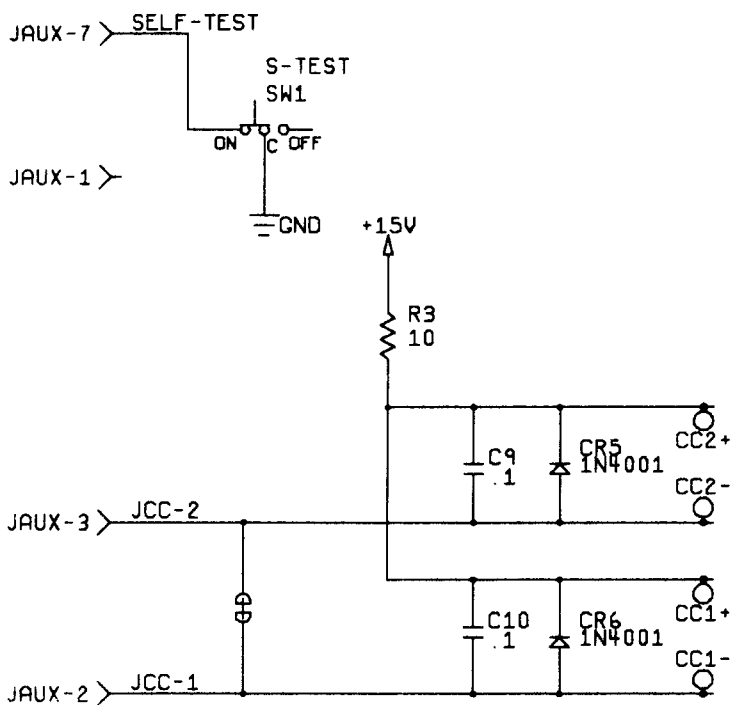


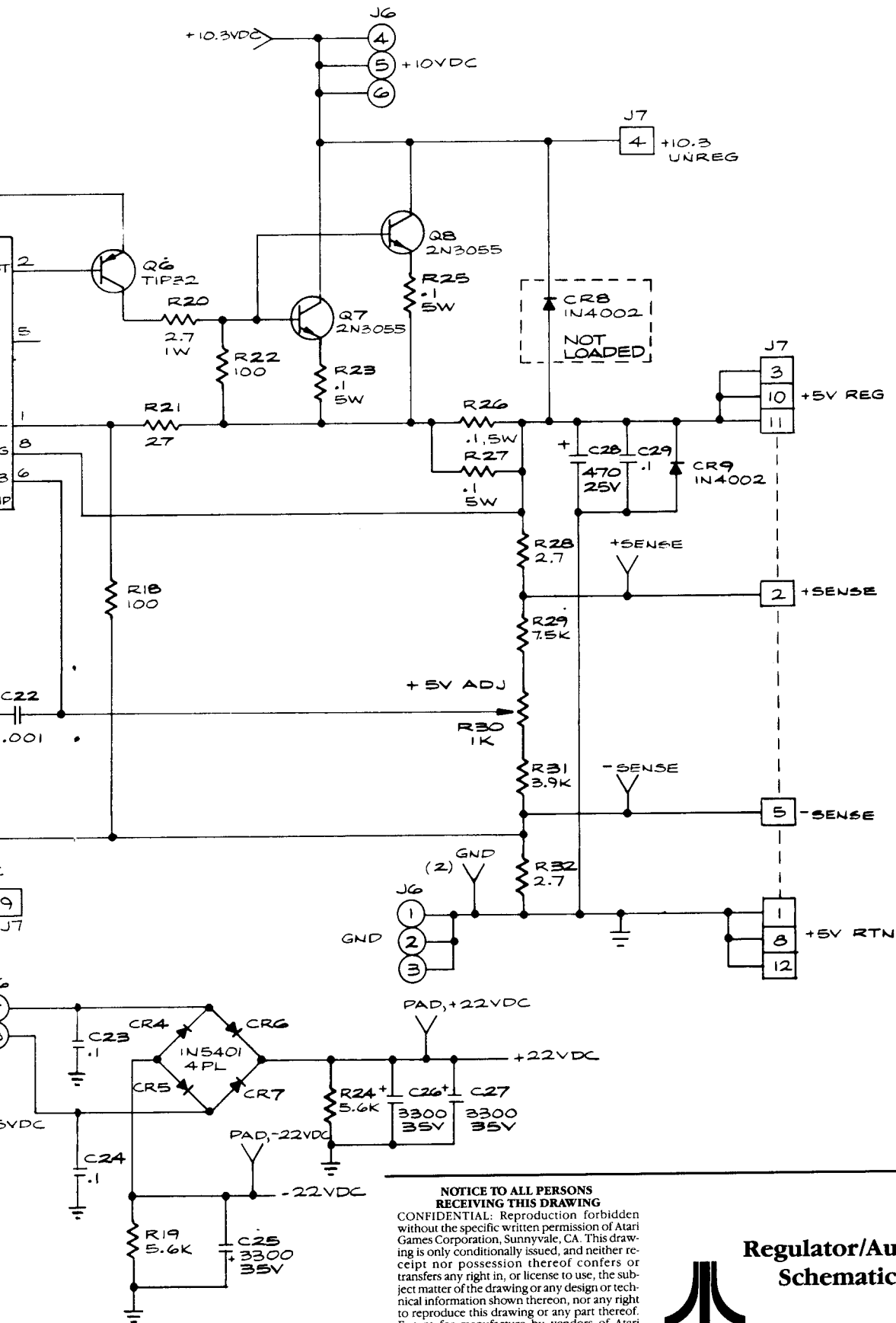
JAUX-9 > AUDIO

JAUX-8 > GND

JAUX-5 > AUDIO

JAUX-4 > GND



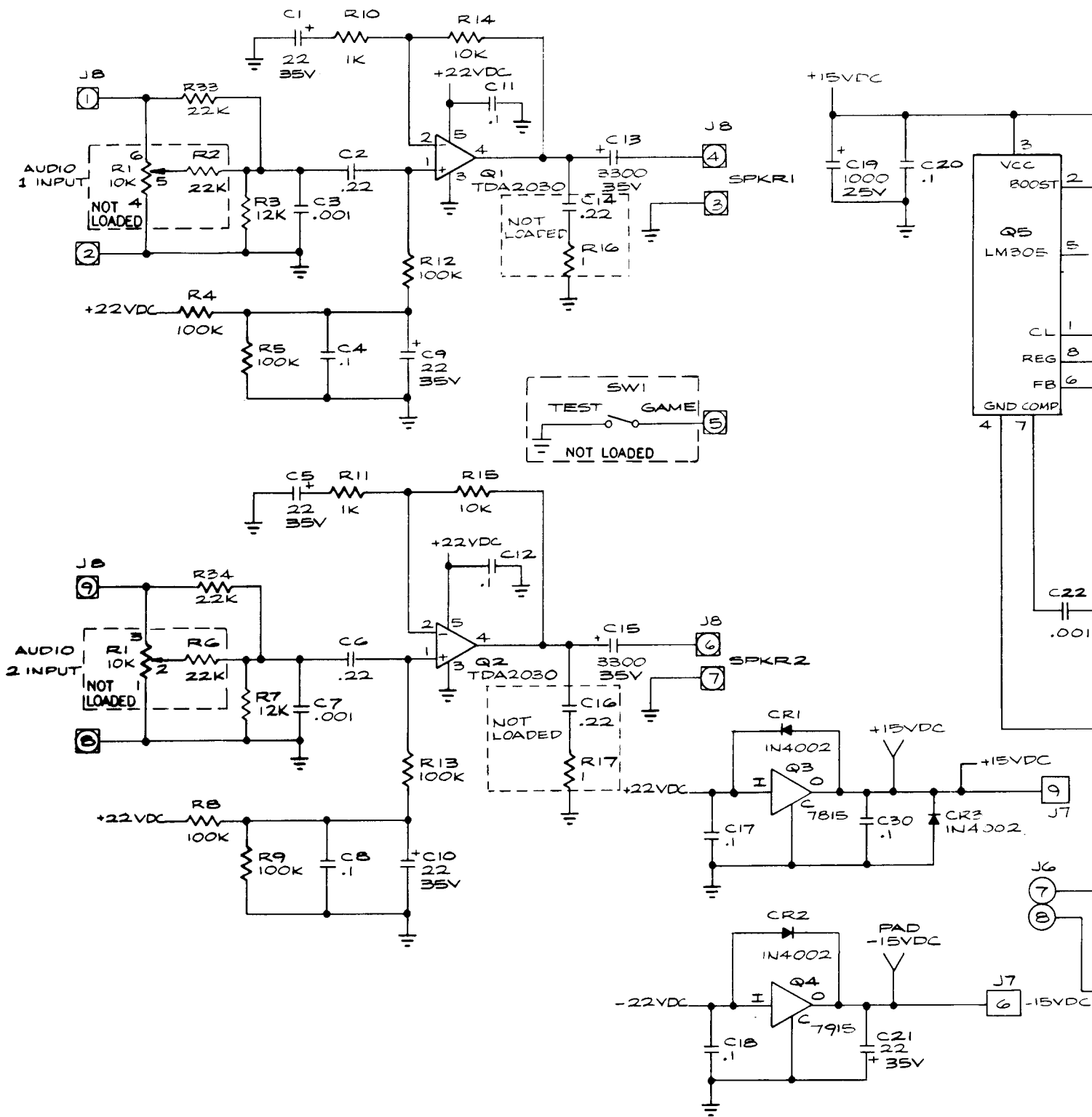


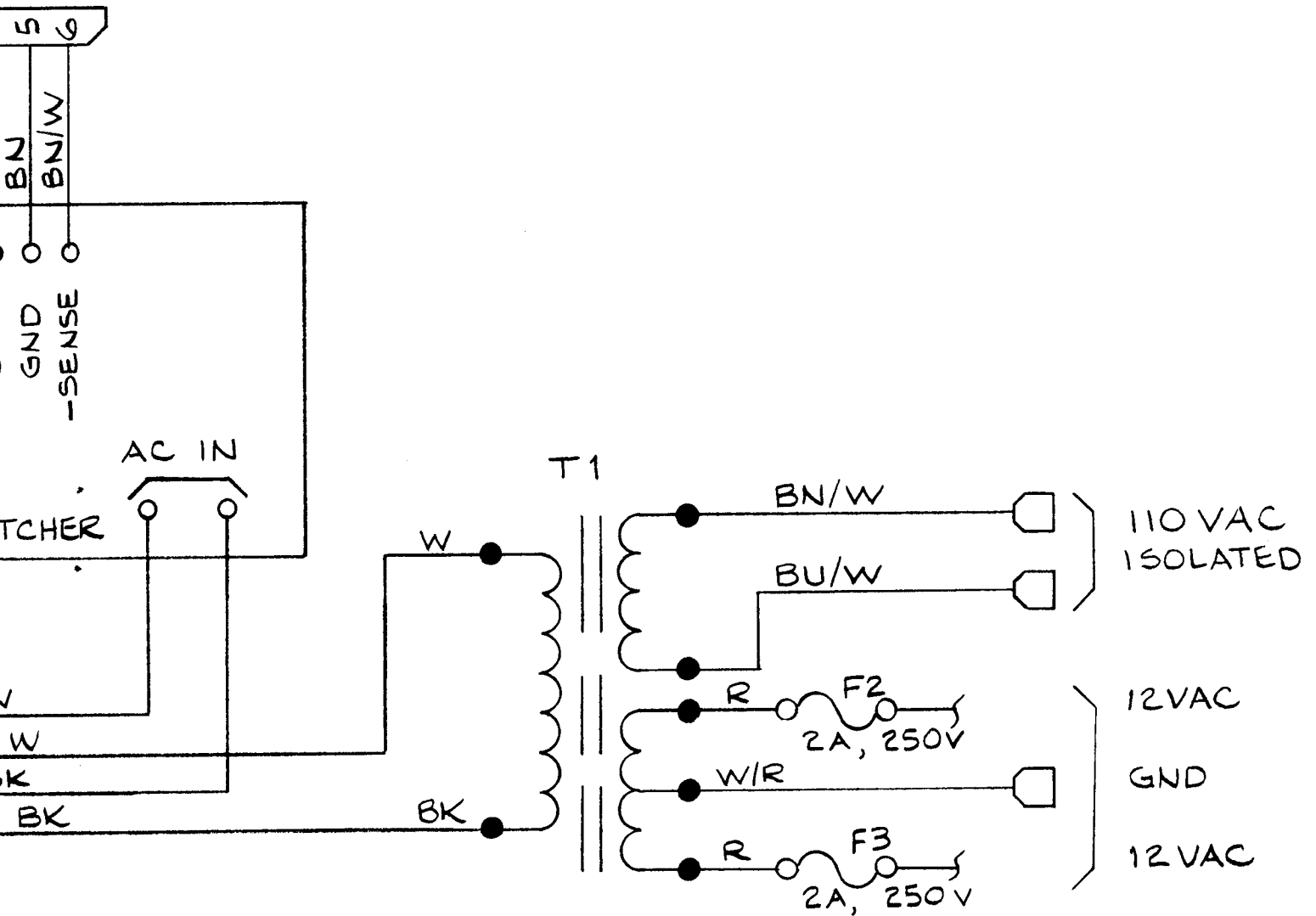
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Regulator/Audio III PCB Assembly Schematic Diagram (Ireland)





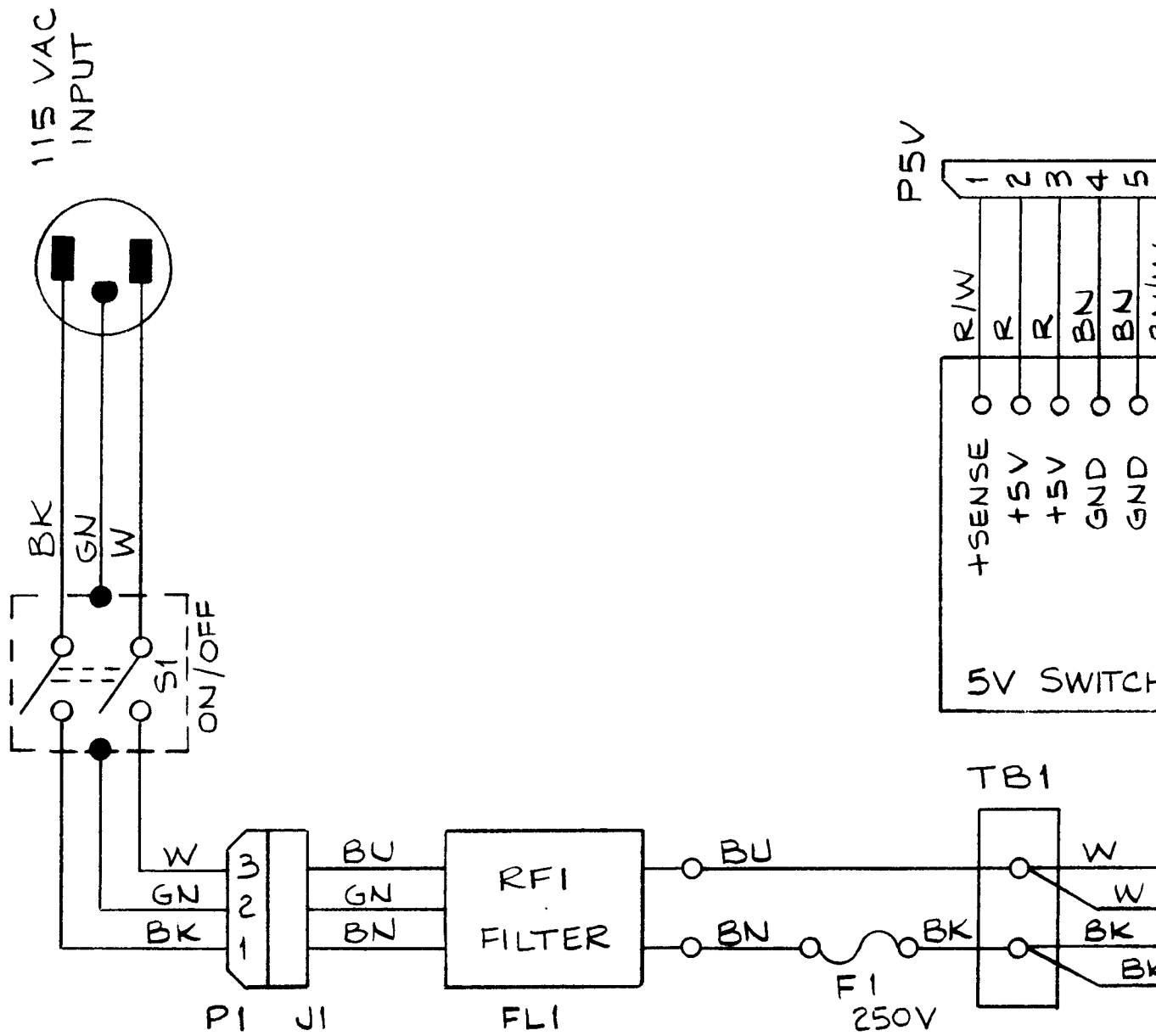


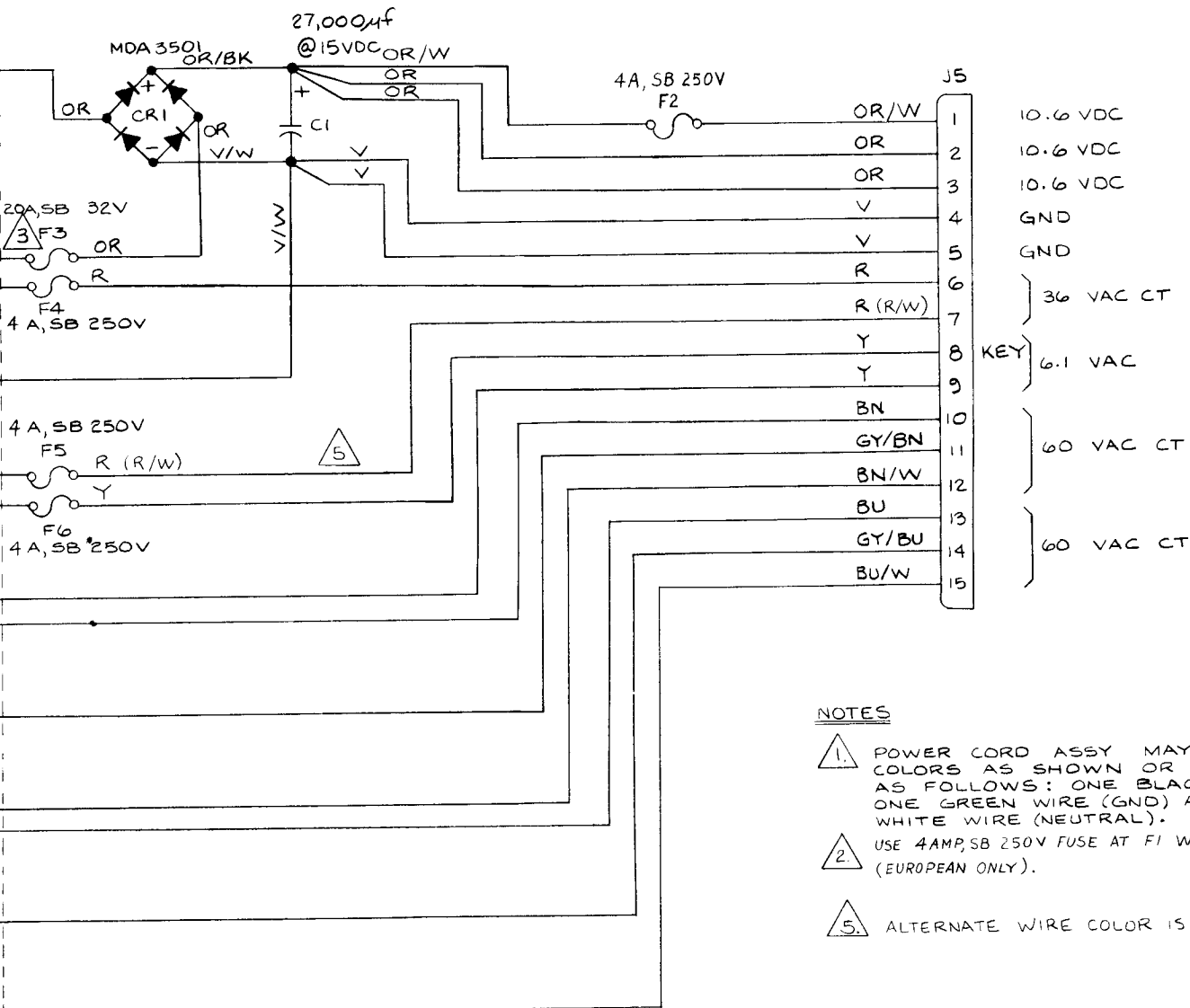
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**Switching/Linear (SL) Power Supply
Wiring Diagram (U.S.)**





NOTES

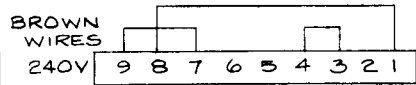
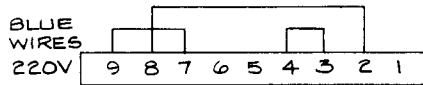
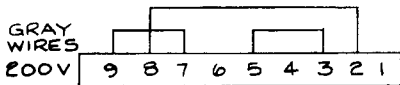
- 1. POWER CORD ASSY MAY HAVE WIRE COLORS AS SHOWN OR WIRE COLORS AS FOLLOWS: ONE BLACK WIRE (AC), ONE GREEN WIRE (GND) AND ONE WHITE WIRE (NEUTRAL).
- 2. USE 4AMP, SB 250V FUSE AT F1 WITH 220V & 240V (EUROPEAN ONLY).
- 5. ALTERNATE WIRE COLOR IS IN PARENTHESES ().

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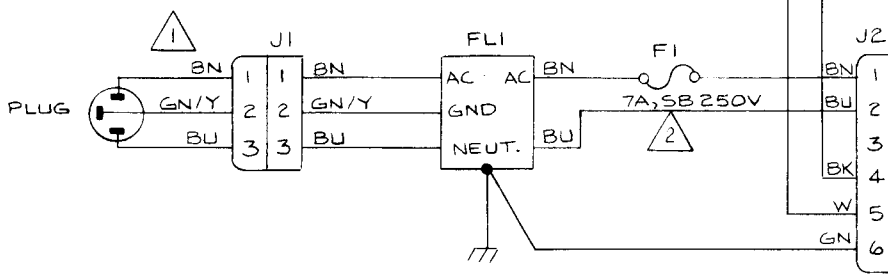
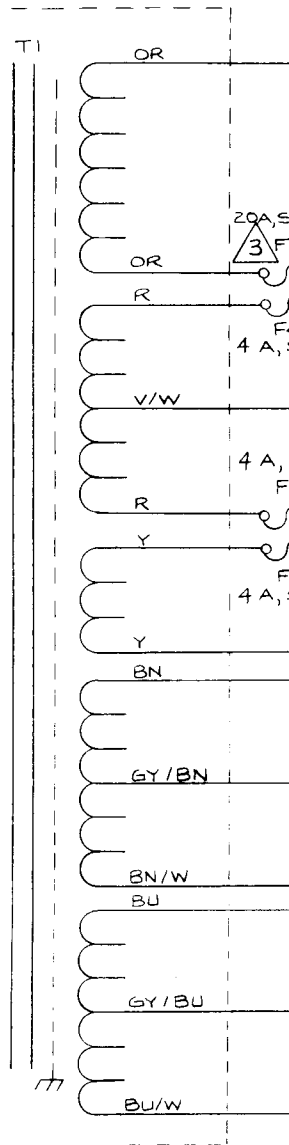
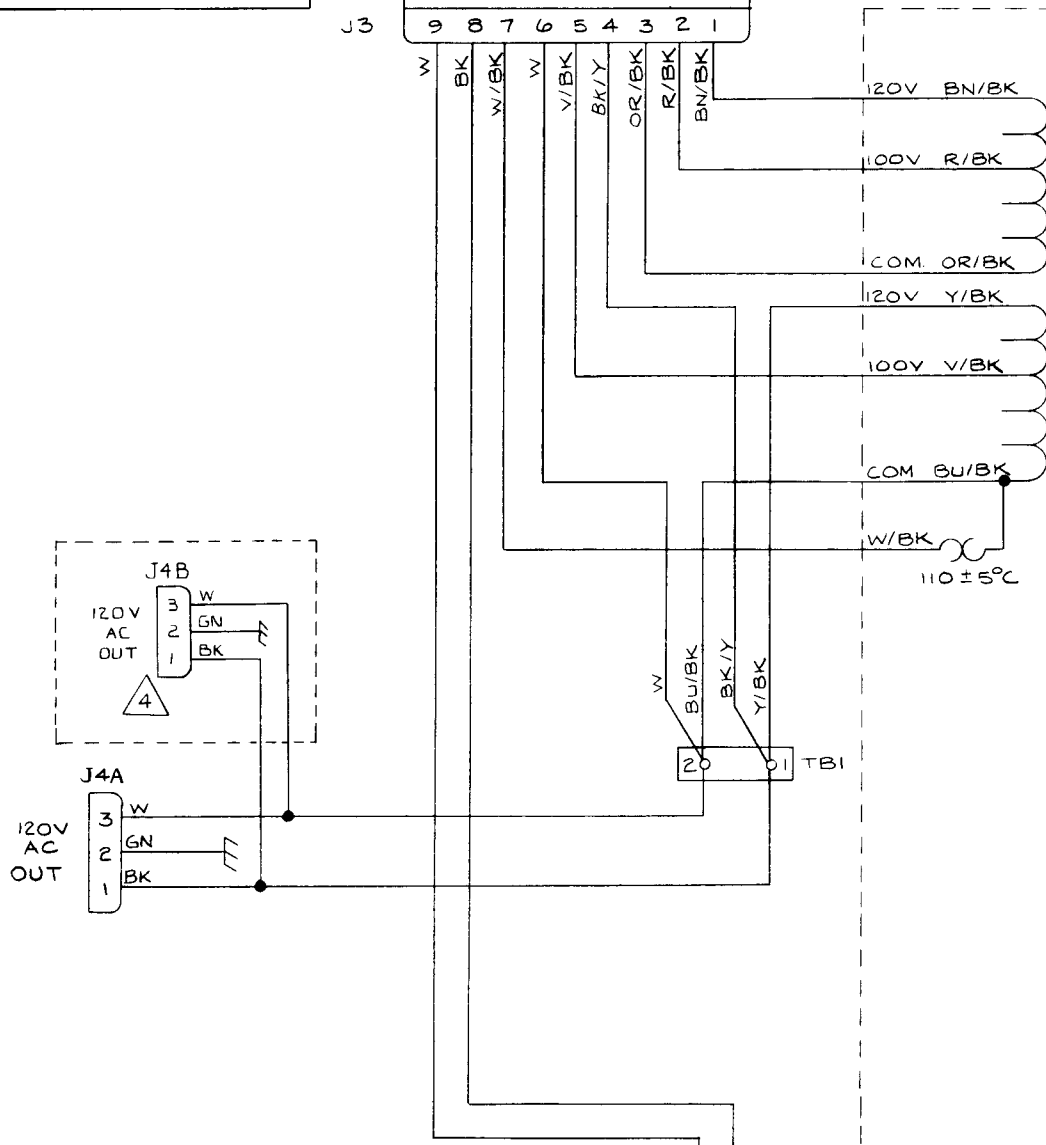
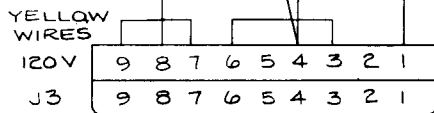
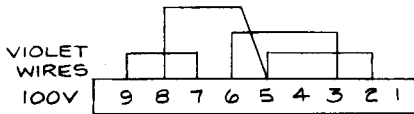
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**Linear Power Supply
Wiring Diagram (Ireland)**

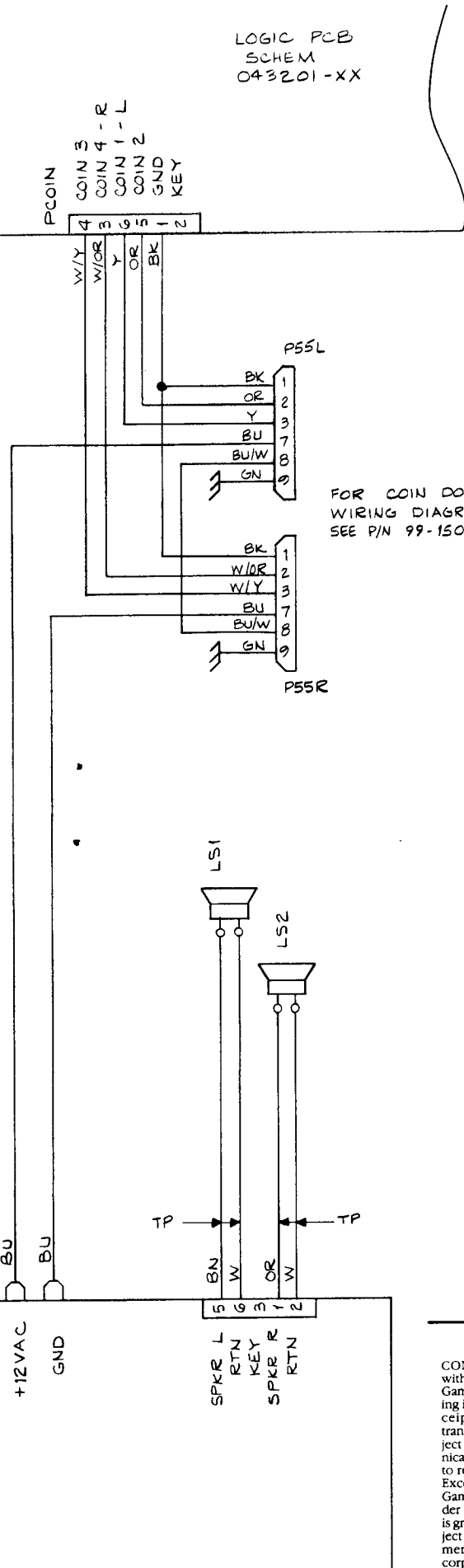


VOLTAGE SELECTION BLOCKS

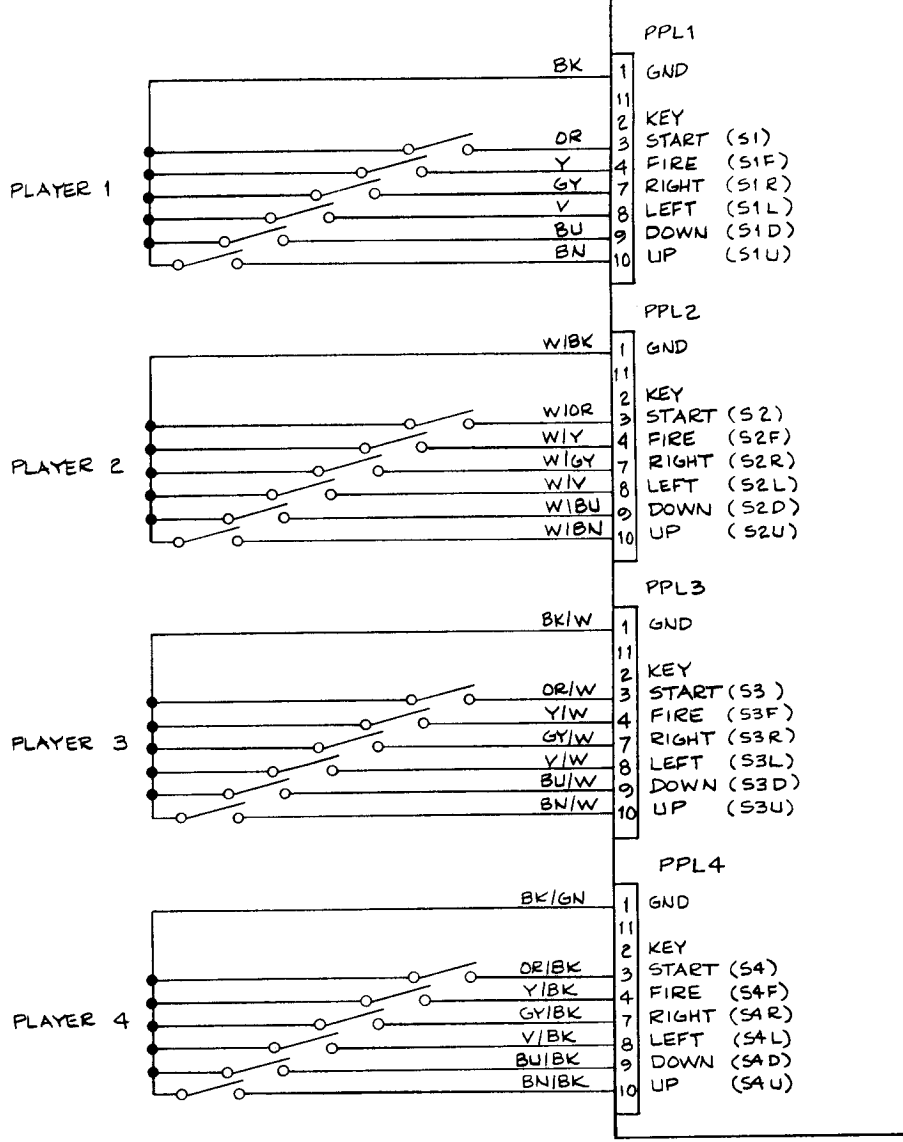


TO ON/OFF
& INTERLOCK SWITCHES

LOGIC PCB
SCHEM
043201-XX



FOR COIN DOOR
WIRING DIAGRAM
SEE P/N 99-15085

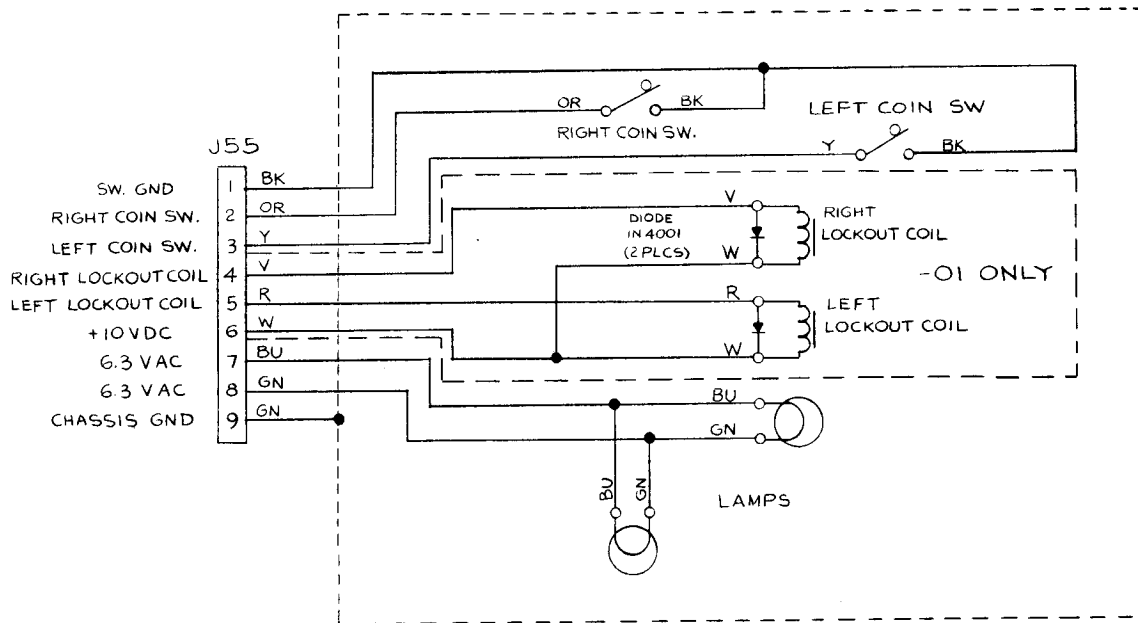
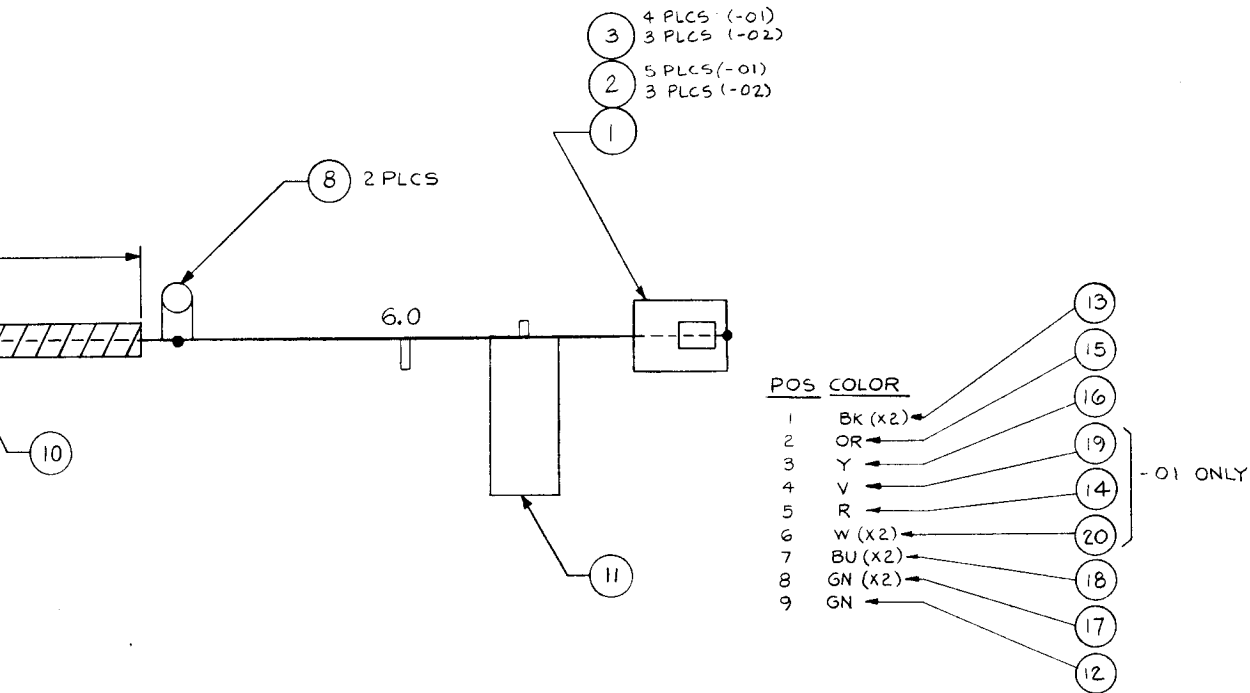


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Gauntlet™ Game Wiring Diagram



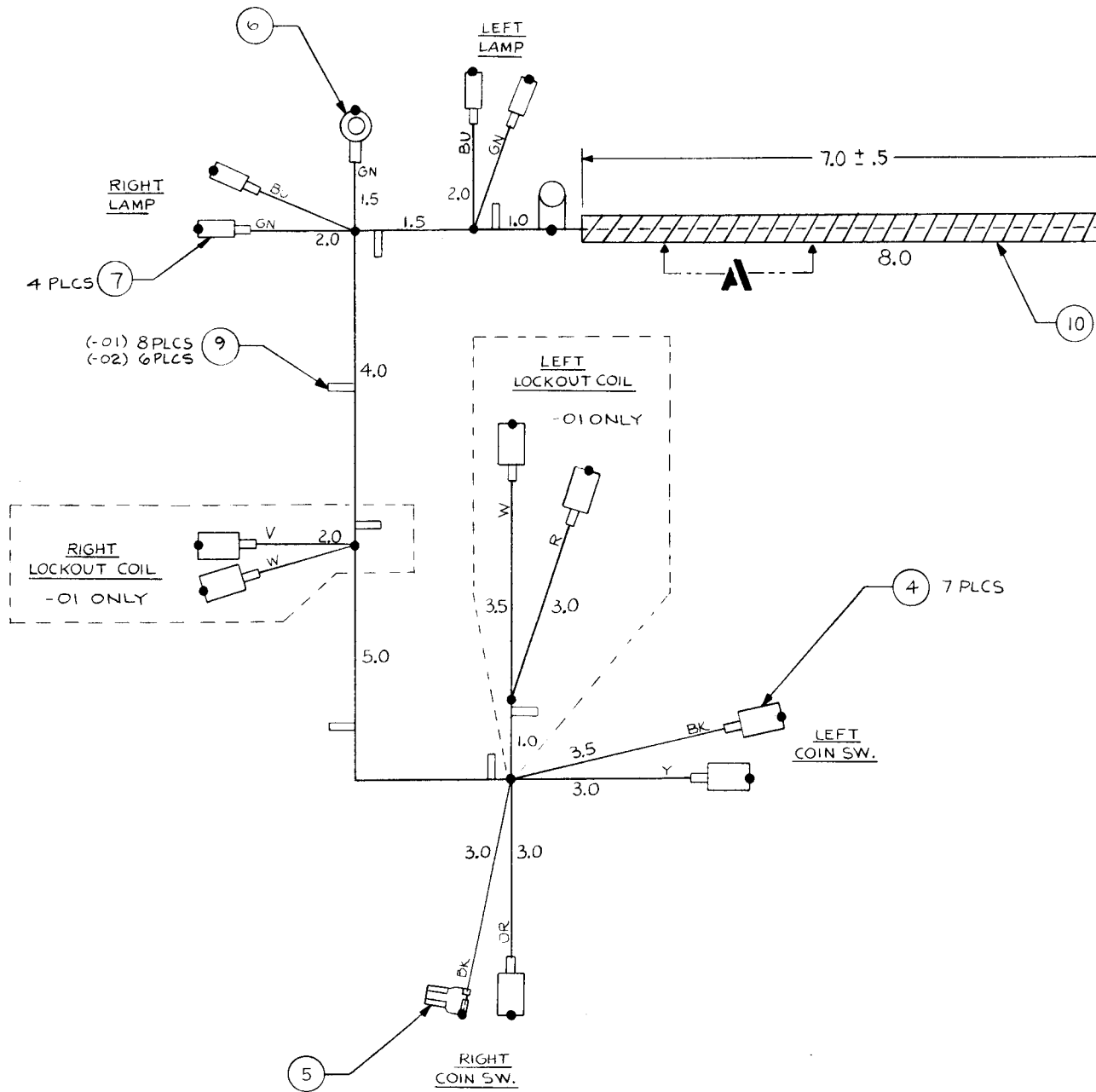
COIN DOOR WIRING DIAGRAM

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Coin Door Wiring Diagram



Gauntlet™ 6502 Memory Map

FUNCTION	ADDRESS	R/W	DATA
Program RAM	0000-0FFF	R/W	D0-D7
Write 68010 Port (Output Buffer)	1000	W	D0-D7
Read 68010 Port (Input Buffer)	1010	R	D0-D7
<i>Audio Mix:</i>			
Speech Mix	1020	W	D5-D7
Effects Mix	1020	W	D3, D4
Music Mix	1020	W	D0-D2
Coin 1 (Left)	1020	R	D3
Coin 2	1020	R	D2
Coin 3	1020	R	D1
Coin 4 (Right)	1020	R	D0
Data Available (@ 1010) (Active High)	1030	R	D7
Output Buffer Full (@ 1000) (Active High)	1030	R	D6
Speech Ready (Active Low)	1030	R	D5
Self-Test (Active Low)	1030	R	D4
Music Reset (Low Reset)	1030	W	D7
Speech Write (Active Low)	1031	W	D7
Speech Reset (Active Low)	1032	W	D7
Speech Squeak (Low = 650KHz Clock)	1033	W	D7
Coin Counter Right (Active High)	1034	W	D7
Coin Counter Left (Active High)	1035	W	D7
Effects	1800-180F	R/W	D0-D7
Music	1810-1811	R/W	D0-D7
Speech	1820	W	D0-D7
Interrupt Acknowledge	1830	R/W	xx
Program ROM (48k bytes)	4000-FFFF	R	D0-D7

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Gauntlet™ 68010 and 6502 Microprocessor Memory Maps

Gauntlet™ 68010 Memory Map

FUNCTION	ADDRESS	R/W	DATA
Program ROM/Operating System	000000–00FFFF	R	D0–D15
Program ROM/SLAPSTIC	038000–03FFFF	R	D0–D15
Program ROM/Main	040000–07FFFF	R	D0–D15
Spare RAM	800000–801FFF	R/W	D0–D15
EEPROM	802001–802FFF	R/W	D7–D0
Player 1 Input (see detail below)	803001	R	D0–D7
Player 2 Input	803003	R	D0–D7
Player 3 Input	803005	R	D0–D7
Player 4 Input	803007	R	D0–D7
<i>Player Inputs:</i>			
Joystick Up			D7
Joystick Down			D6
Joystick Left			D5
Joystick Right			D4
Spare			D3
Spare			D2
Fire			D1
Magic/Start			D0
VBLANK (Active Low)	803009	R	D6
Output/Buffer Full (@ 803170) (Active High)	803009	R	D5
Input/Buffer Full (@ 80300F) (Active High)	803009	R	D4
Self-Test (Active Low)	803009	R	D3
Read Sound Processor (6502)	80300F	R	D0–D7
Watchdog (128 msec. timeout)	803100	W	xx
LED-1 (Low On)	803121	W	D0
LED-2 (Low On)	803123	W	D0
LED-3 (Low On)	803125	W	D0
LED-4 (Low On)	803127	W	D0
Sound Processor Reset (Low Reset)	80312F	W	D0
VBlank Acknowledge	803140	W	xx
Unlock EEPROM	803150	W	xx
Write Sound Processor (6502)	803171	W	D0–D7
Playfield RAM	900000–901FFF	R/W	D0–D15
Motion Object Picture	902000–9027FF	R/W	D0–D15
Motion Object Horizontal Position	902800–902FFF	R/W	D0–D15
Motion Object Vertical Position	903000–9037FF	R/W	D0–D15
Motion Object Link	903800–903FFF	R/W	D0–D15
Spare RAM	904000–904FFF	R/W	D0–D15
Alphanumerics RAM	905000–905FFF	R/W	D0–D15
Playfield Vertical Scroll	905F6E, 905F6F	R/W	D7–D15
Playfield ROM Bank Select	905F6F	R/W	D0, D1
Color RAM Alpha	910000–9101FF	R/W	D0–D15
Color RAM Motion Object	910200–9103FF	R/W	D0–D15
Color RAM Playfield Shadow	910400–9104FF	R/W	D0–D15
Color RAM Playfield	910500–9105FF	R/W	D0–D15
Color RAM (Spare)	910600–9107FF	R/W	D0–D15
Playfield Horizontal Scroll	930000, 930001	W	D0–D8

NOTE

All addresses can be accessed in byte or word mode.

Gauntlet Signal Name Glossary, continued

HSIZ0-HSIZ2	Motion object horizontal size	\overline{MIX}	Latch audio mix data
HSYNC, \overline{HSYNC}	Horizontal sync output	MO/\overline{PF}	Motion object or playfield picture select
\overline{INPUT}	68010 miscellaneous inputs buffer select	$\overline{MOHI}, \overline{MOLO}$	Motion object RAM chip selects
INT0-INT3	Color intensity RAM data	MOSR0-MOSR3	Motion object pixel data, before the line buffers
IOUT0-IOUT3	Intensity latched digital video output	MOSR4-MOSR7	Motion object pixel palette data, before the line buffers
\overline{LATCH}	68010 miscellaneous latched outputs chip select	MPIC0-MPIC7	The lower 8 bits of the motion object picture address
LAUD	Summed left channel audio	MPX0-MPX7	Motion object pixel data, after the line buffers
LBA0-LBA8	Line buffer "A" address bus	MREFL	Motion object stamp horizontal flip state
LBB0-LBB8	Line buffer "B" address bus	MUSIC	Music chip select
LBCKF	Line buffer clock inverted phase	\overline{NEWMO}	Start a new motion object
LBCKR	Line buffer clock	NXL, \overline{NXL}	Next line
LBDA0-LBDA7	Line buffer "A" data bus	(\overline{NXL}^*)	NXL one clock cycle early
LBDB0-LBDB7	Line buffer "B" data bus	NXLDL	NXL delayed one clock cycle
\overline{LDA}	Load line buffer "A" address counters	$\overline{PF1LD-PF256LD}$	Latched playfield horizontal scroll data
\overline{LDAB}	Load line buffer "A" or "B" address counters	PF1V-PF256V	Playfield vertical address counter chain
\overline{LDB}	Load line buffer "B" address counters	PF8H-PF256H	Playfield horizontal address counter chain
\overline{LDS}	68010 lower data strobe	PFBANK0, PFBANK1	Playfield picture bank select
LED1-LED4	LED outputs, players 1-4	$\overline{PFHI}, \overline{PFLO}$	Playfield RAM chip selects
LEFT-1-LEFT-4	Joystick left switch inputs, players 1-4	\overline{PFHST}	Playfield scroll control
\overline{LINK}	Latch motion object link data	PFSR0-PFSR3	Playfield pixel data, before PFHS
\overline{LMPD}	Stop motion object processing for line buffer changeover	PFSR4-PFSR6	Playfield pixel palette data, before PFHS
LNK0-LNK9	Motion object link data	PFX0-PFX6	Playfield pixel data after PFHS
MA1-MA14	68010 address bus buffered	PICST0-PICST7	Motion object picture start address
MATCH	Motion object H and V data matches current playfield position	\overline{PICT}	Latch motion object picture data
MATCHDL	Previous MATCH state	PICTDL	PICT delayed one clock cycle
MBUS	68010 "M" data bus buffers enable	PKAUD	Effects chip audio
MC0, MC1	Motion object parameter control select	$\overline{PL1-PL4}$	Player input chip selects, players 1-4
MCEN	Motion object parameter control enable	PM0-PM2	Effects audio mix control bits
MCKF	Master clock, inverted phase	POKEY	Effects chip select
MCKR	Master clock	PR1-PR6	Pull-up resistors
MD0-MD15	68010 "M" data bus	R/\overline{W}	68010 read/write control, unbuffered
MFLP	Motion object horizontal flip parameter		

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Gauntlet™ Signal Name Glossary

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SP-284 Sheet 24
1st printing

Gauntlet Signal Name Glossary

2.5V	2.5 volts audio amplifier reference	$\overline{\text{COIN}}$	Coin input buffer chip select
+ 5AUD	5 volts audio amplifier reference	COIN1-L, COIN2, COIN3, COIN4-R	Four coin switch inputs
10.3V	Power-on-reset control voltage	$\overline{\text{COMPSYNC}}$	Negative composite sync output
+ 12V	+ 12 volts regulated	CRA0-CRA9	Color RAM address
+ 15V	+ 15 volts unregulated	$\overline{\text{GRAM}}$, GRAM	68010 address decode for color RAM
- 15V	- 15 volts unregulated	$\overline{\text{GRAMWR}}$	Color RAM write enable
- 5V	- 5 volts regulated	D0-D15	68010 data bus, unbuffered
1H-256H	Screen horizontal address counter chain	DOWN1-DOWN4	Joystick down switch inputs, players 1-4
1V-128V	Screen vertical address counter chain	EEPROM	Electrically erasable PROM chip select
$\overline{4H}$	Inverted 4H signal	$\overline{\text{END}}$	Current motion object finished
$\overline{4HD3}$, $\overline{4HD3}$	4H signal delayed three clock cycles	FCLOCK	System clock inverted phase
$\overline{4HDD}$	4H signal delayed two clock cycles	FIRE1-FIRE4	Fire switch inputs, players 1-4
$\overline{4HDL}$	4H signal delayed one clock cycle	$\overline{\text{FLBA}}$	Line buffer "A" fill control
68KBUF	68010 output buffer full (to 6502)	$\overline{\text{FLBB}}$	Line buffer "B" fill control
A1-A23	68010 address bus unbuffered	GCS0-GCS5	Graphics ROMs chip select
$\overline{\text{ACS}}$	"A" line buffer RAMs chip select	$\overline{\text{GLD}}$	Graphics load (to SLAGS chips)
ALC3, ALC4	Alphanumerics palette data bits 3 and 4	GND	System ground
$\overline{\text{ALHI}}$, $\overline{\text{ALLO}}$	Alphanumerics RAM chip selects	GOUT0-GOUT3	Green latched digital video output
APIX0, APIX1	Alphanumerics pixel data	GP0-GP14	Graphics picture address
$\overline{\text{AS}}$	68010 address strobe	GP1V, GP2V, GP4V	Graphics picture stamp sub-address
AUDIO-L, AUDIO-R	Left and right audio outputs (5V peak-to-peak)	GPEN	Graphics picture enable
B02	6502 buffered phase 2 (Φ 2)	GREEN	Green analog video output
BAS	Buffered address strobe (see $\overline{\text{AS}}$)	GRH/L	Graphics ROM high/low select (A14 on a 27256)
$\overline{\text{BCS}}$	"B" line buffer RAMs chip select	GRN0-GRN3	Green color RAM data
BLU0-BLU3	Blue color RAM data	H03	Alphanumerics load (to shift registers)
BLUE	Blue analog video output	HFLP	Graphics stamp horizontal flip
BOUT0-BOUT3	Blue latched digital video output	$\overline{\text{HORZ}}$	Latch motion object horizontal data and palette data
$\text{BR}/\overline{\text{W}}$	68010 read/write control, buffered	$\overline{\text{HORZDL}}$, $\overline{\text{HORZDL}}$	HORZ delayed one clock cycle
$\overline{\text{BUFCLR}}$	Swap "A" and "B" line buffers, clear line buffer counter chain	HPOS0-HPOS8	Motion object horizontal position data
BW/ $\overline{\text{R}}$	68010 read/write inverted, buffered	$\overline{\text{HSCRLD}}$	Latch playfield horizontal scroll data
CA5, CA7	Color RAM address bits 5 and 7		
CCTR1, CCTR2	Coin counter outputs 1 and 2,		
$\overline{\text{CLRA}}$	Clear line buffer "A" address counters		
$\overline{\text{CLRB}}$	Clear line buffer "B" address counters		

NOTE

In this signal name glossary all active-low signals are over-scored, e.g., $\overline{\text{COMPSYNC}}$. In the schematics printed on Sheets 1-16 a slash (/) in front of a signal name indicates an active-low signal.

Gauntlet Signal Name Glossary, continued

VBUS	68010 "V" bus enable (for video RAM)
VCC	System V _{cc} (5 volts regulated)
VCPU	68010-to-video-RAM synchronization control
$\overline{\text{VERT}}$	Latch motion object vertical data and size data
VERTDL, $\overline{\text{VERTDL}}$	VERT delayed one clock cycle
$\overline{\text{VIDBLANK}}$	Video blank (horizontal and vertical blank mixed)
$\overline{\text{VMATCH}}$	Motion object vertical parameter matches current playfield vertical position
VOICE	Speech chip select
VPOS0-VPOS8	Motion object vertical position data
VRA0-VRA11	Video RAM address bus
$\overline{\text{VRAM}}$	68010 address decode for video RAM
$\overline{\text{VRAMRD}}$	68010 read from video RAM
$\overline{\text{VRAMWE}}$	68010 write to video RAM
VRD0-VRD15	Video RAM data bus, unbuffered
VRTACK	Video RAM to 68010 data acknowledge
VSIZ0-VSIZ2	Motion object vertical size parameter
VSYNC, $\overline{\text{VSYNC}}$	Vertical sync
$\overline{\text{WDOG}}$	Watchdog control
$\overline{\text{WH}}$	68010 write high byte
$\overline{\text{WL}}$	68010 write low byte
$\overline{\text{WR68K}}$	6502 write to output buffer (to 68010)
$\overline{\text{YAMRES}}$	Music chip reset
YM0-YM2	Music audio mix control bits
ZREF	Intensity reference for video output

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Gauntlet™ Signal Name Glossary, Continued

Gauntlet Signal Name Glossary, continued

RAM0, RAM1	68010 working RAM chip selects	$\overline{\text{SNDBUF}}$	6502 output buffer full (to 68010)
RAUD	Summed right channel audio	$\overline{\text{SNDINT}}$	68010 interrupt from 6502
RCLOCK	System clock	$\overline{\text{SNDIRQ}}$	6502 4-millisecond interrupt
RD0–RD15	68010 ROM data bus	$\overline{\text{SNDNMI}}$	6502 non-maskable interrupt
$\overline{\text{RD68K}}$	6502 read 68010 output buffer	$\overline{\text{SNDRD}}$	68010 read buffer from 6502
RED	Red analog video output	$\overline{\text{SNDRES}}$	6502 master reset (controlled by 68010)
RED0–RED3	Red color RAM data	$\overline{\text{SNDWR}}$	68010 write to output buffer (to 6502)
RIGHT-1– RIGHT-4	Joystick right switch inputs, players 1–4	SOD	Serial output data
ROM	68010 ROM data bus enable	$\overline{\text{SPHRDY}}$	Speech chip ready
$\overline{\text{ROM0}}\text{--}\overline{\text{ROM4}}$	68010 program ROM chip selects	$\overline{\text{SPHRES}}$	Speech chip reset
ROMH/L	68010 program ROM high/low select (A14 on a 27256)	$\overline{\text{SPHWR}}$	Speech chip write
ROUT0–ROUT3	Red latched digital video output	SQUEAK	Speech chip operating frequency control
SA0–SA15	6502 address bus unbuffered	$\overline{\text{SRD}}$	6502 read phase
SBA0–SBA13	6502 buffered address bus	START-1–START-4	Start switch inputs, players 1–4
SBD0–SBD7	6502 buffered data bus	STEST	Self-test switch input
SBR/ $\overline{\text{W}}$	6502 buffered read/write control	$\overline{\text{SWR}}$	6502 write phase
SBW/ $\overline{\text{R}}$	6502 buffered read/write control inverted	$\overline{\text{SYSRES}}$	System reset (power up)
SD0–SD7	6502 data bus unbuffered	$\overline{\text{UDS}}$	68010 upper data strobe
$\overline{\text{SELFTTEST}}$	Self-test switch input test pad	$\overline{\text{UNLOCK}}$	EEPROM write enable control
SID	Serial input data	UP-1–UP-4	Joystick up switch inputs, players 1–4
$\overline{\text{SIORD}}$	6502 miscellaneous input read control	VAS0, VAS1 (VAS0*), (VAS1*)	Video RAM address control VAS0 and VAS1 before being latched
$\overline{\text{SIOWR}}$	6502 output latch control	VBD0–VBD15	Video RAM buffered data bus
$\overline{\text{SIQACK}}$	6502 interrupt acknowledge	$\overline{\text{VBKACK}}$	Vertical blank interrupt acknowledge
SLAPSTK	SLAPSTIC chip select	$\overline{\text{VBKINT}}$	Vertical blank interrupt
SM0–SM2	Speech audio mix control bits	$\overline{\text{VBLANK}}$	Vertical blank