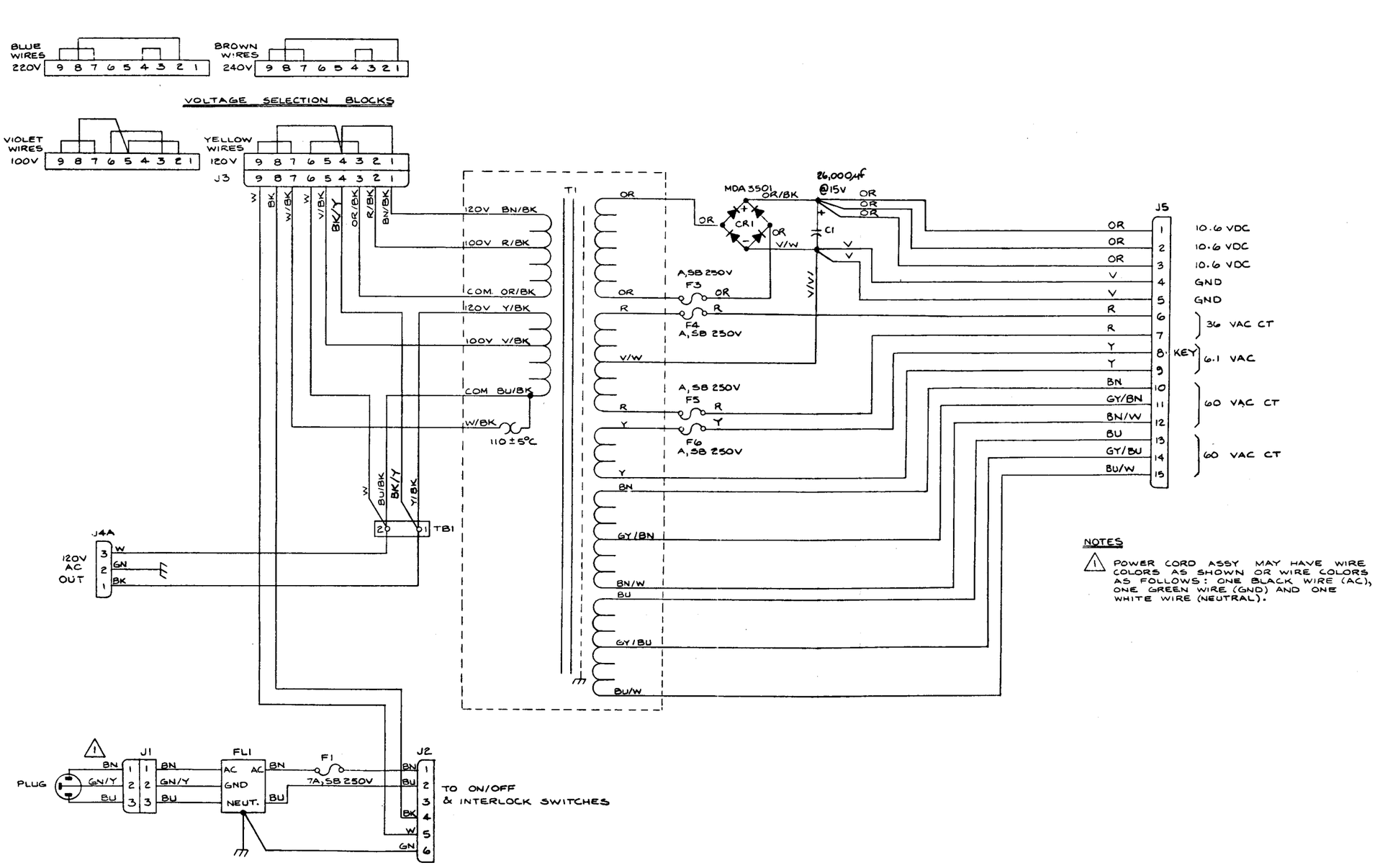
Power Supply Schematic (037669-01 C)



Regulator Audio II PCB

Regulator/Audio II PCB

The Regulator/Audio II PCB has th
ulating the +5 VDC logic power to
plifying the audio from the game PC

Regulator Circuit

The regulator consists of voltag
pass transistor Q3 and Q3's driver tr
tor accurately regulates the logic p
PCB by monitoring the voltage thro
puts +SENSE and −SENSE. The
the +5 VDC and ground inputs to th
the regulator regulates the voltage
eliminates a reduced voltage due
harness between the regulator and
resistor R8 is adjusted for the +5
Once adjusted, the voltage at the inp
remain constant at this voltage.

Regulator Adjustment

1. Connect a voltmeter between +
of the game PCB.
2. Adjust variable resistor R8 on
PCB for +5 VDC reading on th
3. Connect a voltmeter between
the Regulator/Audio II PCB. Vo
be greater than +5.5 VDC. If gr
connectors on both the game
tor/Audio II PCB.
4. If cleaning PCB edge connector
age difference, connect minus le
test point of Regulator/Audio I
GND test point of game PCB. N
Now connect minus lead of vo
point on Regulator/Audio II PCB
test point on game PCB. From
harness circuit is dropping the
the appropriate harness wire or

Audio Circuit

The audio circuit contains two in
fiers. Each amplifier consists of a TD
an effective gain of 2.2.

Der

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ATARI®

Drawing Package Supplement

to

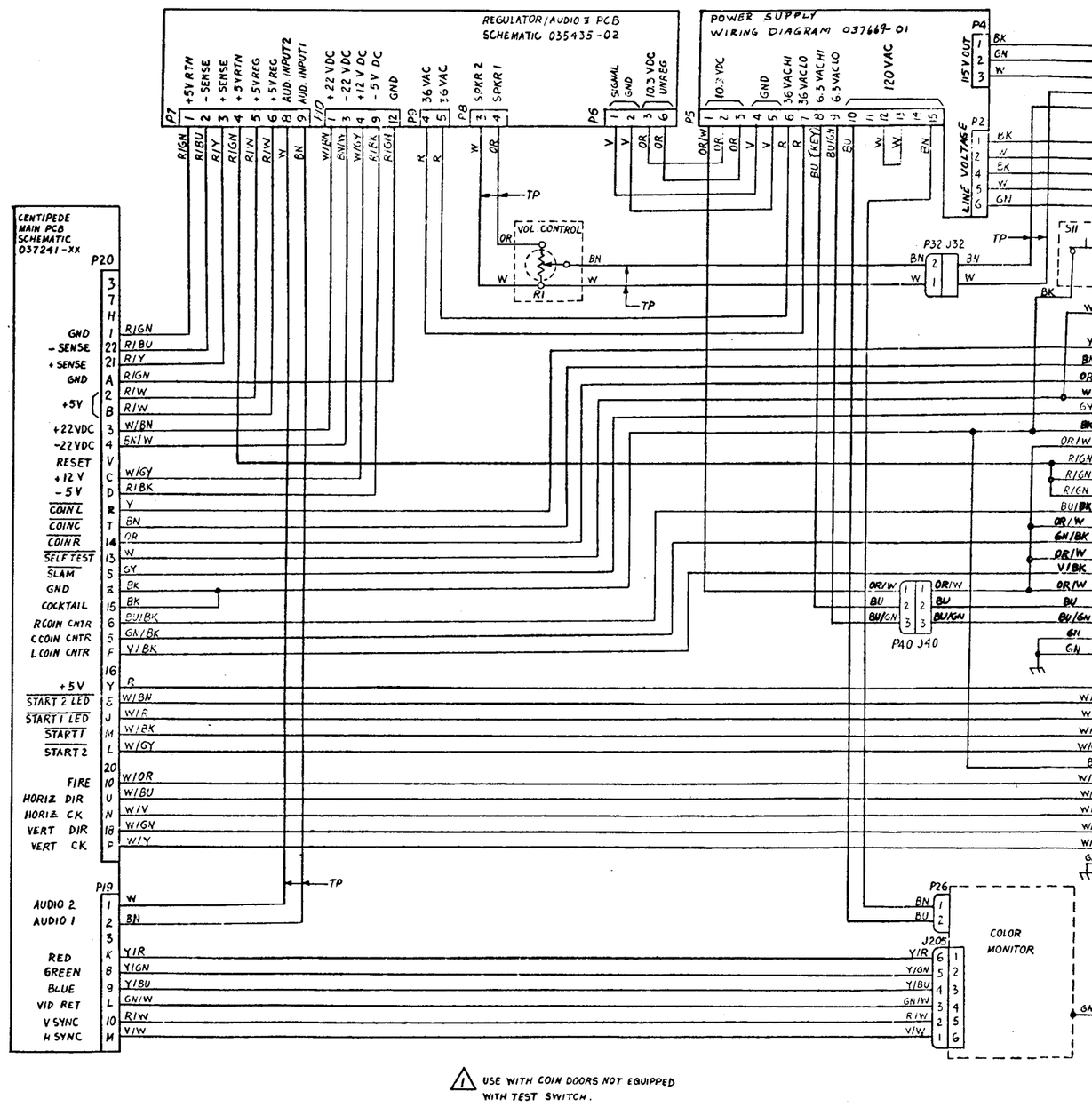
Centipede™

Operation, Maintenance and Service Manual

Contents of this Drawing Package

A Warner Communications Company

Centipede Wiring Diagram (037432-01 C)



CB Schematic (035435-02 E)

s the dual functions of reg-
r to the game PCB and am-
e PCB.

ltage regulator Q1, power
er transistor Q2. The regula-
c power input to the game
hrough high-impedance in-
he inputs are directly from
o the game PCB. Therefore,
ge on the game PCB. This
ue to IR loss in the wire
nd the game PCB. Variable
- 5 VDC on the game PCB.
input of the game PCB will

+ 5 V and GND test points

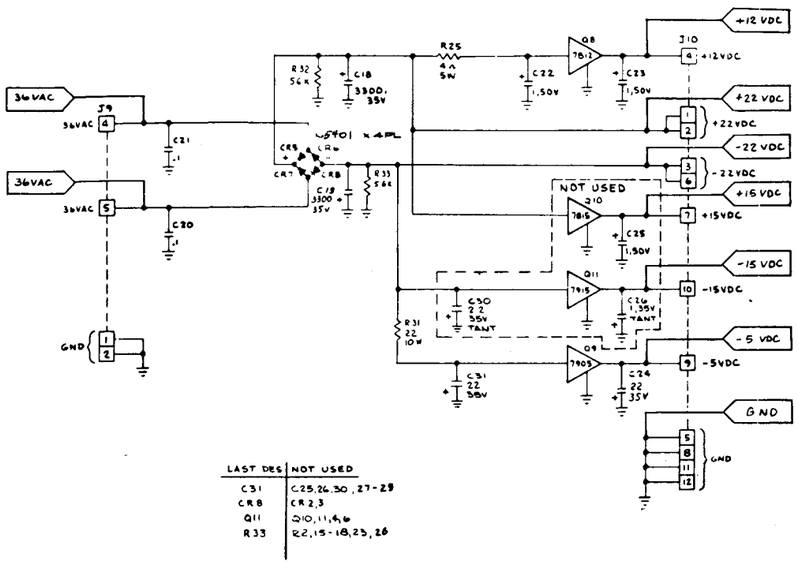
on the Regulator/Audio II
the voltmeter.

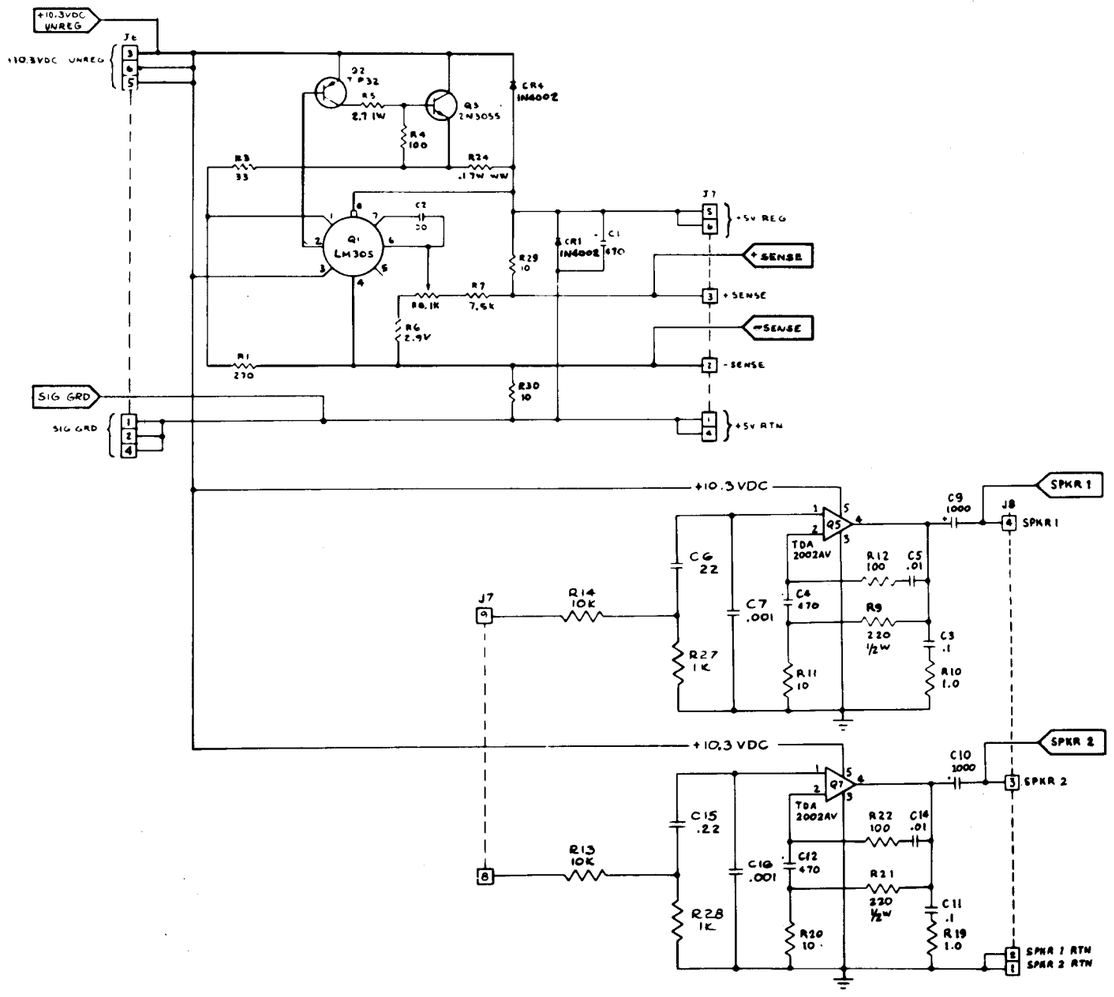
n + 5 V REG and GND on
Voltage reading must not
f greater, try cleaning edge
me PCB and the Regula-

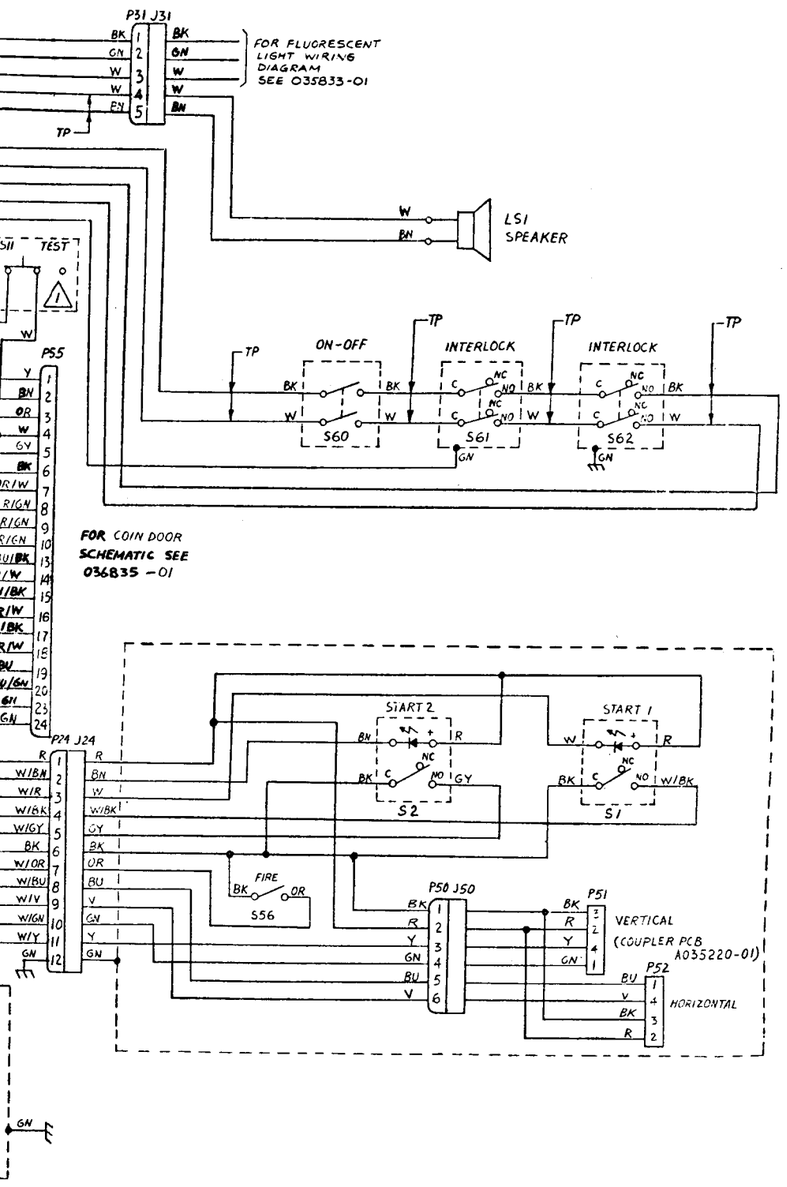
ctors doesn't decrease volt-
s lead of voltmeter to GND
o II PCB and plus lead to
3. Note the voltage.
f voltmeter to + 5 REG test
PCB and plus lead to + 5 V
om this you can see which
the voltage. Troubleshoot
or harness connector.

independent audio ampli-
TDA2002AV amplifier with

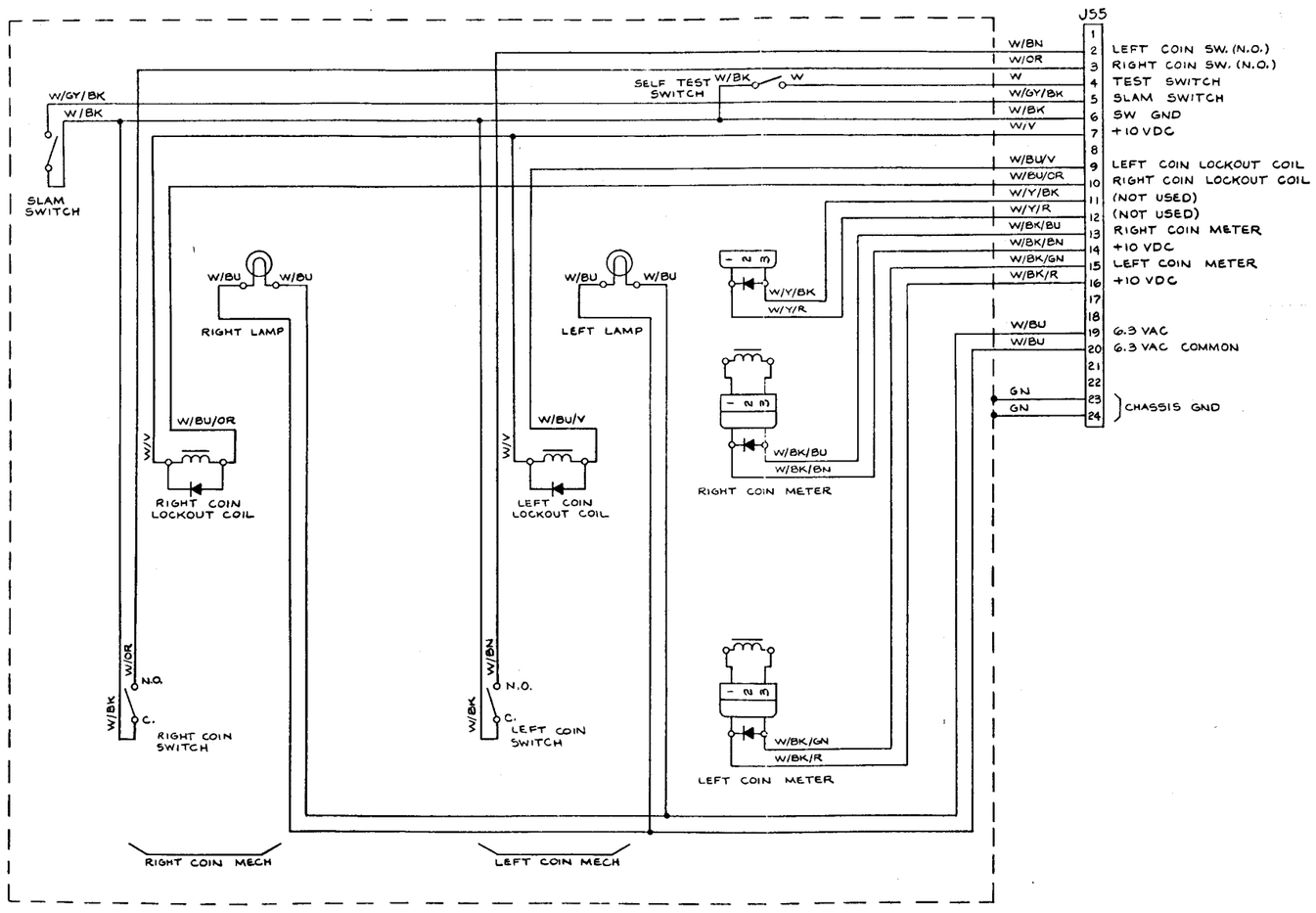
Denotes a test point



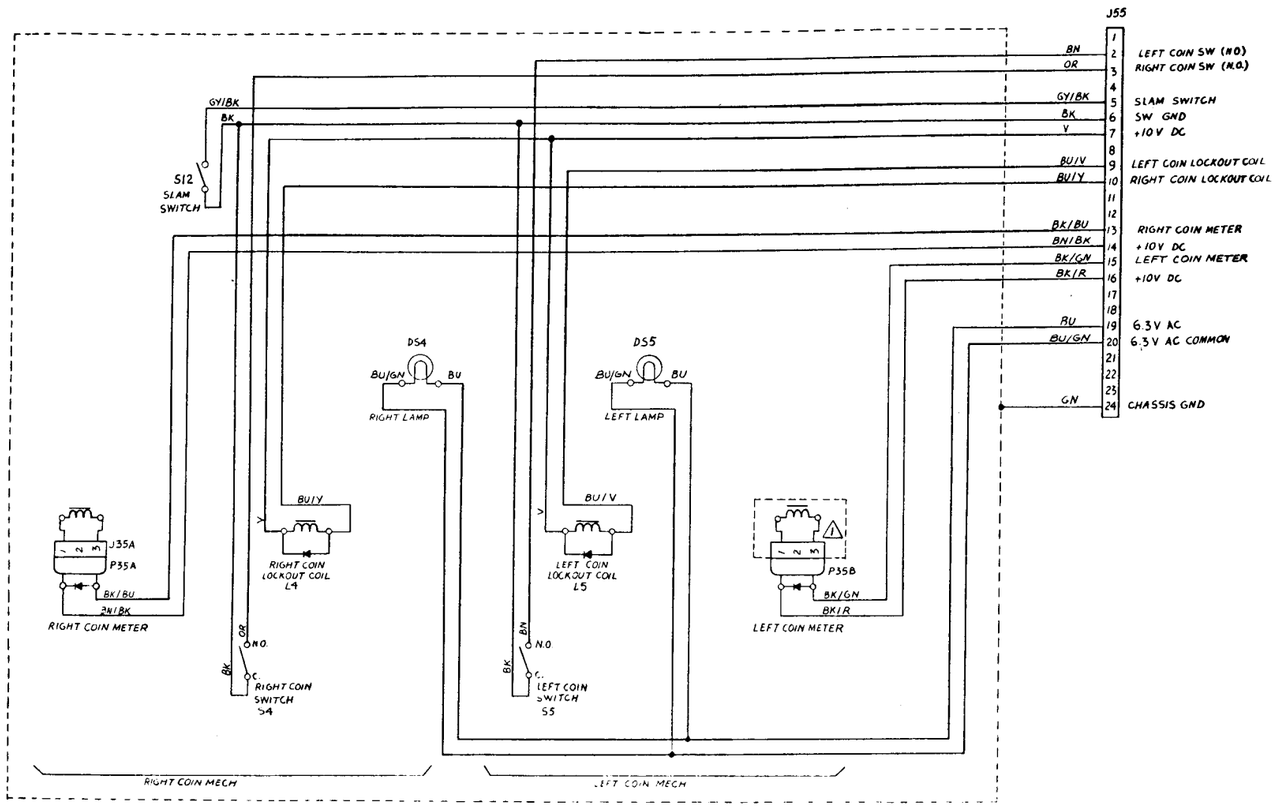




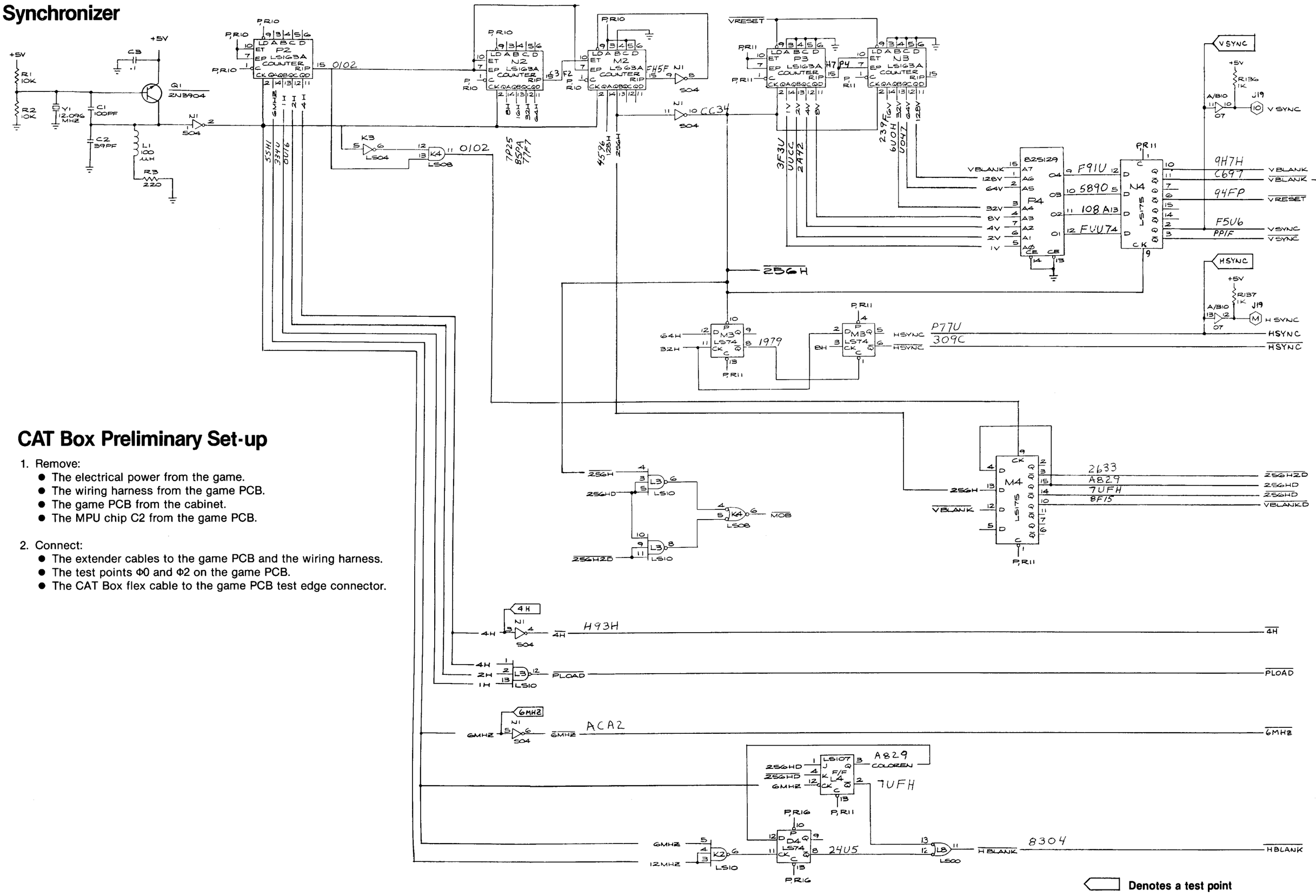
American-Made Coin Door Schematic (036835-01 B)



British-Made Coin Door Schematic (037050-01 A)



Synchronizer



CAT Box Preliminary Set-up

1. Remove:
   - The electrical power from the game.
   - The wiring harness from the game PCB.
   - The game PCB from the cabinet.
   - The MPU chip C2 from the game PCB.

2. Connect:
   - The extender cables to the game PCB and the wiring harness.
   - The test points Φ0 and Φ2 on the game PCB.
   - The CAT Box flex cable to the game PCB test edge connector.

Diagnostic Tests

Instruction	Use of Test
1. Hold the slam switch closed, while setting the self-test switch to the **on** position.	The monitor displays the color hue adjustment pattern of 16 rectangles, as follows. **Do not attempt any color hue or brightness adjustments unless you are a qualified color TV technician!** Pale Yellow-Green / Orange / White / Deep Yellow Light Green / Dark Green / Light Blue / Lime Green Deep Rose / Red / Purple / Red Navy Blue / Black / Royal Blue / Black
2. Activate any of the coin switches on the coin door.	A convergence pattern appears with a grid of white dots on a black screen. **Do not attempt any convergence adjustments unless you are a qualified color TV technician!**
3. Set self-test switch to the **off** position.	Check attract-mode display and readjust brightness if necessary.

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Sheet 1, Side B

Centipede™

Synchronizer
CAT Box Preliminary Set-Up
Power Input
Microprocessor
Address Decoder
RAM
ROM
Memory Map

Section of 037241-01 G

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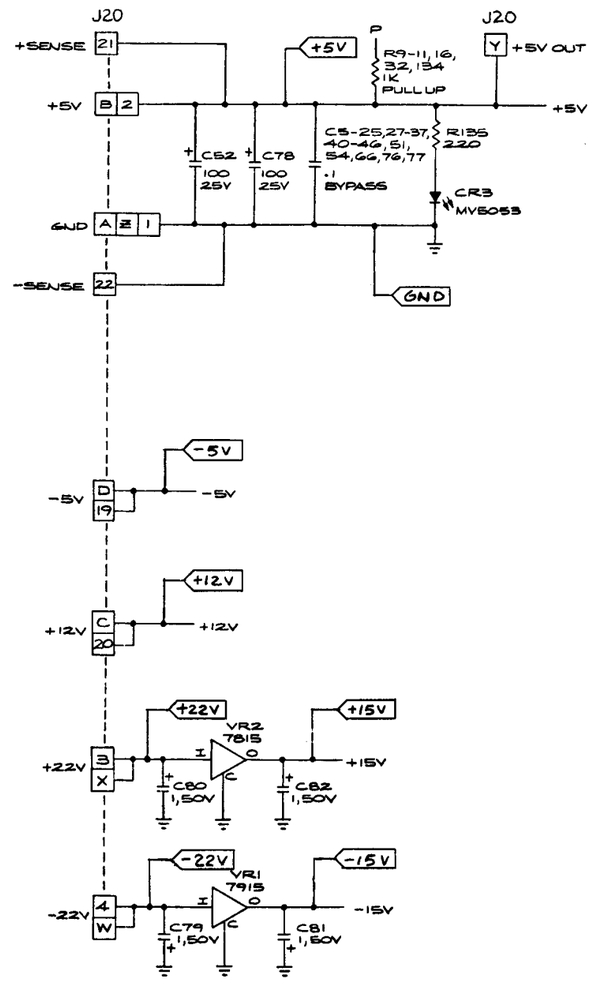
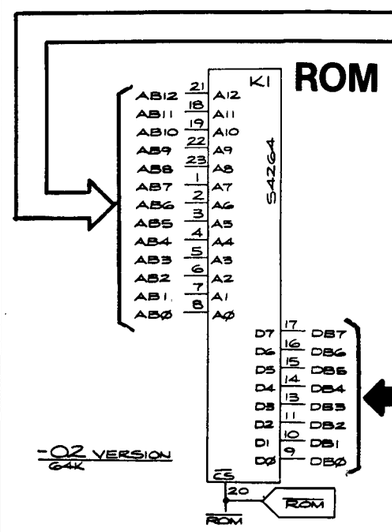
Power Input



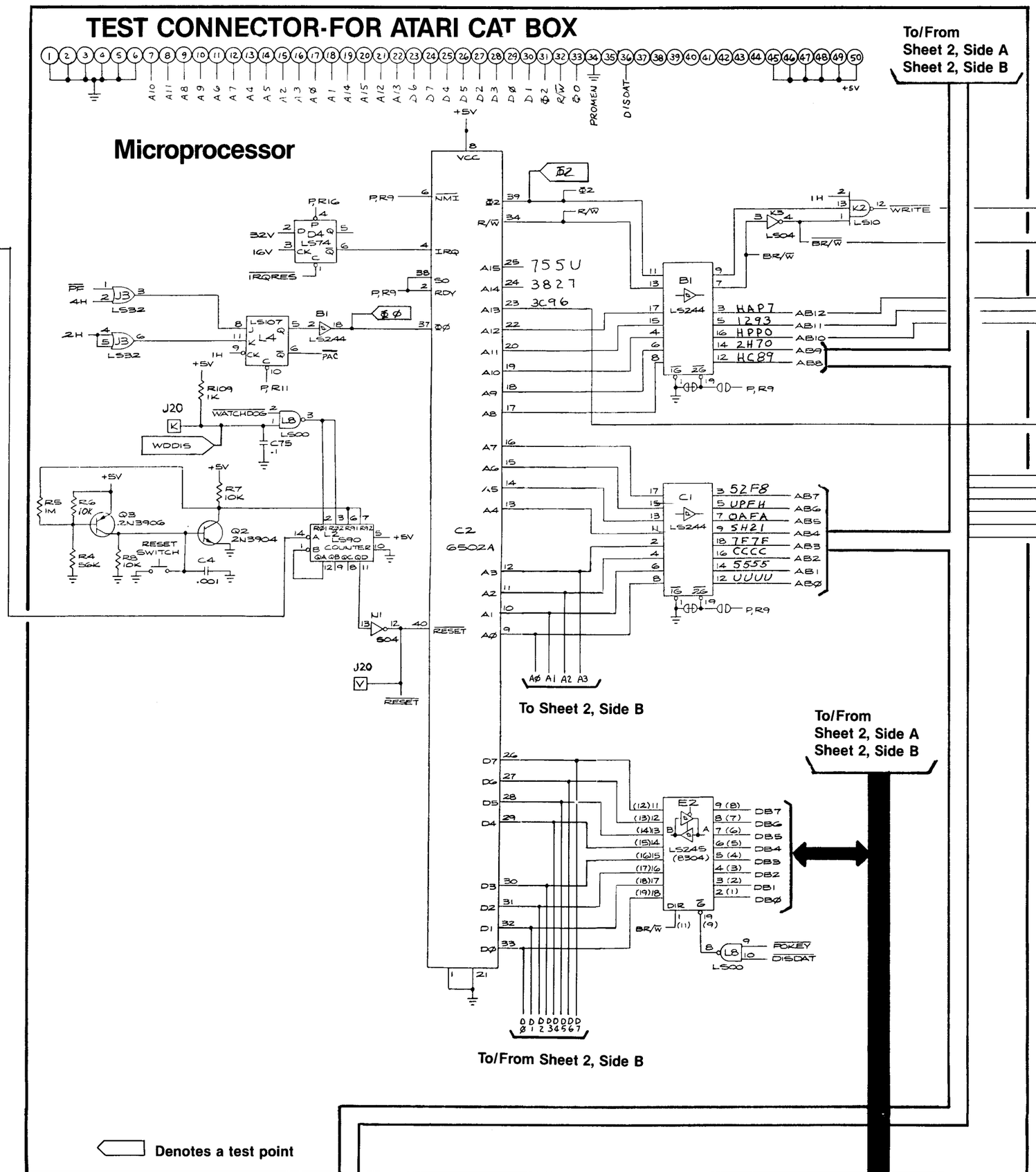
Testing the RA

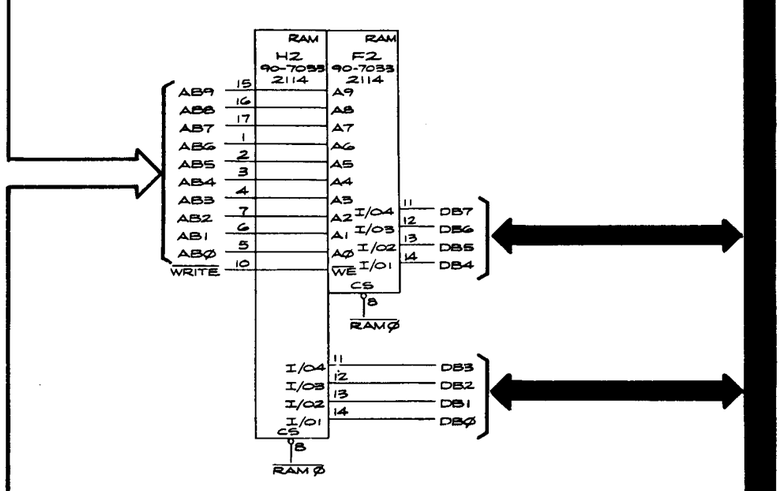
1. Perform the CAT Box
2. Set the CAT Box swit
   a. Press TESTER RE
   b. DBUS SOURCE T
   c. BYTES to 1024
   d. R/W MODE to (OF
   e. R/W to WRITE
   f. Key in 0000
   g. Set R/W MODE to
   h. R/W to READ
   i. Set R/W MODE to
3. If the CAT Box reads a PARE ERROR LED li shows the failing adc PLAY switch is enable
4. If the COMPARE ERR peat the test with the ensures that the data COMPARE ERROR LE is good.



Sheet 1, Side B
DP-182-01 5th printing
Centipede

A Warner Communications Company





RAM

Box preliminary set-up.

switches as follows:

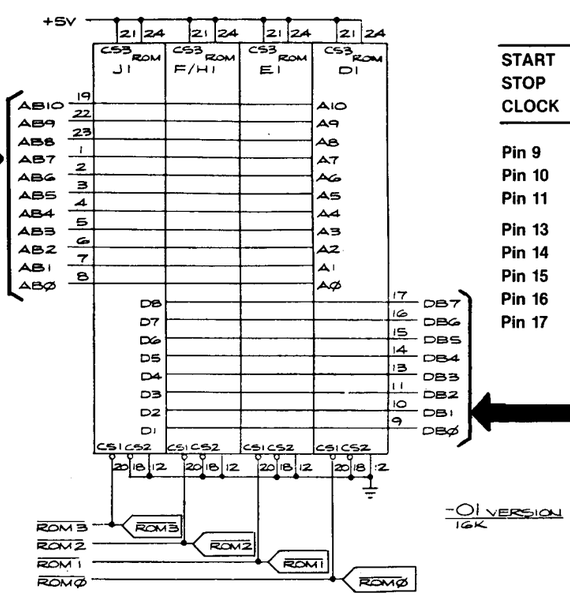
R RESET
CE TO ADDR
4
(OFF)
E

E to PULSE, then to OFF.

E to PULSE, then to OFF.

ads an address that doesn't compare, the COM-
ED lights, the ADDRESS/SIGNATURE display
g address location, and the ERROR DATA DIS-
nabled.

ERROR LED does not light, rekey 0000 and re-
n the DBUS SOURCE switch set to ADDR. This
data bits at address 0000 will go high. If the
OR LED does not light after this step, the RAM



-200 Version	D1	E1	F/H1	J1
START	Pin 20	Pin 20	Pin 20	Pin 20
STOP	Pin 20	Pin 20	Pin 20	Pin 20
CLOCK	Φ 2	Φ 2	Φ 2	Φ 2
Pin 9	5AF2	13PH	CU62	476H
Pin 10	3276	C4P5	9553	2A2C
Pin 11	48UH	11F3	7756	2337
Pin 13	P316	098P	A7CF	FP07
Pin 14	PF7A	5H24	6081	A9AF
Pin 15	H973	0548	5HAC	12HA
Pin 16	3F34	33P7	6U43	2367
Pin 17	U638	80AA	F83H	8P82

-300 Version	D1	E1	F/H1	J1
START	Pin 20	Pin 20	Pin 20	Pin 20
STOP	Pin 20	Pin 20	Pin 20	Pin 20
CLOCK	Pin 20	Pin 20	Pin 20	Pin 20
Pin 9	8H07	2956	77C1	75CU
Pin 10	7916	18F6	04CC	3FFA
Pin 11	7052	F829	11F0	F717
Pin 13	H3FH	6200	6UC2	H5U0
Pin 14	H6F1	47C0	1300	959U
Pin 15	1322	F341	6572	5050
Pin 16	U577	67FP	U047	C439
Pin 17	F189	8UF5	9U68	HF82

Memory Map

MEMORY MAP

HEXA-DECIMAL ADDRESS	R/W	DATA D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0000-03FF		D	D	D	D	D	D	D	D	RAM
0400-07BF		D	D	D	D	D	D	D	D	Playfield RAM
07C0-07CF		D	D	D	D	D	D	D	D	Motion Object Picture
07D0-07DF		D	D	D	D	D	D	D	D	Motion Object Vert.
07E0-07EF		D	D	D	D	D	D	D	D	Motion Object Horiz.
07F0-07FF				D	D	D	D	D	D	Motion Object Color
0800	R	D	D	D	D	D	D	D	D	Option Switch 1 (0 = On)
0801	R	D	D	D	D	D	D	D	D	Option Switch 2 (0 = On)
0C00	R	D				D	D	D	D	Horizontal Mini-Trak Ball™ Inputs
	R		D							VBLANK (1 = VBlank)
	R			D						Self-Test (0 = On)
	R				D					Cocktail Cabinet (1 = Cocktail)
0C01	R	D	D	D						R,C,L Coin Switches (0 = On)
	R				D					SLAM (0 = On)
	R					D				Player 2 Fire Switch (0 = On)
	R						D			Player 1 Fire Switch (0 = On)
	R							D		Player 2 Start Switch (0 = On)
	R								D	Player 1 Start Switch (0 = On)
0C02	R	D				D	D	D	D	Vertical Mini-Trak Ball™ Inputs
0C03	R	D	D	D	D					Player 1 Joystick (R, L, Down, Up)
	R					D	D	D	D	Player 2 Joystick (0 = On)
1000-100F	R/W	D	D	D	D	D	D	D	D	Custom Audio Chip
1404	W					D	D	D	D	Playfield Color RAM
140C	W					D	D	D	D	Motion Object Color RAM
1600	W	D	D	D	D	D	D	D	D	EA ROM Address & Data Latch
1680	W					D	D	D	D	EA ROM Control Latch
1700	R	D	D	D	D	D	D	D	D	EA ROM Read Data
1800	W									IRQ Acknowledge
1C00	W	D								Left Coin Counter (1 = On)
1C01	W	D								Center Coin Counter (1 = On)
1C02	W	D								Right Coin Counter (1 = On)
1C03	W	D								Player 1 Start LED (0 = On)
1C04	W	D								Player 2 Start LED (0 = On)
1C07	W	D								Trak Ball™ Flip Control (0 = Player 1)
2000	W									WATCHDOG
2400	W									Clear Mini-Trak Ball™ Counters
2000-3FFF	R									Program ROM

Playfield Address Selector

The Playfield Address Selector controls the access to the playfield memory. It allows either the game MPU or the sync generator to scan the playfield memory. The Playfield Address Selector consists of multiplexers P5, and P7 and gate K4.

When $\overline{4H}$ on pin 1 of P5 and P7 is low and pin 15 on P7 is low, the Playfield Address Selector receives 8H, 16H, 32H, and 64H on P5 and 16V, 32V, 64V, and 128V on P7 from the sync generator. These signals enable the sync generator circuits to access the playfield memory.

When $\overline{4H}$ goes high the game MPU addresses the playfield memory (via AB0-AB9) for the positioning of the graphics. During horizontal blanking (pin 15 of P7 is high) the outputs of P7 (PFA4-PFA7) are held high enabling the motion object circuitry to access the playfield memory for the motion objects to be displayed.

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Sheet 2, Side A

Centipede™

Playfield Address Selector
Playfield Memory
Playfield Multiplexer
Picture Data ROM Circuitry
Motion Object Circuitry (Vertical)
Motion Object Circuitry (Horizontal)

Section of 037241-01 H

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Sheet 2, Side A
DP-182-02 5th printing
Centipede

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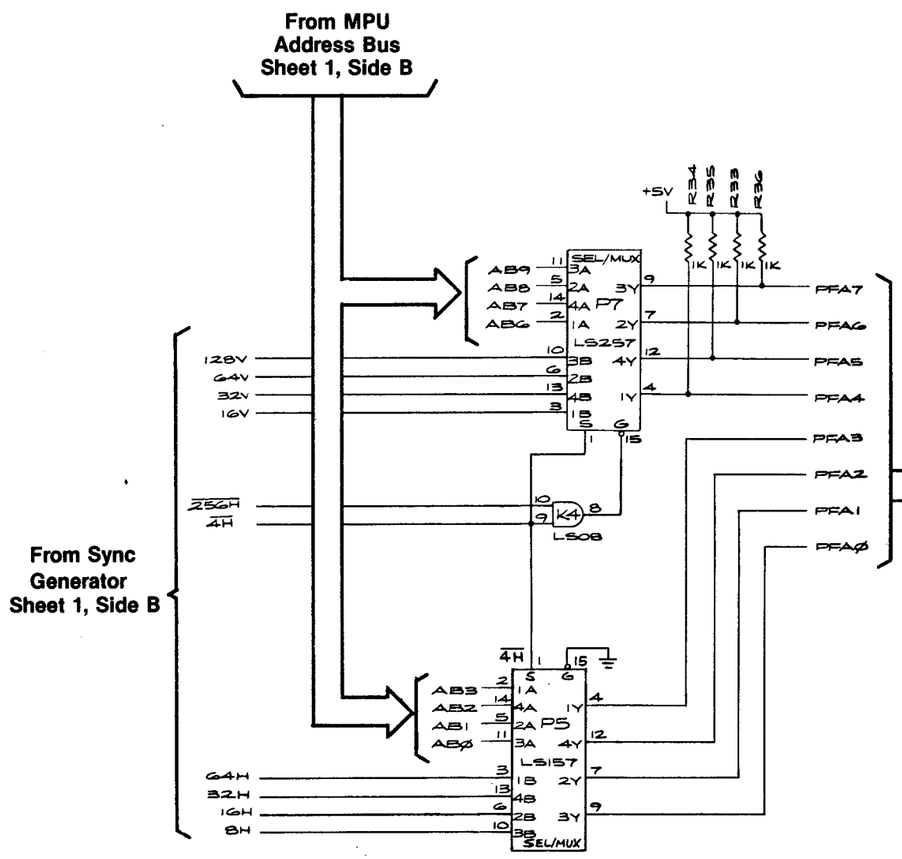
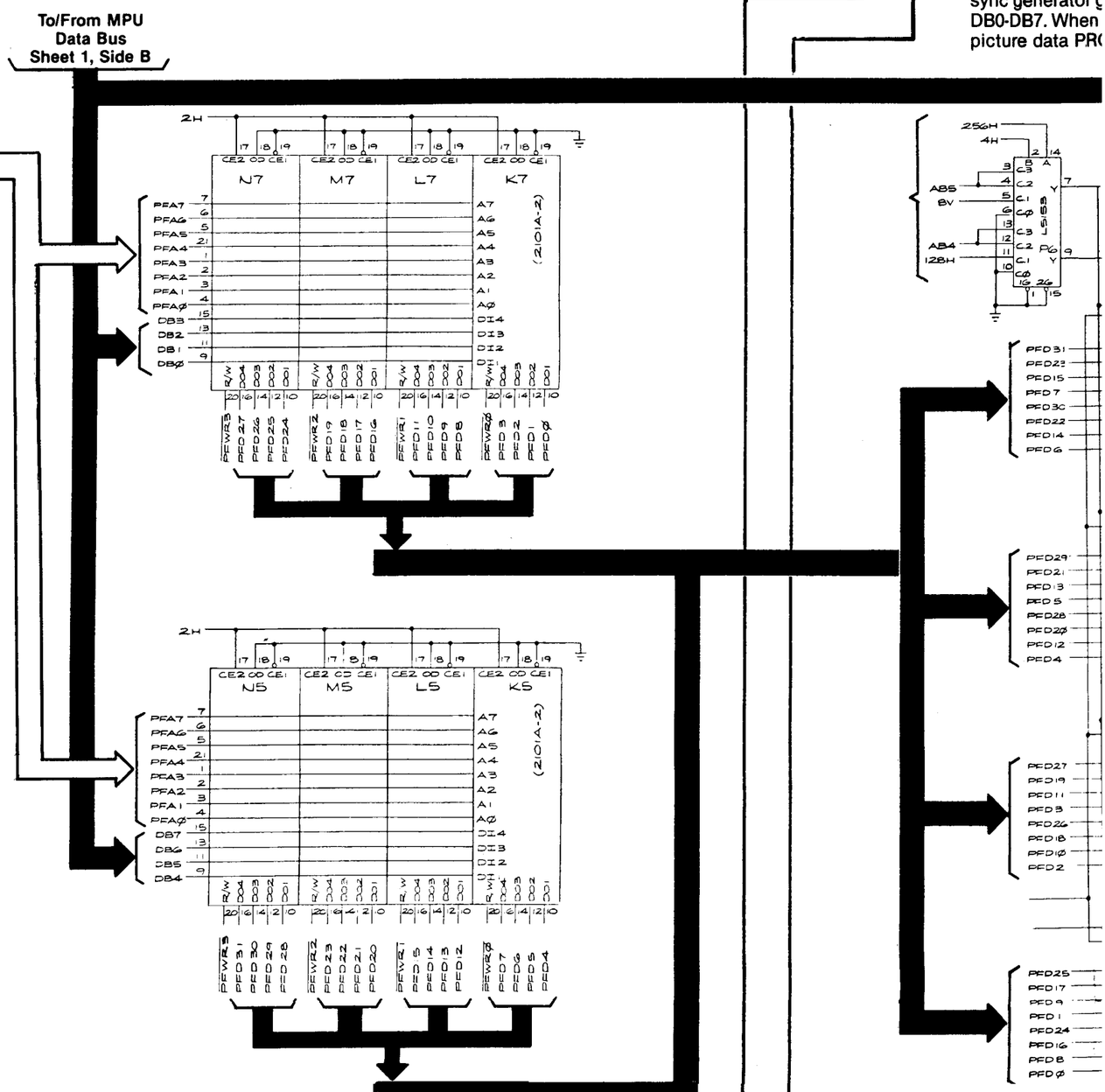
Centipede Playfield RAM

Testing the Playfield RAM

1. Perform the CAT Box preliminary set-up.
2. Set the CAT Box switches as follows:
   a. Press TESTER RESET
   b. DBUS SOURCE TO ADDR
   c. BYTES to 1024
   d. R/$\overline{W}$ MODE to (OFF)
   e. R/$\overline{W}$ to WRITE
   f. Key in 0400
   g. Set R/$\overline{W}$ MODE to PULSE, then to OFF.
   h. R/$\overline{W}$ to READ
   i. Set R/$\overline{W}$ MODE to PULSE, then to OFF.
3. If the CAT Box reads an address that doesn't compare, the COMPARE ERROR LED lights, the ADDRESS/SIGNATURE display shows the failing address location, and the ERROR DATA DISPLAY switch is enabled.
4. If the COMPARE ERROR LED does not light, rekey 0400 and repeat the test with the DBUS SOURCE switch set to $\overline{ADDR}$. This ensures that the data bits at address 0400 will go high. If the COMPARE ERROR LED does not light after this step, the Playfield RAM is good.

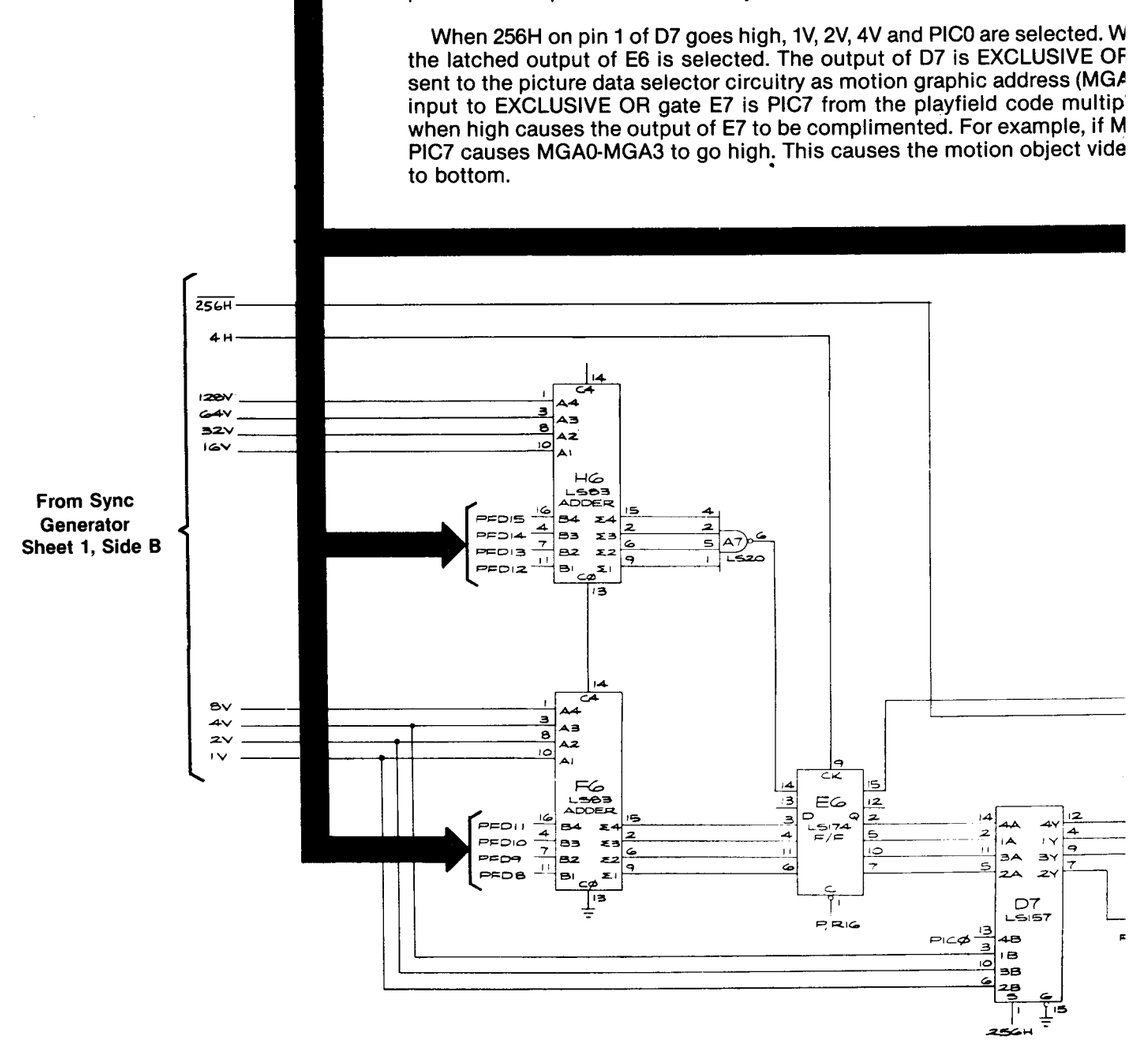




Motion Object Circuitry (Vertical

The Motion Object Circuitry (vertical) receives playfield data and verti sync generator circuitry to generate the vertical component of the motion 15 from the playfield memory and 1V-128V from the sync generator are com The output is gated by A7 when a motion object is on one of the sixteen latched by E6 to AND gate B7. A low on B7 pin 8 indicates the presence of one of the vertical lines during non-active video time. This signal (MATCH plexers in the picture data circuitry.

When 256H on pin 1 of D7 goes high, 1V, 2V, 4V and PIC0 are selected. W the latched output of E6 is selected. The output of D7 is EXCLUSIVE OF sent to the picture data selector circuitry as motion graphic address (MGA input to EXCLUSIVE OR gate E7 is PIC7 from the playfield code multip when high causes the output of E7 to be complimented. For example, if M PIC7 causes MGA0-MGA3 to go high. This causes the motion object vide to bottom.

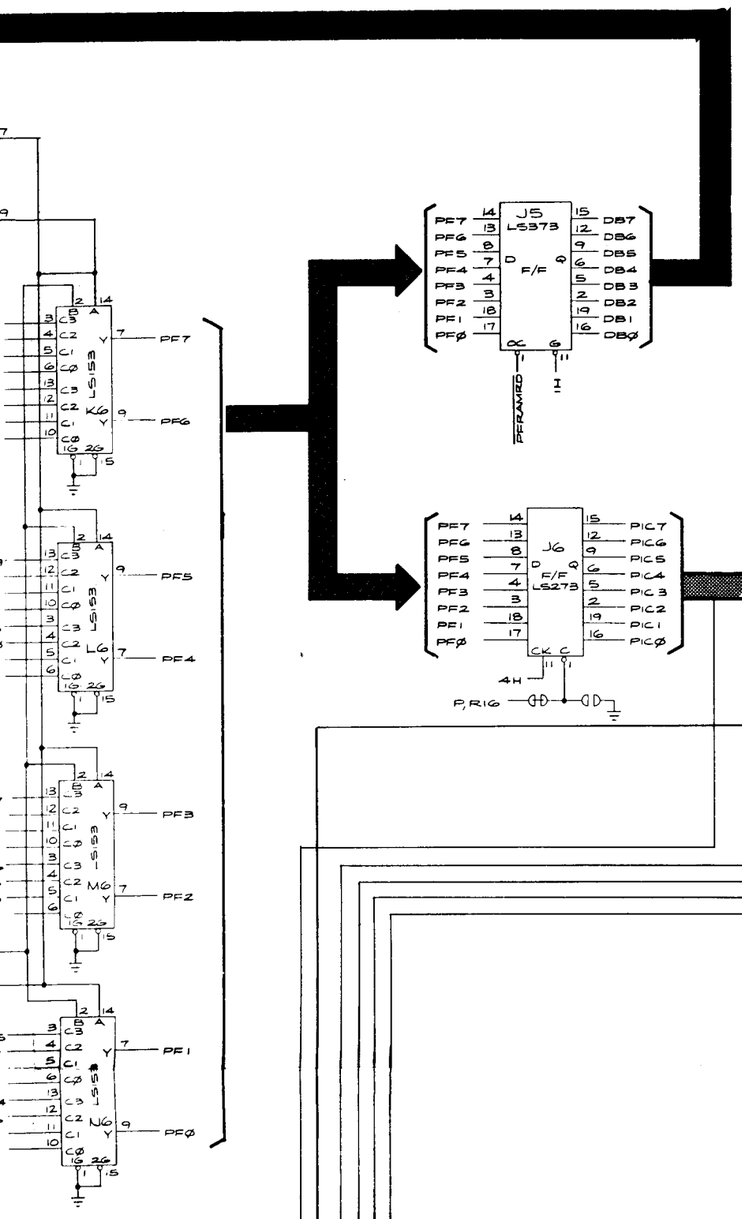


Playfield Multiplexer

field Multiplexer receives playfield data from the playfield memory 31) and the output (PF0-PF7) is a code that determines what is 1) dis- ne monitor, or2) read or updated by the MPU. The Playfield Multiplexer select multiplexers K6, L6, M6, N6 and P6.

6H is low and 4H is high, AB4 and AB5 from the MPU address bus is the tput from P6. This output is applied to multiplexers K6, L6, M6, and N6 puts. When the MPU is accessing the playfield code multiplexer, the ta is either being read or updated by the MPU. When 256H is high and 4H nputs from the sync generator (128H and 8V) are the selected outputs. als then select which bits of data PFD0-PFD31 are sent out via K6, L6, for the playfield codes that eventually are displayed on the monitor.

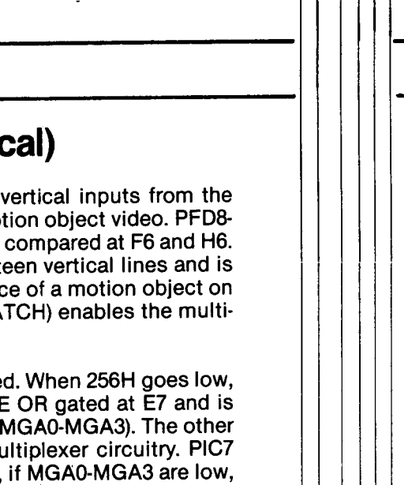
ield codes (PF0-PF7) are latched by J5 and J6 to the MPU data bus (J5) icture data PROM circuitry (J6). When PFRAMRD is low and 1H from the ator goes high, the inputs on J5 (PF0-PF7) are latched out to the MPU via hen 4H on pin 11 of 16 goes high, the inputs (PF0-PF7) are latched to the a PROM circuitry.



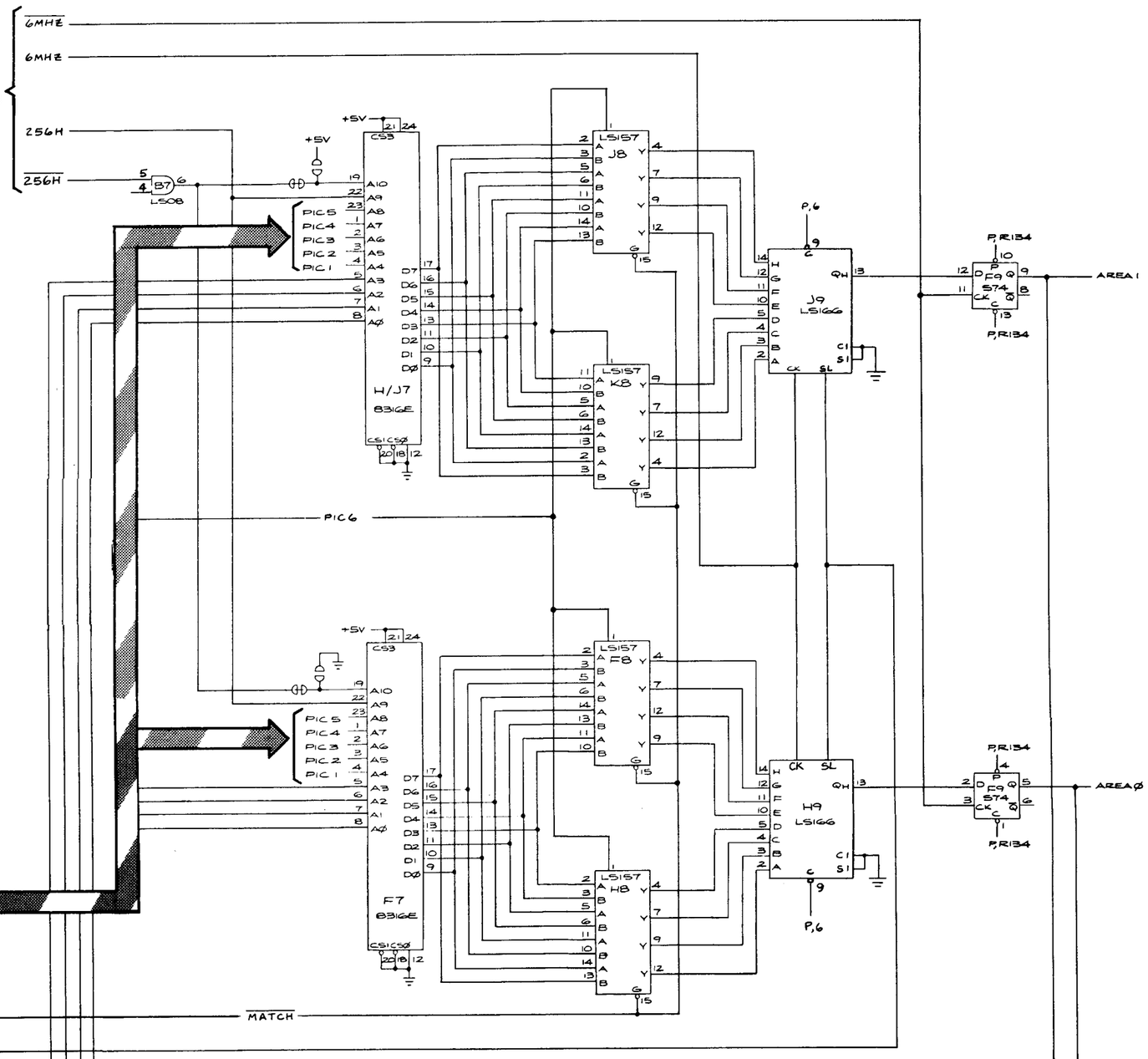
cal)

vertical inputs from the tion object video. PFD8- compared at F6 and H6. een vertical lines and is ce of a motion object on TCH) enables the multi-

d. When 256H goes low, E OR gated at E7 and is MGA0-MGA3). The other ultiplexer circuitry. PIC7 , if MGA0-MGA3 are low, video to be inverted top



From Sync Generator Sheet 1, Side B



Picture Data ROM Circuitry

The picture data ROM circuitry receives picture information, assigns a color code to the information and sends it to the color PROM circuitry. The picture data ROM circuitry consists of ROM devices F7 and H/J7, multiplexers F8, H8, J8, K8, shift registers H9 and J9, and latch F9.

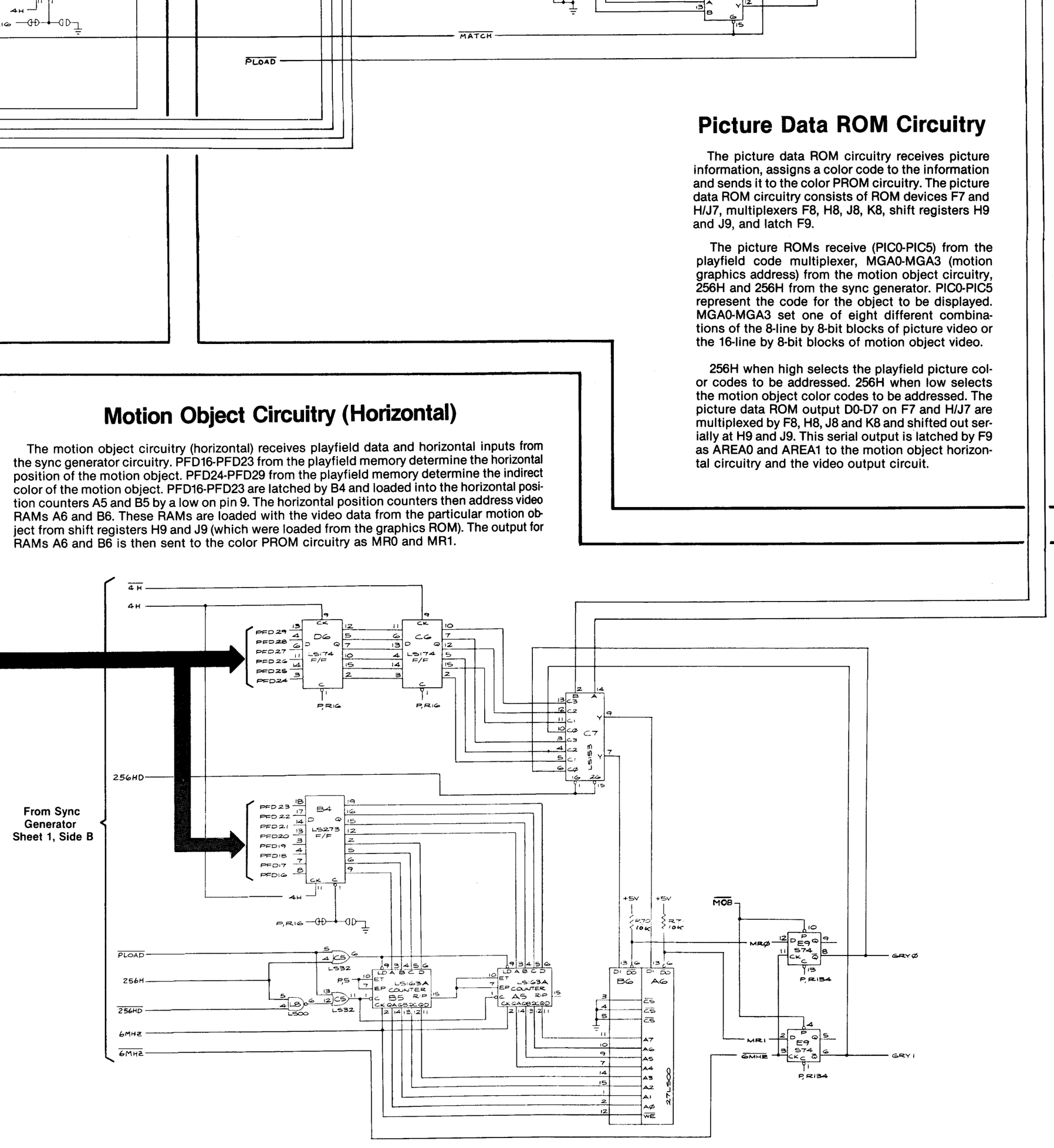
The picture ROMs receive (PIC0-PIC5) from the playfield code multiplexer, MGA0-MGA3 (motion graphics address) from the motion object circuitry, 256H and 256H from the sync generator. PIC0-PIC5 represent the code for the object to be displayed. MGA0-MGA3 set one of eight different combinations of the 8-line by 8-bit blocks of picture video or the 16-line by 8-bit blocks of motion object video.

256H when high selects the playfield picture color codes to be addressed. 256H when low selects the motion object color codes to be addressed. The picture data ROM output D0-D7 on F7 and H/J7 are multiplexed by F8, H8, J8 and K8 and shifted out serially at H9 and J9. This serial output is latched by F9 as AREA0 and AREA1 to the motion object horizontal circuitry and the video output circuit.

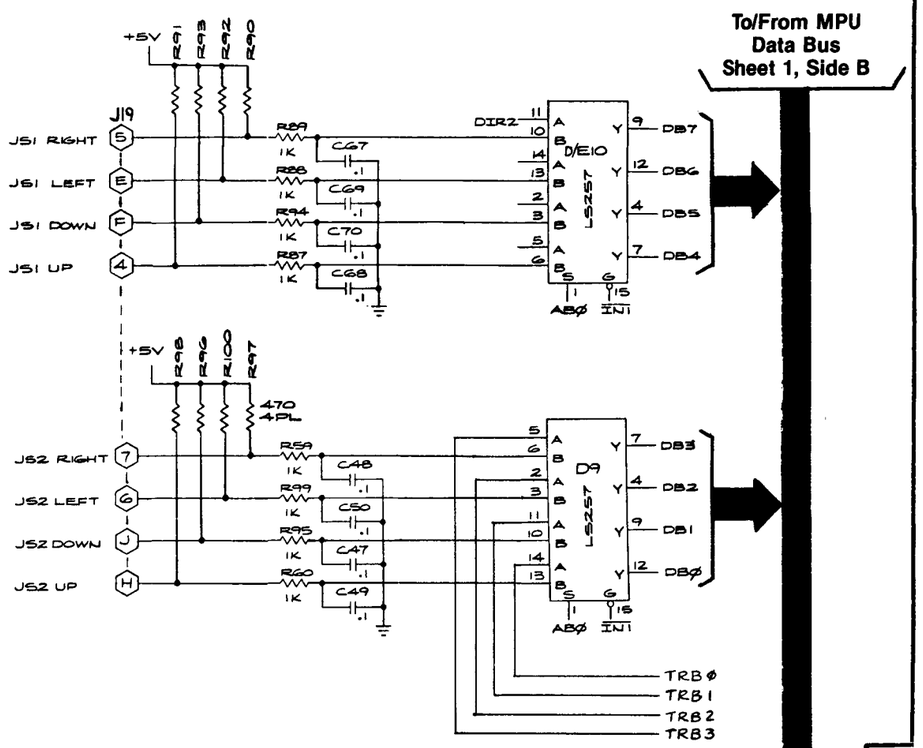
Motion Object Circuitry (Horizontal)

The motion object circuitry (horizontal) receives playfield data and horizontal inputs from the sync generator circuitry. PFD16-PFD23 from the playfield memory determine the horizontal position of the motion object. PFD24-PFD29 from the playfield memory determine the indirect color of the motion object. PFD16-PFD23 are latched by B4 and loaded into the horizontal position counters A5 and B5 by a low on pin 9. The horizontal position counters then address video RAMs A6 and B6. These RAMs are loaded with the video data from the particular motion object from shift registers H9 and J9 (which were loaded from the graphics ROM). The output for RAMs A6 and B6 is then sent to the color PROM circuitry as MR0 and MR1.

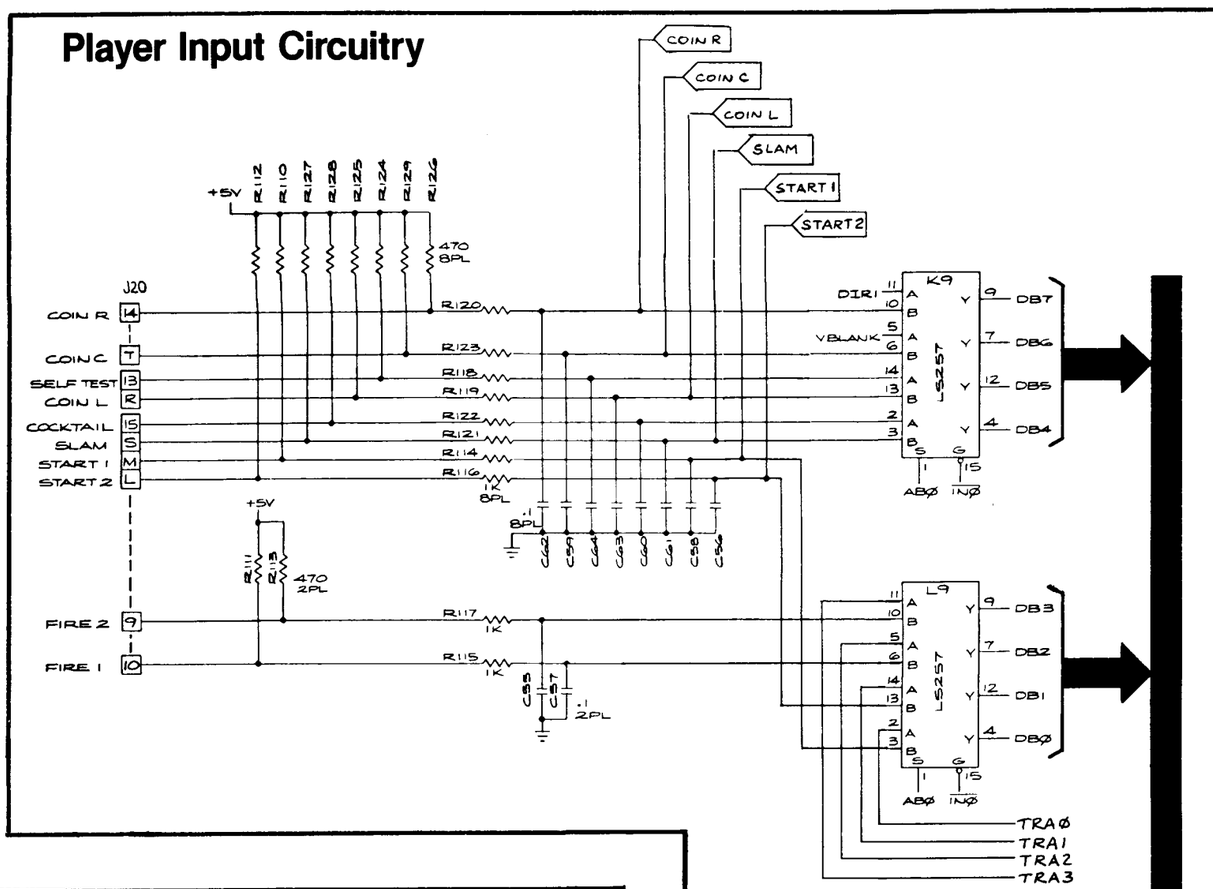
From Sync Generator Sheet 1, Side B



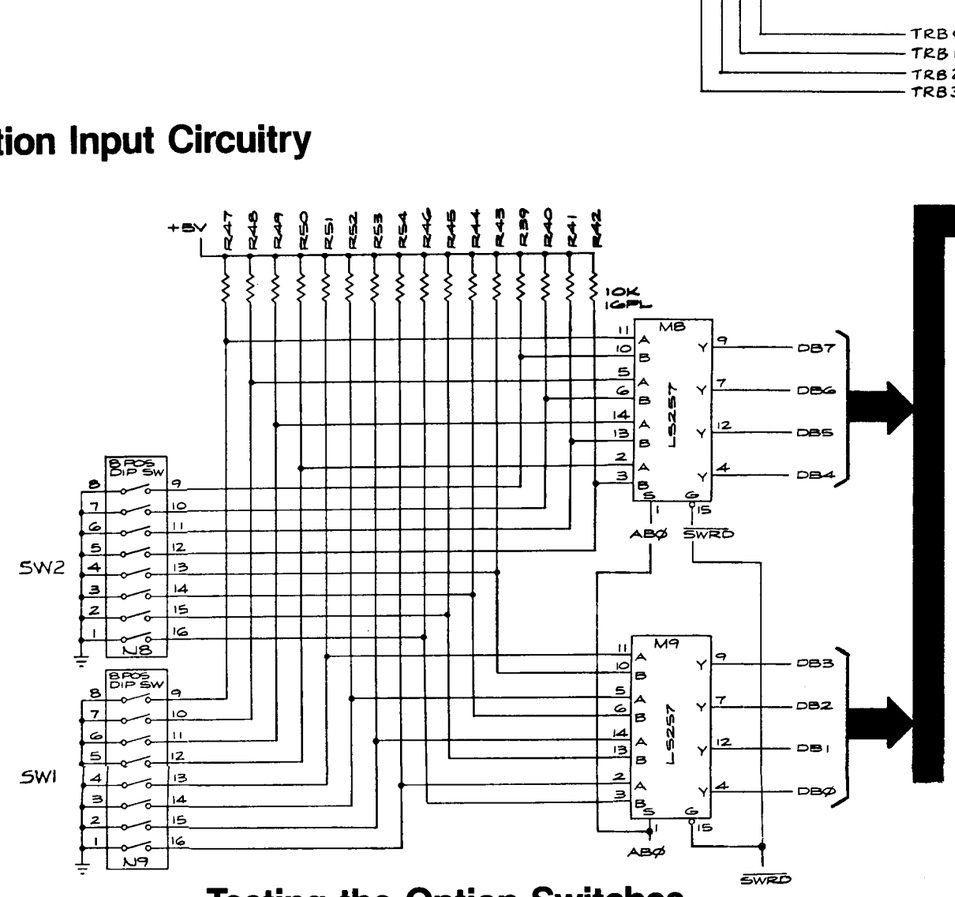
Joystick Circuitry



Player Input Circuitry



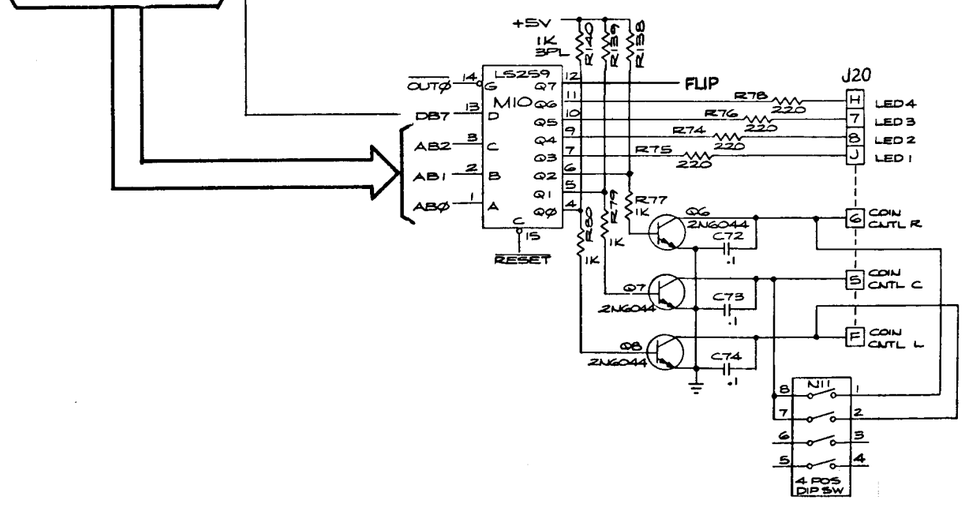
Option Input Circuitry



Testing the Option Switches

1. Perform the CAT Box preliminary set-up.
2. Set the CAT Box switches as follows:
   a. DBUS SOURCE to DATA
   b. BYTES to 1
   c. R/$\overline{W}$ to READ
   d. Key in address 0800 (N9) or 0801 (N8)
   e. R/$\overline{W}$ MODE to STATIC
3. Activate the switch while monitoring the DATA DISPLAY. The DATA DISPLAY will change if the switch is operating properly.

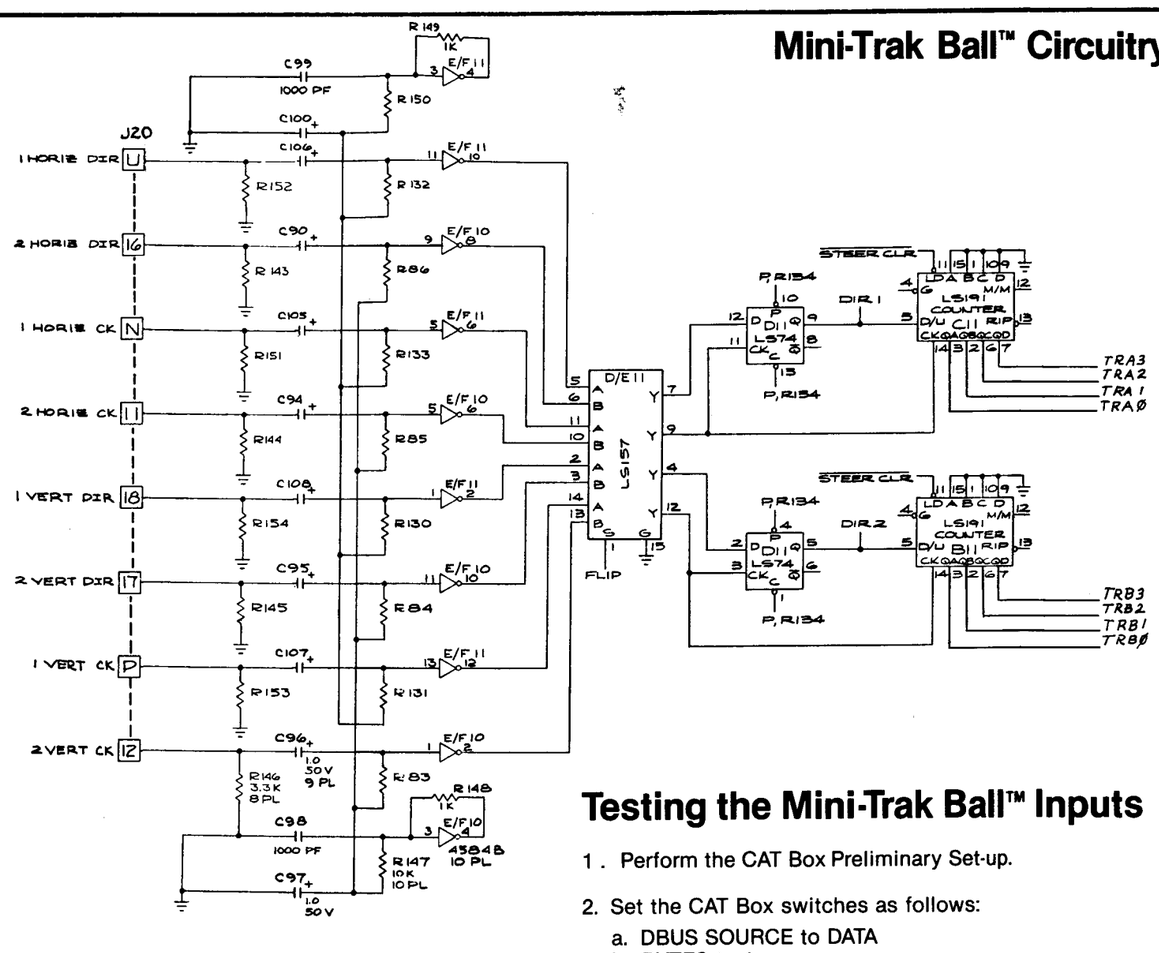
Coin Counter Output Circuitry



Coin Counter Output Circuit

This circuit consists of coin counter drivers Q6, Q7, and Q8 and data latch M10. The circuit is addressed by the MPU on AB0-AB2 and written by the MPU on data line DB7. When the input to a driver is clocked high, its collector goes low grounding the return of the coin door.

Mini-Trak Ball™ Circuitry



Testing the Mini-Trak Ball™ Inputs

1. Perform the CAT Box Preliminary Set-up.
2. Set the CAT Box switches as follows:
   a. DBUS SOURCE to DATA
   b. BYTES to 1
   c. R/$\overline{W}$ to READ
   d. Key in address 0C00 (vertical) or 0C02 (horizontal)
   e. R/$\overline{W}$ MODE to PULSE
3. Spin the Mini-Trak Ball™ while monitoring the DATA DISPLAY. The DATA DISPLAY will change if the Mini-Trak Ball input is operating properly.

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Centipede™

Joystick Circuitry
Mini-Trak Ball™ Circuitry
Player Input Circuitry
Video Output Circuitry
Audio Output Circuitry
Coin Counter Output Circuitry
Option Input Circuitry
High Score Memory Circuitry

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Centipede

Testing the Player Inputs

1. Perform the CAT Box Preliminary Set-up.
2. Set the CAT Box switches as follows:
   a. DBUS SOURCE to DATA
   b. BYTES to 1
   c. R/$\overline{W}$ to READ
   d. Key in address 0C00 (self-test switch only) or 0C01 (all others).
   e. R/$\overline{W}$ MODE to STATIC
3. Activate the following player input switches, one at a time, while monitoring the DATA DISPLAY:
   a. Coin Right
   b. Coin Left
   c. SLAM
   d. FIRE
   e. START 1
   f. START 2
4. The DATA DISPLAY will change if the switches are operating properly.

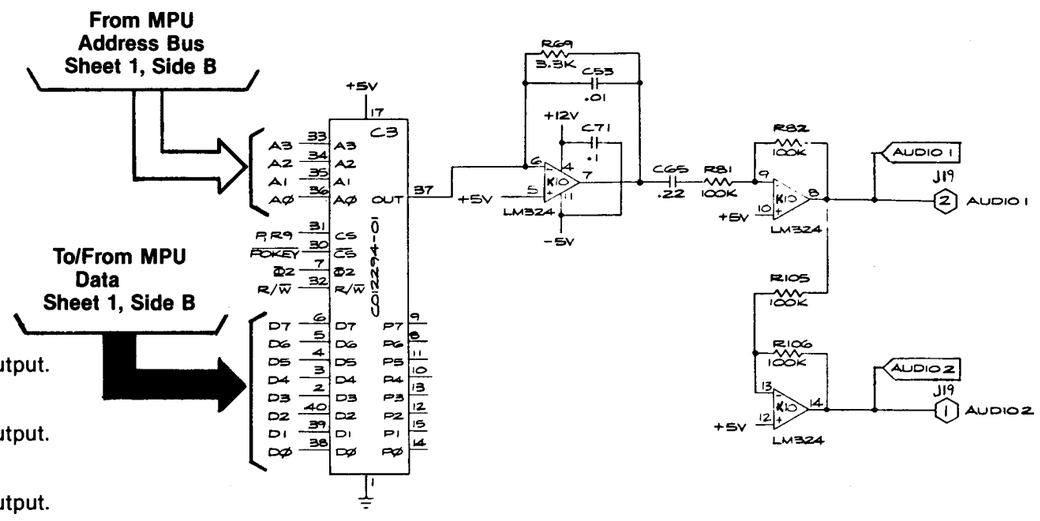
Denotes a test point

Testing the Audio Outputs

1. Perform the CAT Box preliminary set-up.
2. Set the CAT Box switches as follows:
   a. DBUS SOURCE to DATA
   b. BYTES to 1
   c. R/$\overline{W}$ to WRITE
   d. Key in address or press ADDRESS INCR
   e. Press DATA SET
   f. Key in data
   g. Set R/$\overline{W}$ MODE to PULSE, then to OFF.
   h. For each address, repeat sequence starting at Step d.

ADDRESS	DATA	RESULTS
100F	00	
100F	03	
1000	55	
1001	AF	Pure tone is heard from channel 1 output.
1001	00	Channel 1 output is turned off.
1002	55	
1003	AF	Pure tone is heard from channel 2 output.
1003	00	Channel 2 output is turned off.
1004	55	
1005	AF	Pure tone is heard from channel 3 output.
1005	00	Channel 3 output is turned off.
1006	55	
1007	AF	Pure tone is heard from channel 4 output.
1007	00	Channel 4 output is turned off.

Audio Output Circuitry



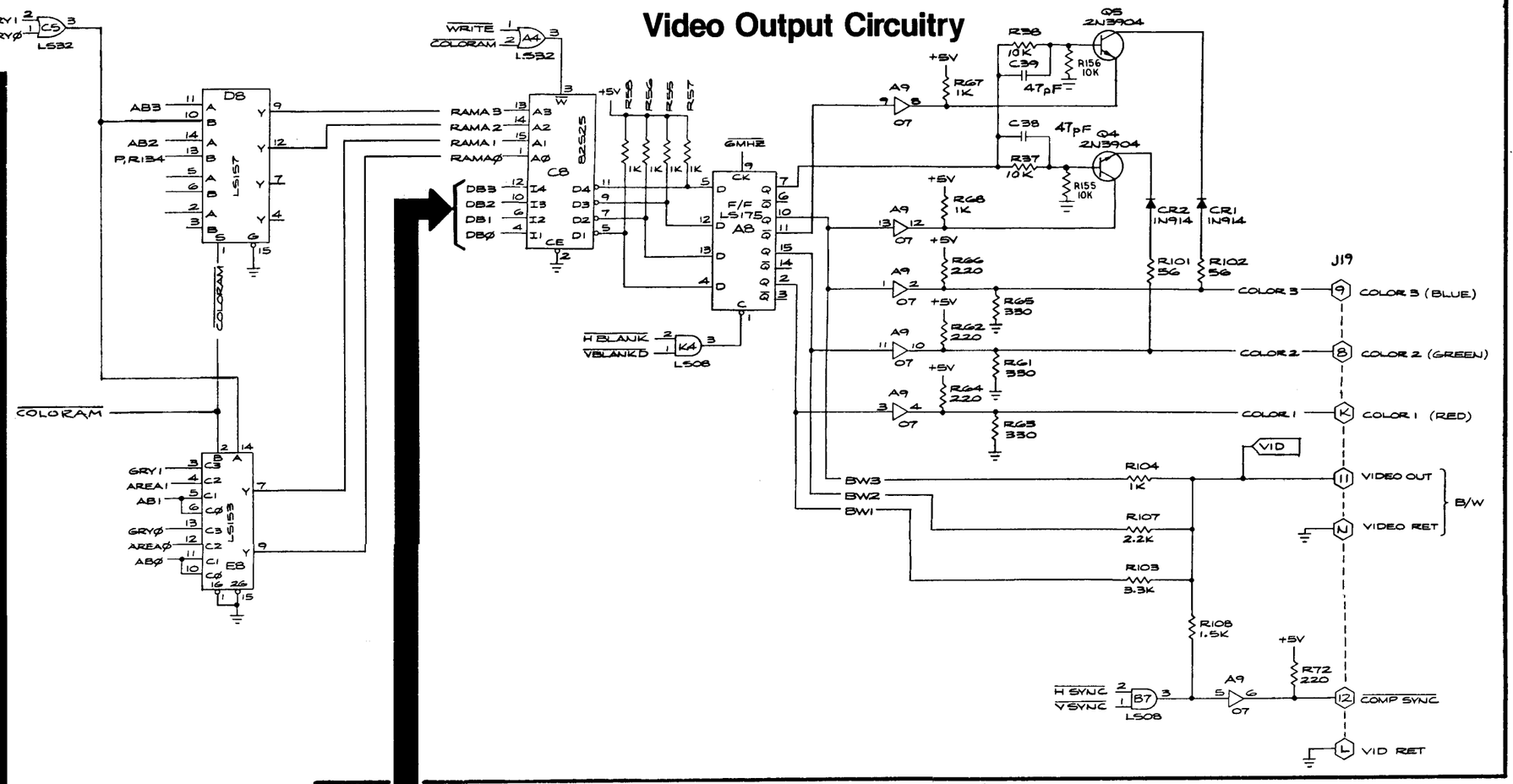
Video Output Circuitry

The video output circuit receives motion object, playfield, address and data inputs and produces a video output to be displayed on the game monitor. In order to read out of the color RAM, GRY0 and GRY1 from the motion object circuitry are multiplexed with AREA0 and AREA1 from the playfield circuit by E8. The output, selected by GRY0 or GRY1, is RAMA0-RAMA3 (RAM ADDRESS).

RAMA0-RAMA3 are applied to color RAM C8. The colors red, green, blue and an alternate color bit are outputs. The three color bits are latched by A8 as the game video in the three basic colors (or shades of gray in a black and white monitor). When the alternate color bit (C8 pin 11) is active, an alternate shade of blue or green is available.

The following conditions, along with the various combinations of COLOR 1 (red), COLOR 2 (green) and COLOR 3 (blue), provide 6 extra colors for a total of 14.

1. If A8 pin 11 is low, transistor Q5 conducts and draws current from COLOR 3. The result is a pale blue when COLOR 1 and COLOR 2 are off.
2. If A8 pin 10 is low, transistor Q4 conducts and draws current from COLOR 2. The result is a pale green when COLOR 1 and COLOR 3 are off.



High Score Memory Circuitry

The High Score Memory circuit stores the three best scores and other pertinent information. These scores are saved even if power is removed from the game. The High Score Memory circuit consists of an erasable reprogrammable ROM E5, latches E4, H4, J4, buffer H5 and timer A11.

A11 produces a 0-15V square wave at a 1V rate. This signal, when +15V, forward biases diode CR5 and allows capacitor C86 to charge to −29V. When the signal is 0V, CR5 is cutoff and CR4 is forward-biased which causes C84 to develop a charge. C84 charges to approximately −28V. This is the potential required for EAROM C0 to operate.

The MPU addresses the EAROM (AB0-AB5) when a low $\overline{EAADDR}$ gates $\overline{WRITE2}$ at gate A4. The trailing edge of the gated pulse latches the address information to the EAROM E5 via J4. Data is latched by H4 at the same time. The EAROM mode (read, write or erase) is determined by DB0-DB3 at latch E4. A low $\overline{EACONTROL}$ gates $\overline{WRITE2}$ at gate A4. The trailing edge of this gated pulse latches the data into the EAROM E5 via latch H4.

Data is read from the EAROM when $\overline{EAREAD}$ on pin 1 of buffer H4 goes low.