

Section of 036471-01 and -02

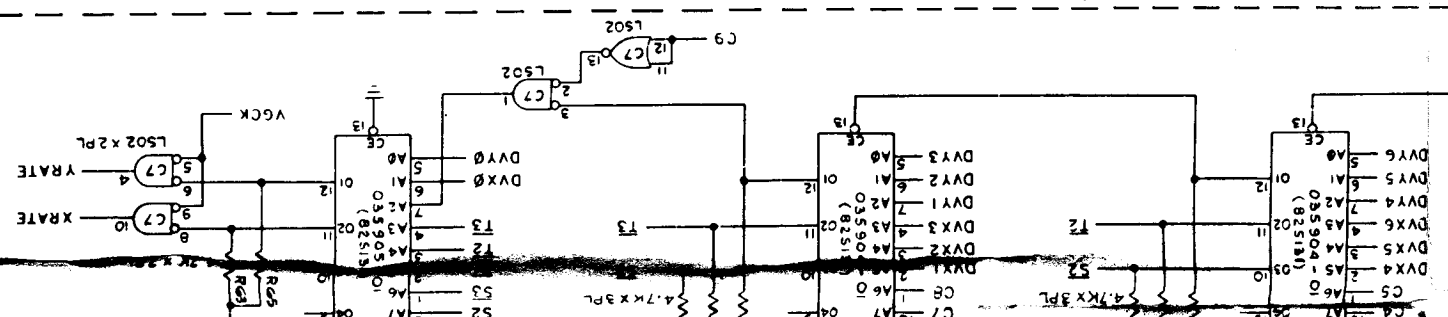
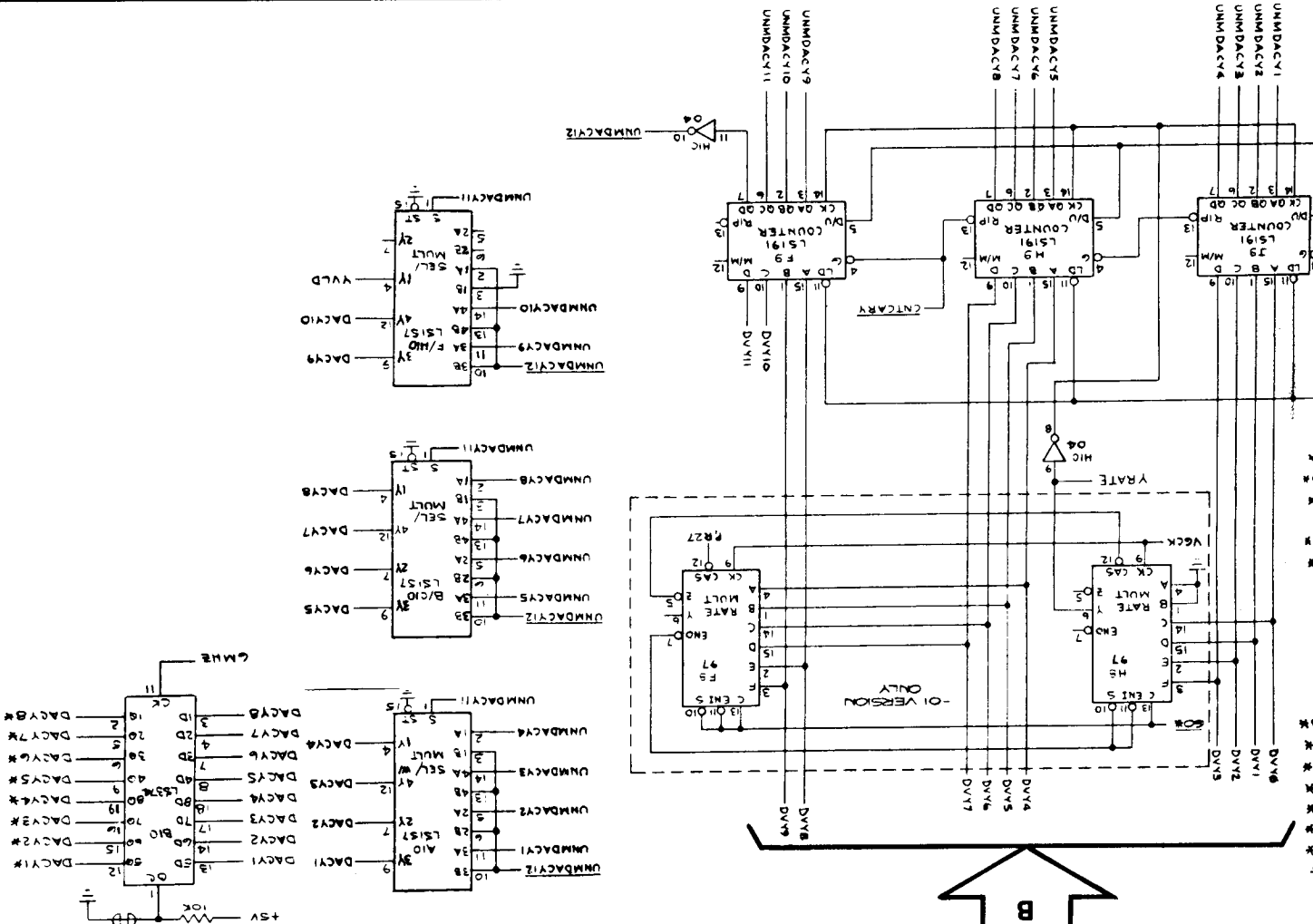
Video Generator ASTEROIDS DELUXE™

Sheet 2, Side A

A Warner Communications Company



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enter signals) are transferred and stored at the output of
 the DACs) in the X video output.
 DACX1 thru DACX10 signals are
 digital-to-analog converters (DACs) in the X video output.
 DACX1 and DACX10 outputs represent the physical placement
 on the monitor. The far left of the monitor screen is 0, the
 2, and the far right is 1023. Therefore, if the DACX1 thru
 1023, the monitor beam would go off
 the screen and start again on the left side of the
 "wraparound" condition. To prevent a wraparound, the
 select input from UNMDACX11 goes high when the
 from the multiplexers to the DACs, forcing all zeros or all
 1023 or less than 0. This selects UNMDACX12 to
 read of allowing it to wraparound.
 and Y valid) outputs from the X- and
 counter multiplexers are latched (F10) and gated together to
 axis output, BVLDD (beam valid)).

X- AND Y-POSITION COUNTERS

-position counters are two identical circuits. Therefore, description discusses only the X-position counters. Position counters contain rate multipliers (J8 and K8), latch gates (B8 and H10), the output of the down/up 12-bit binary number that represents the horizontal location on the monitor screen (or X axis), with 0 being the far left and 1023 being the far right side of the screen. Decreasing this binary number output will cause the vector to the right or left, respectively. The vector generator decodes instructions from its memory, and then is capable that data to alter the binary count of these counters in its.

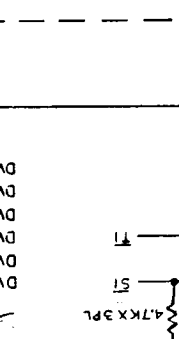
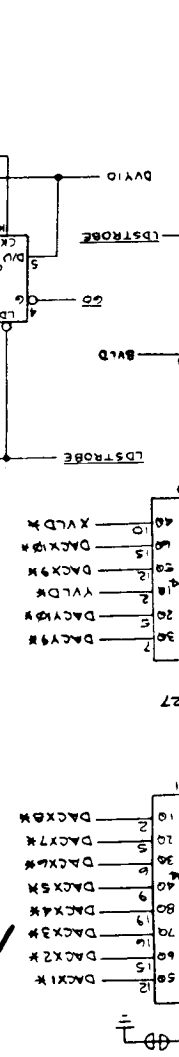
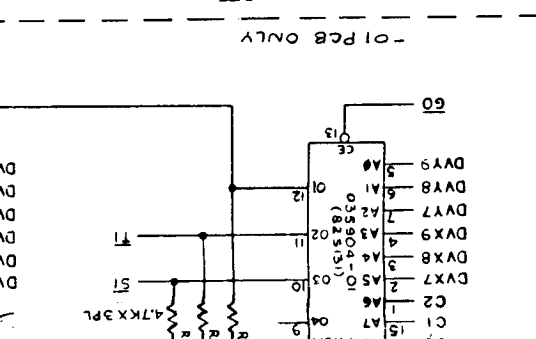
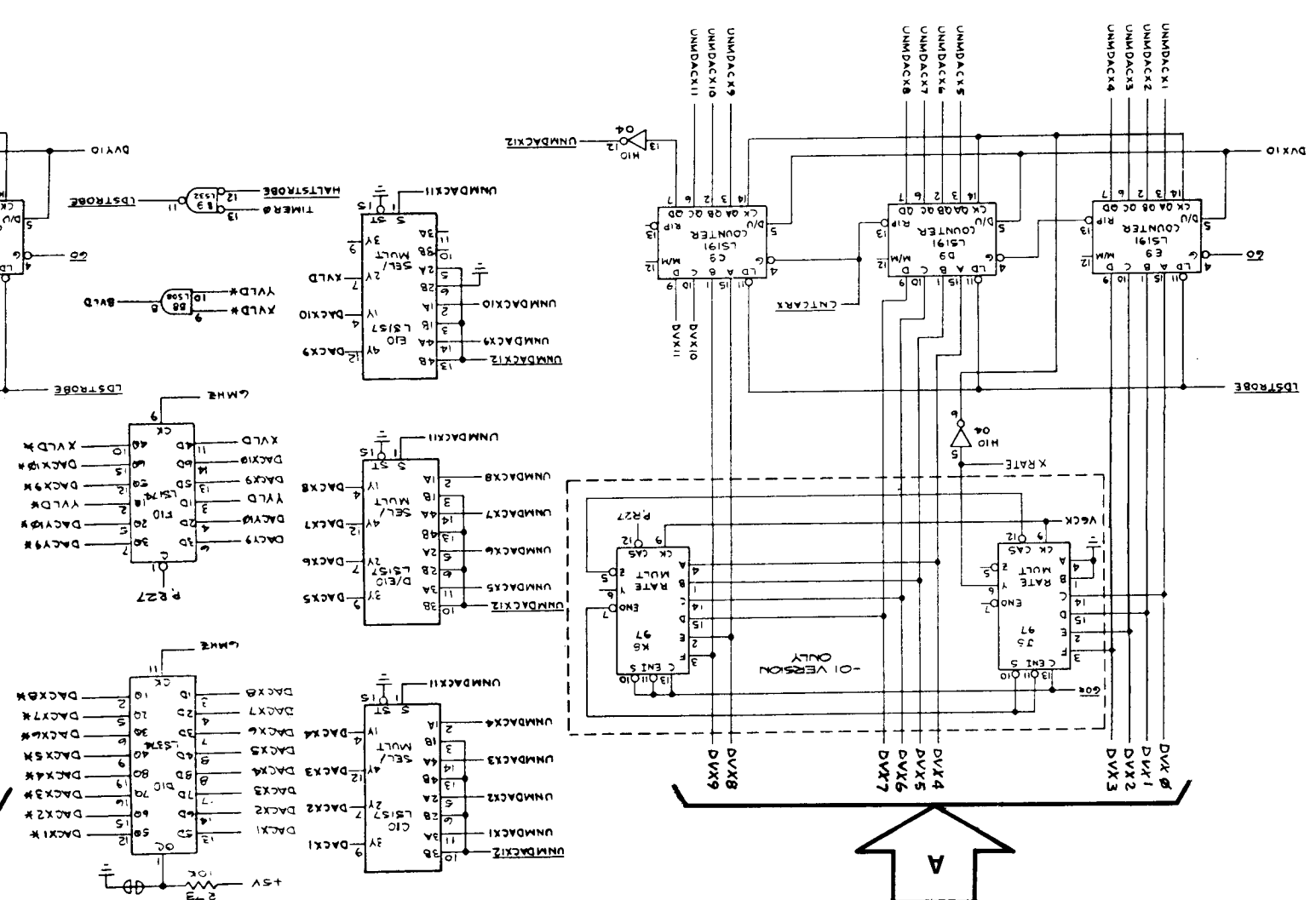
Each can preset these counters to an entirely different location on the monitor screen. This will cause the beam to their previous contents. While the beam is "jumping" to this new vector ended. While the beam is "jumping" to this new location on the monitor screen instantaneously, i.e., new vector from a different starting position than where the beam itself is turned off to prevent unwanted lines from the screen. To preset this new position into the counters, the vector causes **L8DSTROBE** to go low. At this time, a new

The state machine can also instruct these counters to count up or down any specific number of counts. This will cause the beam to move to the left or to the right a specific distance relative to where it was. During this beam movement, the beam is turned on with the desired intensity. This is the procedure used to draw a vector on the monitor screen. The direction (to the left or right) and length (0 to 1023) of the vector to be drawn relative to the beam's current position is determined by DVX0-11 (from the vector generator memory data latches). This data contains information that determines how many clock pulses the counters will receive and whether the counters will count up or down.

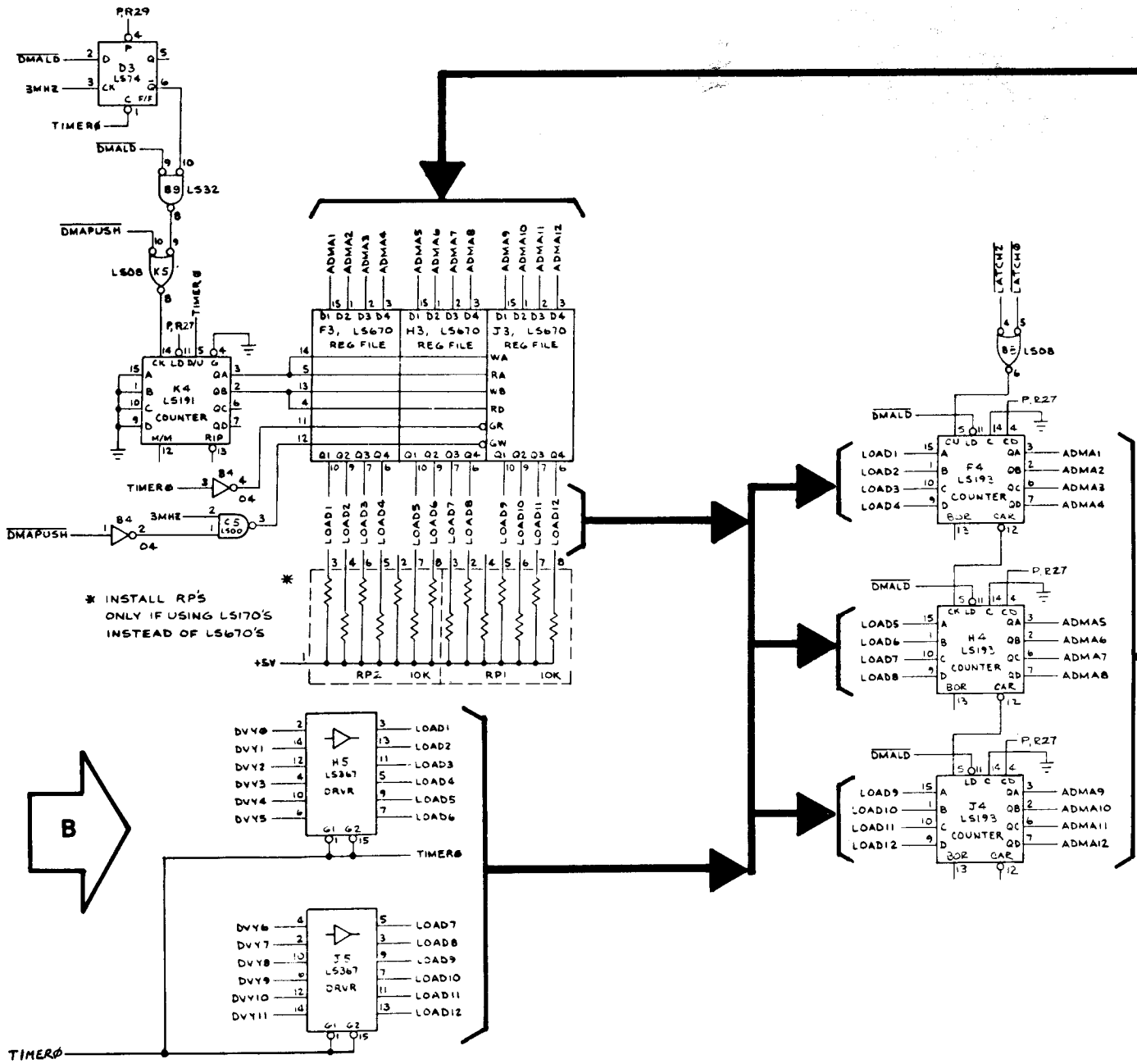
DVX0-9 memory data is loaded into rate multipliers J8 and K8. The function of these devices is to space the desired number of counter clock pulses at equal intervals over the time period that it will take to draw the desired vector. This insures that vectors of different lengths will still be displayed with the same relative beam intensity. DVX10 and 11 are loaded directly into the counters. DVX11 determines the quadrant of the vector being drawn.

The UNMDAC generator memory data latches.

12-bit number (DVX0-11) is loaded into the counters from the vector



PROGRAM COUNTER

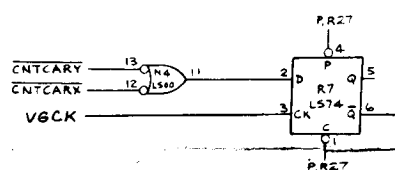
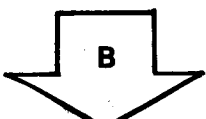


Counters F4, H4 and J4 contain the address of the next data byte (instruction) to be fetched from the Vector Generator memory. Because these counters point to the next instruction in memory to be retrieved and performed, they are called the program counter. This program counter is incremented one count (to the next sequential address) each time the information at its current address is loaded into data latch 0 or data latch 2.

The program counter may also be preset to "jump" to a new address. This new address can be loaded into the program counter from the vector generator memory via data latches F6 and H6 and buffers H5 and J5.

The program counter may also be preset to "return" to a previous address which it had stored in its "stack". The stack consists of register files F3, H3, & J3, and down/up counter K4. The stack is a 4-word 12-bit memory, used to save the contents of the program counter for future reference. It is loaded when DMAPUSH is low. Immediately after information is written into the stack, counter K4 increments one count. Immediately before loading the program counter from the stack, counter K5 decrements one count.

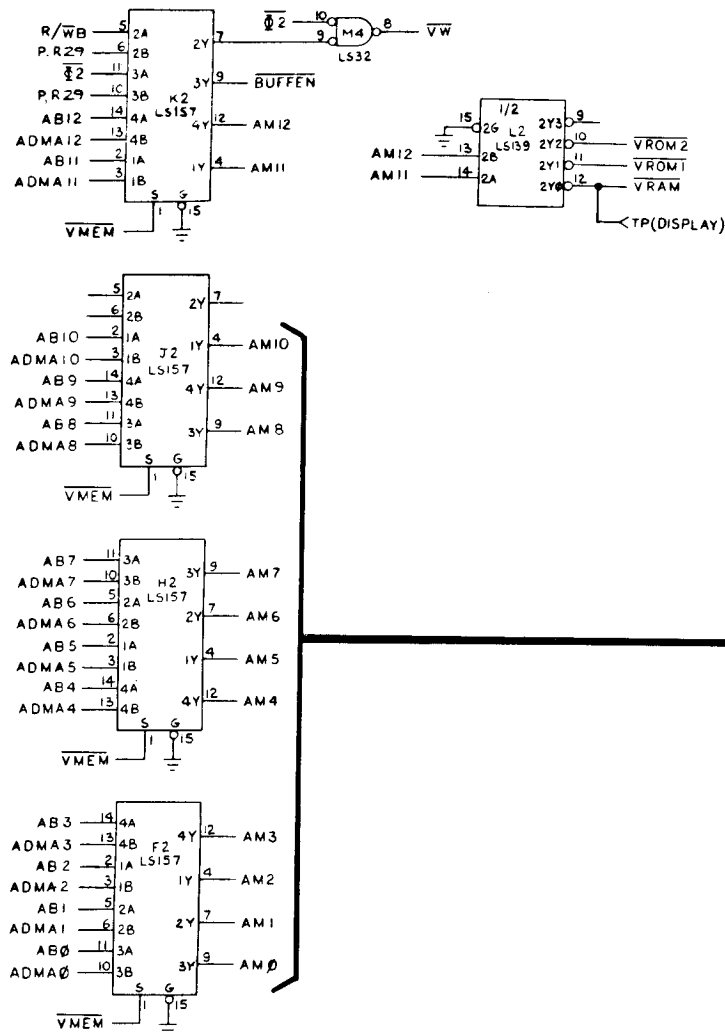
STATE MACHINE



FROM
MICROCOMPUTER
SHEET 1, SIDE B

VECTOR GENERATOR MEMORY ADDRESS SELECTOR

VECTOR

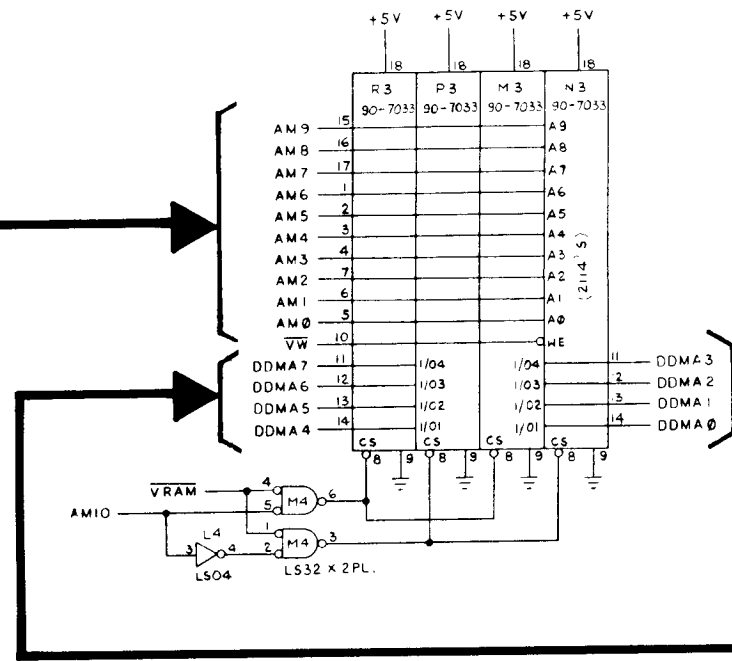


The address selector consists of multiplexers F2, H2, J2 and K2. When \overline{VMEM} is low, the MPU of the microcomputer gains access to the address inputs of the vector generator memory. In this state, \overline{BUFFEN} is from $\overline{\phi 2}$ and \overline{VW} (vector generator write) is low when $\overline{\phi 2}$ and $\overline{R/WB}$ are both low. When \overline{VMEM} is high, the address input to the vector generator memory is from the vector generator program counter and state machine. In this state, \overline{BUFFEN} and \overline{VW} are both held high by the pullup resistors connected to the 2B and 3B inputs of multiplexer K2.

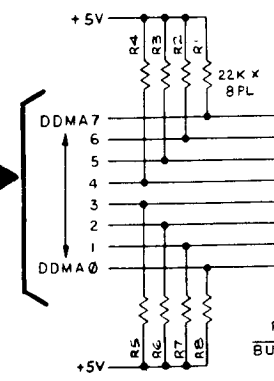
Address decoder L2 decodes address bits A11 and A12, and selects the RAM or one of three ROMs of the vector-generator memory.

This address-selecting arrangement allows the game MPU to access the vector-generator memory, i.e., write data into the vector-generator RAM to instruct the vector generator what it should do next. The address selector can then allow the vector-generator program counter and state machine to access this same area of RAM also, and read what instructions were sent to it by the game MPU.

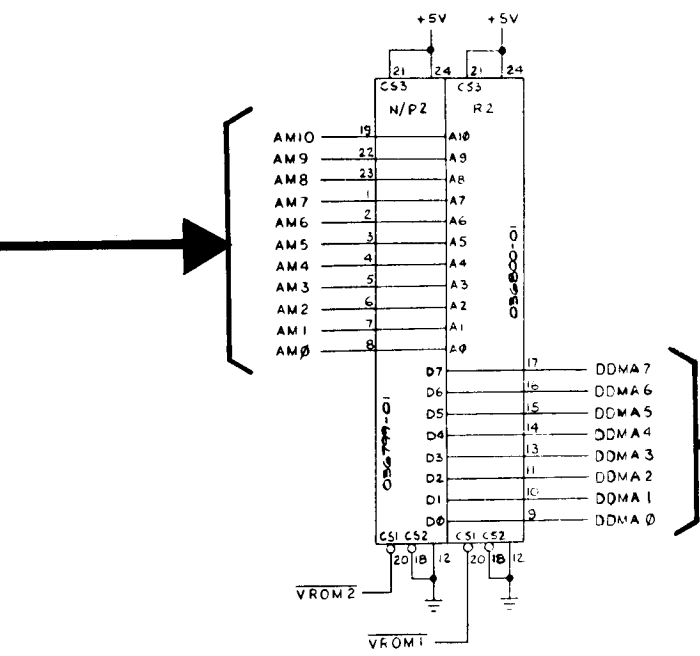
GENERATOR RAM



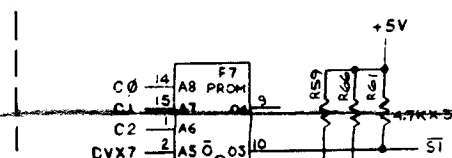
VECTOR GENERATOR DATA BUFFER



VECTOR GENERATOR ROM

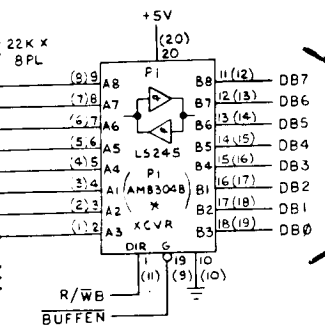


The latch are the
 Latch of the vector
 LATCH clear
 Latch

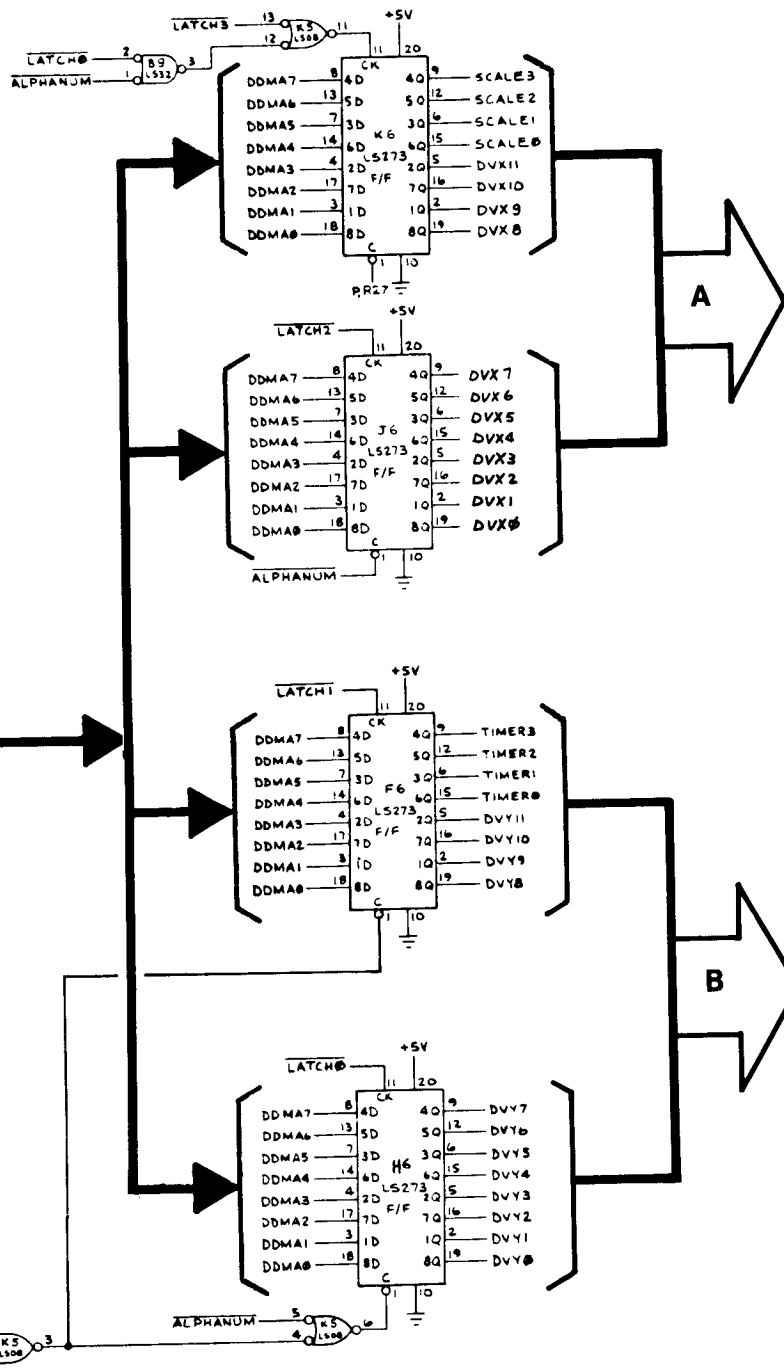


OR

TO/FROM
MPU DATA BUS
SHEET 1, SIDE B



VECTOR GENERATOR MEMORY DATA LATCHES



The data latches consist of latch 0 (H6), latch 1 (F6), latch 2 (J6), and latch 3 (K6). Inputs DDMA0 thru DDMA7 are the data outputs from the vector-generator memory.

Latches 0 thru 2 are directly clocked by the rising edge of the LATCH0, LATCH1, and LATCH2 outputs from the vector generator's state machine. Latch 3 is clocked by LATCH3 or by LATCH0, if ALPHANUM is low. Latch 0 is cleared when RESET, DMAGO, or ALPHANUM goes low. Latch 1 is cleared by ALPHANUM.

