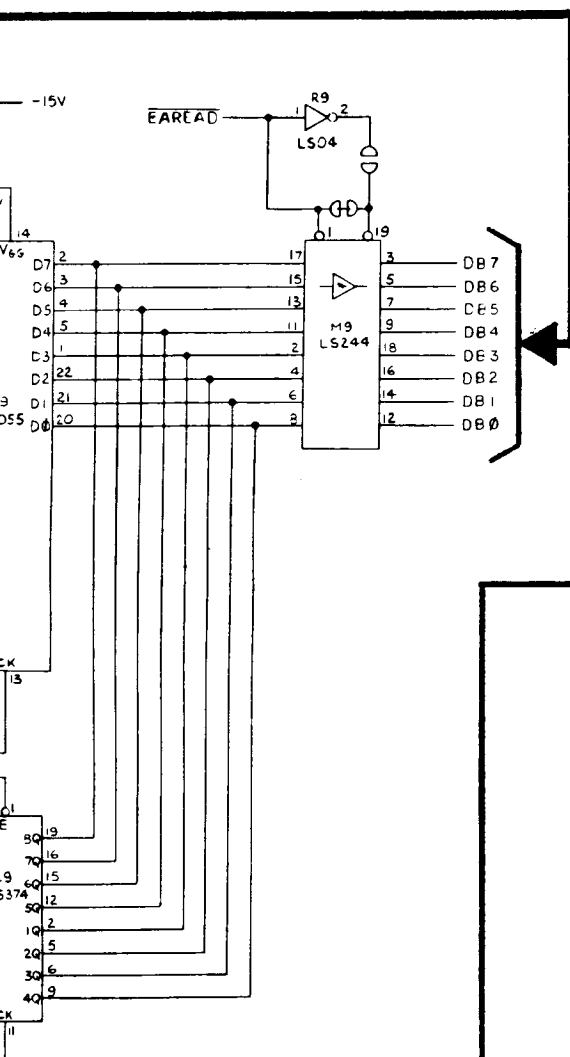


1	1	0	0	R	Program ROM
1	1	0	1	R	Program ROM
1	1	1	0	R	Program ROM
1	1	1	1	R	Program ROM



The High Score Memory circuit consists of an erasable reprogrammable ROM N9, latches L9, P9, N10 buffer M9, and timer N11.

N11 produces a 12KHz 0-15V squarewave. This signal when + 15, forward biases diode CR4 and allows capacitor C50 to charge th -29V. When it's 0V, CR4 is then cut-off and CR3 is forward biased which causes C49 to develop a charge. C49 charges to approximately -28V. This is the potential required for EAROM N9 to operate.

The MPU addresses the EAROM (AB0-AB5) via latch N10, when EAADDR1 goes high, and data is latched into the EAROM on DB0-DB7 through latch L9.

The function of the EAROM (read, write or erase) is determined by the MPU on data lines DB0-DB3. Latch D9 receives a high EACONTROL signal from the MPU address decoder and function data is passed to the EAROM.

Data in the EAROM is read by the MPU when the EAREAD is addressed by the MPU after a reset pulse or during self-test.

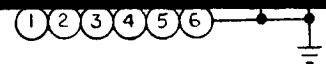
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Sheet 1, Side B
ASTEROIDS DELUXE™
Microprocessor
Section of 036471-02 C

Power is disabled by RESET. During Self-Test, the NMI is disabled by TEST.

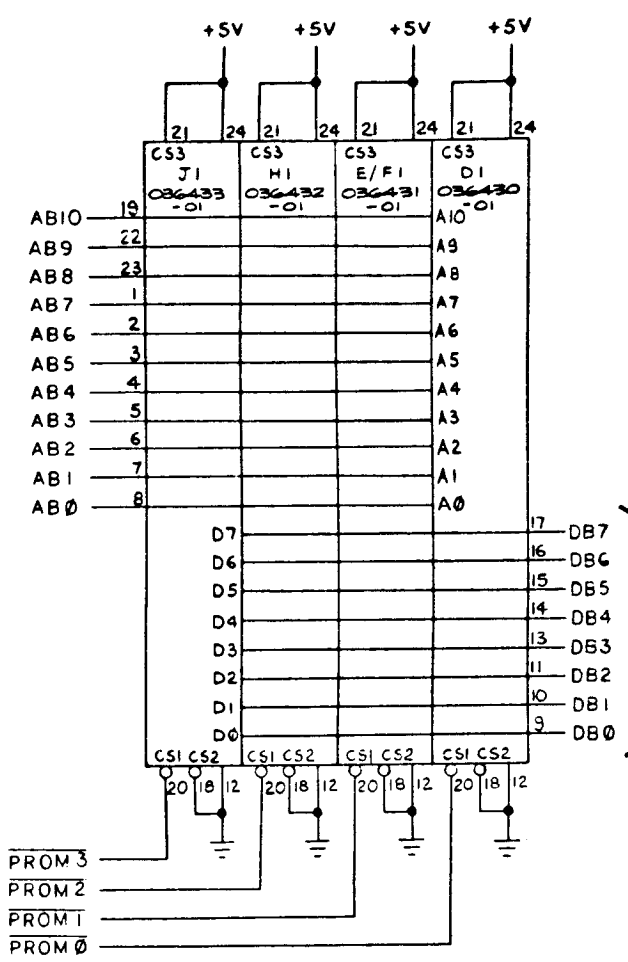
NOTE:
Either a 74LS245 or an AM8304B may be used at location E2. Pin numbers not enclosed in parentheses are for 74LS245. Pin numbers in parentheses are for an AM8304B.



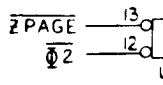
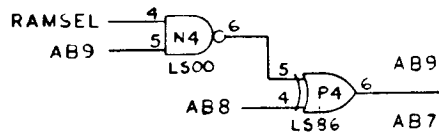
ROM/PROM CIRCUITRY

FROM SWITCH INPUTS
SHEET 2, SIDE B

Program memory for the Asteroids Deluxe™ game is contained in three ROMs.



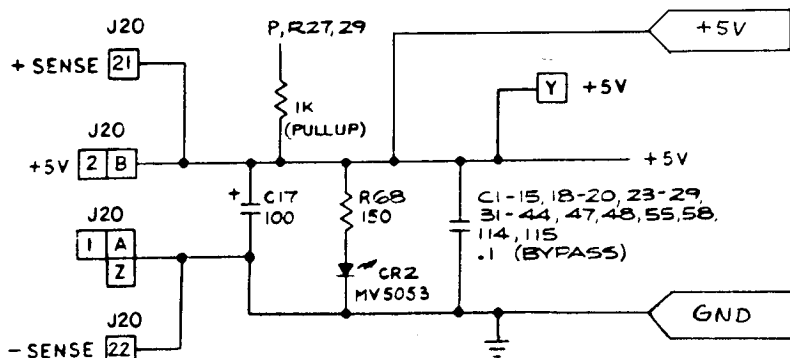
RAM CIRCUITRY



The RAM is the temporary memory for the MPU and is enabled when the Page enable (pin 13) is low. When the Page enable (pin 13) is high, the MPU is low, the RAM stores the MPU output (DB0 thru DB7) at the address selected by the MPU address bus (AB0 thru AB9). When R/WB is high, the MPU reads the byte at the addressed location.

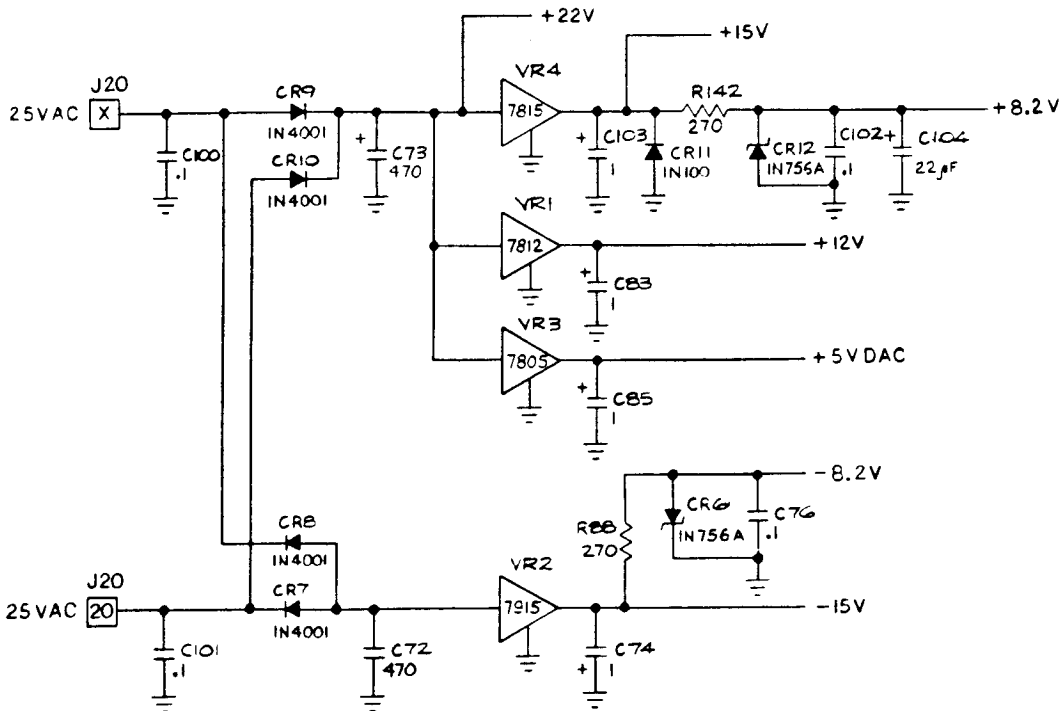
The signal RAMSEL, which is the effect of swapping pages, enables the RAM. This allows greater flexibility.

POWER INPUT



This circuitry consists of the PCB inputs and outputs for the + 5 VDC logic power and 25 VAC input to the on board regulators. The + 5 VDC inputs and outputs are discussed on Sheet 1, Side A of this schematic set.

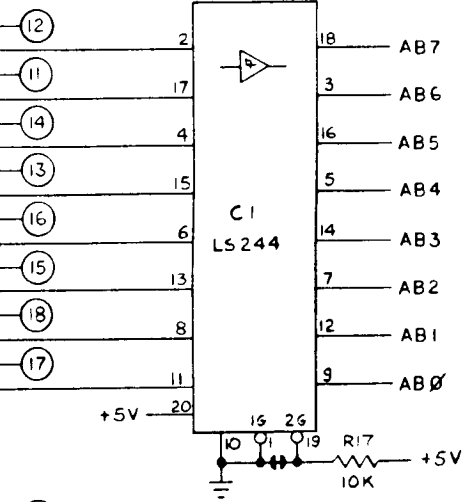
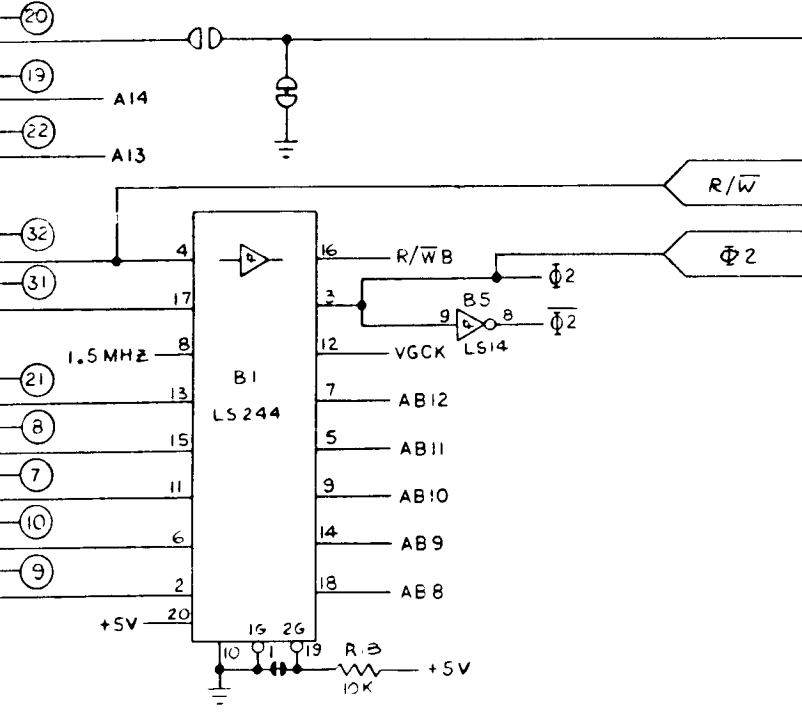
The 25 VAC inputs are received by two full wave rectifiers. Diodes CR9 and CR8 rectify the negative cycle of the input and the 7915 regulates the voltage at -15 VDC. Diodes CR9 and CR10 rectify the positive pulse of the 25 VAC input and the 7815 regulates the voltage at +15 VDC. The 7812 regulates the voltage at +12 VDC. The 7805 regulates an additional 5 VDC for the DACs. Zener diode CR12 supplies the +8.2 VDC for the sample and hold circuit. The +22V (unregulated) is used to power operational amplifiers P11 and L8 in the audio output.



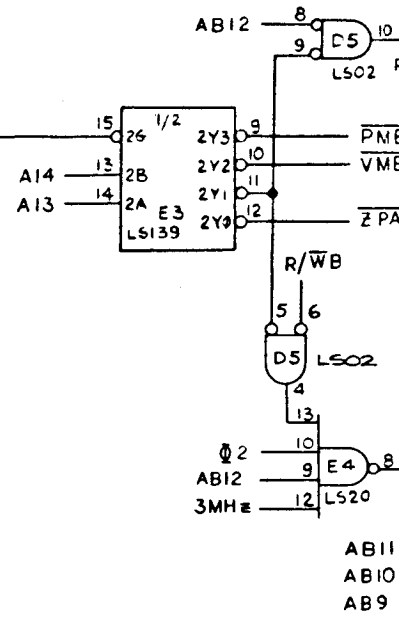
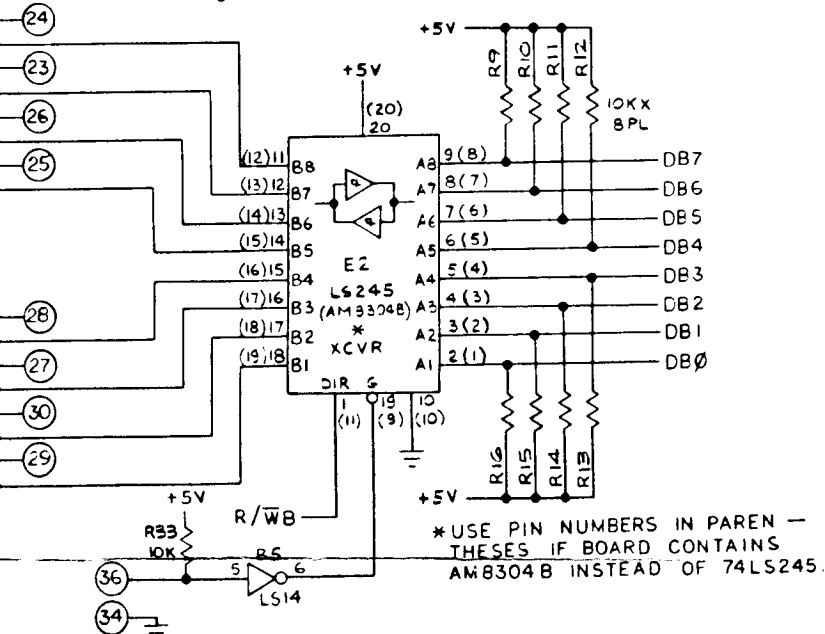
Denotes a test point

ADDRESS DECODING

NOTE:
DO NOT USE split pads on PCB for trouble-shooting purposes.



NOTE:
DO NOT USE split pads on PCB for trouble-shooting purposes. If a 74LS244 is installed at location B1 and/or C1, the split pad for that location should be filled with solder. If a 74LS241 is used, the appropriate split pad should be open.



INPUTS

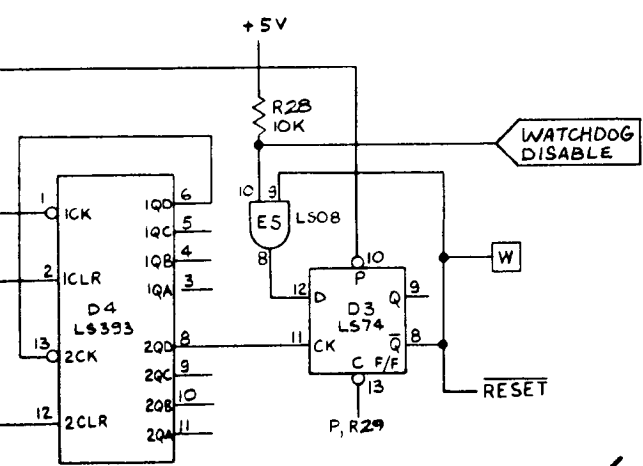
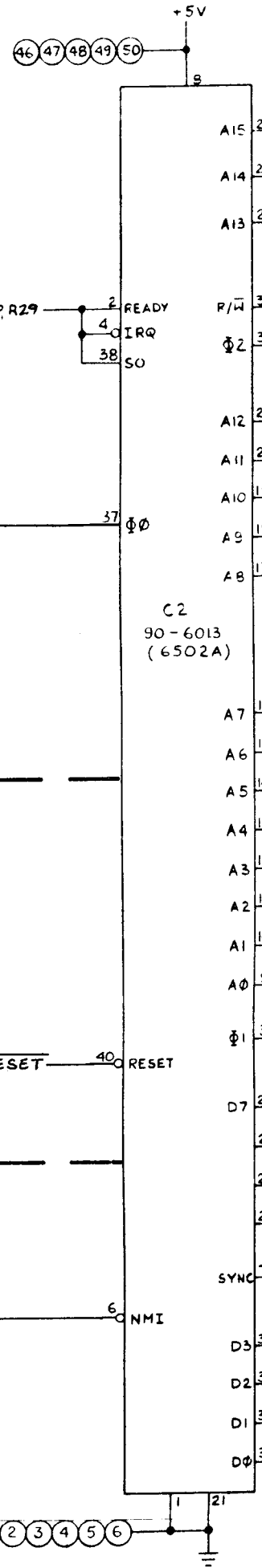
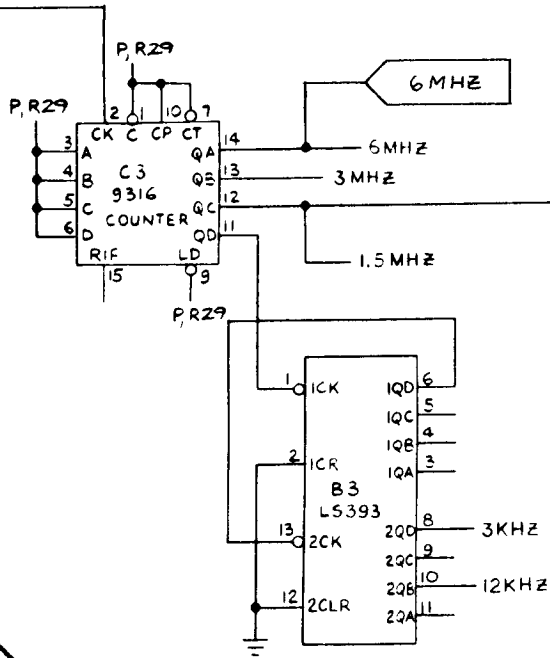
OUTPUTS

RAM, ROM

HEXADECIMAL	A15	A14
0-3FF		0
2000		0
2001		0
2002		0
2003		0
2004		0
2006		0
2007		0
2400		0
2401		0
2402		0
2403		0
2404		0
2405		0
2406		0
2407		0
2800		0
2801		0
2802		0
2803		0
2000		0
2C40		0
3000		0
3200		0
3400		0
3600		0
3600		0
3800		0
3A00		0
3C00		0
3C01		0
3C02		0
3C03		0
3C04		0
3C05		0
3C06		0
3C07		0
3E00		0
4000		1
4400		1
4800		1
5000		1
6000		1
6800		1
7000		1

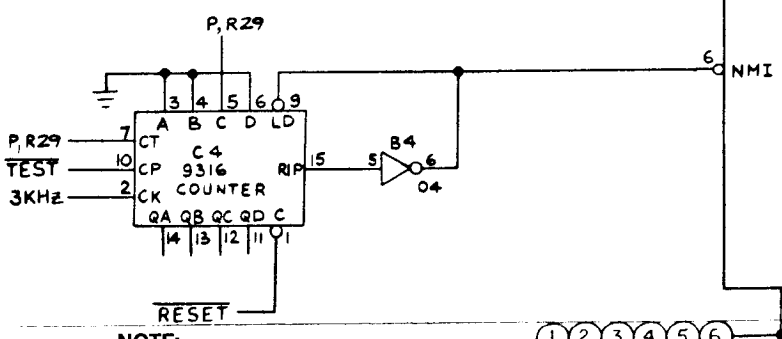
MPU CIRCUITRY

of crystal Y1 and associated in-
B3. Counters C3 and B3 count the
the frequencies necessary for the



COUNTER

(non-maskable interrupt) counter causes an interrupt
out of the MPU every 4 msec. The interrupt is derived
KHz by a factor of 12 through counter C4. The inter-
when pin 6 of inverter B4 goes low. During power-up,
ter is disabled by RESET. During Self-Test, the NMI
TEST.



NOTE:
Either a 74LS245 or an AM8304B may be used at
pin 21. Pin numbers not enclosed in paren-

