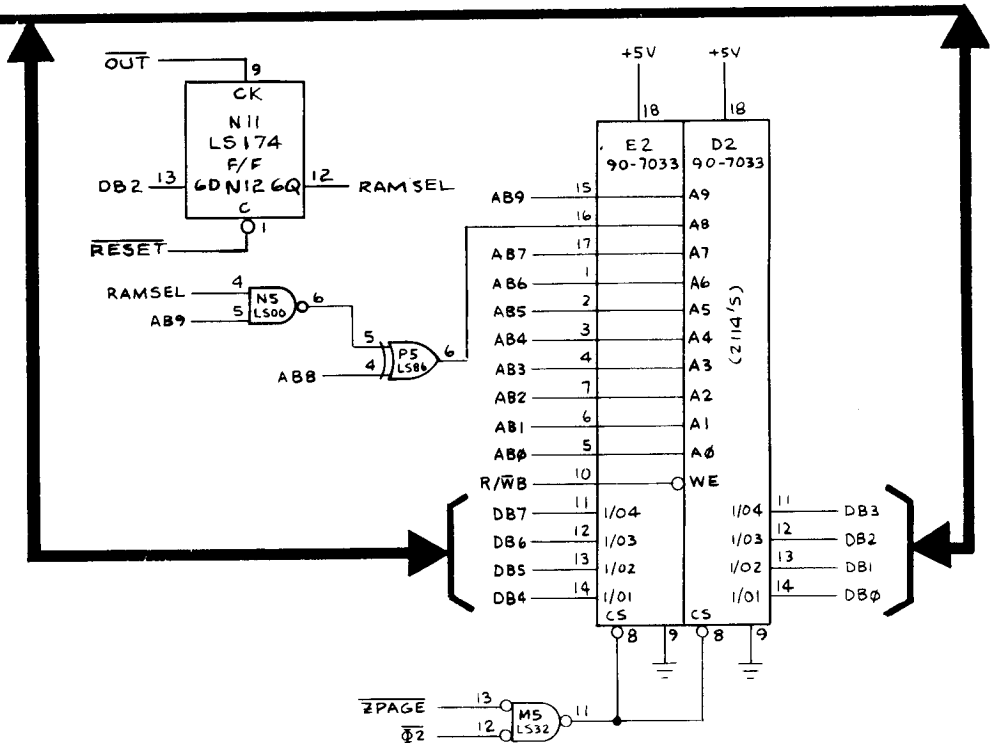
	0 0 0	1 1 1	1 1 1	1 1 1	1 1 1	0 0 1						1	0	1	W W	D									LIFE SOUND NOISE RESET
	1 1 1	0 0 1	0 1 0	0 A 1	A A A	A A A	A A A	A A A	A A A	A A A	A A A	A A A	A A A	A A A	A A A	A A A	R R	D D D	D D D	D D D	D D D	D D D	D D D	D D D	D D D	D D D	VECTOR RAM VECTOR ROM PROGRAM

RCUITRY

e RAM is the temporary storage space for MPU and is enabled when $\overline{\text{ZPAGE}}$ (Zero enable) is low. When R/$\overline{\text{W}}$B (from the is low, the RAM stores the data byte in- DB0 thru DB7) at the location addressed e MPU address bus (AB0 thru AB7). When is high, the MPU reads the stored data at the addressed location.

e signal RAMSEL, when low, has the ef- of swapping pages 2 and 3 within the This allows greater programming flex-



-04 P.C. Boards (ROMs)		-05 and -06 P.C. Boards (ROMs)	
035143-02	C1	035143-02	E/F2
035144-02	D/E1	035144-02	H2
035145-02	F1	035145-02	J2

ATARI®

A Warner Communications Company

Sheet 1, Side B

ASTEROIDS
Microprocessor

Section of 034986-01 thru -04 H
034986-05 and -06 B

NOTE:
EITHER A 74LS245 OR AN AM8304B MAY BE USED AT LOCATION E3. PIN NUMBERS NOT ENCLOSED IN PARENTHESIS ARE FOR 74LS245. PIN NUMBERS IN PARENTHESIS ARE FOR AN AM8304B.

3E00

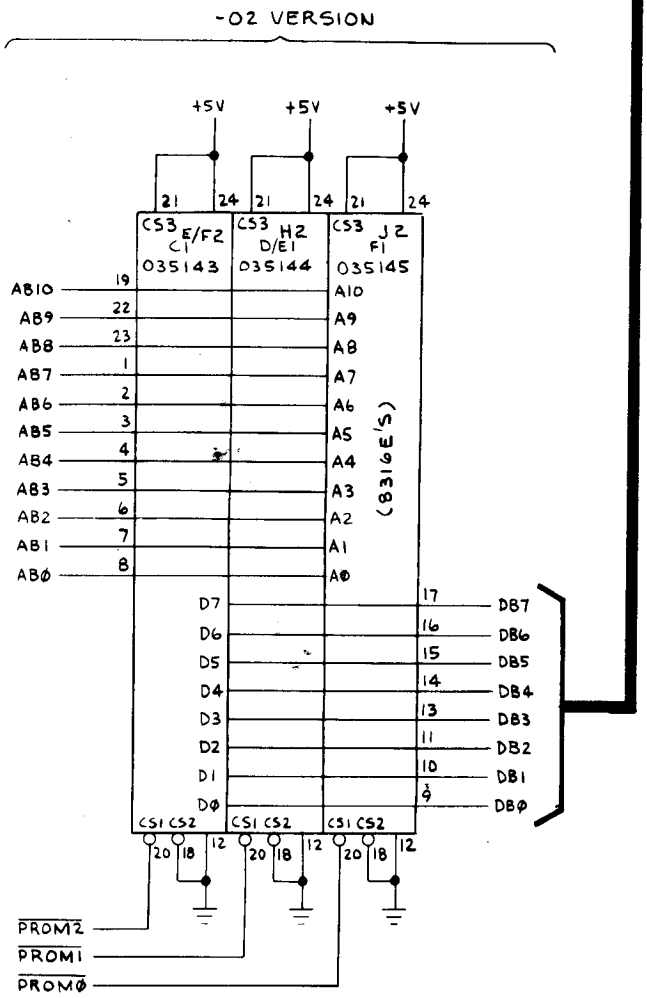
4000-47FF
5000-57FF
6800-7FFF

Asteroids game is con-
version of the PCB or
the PCB. One ROM is
ll PROMs connected to
removed before replac-
ble, remove PROMs at
before replacing with

RAM CIR

The RA
the MPU
Page en
MPU) is
put (DB0
by the M
R/WB is
byte at t

The si
fect of
RAM. Th
ibility.



NOTE:

All reference designations in red are for the -05 and -06 PCB assemblies only. For example, the 8316E ROM above is at location F1 on the -01 thru -04 PCB, but is at location J2 on a -05 and -06 PCB.

The reference designations, used in the circuit descriptions, refer to the -01 thru -04 PCB assemblies only.

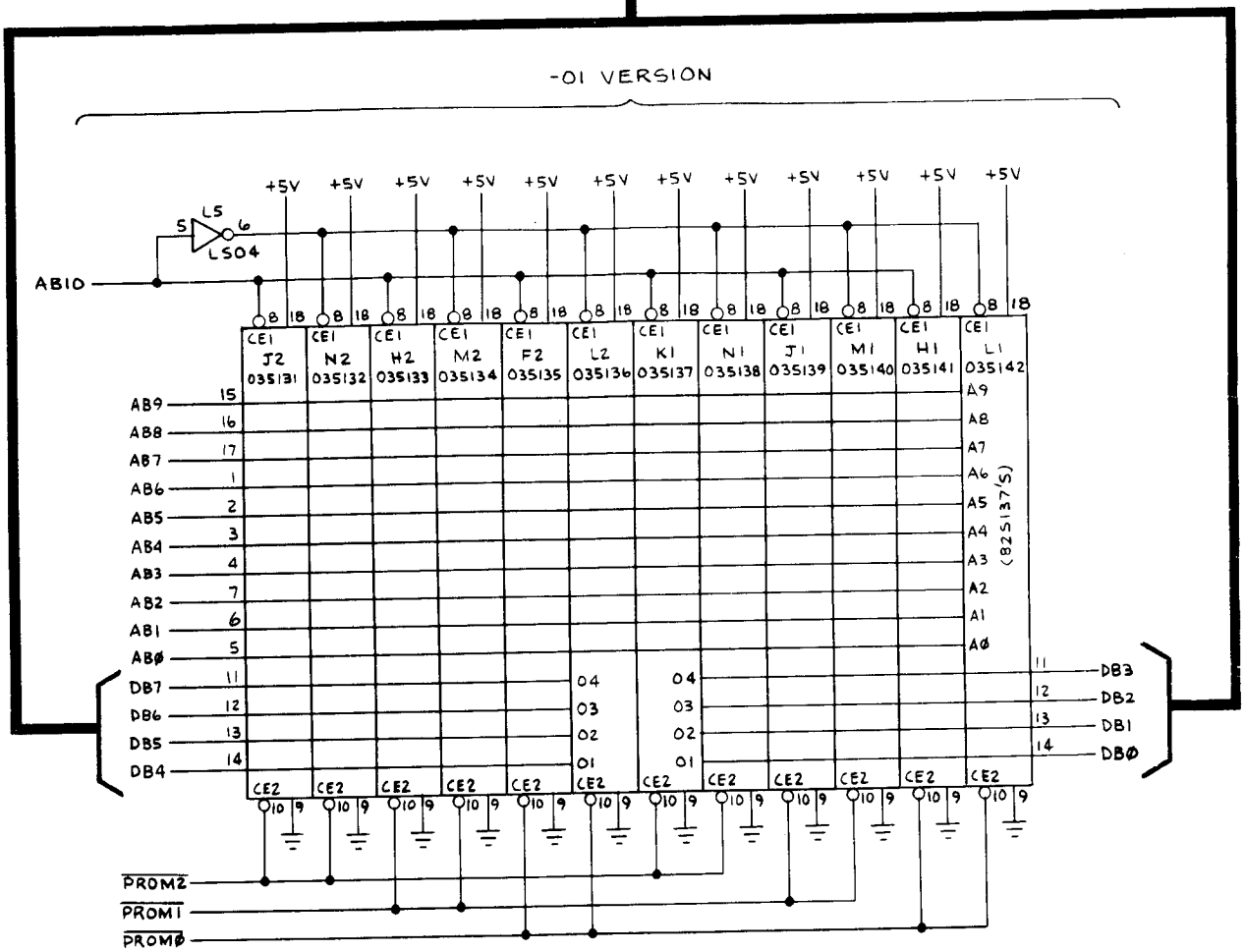
-03 P.C. Boards (PROMs)		Alternate -03 P.C. Boards (PROMs)	
035131-02	J2	035150-02	J2
035132-02	N2		
035137-02	K1	035153-02	K1
035138-02	N1		
035133-02	H2	035151-02	H2
035134-02	M2		
035139-02	J1	035154-02	J1
035140-02	M1		
035135-02	F2	035152-02	F2
035136-02	L2		
035141-02	H1	035155-02	L1
035142-02	L1		

The NMI (non-maskable interrupt) counter causes an interrupt at the NMI input of the MPU every 4 msec. The interrupt is derived by dividing 3 KHz by a factor of 12 through counter C5. The interrupt occurs when pin 6 of inverter B5 goes low. During power-up, the NMI counter is disabled by RESET. During Self-Test, the NMI is disabled by TEST.

FROM SWITCH INPUTS
SHEET 2, SIDE B

ROM/PROM CIRCUITRY

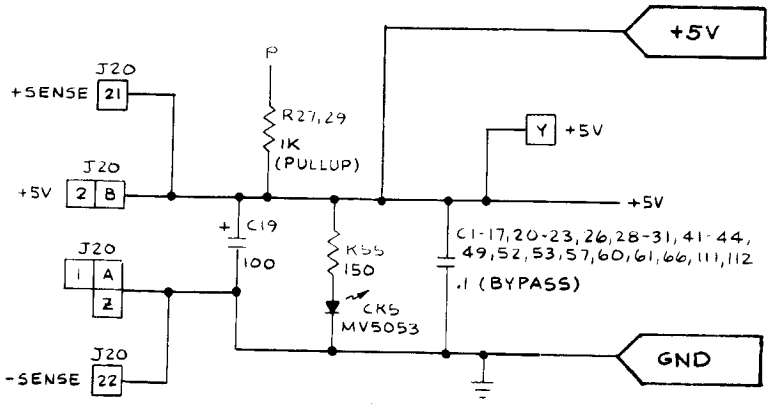
Program Memory for the Asteroid
tained in PROMs for the -01 version
ROMs for the -02 version of the PC
equivalent to four PROMs. All PROM
a common enable must be removed
ing with a ROM. For example, rem
locations F2, H1, L2 and L1 before
ROM at location F1.



denotes change by indica ec

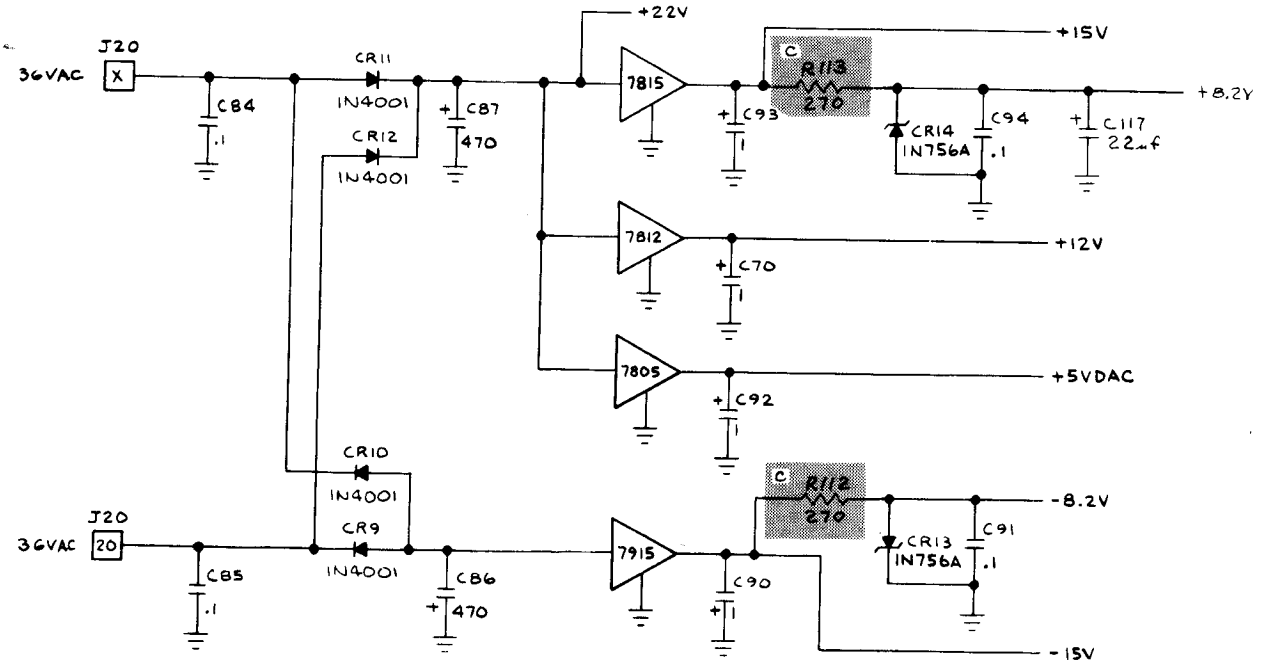
denotes a test point

POWER INPUT

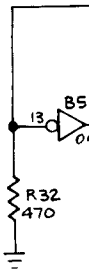


This circuitry consists of the PCB inputs and outputs for the +5 VDC logic power and 36 VAC input to the on board regulators. The +5 VDC inputs and outputs are discussed on Sheet 1, Side A of this schematic set.

The 36 VAC inputs are received by two full wave rectifiers. Diodes CR9 and CR10 rectify the negative cycle of the input and the 7915 regulates the voltage at −15 VDC. Diodes CR11 and CR12 rectify the positive pulse of the 36 VAC input and the 7815 regulates the voltage at +15 VDC. The 7812 regulates at +12 VDC. The 7805 regulates an additional 5 VDC for the DACs. Zener diode CR14 supplies the +8.2 VDC for the sample and hold circuit. The +22V (unregulated) is used to power operational amplifiers P11 and L8 in the audio output.

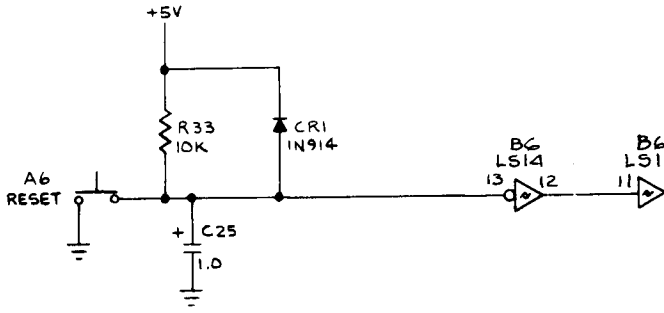


CLOCK CIRCUIT



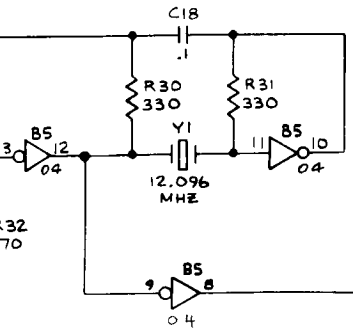
The clock circuit consists o
verters and counters C4 and B4
crystal frequency down to the
Asteroids game.

POWER RESET AN

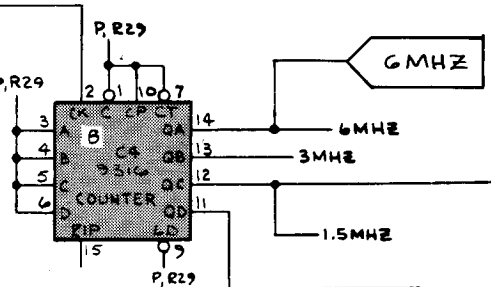


During inital power-up, the delayed charging of capacitor C25 causes a preset of flip-flop D4 and a clear of counter D5. This results in holding $\overline{\text{RESET}}$ input to the MPU low. When the charge of C25 reaches about 1.5 VDC, preset and clear inputs are removed. Counter D5 counts to 128 at 3 KHz rate and $\overline{\text{RESET}}$ is removed (goes high) from the input of the MPU. This allows the logic power input to the PCB to stabilize before allowing the MPU to begin its initialization routine.

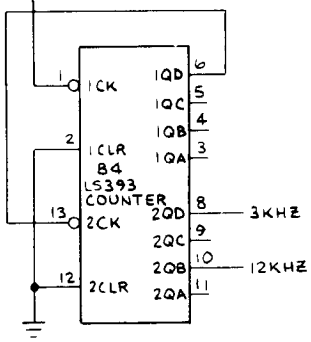
If the MPU program is operating properly, the MPU address decoding circuitry will output the $\overline{\text{WDCLR}}$ (Watchdog clear) signal at predetermined intervals. This serves to clear counter D5 before it counts up to the state that will create the $\overline{\text{RESET}}$ condition. If the MPU program strays from its intended sequence and does not output the $\overline{\text{WDCLR}}$ signal, counter D5 will count up to the $\overline{\text{RESET}}$ state and cause the MPU to return to its initialization routine.



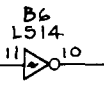
NOTE:
THE MPU IN THIS GAME OPERATES AT A FREQUENCY OF 1.5 MHZ. THEREFORE THE MPU CHIP MUST BE 6502A. THE 6502'S MAXIMUM FREQUENCY IS 1 MHZ AND IS NOT COMPATIBLE WITH THIS GAME.

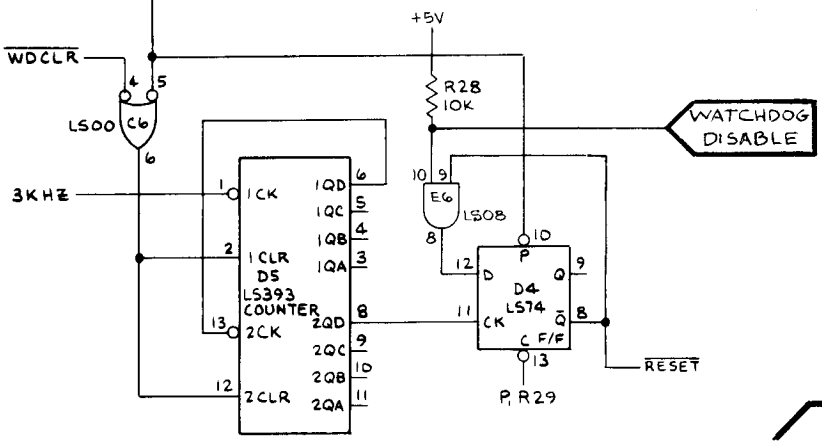


sts of crystal Y1 and associated in-
d B4. Counters C4 and B4 count the
the frequencies necessary for the



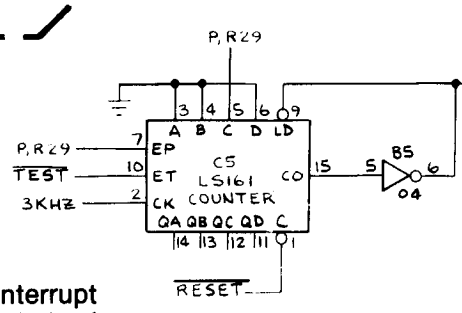
AND WATCHDOG COUNTER





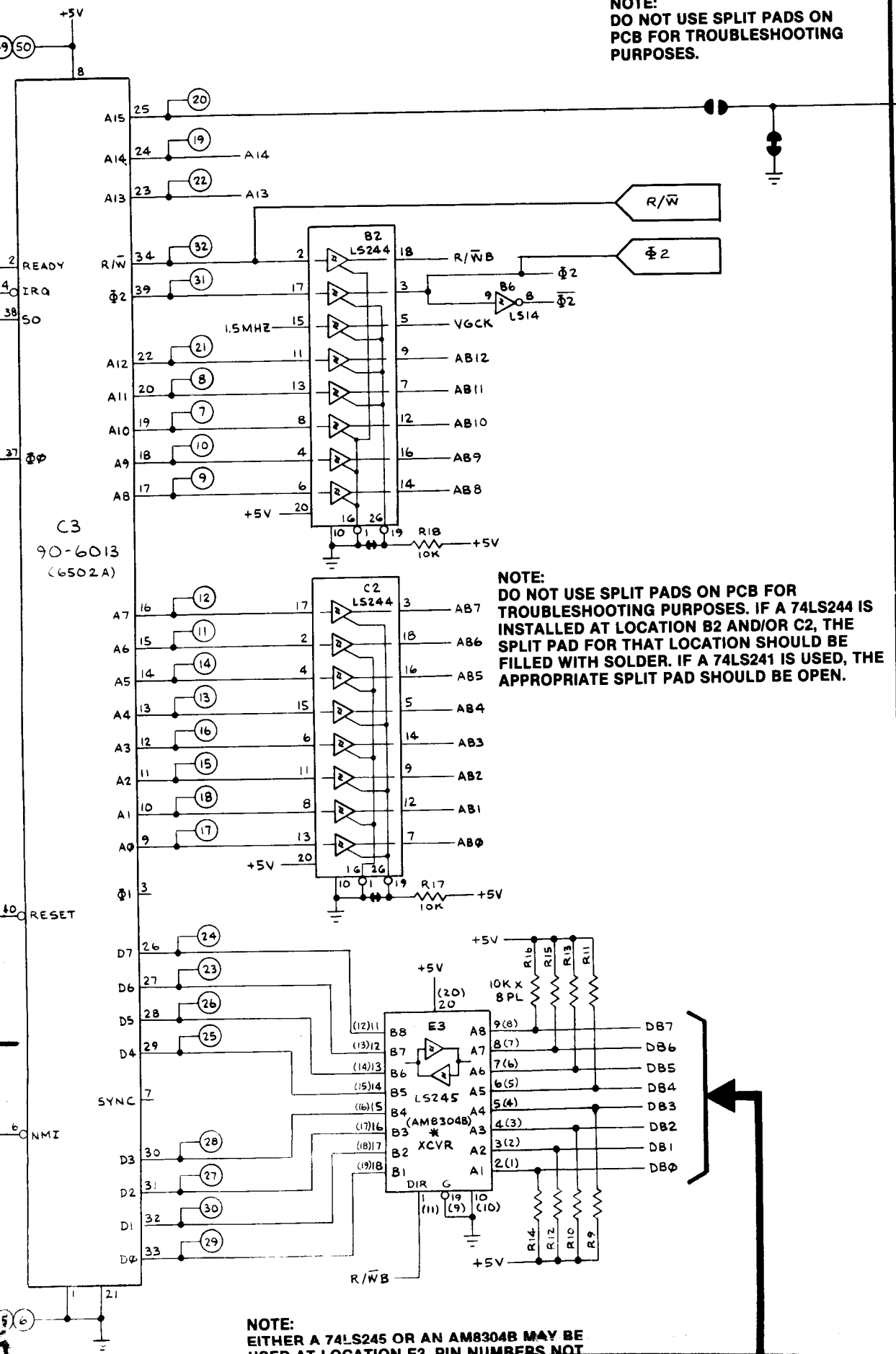
RESET

NMI COUNTER



The NMI (non-maskable interrupt) counter causes an interrupt at the NMI input of the MPU every 4 msec. The interrupt is derived *by dividing* 3 KHz by a factor of 12 through counter C5. The inter-
rupt occurs when pin 6 of inverter B5 goes low. During power-up,

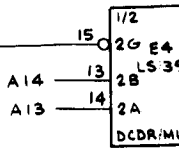
MPU CIRCUITRY



NOTE:
DO NOT USE SPLIT PADS ON PCB FOR TROUBLESHOOTING PURPOSES. IF A 74LS244 IS INSTALLED AT LOCATION B2 AND/OR C2, THE SPLIT PAD FOR THAT LOCATION SHOULD BE FILLED WITH SOLDER. IF A 74LS241 IS USED, THE APPROPRIATE SPLIT PAD SHOULD BE OPEN.

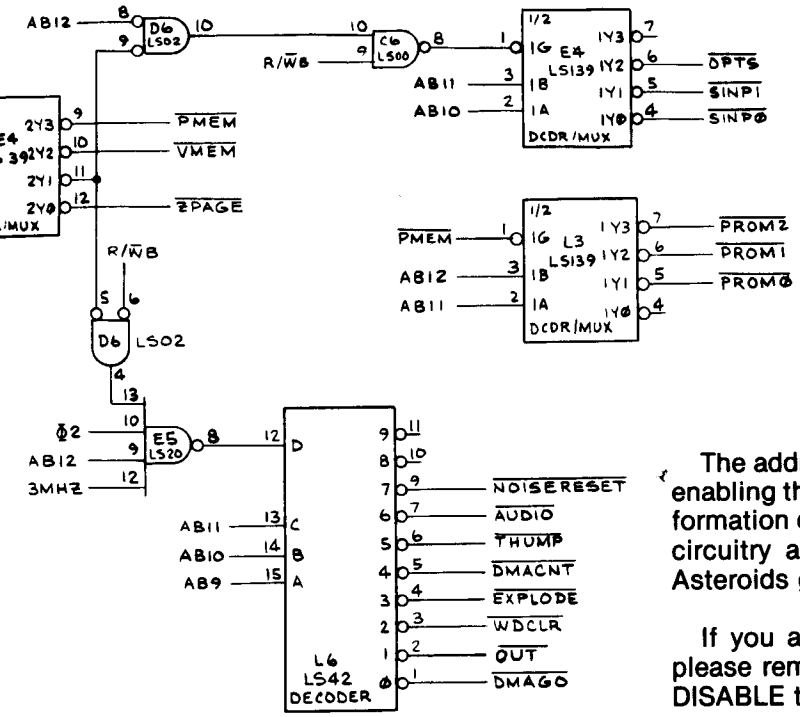
NOTE:
EITHER A 74LS245 OR AN AM8304B MAY BE

ADDRESS D



HEXADECIMAL	A15
0000-01FF 0200-02FF 0300-03FF	
2001 2002 2003 2004	
2005 2006 2007 2400	
2401 2402 2403 2404	
2405 2406 2407 2800	
2801 2802 2803	
3000 3200 3200 3200	
3200 3200 3200 3400	
3600 3600 3A00 3A00	
3C00 3C01 3C02 3C03	
3C04 3C05 3E00	
4000-47FF 5000-57FF 6800-7FFF	

DECODING CIRCUITRY



The address decoder performs the function of turning on or enabling the appropriate circuitry at the critical time, so that information can be transferred back and forth between the game circuitry and the MPU. The memory map below is for the Asteroids game.

If you are going to use the Automatic RAM/ROM Tester, please remember to remove MPU C3 and ground the WDOG DISABLE test point.

ADDRESS																DATA									
5	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	0	0				0	1	A	A	A	A	A	A	A	A		D	D	D	D	D	D	D	D	ZERO & ONE PAGE RAM
	0	0				1	0	A	A	A	A	A	A	A	A		D	D	D	D	D	D	D	D	PLAYER 1 RAM
	0	0				1	1	A	A	A	A	A	A	A	A		D	D	D	D	D	D	D	D	PLAYER 2 RAM
	0	1	0	0	0								0	0	1	R	D								3 KHz
	0	1	0	0	0								0	1	0	R	D								HALT
	0	1	0	0	0								0	1	1	R	D								HYPERSPACE SW
	0	1	0	0	0								1	0	0	R	D								FIRE SW
	0	1	0	0	0								1	0	1	R	D								DIAG. STEP
	0	1	0	0	0								1	1	0	R	D								SLAM SW
	0	1	0	0	0								1	1	1	R	D								SELF TEST SW
	0	1	0	0	1								0	0	0	R	D								LEFT COIN SW
	0	1	0	0	1								0	0	1	R	D								CENTER COIN SW
	0	1	0	0	1								0	1	0	R	D								RIGHT COIN SW
	0	1	0	0	1								0	1	1	R	D								1 PLYR START SW
	0	1	0	0	1								1	0	0	R	D								2 PLYR START SW
	0	1	0	0	1								1	0	1	R	D								THRUST SW
	0	1	0	0	1								1	1	0	R	D								ROT RIGHT SW
	0	1	0	0	1								1	1	1	R	D								ROT LEFT SW
	0	1	0	1	0									0	0	R							D	D	OPT SW (SW8, SW7)
	0	1	0	1	0									0	1	R							D	D	OPT SW (SW6, SW5)
	0	1	0	1	0									1	0	R							D	D	OPT SW (SW4, SW3)
	0	1	0	1	0									1	1	R							D	D	OPT SW (SW2, SW1)
	0	1	1	0	0	0										W								D	DMAGO
	0	1	1	0	0	1										W									2 PLYR START LAMP
	0	1	1	0	0	1										W							D		1 PLYR START LAMP
	0	1	1	0	0	1										W						D			RAMSEL
	0	1	1	0	0	1										W					D				COIN CNTRL LEFT
	0	1	1	0	0	1										W				D					COIN CNTRC CENTER
	0	1	1	0	0	1										W			D						COIN CNTRR RIGHT
	0	1	1	0	0	1										W									WDCLR
	0	1	1	0	1	1										W	D	D							EXPLOSION PITCH
	0	1	1	0	1	1										W			D	D	D	D			EXPLOSION VOLUME
	0	1	1	1	0	0										W				D					THUMP VOLUME
	0	1	1	1	0	0										W					D	D	D	D	THUMP FREQUENCY
	0	1	1	1	1	0							0	0	0	W	D								SAUCER SOUND
	0	1	1	1	1	0							0	0	1	W	D								SAUCER FIRE SOUND
	0	1	1	1	1	0							0	1	0	W	D								SAUCER SOUND SELECT
	0	1	1	1	1	0							0	1	1	W	D								SHIP THRUST SOUND
	0	1	1	1	1	0							1	0	0	W	D								SHIP FIRE SOUND
	0	1	1	1	1	0							1	0	1	W	D								LIFE SOUND
	0	1	1	1	1	1										W									NOISE RESET
	1	0	0	0	A	A	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	D	VECTOR RAM
	1	0	1	A	A	A	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	D	VECTOR ROM