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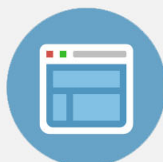

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"Silicon millefeuille": From a silicon wafer to multiple thin crystalline films in a single step

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During the last years, many techniques have been developed to obtain thin crystalline films from commercial silicon ingots. Large market applications are foreseen in the photovoltaic field, where important cost reductions are predicted, and also in advanced microelectronics technologies as three-dimensional integration, system on foil, or silicon interposers [Dross *et al.*, Prog. Photovoltaics **20**, 770-784 (2012); R. Brendel, *Thin Film Crystalline Silicon Solar Cells* (Wiley-VCH, Weinheim, Germany 2003); J. N. Burghartz, *Ultra-Thin Chip Technology and Applications* (Springer Science + Business Media, NY, USA, 2010)]. Existing methods produce "one at a time" silicon layers, once one thin film is obtained, the complete process is repeated to obtain the next layer. Here, we describe a technology that, from a single crystalline silicon wafer, produces a large number of crystalline films with controlled thickness in a single technological step. © *2013 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4803009]

The demand for thin (<100 μm) and ultra-thin (<40 μm) crystalline silicon wafers is increasing pushed by three-dimensional (3D) circuit integration, Micro-Electro-Mechanical-Systems (MEMS) fabrication, and photovoltaics.[1–3] Thickness of commercial solar cells, for instance, has been historically determined by wafering, instead of performance. Single wafers are obtained from ingots by sawing. Progressively, sawing process has improved and commercial silicon solar cells, willing to reduce cost while maintaining efficiency, have reduced their thickness from 350 μm in the 90's to 180 μm nowadays, being difficult to achieve further reductions with this technique. Nevertheless, lower thicknesses still support high conversion efficiencies, as an example, 21.5% efficiency has been demonstrated in 50 μm thick silicon solar cells.[4–6] Furthermore, the use of nanophotonic light-trapping approaches has recently shown that c-Si thin films with thicknesses below 10 μm can absorb as much sunlight as 300 μm thick crystalline substrates.[7] At the same time, from the microelectronic area, the International Roadmap for Semiconductors (ITRS)[8] claims for even thinner substrates, down to 10 μm, which will allow for 3D circuit integration. In the microelectronics industry, where an extra cost can be assumed, mechanical thinning instead of sawing is used in the range of 50 μm, being the uniformity of the final layer a limiting factor. For lower thicknesses, in the order of 1 to 10 μm, the usual fabrication technique is to mechanically and chemically etch Silicon on Insulator (SOI) wafers. Although costly, excellent uniformity can be obtained.[9,10]

Trying to overcome the limitations of both sawing and polishing/etching, several alternatives have been proposed, some of them reaching the pre-industrial stage.[11] Two main approaches have been followed, namely (a) induced cleaving and (b) porous silicon based methods. Induced cleaving methods are in principle "kerf-free," i.e., saw cut and/or wafer thinning losses are avoided. Cleaving can be promoted either through hydrogen implantation, by laser cutting or via stress induced by a thick metal deposition.[12,13] Those procedures allow obtaining crystalline silicon layers in the 20–50 μm range. On the other hand, porous silicon based methods involve the creation of two layers with different porosities on the top of the wafer, a low porosity layer allowing the epitaxial growth of c-Silicon and a high porosity layer that weakly attaches to the substrate to detach the grown thin film. Once the upper layer detaches, the substrate can be re-used.[5,14] Finally, an "epi-free" method has recently been proposed where the patterning of the surface with close-packed tiny holes results into a sort of porous structure. After a strong annealing in a non-oxidizing ambient (argon or hydrogen), the surface reorganizes leading to the formation of a 1–2 μm thick silicon layer on an empty plate.[15–19] The physical reason for this surprising behavior is that, at high temperature, pores try to minimize their surface energy by transforming into spheroids that will be trapped into the material. If pore geometry is properly adjusted, spheroids collapse forming a single cavity below the thin crystalline surface.

All these methods produce one single layer of silicon at a time. If a second one is needed, the process must be repeated from the beginning. Here, we show how to obtain, from a single silicon wafer and on a single fabrication step, multiple "epi-free" c-Silicon thin layers with controlled thickness or, as we call it, a "millefeuille" of crystalline silicon. The methodology is also based on the annealing of porous silicon structures. In such process, the evolution of the pores during annealing is governed by surface diffusion as described by the Mullin's equation.[20–22] Recently, sine generated curves (i.e., curves whose curvature is a sine function of the arc-length parameter), which have been used in the past to describe river meanders,[23] have been found to describe the evolution of high aspect ratio surfaces mediated

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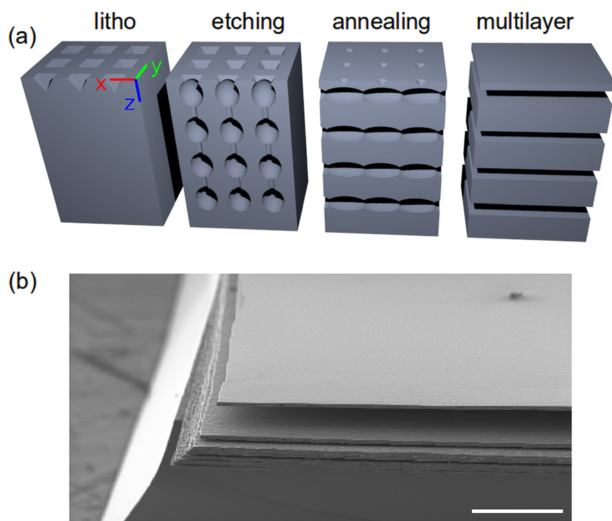

FIG. 1. Silicon "millefeuille" fabrication process: (a) Schematic view of the four stages of c-Si multiple layers formation: lithography, electrochemical etching, annealing, and thin layer formation. (b) SEM image of a final "millefeuille" structure standing on the silicon wafer. Scale bar is 100 μm.

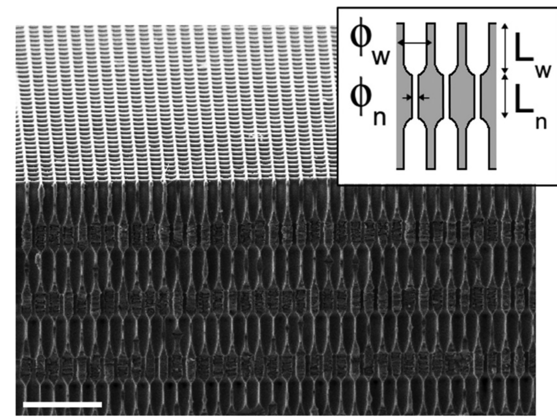

FIG. 2. Bird's eye SEM image showing a square array of modulated pores alternating wide and narrow diameter sections in depth. Scale bar is 10 μm. The inset shows the main parameters of pore modulation: length L and diameter ϕ. Subindexes w and n stand for *wide* and *narrow*.

by surface diffusion.[24] A detailed inspection of these results suggests that, by accurately controlling the profile of the pores, it should be possible to obtain multiple crystalline layers separated by voids. Hereafter, we show how, through a precise in-depth modulation of pore diameter, both the number of layers and their thickness can be controlled.

Fig. 1(a) summarizes the fabrication procedure. The base material was Czochralski (CZ) *n*-type silicon wafers, ⟨100⟩ oriented, with 0.5 Ω·cm resistivity and an initial thickness of 350 μm. Different resistivity values, including *p*-type substrates,[25] and different thicknesses can be used with proper adjustment of the etching parameters. Standard photolithography is used at first step to define pore distribution. A square distribution of 1 μm holes, 2 μm pitch, is patterned on the surface by Reactive Ion Etching (RIE) and tetramethylammonium hydroxide (TMAH) solution at 90 °C to create an inverse pyramid configuration on the silicon, marking the starting points for growing pores. Then, the in-depth modulated pores are created by electrochemical etching of silicon in hydrofluoric acid (HF) solution (5 wt. %) at 10 °C.[26–28] During the etching process, the applied current and voltage are controlled in order to obtain the desired pore modulation. System current is controlled by backside illumination between 2 and 12 mA/cm^2. System voltage is controlled between 2 and 5 V. This generates the positive carriers required to activate and control the dissolution of silicon at each time and depth, and control this way the pore diameter in depth. The "millefeuille" structure is formed by high temperature annealing under argon atmosphere at 1200 °C for 2 h. Pore reorganization can also take place at lower temperatures but for longer annealing times. Load/unload is done at 600 °C and the temperature is risen/lowered at 15 °C/min. Finally, individual thin films are exfoliated from the substrate.

In this way, we achieve both full wafer area and layer thickness fabrication control. In principle, the whole wafer can be sliced in a single step following this process, being the resulting number of layers only determined by wafer initial thickness and the thicknesses of the layers. Fig. 1(b) shows a Scanning Electron Microscope (SEM) image of a final sample before exfoliation where the formation of independent thin layers over the silicon bulk is clearly observed. The given image reveals the fabrication of 10 layers (not all clearly visible) with thicknesses around 6 μm. The ten thin films reported in the figure were produced in 3 h etch (120 μm depth pores).

Pore modulation is designed to present alternate wide sections, with diameter ϕ_w and length L_w, and narrow sections, with diameter ϕ_n and length L_n, along depth. Fig. 2 shows a SEM image of the typical initial pore structure and a simplified schema of the presented structural parameters. Each modulation (a section of length L_n followed by a section of length L_w) is the origin of a single silicon layer, with thickness approaching L_n, standing on a void. Several experiments have been conducted to further characterize the formation of crystalline silicon layers from a given initial pore modulation. The experiments are reported in Fig. 3, where each circle denotes proper thin film formation (the formation

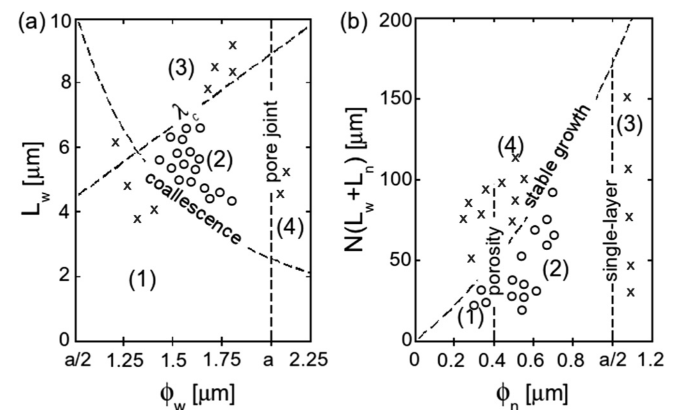

FIG. 3. (a) Experimental conditions for void layer formation as a function of initial modulation parameters: (1) no-void formation because of insufficient porosity; (2) parameter region for void formation; (3) uncontrolled recrystallization; and (4) no-void formation because of excessive porosity. (b) Experimental conditions for silicon layer formation as a function of initial modulation parameters: (1) solid layer formation; (2) layer formation with a row of small pores inside; (3) highly porous monolayer formation; and (4) unstable pore growth. Circles denote the formation of a set of thin films separated by voids and crosses mark the failed experiments.

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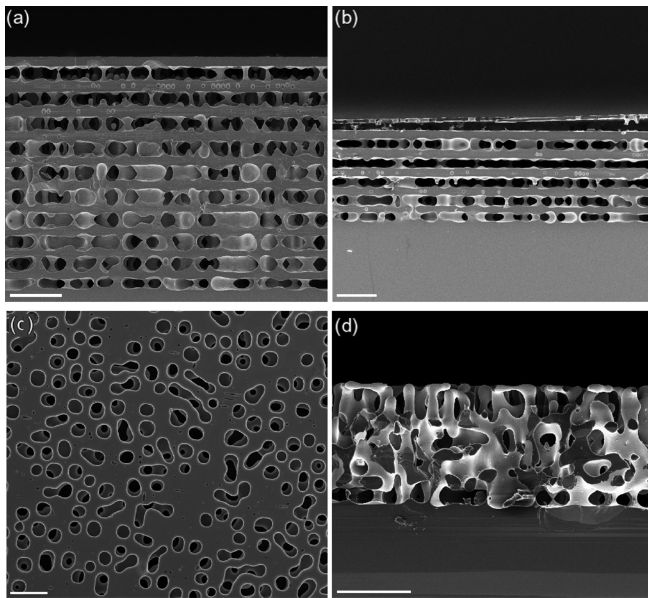

FIG. 4. Annealing results for an initial sample with (a) and (b) insufficient pore volume provoking the maintenance of silicon pillars; and (c) and (d) originally interconnected pores provoking a sort of pore melting. Scale bars are 20 μm.

of a set of continuous silicon films separated by voids) and each cross a failed formation.

Opening the discussion on void layer formation, as pores try to minimize their surface energy by transforming into spheroids during the annealing, in our modulated structure, each wide pore section will turn into a single spheroid that must contact with adjacent spheroids in order to collapse into a void layer (the so-called coalescence condition). This defines the following condition: $\pi/4\ L_w\ \phi_w^2 > \pi/6\ a^3$, where the first term of the equation is the volume of the wide pore section, and the second is the volume of a sphere with diameter the lattice constant a. This divides the (L_w, ϕ_w) plane into regions (1) and (2) in Fig. 3(a). Void layers cannot be obtained for conditions in region (1), where the initial pore volume is too small to make the spheroids interconnect during annealing, and some pillars remain between silicon layers (Figs. 4(a) and 4(b)). For longer cylindrical pores, wide pore regions tend to evolve forming more than a single spheroid during annealing, being $\lambda_c = 4.45\phi_w$ the critical distance between separated attempts of sphere formation,[19] and making the formation of a void layer uncontrollable. This defines region (3) in Fig. 3(a), where $L_w \gg \lambda_c$. Finally, in region (4), where $\phi_w > a$, pores interconnect during the etching process making impossible to obtain continuous and smooth void layers and, as a consequence, neither Si layers (Figs. 4(c) and 4(d)). The set of parameter values that corresponds to stable void formation is then limited to region (2) in Fig. 3(a).

Regarding the formation of crystalline silicon layers, it is well known in the field of electrochemical etching of pores in silicon that there is a relation between the minimum pore diameter that can be obtained and depth.[26] For a given silicon resistivity and etching conditions, in order to keep stable pore growth, minimum pore diameter must be progressively increased if greater depth has to be obtained. This is shown in Fig. 3(b), where experiments are located attending to the diameter of the narrow region, ϕ_n, and the total modulation length, $N\cdot(L_w + L_n)$, with N the number of periods (i.e., the final number of formed layers). Again, crosses represent failed experiments, while circles the formation of a set of silicon layers separated by voids. Region (4) corresponds to the mentioned region of unstable pore growth, which has been experimentally found, that impedes the formation of uniform multiple layers. Below region (4) in Fig. 3(b), where stable pore growth is guaranteed, we can distinguish 3 zones. Solid silicon films are obtained in region (1) within the lower values of ϕ_n. However, these low diameters are only compatible with shallow pores (stable pore growth), limiting the number of layers that can be obtained. For a high number of silicon layers, pore length must be larger and, consequently, the diameter in the narrow zone also has to increase, falling in region (2). In this region, silicon layers are formed with a row of embedded spherical voids inside. Similar results, for the same reasons, are obtained when L_n is highly increased to obtain thicker silicon layers. Finally, we found that for large values of ϕ_n in region (3), which actually define a low-amplitude pore modulation, a thick and highly porous silicon layer is obtained.

The presented discussion is depicted in Fig. 5, where SEM images of different final structures are presented. Solid layer formation is observed in image (a). A total number of 3 layers with average thickness of 6.5 μm, plus a very thin top one, have been fabricated. Larger number of layers is shown in image (b), where the presence of trapped spheres is observed due to the larger ϕ_n value. Image (c) shows the result of a low-amplitude pore modulation, as previously

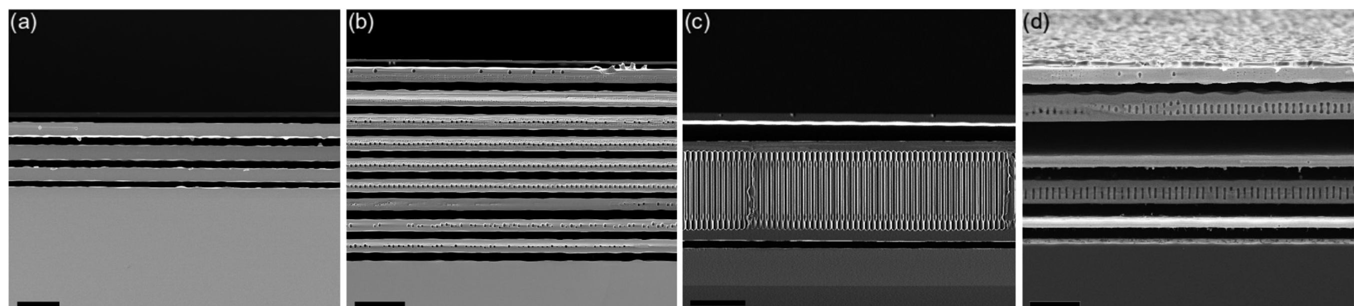

FIG. 5. SEM images of final layers' formation: (a) solid layers with 6.5 μm average thickness; (b) 10 layers with 5.9 μm average thickness with a row of pores inside; (c) thick layer formation (38 μm) due to low-amplitude pore modulation; and (d) controlled thickness multilayer with alternate films of 4 and 8 μm thickness. Scale bars are 20 μm.

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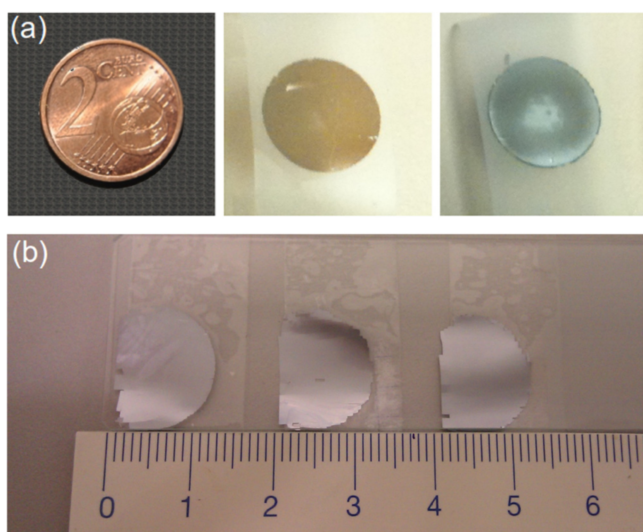

FIG. 6. Tape-exfoliated thin c-Silicon films: (a) Image of two layers presenting brownish and grayish colour due to the different thicknesses, 1–2 μm and 6–7 μm, respectively. A 2 cent coin is included for size comparison. (b) Thin films attached to a glass substrate. Ruler is in centimetres.

discussed, leading to the formation of a first solid thin layer followed by a highly porous layer with nearly 40 μm thickness. Finally, SEM image (d) shows alternate layers with thicknesses of 4 and 8 μm. An important feature of the presented fabrication technique is that the length L_n can be independently controlled, which makes it possible to obtain, from a single initial wafer, different layers with different thicknesses.

After layer formation, silicon thin films are tape-exfoliated from the substrate to characterize their structural properties. Some exfoliated films are shown in Fig. 6. Thinner layers, around 1–2 μm, present brown color (Fig. 6(a)) due to optical transmission properties of silicon and thicker layers present the typical gray-silicon color. Additionally, in Fig. 6(b), we present a set of three samples exfoliated from the same original silicon "millefeuille." Films have been sticked to a glass slide for characterization. We expect, from the properties of the presented technique, that the formed multiple layers should preserve the crystallographic orientation of the bulk, which is important for applications. We have confirmed it by X-ray texture analysis on different final layers, with and without pores inside. A single crystallographic peak is found at 69.3° marking the ⟨400⟩ silicon orientation, as it was in bulk, in all analyzed layers. The same results have been obtained in all samples. We have also characterized the roughness of the obtained layers by interferometry. Thinner layers, around 1–2 μm, present an average roughness of 100–130 nm, while the average roughness of the thicker layers is in between 250 and 300 nm. Although the crystal quality of the reported thin films is good as stated in Ref. 18, stacking fault density and dislocations among the structure are currently under investigation.

In conclusion, multiple silicon layers from a single wafer in a controlled way have been produced. We have shown that, by choosing optimized diameter modulation of the pores, we are able to obtain different numbers of layers whose thickness can also be varied in a large extent. In this proof of concept, samples' area has been limited to 15 mm diameter for convenience, although the technology is scalable to full wafer scale. Further work is needed in order to in-depth explore the possibilities and limitations of the proposed technique.

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