A Fully Integrated 144 MHz Wireless-Power-Receiver-on-Chip with an Adaptive Buck-Boost Regulating Rectifier and Low-Loss H-Tree Signal Distribution

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Abstract

An adaptive buck-boost resonant regulating rectifier (B^2R^3) with an integrated on-chip coil and low-loss H-Tree power/signal distribution is presented for efficient and robust wireless power transfer (WPT) over a wide range of input and load conditions. The B^2R^3 integrated on a 9 mm^2 chip powers integrated neural interfacing circuits as a load, with a TX-load power conversion efficiency of 2.64 % at 10 mm distance, resulting in a WPT system efficiency FoM of 102.

Introduction

Emerging applications such as mm-sized modular neural interfacing devices [1] are now being enabled by fully integrating wireless power transfer (WPT) functionality on-chip. Conventional designs, which first rectify then regulate, suffer from cascaded losses that limit efficiencies [2-5], while prior-art regulating rectifiers require a large external coil. Although recent work has demonstrated complete on-chip integration of a regulating rectifier [6], robustness to link variations was limited. In addition, >100 MHz-range RF power delivered to an on-chip coil induces eddy currents in auxiliary on-chip wiring and metal planes, degrading WPT efficiency while also potentially disrupting the functionality of underlying circuitry. To avoid large metal planes, [3] reduced decoupling capacitance (decaps) to only 20 pF through inclusion of a high-performance high-power linear regulator.

Buck-Boost Resonant Regulating Rectifier (B^2R^3)

This paper introduces a fully-on-chip B^2R^3 architecture that robustly receives wireless power over a wide range of conditions by: 1) fully-integrating an on-chip coil with distributed perpendicular decoupling and loop-free H-tree geometry power line/signal distribution networks optimized for maximum RF power collection and minimum RF interference; 2) employing a regulating rectifier that dynamically adapts to a wide range (>14 dB) of RF input by switching between boost and buck modes, while providing a dual-rail supply from lower magnitude RF input signals than prior work [6]; and 3) including a 0.86 μW control feedback loop that offers fast load regulation performance while supporting both boost and buck regulating rectifiers.

The proposed B^2R^3 system is shown in Fig. 1. Here, RF energy received by an on-chip coil passes through the B^2R^3, to establish dual DC rails, *VH* and *VL*. Unfortunately, RF energy also couples to load circuits, and ad hoc routing of supply lines and placement of decaps can create many loops and metal planes, reducing the RX coil's *Q* by over 60 % (thereby reducing WPT efficiency), while also introducing noise to sensitive circuits. To remove loops and large planes from the layout, a fractal H-tree power and signal distribution network with 1 nF of distributed decaps is proposed. HFSS simulation and measurements show negligible loss in *Q* compared to an ideal, isolated coil. Furthermore, the same H-tree topology serves as a network backbone for cancellation of differential-mode interference in sensitive analog differential signals.

Although 2-step rectification and regulation can operate at wide input range, regulation is increasingly inefficient at larger RF input voltage as illustrated in Fig. 2. The proposed B^2R^3 accomplishes regulated rectification over wide input range through a mode arbiter that adapts to the sensed RF envelope. BOOST mode converts low RF voltage to larger regulated DC voltage, while $BUCK_{1,2,3}$ modes efficiently convert larger RF voltage down. For smooth transition between modes, a combined BUCK-BOOST mode operates at an intermediate region. Shown in Fig. 3, *VHS* tracks *VH* with DC offset defining a target *VH*. To retain the fast settling of conventional integrator-less bang-bang control, *VHS* is directly fed to the latch (path 2) while a parallel integration path (path 1) performs PID control to additionally remove static error at *VH*. The boost regulating rectifier employs a feedback-controlled V_{TH} cancellation scheme for regulation. The feedback loop dynamically determines the amount of V_{TH} cancellation through V_{OTA}. Conversely, the buck regulating rectifier is activated by V_{COMP} from the feedback, turning the rectifier on/off according to *VHS* and V_{OTA}.

In Fig. 4, the switched capacitor circuits implement floating voltage sources by transferring V_{OTA} to the NMOS devices in the boost rectifier. A zero short-circuit-current level-shifter consumes 190 nW at 1 MHz, a 35**x** improvement over a conventional design. In buck mode, the regulating rectifier dynamically determines the duty-cycle of the active switches (i.e., t_d and t_{pw}) with 1 MHz clock for maximizing t_{pw}. Instead of a high-speed comparator [6], low-power delay controlled inverter chains operating with a local feedback are employed. To prevent undesired energy transfer from large RF input, the power PMOSs are gated with a voltage (VHH) larger than the RF envelope. Three power switches are implemented in parallel ($BUCK_{1,2,3}$) to optimize PCE according to RF input.

Measurement Results

The B^2R^3 is tested with a 470 mm^2 TX coil located 6-16 mm away from the chip. In Fig. 5, the B^2R^3 produces regulated output voltages even under 50 % amplitude variation in PA input by adapting its modes dynamically. Load regulation is measured in Fig. 6. Owing to its fast loop response, even with only 0.25 nF decaps (two 0.5 nF in series), no sharp peak in V_{OUT} is shown, unlike typical >100 mV overshoot otherwise. Thanks to mode switching and high voltage gating, a link dynamic range of at least 14dB at 10mm distance is demonstrated in Fig. 7. The TX-RX link efficiency is -12.6 dB at 6.35 mm. The TX-load WPT efficiency is measured as 3.66 %, indicating a regulating rectifier PCE of 66.5 % (within 1.5 % of simulation). RF powering to integrated load circuits is validated by demonstrating regulated supplies during data transfer from the TX coil to the on-chip ASK demodulator through the integrated coil, shown in Fig. 8. Table I shows comparison with the state-of-the art. Standardized comparison for overall PCE (TX-regulated DC) is provided by the WPT system efficiency (WSE) FoM, defined here as overall PCE times cube of distance between TX and RX coils divided by cube square root of the RX coil area [3].

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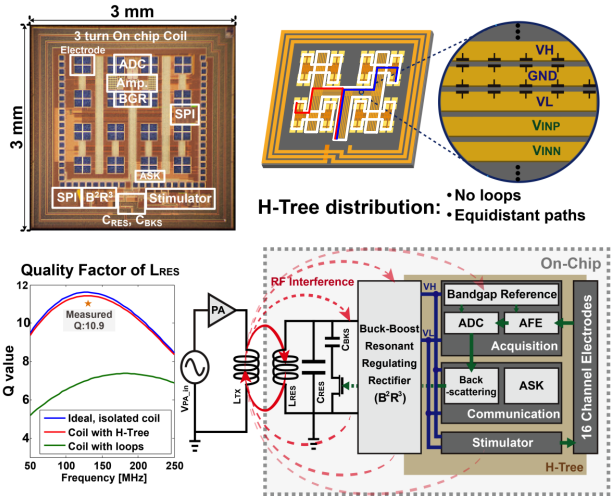

Fig. 1 Depiction of the on chip coil and the fractal H-Tree network. Significant routing is accomplished systematically and with minimal decrease in on-chip coil quality factor, and minimal RF interference to sensitive analog components.

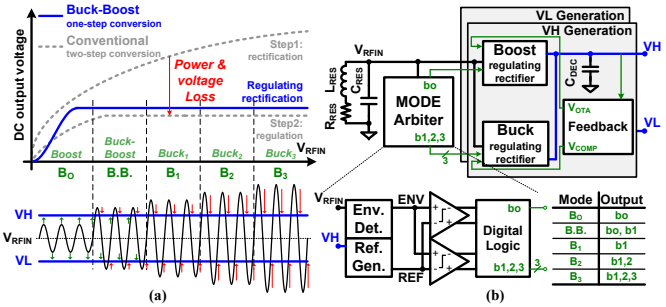

Fig. 2 (a) Conceptual operation of the conventional 2-step power conversion and the B^2R^3 showing the 5 regulating rectification modes that efficiently generate a dual supply according to RF input. (b) Overview schematics of the adaptive B^2R^3 mechanism with mode arbiter and its block diagram.

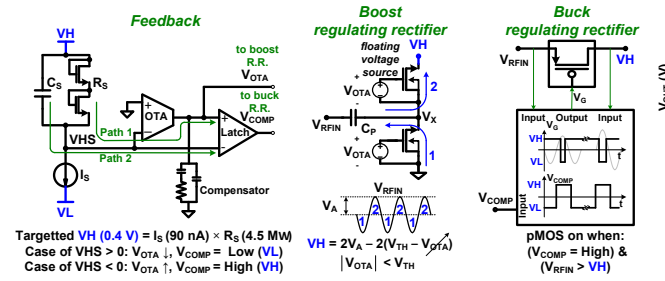

Fig. 3 (a) Schematic of the main feedback block (shown in Fig. 2). DC target voltage is defined with I_S and R_S as the main feedback loop forcing VHS to be close to GND. (b) With the floating voltage source, V_{TH} of NMOS in the boost regulating rectifier is cancelled dynamically by V_{OTA} from the feedback block for regulation fucntionality. (c) V_{COMP} from the feedback turns on/off the buck regulating rectifier to regulate VH.

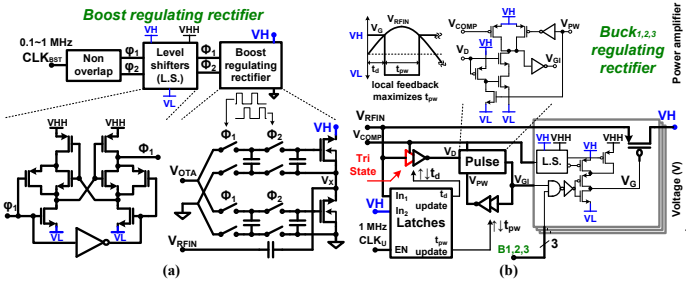

Fig. 4 Simplified schematic of the boost and buck regulating rectifiers. (a) Switched capacitors implement floating voltage sources with a no short-circuit-current level-shifter. (b) Local feedback loop defines t_d and t_{pw} with 1MHz updating CLK. PMOS is gated with higher voltage to avoid making a diode connection at large RF input.

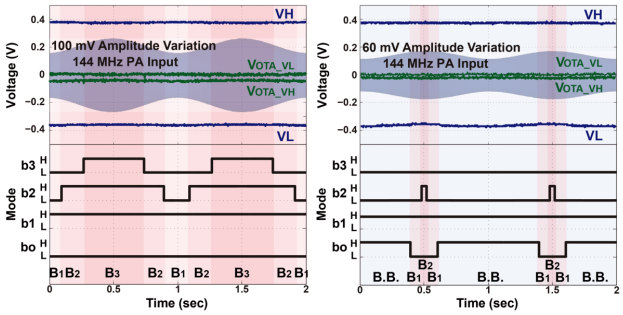

Fig. 5 Measurement shows robustness of B^2R^3 to changes in RF input power dynamically thanks to the mode-change by the proposed mode arbiter. RF input power can vary due to a number of reasons such as link distance, alignment, and impedance matching.

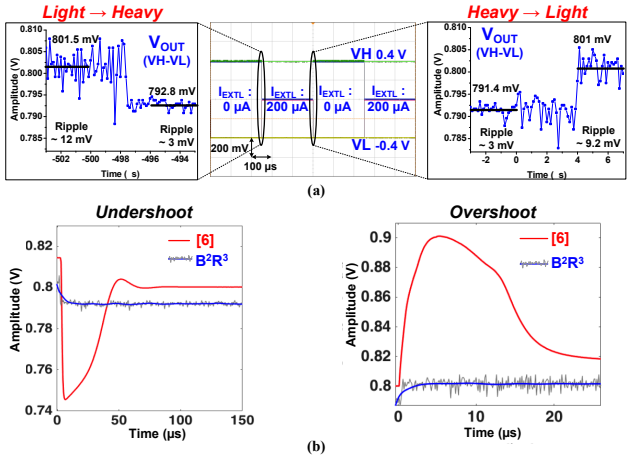

Fig. 6 (a) Measured load regulation response to external load perturbation, from open to 200 µA. Light to heavy load transition in left, and heavy to light load transition in right, showing 9.6 mV static ΔV_{OUT} (VH – VL). (b) Owing to the fast feedback loop, negligible over/undershoot is observed while a conventional design shows >100 mV overshoot.

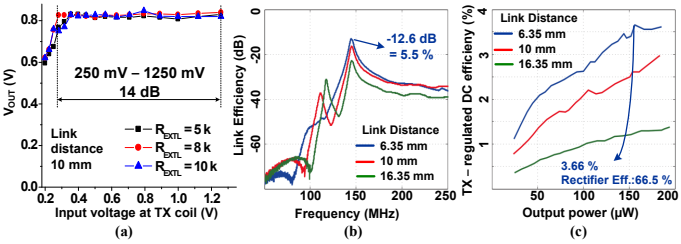

Fig. 7 (a) Measured transfer function showing wide input-range. At low RF inputs, boost mode can develop V_{OUT} while, at large RF input, high voltage gating helps regulation. (b) Link efficiency at various link distance and frequency, and (c) overall PCE (TX coil to regulated DC) are measured.

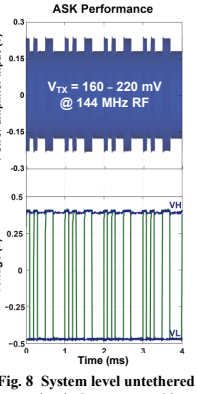

Fig. 8 System level untethered operation is demonstrated by the ASK demodulation.

Table I State of the art comparison

	[2]	[3]	[4]	[5]	[6]	This Work
Res. Freq. (MHz)	300	160	535	915	144	144
RX Coil/ Value(nH)/ Area(mm²)	Off-chip/ 32/ 42.25	On-chip/ 130/ 4.36	Off-chip/ 5.73/ 1	Off-chip/ N/R/ 4	On-chip/ 23.7/ 8.64	On-chip/ 60.3/ 8.74
# of modes	1	1	1	1	1	5
Regulator	separate LDO	separate LDO	separate LDO	separate LDO	regulating rectifier	regulating rectifier
Regulation*(%)	N/R	N/R	N/R	N/R	1.87	1.12
Overshoot (mV)	N/R	N/R	N/R	N/R	100	< 1
Dec. Cap (nF)	4	0.02	1.39	N/R	1	0.25
Process	65 nm CMOS	0.13 µm CMOS	65 nm CMOS	0.13 µm CMOS	0.18 µm CMOS SOI	0.18 µm CMOS SOI
Overall PCE(%)	1.19[a]	0.62[b]	0.02 (-37 dB)	0.048 (-33.2 dB)	2.04	2.64
Distance (mm)	12.5	10	13	15	10	10
WSE FoM**	8.46	68.1	43.94	20.25	80.3	102.1

[a]estimated from provided data, TX PW: 13mW, P_{DC_LOAD}: 0.160mW

[b]estimated from provided data, estimated η_{LDO}: 68 % (V_{DD}: 3.1 V, V_{REC2}: 4.5 V), provided η from TX coil to output of the rectifier: 0.9 %

*Regulation = Static ΔV_{OUT} / nominal V_{OUT}

**WPT System Efficiency FoM = $\frac{\eta_{overall} \times D^3}{A^{1.5}}$, where $\eta_{overall}$ is TX-regulated DC efficiency; D is distance between TX-RX coils; and A is area of the RX coil.