Frequency-Domain Characterization of Sliding Mode Control of an Inverter Used in DSTATCOM Application

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***Abstract*—In this paper, the commonly used switching schemes for sliding mode control of power converters is analyzed and designed in the frequency domain. Particular application of a distribution static compensator (DSTATCOM) in voltage control mode is investigated in a power distribution system. Tsypkin's method and describing function is used to obtain the switching conditions for the two-level and three-level voltage source inverters. Magnitude conditions of carrier signals are developed for robust switching of the inverter under carrier-based modulation scheme of sliding mode control. The existence of border collision bifurcation is identified to avoid the complex switching states of the inverter. The load bus voltage of an unbalanced three-phase nonstiff radial distribution system is controlled using the proposed carrier-based design. The results are validated using PSCAD/EMTDC simulation studies and through a scaled laboratory model of DSTATCOM that is developed for experimental verification.**

***Index Terms*—Bifurcation, distribution static compensator (DSTATCOM), forced-switching, sliding mode, Tsypkin's locus.**

I. Introduction

ANALYSIS of sliding mode control in the frequency domain has been of recent interest for the characterization of limit cycle with relay controller [1]–[3]. Limitation of the describing function is well understood, and Tsypkin's method needs to be replaced for more accurate results [2]–[4]. For power converters, the relay output is the pulsewidth-modulated (PWM) input to the switching element of the inverter and, for high-power applications, the switching loss increases linearly with the switching frequency. Therefore, the switching device needs to switch at low frequency. As opposed to the signum function used in the ideal sliding mode, a hysteresis band needs to be introduced in two-level switching in order to limit the switching frequency of converters. However, at low switching frequency, low attenuation of the system leads to the high magnitude of switching harmonics. There have been a few proposals for the calculation of the switching frequency for simple circuits [5]. However, trial and error procedure are usually employed to arrive at the correct switching frequency for higher order circuits [6]. In order to reduce the switching losses and switching harmonics, a few configuration of three-level inverters have been proposed [7], [8]. However, both the two-level and three-level inverters lead to the variable switching frequency over one fundamental cycle of power frequency. The switching condition also varies with the variation of parameters [9], [10]. Carrier-based modulation is used to achieve constant switching frequency [5], [7], [9]–[11] at the expense of a small sacrifice in transient and steady-state characteristics. Magnitude of the carrier is an important design parameter, and there is a minimum magnitude below which the synchronism is lost. Both the steady-state and transient performances deteriorate with the increase in the magnitude of the carrier.

In this paper, sliding mode control for a distribution static compensator (DSTATCOM) is designed for a power distribution system. Commonly used switching schemes for power converters of sliding mode, e.g., two-level, three-level, variable hysteresis, and carrier-based modulation, are analyzed and designed in the frequency domain. Tsypkin's locus of linear system and describing function of nonlinear relay [12], [13] are used to determine the stable switching of power converters. Analytical and graphical procedures are used for the characterization of switching frequency for the two- and three-level inverters. Further, the variable switching conditions are analyzed, and a procedure to maintain constant maximum switching frequency is suggested. A switching algorithm for the three-level inverter is used with a small dead zone. Commonly used carriers for the forced switching of inverters are also dealt with in the frequency domain. Sinusoidal signal is introduced as the fundamental carrier signal for the carrier-based modulation of sliding mode control. Minimum magnitude conditions of different carriers are determined for fixed frequency switching. Below this, the synchronism is lost. For robust switching at prefixed frequency, the concept of parameter sensitivity is introduced. The load bus voltage of a three-phase nonstiff radial distribution system is controlled using sliding mode control of DSTATCOM. Conditions of unbalancing, uncertainty, and parameter variations are considered for robust switching of inverter using carrier-based modulation. Border collision bifurcation is identified for the carrier-based modulation, and it is shown that the hysteresis band and carrier magnitude must be chosen carefully to avoid chattering and harmonic switching, respectively. An experimental verification of the switching schemes developed in this paper is provided using scaled laboratory model of a single-phase DSTATCOM.

Manuscript received November 4, 2004; revised April 28, 2005 and June 30, 2005. This work was supported in part by the Central Power Research Institute, Bangalore, India through the project "Development of Active Power Line Conditioners for Power Distribution Systems." This paper was recommended by Associate Editor M. K. Kazimierczuk.

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Digital Object Identifier 10.1109/TCSI.2005.859053

II. Sliding Mode Control of DSTATCOM

A. DSTATCOM Model

In this section, a single-phase topology of DSTATCOM is assumed [14]. A typical DSTATCOM connected distribution system is shown in Fig. 1. It is desired to control the output voltage of DSTATCOM such that the load terminal voltage (v_t) is regulated. This is called the operation of DSTATCOM in voltage control mode [15], [16].

With respect to Fig. 1, the load is supplied by a voltage source v_s through a feeder (R_s, L_s). DSTATCOM constitutes an H-bridge voltage-source inverter (VSI) with the switches Sw_1–Sw_4 consists of a power semiconductor device like IGBT or GTO and an antiparallel diode. The dc link voltage V_{dc} is connected through a transformer (T_1), where L_T is its leakage inductance referred to the high voltage side and R_T represents the equivalent loss resistance due to inverter switching and copper loss in the transformer. The point of common coupling (PCC) terminal voltage across the filter capacitor (C_f) is v_t. It is assumed that the load is nonlinear with an input impedance of R_l, L_l. The load current is denoted by i_l. The nonlinear load is assumed to be a voltage source type that is represented by a periodic harmonic voltage source v_d [17] and may be called harmonic perturbation. Where more generalized analysis is required, v_d may be a current controlled voltage source but periodic in the steady state. The other currents flowing through the different branches are: the source current i_s, the inverter output current $i_{\rm in}$, the current through the filter capacitor (C_f) is $i_{\rm cf}$ and the current injected in shunt branch is $i_{\rm sh}$. The voltage at the output of the transformer is assumed to be $u.m.V_{\rm dc}$, where $u = \pm 1$ is the switching action and m is the transformer voltage ratio. Choosing the state vector $x^T = [i_{\rm sh}\ i_{\rm cf}\ v_t\ i_l]$, the following state space representation is obtained:

$$\dot{x} = Ax + b_1 v_s + b_2 u + b_3 v_d \tag{1}$$

where

$$A = \begin{bmatrix} -\frac{R_s}{L_s} & 0 & \left(\frac{1}{L_s}+\frac{1}{L_l}\right) & \left(\frac{R_s}{L_s}-\frac{R_l}{L_l}\right) \\ \left(\frac{R_s}{L_s}-\frac{R_T}{L_T}\right) & -\frac{R_T}{L_T} & -\left(\frac{1}{L_s}+\frac{1}{L_T}+\frac{1}{L_l}\right) & \left(-\frac{R_s}{Ls}+\frac{R_l}{L_l}\right) \\ 0 & \frac{1}{C_f} & 0 & 0 \\ 0 & 0 & \frac{1}{L_l} & -\frac{R_l}{L_l} \end{bmatrix}$$

$$b_1 = \begin{bmatrix} -\frac{1}{L_s} \\ \frac{1}{L_s} \\ 0 \\ 0 \end{bmatrix}$$

$$b_2 = \begin{bmatrix} 0 \\ \frac{mV_{dc}}{L_T} \\ 0 \\ 0 \end{bmatrix}$$

$$b_3 = \begin{bmatrix} -\frac{1}{L_l} \\ \frac{1}{L_l} \\ 0 \\ -\frac{1}{L_l} \end{bmatrix}.$$

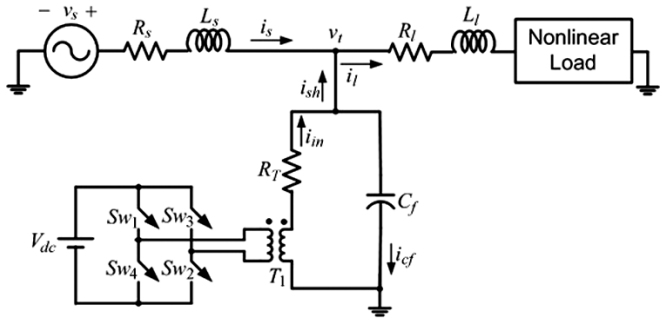

Fig. 1. Single-phase model of DSTATCOM controlled distribution system.

Taking the load terminal voltage as the output, the output equation can be written as

$$y = Cx = [0 \quad 0 \quad 1 \quad 0]x. \tag{2}$$

B. Sliding Mode Control

Consider the DSTATCOM circuit of Fig. 1. In order to design a control law independent of load and source parameters, a new state vector is defined as follows:

$$z^T = [\dot{v}_t \qquad v_t]. \tag{3}$$

The state space equation of the system may be written as

$$\dot{z} = Fz + g_1 u + g_2 d \tag{4}$$

where

$$F = \begin{bmatrix} -\frac{R_T}{L_T} & -\frac{1}{C_f L_T} \\ 1 & 0 \end{bmatrix}$$

$$g_1 = \begin{bmatrix} \frac{mV_{dc}}{C_f L_T} \\ 0 \end{bmatrix}$$

$$g_2 = \begin{bmatrix} 1 \\ 0 \end{bmatrix}.$$

Variable d is considered to be the disturbance and depends upon the shunt current as

$$d = -\frac{1}{C_f}\left(\frac{di_{\rm sh}}{dt}\right) - \left(\frac{R_T}{C_f L_T}\right) i_{\rm sh}. \tag{5}$$

For deriving the sliding mode control for (4), the following are required.

1) Switching surface $s(z_e)$ defined by the following state feedback law:

$$s(z_e) = Kz_e = k_1(\dot{v}_{tref} - \dot{v}_t) + k_2(v_{tref} - v_t) \tag{6}$$

where $z_e = [\dot{v}_{\rm tref} - \dot{v}_t\ v_{\rm tref} - v_t]^T$ is the error state vector with k_1 and k_2 are the feedback gains for the two states z_{e1} and z_{e2}, respectively.

2) A variable structure control is given by

$$\begin{aligned} u &= +1, \quad \text{for } s(z_e) > 0 \\ u &= -1, \quad \text{for } s(z_e) < 0. \end{aligned} \tag{7}$$

The existence condition of sliding mode control is expressed as

$$\begin{aligned} \dot{s} &> 0, \quad \text{when } s < 0 \\ \dot{s} &< 0, \quad \text{when } s > 0 \end{aligned} \tag{8}$$

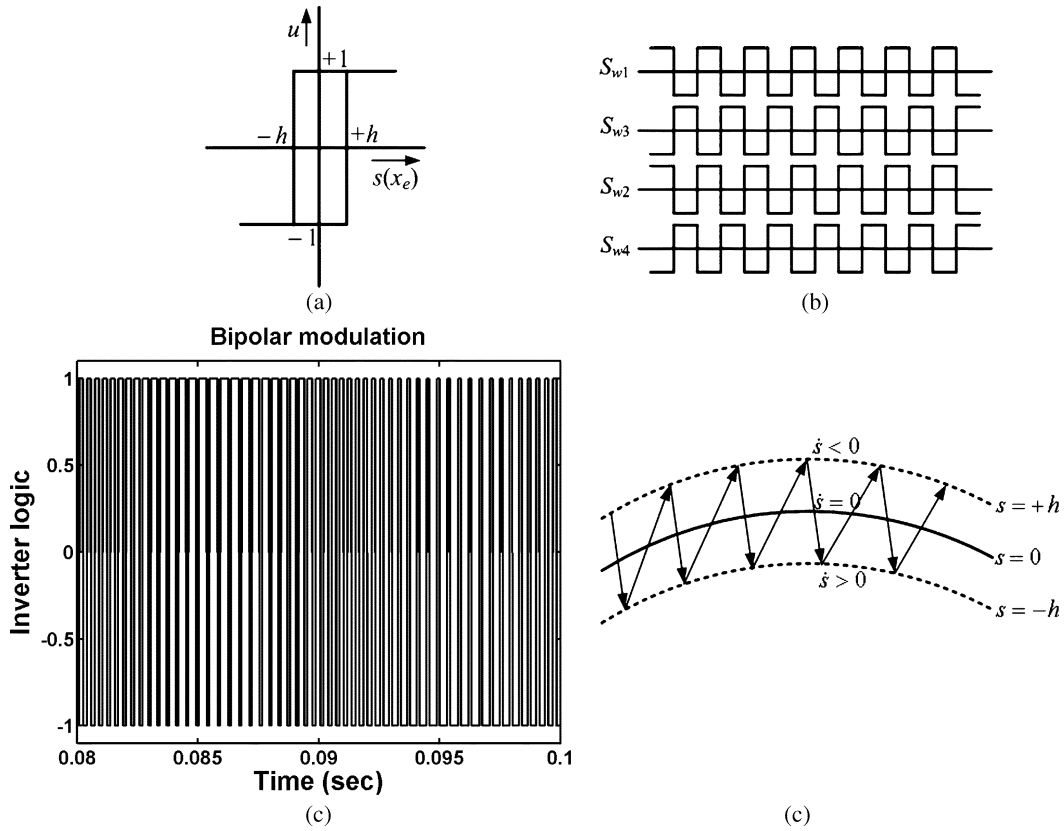

Fig. 2. Two-level switching. (a) Relay with hysteresis. (b) Switching diagram. (c) Bipolar modulation. (d) Switching surface.

or, equivalently, $s\dot{s} < 0$. If u in (7) is chosen to satisfy (8), the system will operate in sliding mode and z_e will tend to origin. Further, it is assumed that the equivalent control satisfies the limiting condition on switching input such that the evolution of system states lies in the existence domain [18].

In order to derive a model following sliding mode control, it is shown in [18] that the error state dynamics are given by

$$\dot{z}_e = F^* z_e \tag{9}$$

where $F^* = \begin{bmatrix} -(k_2/k_1) & 0 \\ 0 & 0 \end{bmatrix}$.

The matrix F^* has eigenvalues of $\lambda_1 = 0$ and $\lambda_2 = -(k_2/k_1)$. So long as the eigenvalue λ_2 is in the left half of the s-plane, the sliding surface is stable. After an initial transient, the weighted tracking error (6) will converge to origin depending upon the time constant $T = k_1/k_2$, and, under steady state, the states follow the references independent of system parameters. Note that the control law (6) requires the derivative of terminal voltage. This can be easily obtained from the measurement of filter capacitor current $i_{\rm cf}$ and dividing it by filter capacitor (C_f). The equivalent of (6) when implemented with (1) may be defined as

$$s(x_e) = K_e x_e = k_{e1}(i_{\rm cfref} - i_{\rm cf}) + k_{e2}(v_{\rm tref} - v_t) \tag{10}$$

where $K_e = [0\, k_{e1}\, k_{e2}\, 0] = [0\, k_1/C_f\, k_2\, 0]$.

III. Various Switching Schemes

The ideal sliding mode requires infinite frequency, and that leads to the chattering phenomenon. In the inverter-fed applications, the switching elements are IGBT and GTO, which have finite switching frequency. To bring the switching frequency into the limit of practical devices, a hysteresis logic with suitable width (h) is required. There are various switching schemes to achieve the desired switching frequency. The following three switching schemes are presented in this section:

- two-level switching (bipolar modulation);
- three-level switching (unipolar modulation);
- forced switching (carrier modulation).

The three switching schemes are now discussed briefly.

1) Two-Level Switching: This is the most commonly used switching scheme for sliding mode control. The inverter is operated under bipolar modulation with two levels of output $+1$ and -1. The switches S_{w1}, S_{w2} and S_{w3}, S_{w4} in Fig. 1 are operated in pair. Fig. 2(a) shows the switching logic, and Fig. 2(b) and (c) shows the switching diagram and inverter output level, respectively. In each cycle, two switches are turned off, and two switches are turned on. If f_s is the switching frequency, then the switching loss per on–off is proportional to the switching frequency (f_s) and given by $P_c = kf_s$. The total switching loss is $2P_c$. A variable structure control of (7) will now be followed by

$$\begin{aligned} u &= +1, \quad \text{for } s(x_e) > +h \\ u &= -1, \quad \text{for } s(x_e) < -h. \end{aligned} \tag{11}$$

As shown in Fig. 2(d), the velocity vector $\dot{s}$ crosses the switching surface $s(x_e)$ at every switching instant, satisfying the existence condition (8).

2) Three-Level Switching: There are various schemes of three-level switching proposed for sliding mode control [7], [8].

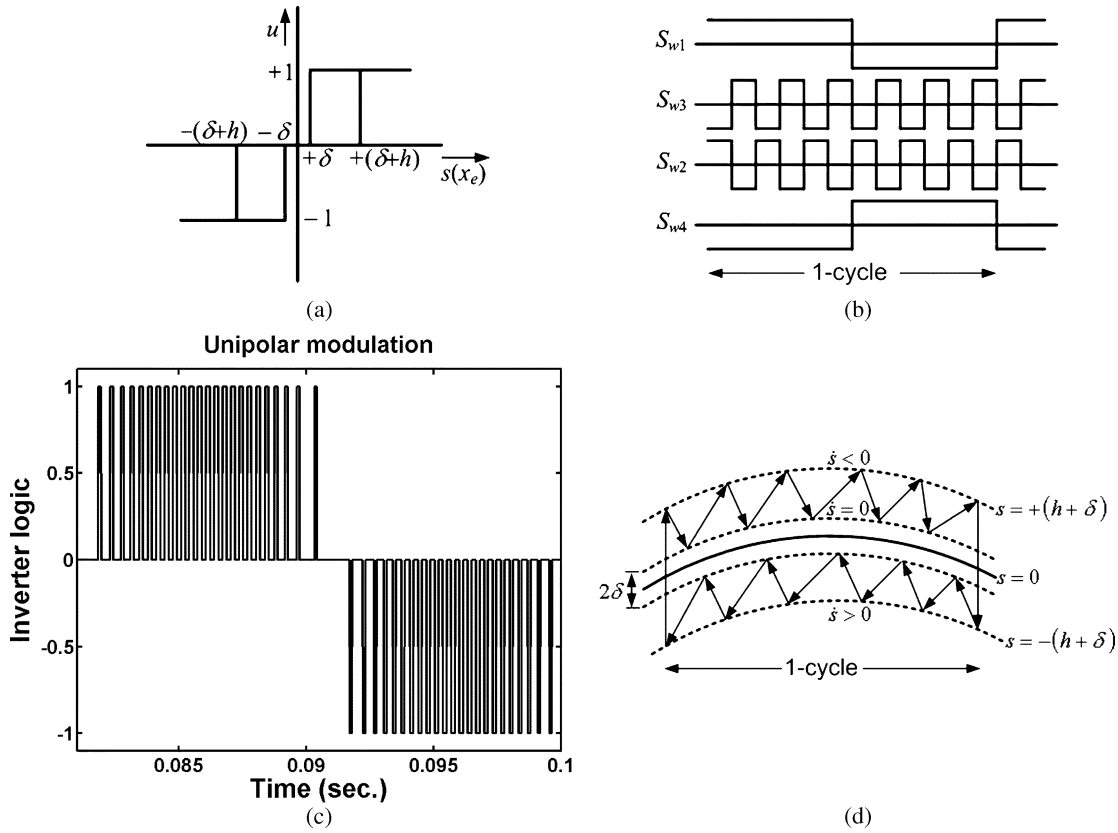

Fig. 3. Three-level switching. (a) Relay with hysteresis and dead zone. (b) Switching diagram. (c) Unipolar modulation. (d) Switching surface.

The scheme presented in this paper is based on the following variable structure control algorithm and shown in Fig. 3(a).

If $s(x_e) > 0$ then

$$\begin{array}{ll} u = +1 & \text{for } s(x_e) > +(h+\delta) \\ u = 0 & \text{for } s(x_e) < +\delta \end{array} \tag{12}$$

else if $s(x_e) < 0$ then

$$\begin{array}{ll} u = -1 & \text{for } s(x_e) < -(h+\delta) \\ u = 0 & \text{for } s(x_e) > -\delta \end{array}$$

It is assumed that the variable structure control (12) satisfies the existence condition of the sliding mode control (8) for switching surface s shifted by a factor $+(\delta + h/2)$ and $-(\delta + h/2)$ from its $s = 0$ value for the condition of $s(x_e) > 0$ and $s(x_e) < 0$, respectively, in (12). This scheme leads to unipolar modulation, and the inverter has three levels of output, i.e., -1, 0, and $+1$, as shown in Fig. 3(c). In this scheme, the left leg is kept at low switching frequency, thus accordingly lowering the operational cost. Fig. 3(b) shows the pair of switches S_{w1} and S_{w4} that change their status at every half cycle of switching function at power frequency as the switching function $s(x_e)$ is never allowed to touch the surface $s(x_e) = 0$, and reverses its polarity with every half cycle of switching function as shown in Fig. 3(d). A suitably small value of dead zone (δ) is introduced to avoid any bipolar modulation while $s(x_e)$ approaches zero. The possibility of bipolar modulation is there due to the finite sampling measurement. This is because, in between the two sampling instants, the switching function $s(x_e)$ might cross the surface $s(x_e) = 0$ and the switching algorithm (12) of opposite polarity will follow. However, the increase in the dead zone increases the steady-state tracking error. Therefore, the dead zone (δ) should be chosen as a minimum to just avoid any crossing of $s(x_e) = 0$. The right leg comprising switches S_{w2} and S_{w3} is kept at high switching frequency similar to the two-level scheme. Although the switching frequency as seen by the system is the same, the switching losses are reduced to approximately half, i.e., P_c plus a small amount due to a low-frequency switching leg. Moreover, due to the reduction of pulse height of the inverter output to half, the ripple in the system output is also reduced to half.

Both conditions (11) and (12) lead to the quasi-sliding regime. The two switching schemes presented above possess an excellent robust tracking that is insensitive to parameter changes. However, both schemes suffer from the disadvantage of variable switching frequency. To overcome this disadvantage, there are two methods prevailing in the practice: carrier-based modulation and variable hysteresis band. The first method is discussed below while the second method is presented in Section IV-B.

3) Forced Switching: Prefixed switching frequency can be obtained by comparing the switching function with fixed frequency carrier signal. Fig. 4(b) shows the block diagram for two-level forced switching using carrier and hysteresis band (h). The carrier signal may be either a sinusoidal, triangular, or

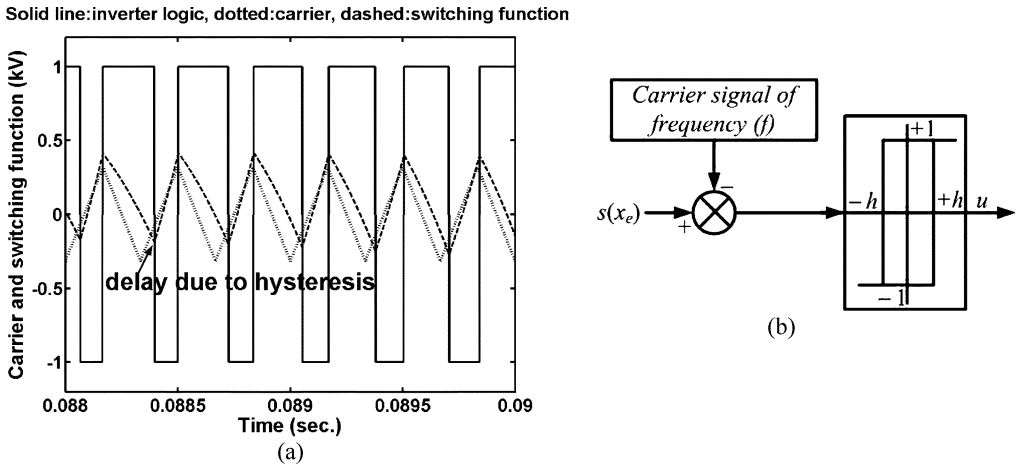

Fig. 4. Carrier-based modulation. (a) Switching function modulation. (b) Block diagram.

three-level disturbance signal. In this method, the sliding mode controller changes the control input at the crossing of the carrier and is delayed by hysteresis band (h), as shown in Fig. 4(a). The technique retains the robustness properties of hysteresis controller while achieving the constant switching frequency. There is, however, a small tracking error depending upon the type and magnitude of carrier signal. Further, there is a minimum magnitude of different carriers at different frequencies to lock the inverter at a fixed carrier frequency. The inverter may enter into complex switching states below this magnitude. Moreover, the tracking error and settling time increase with the increase in the magnitude of the carrier. Therefore, it is essential to use the correct carrier with optimal magnitude.

IV. Frequency-Domain Characterization

In the sliding mode control of power converters, the relay output is implemented as the PWM input to the plant. This is the normal operating mode of the system. Hysteresis is the design parameter that is intentionally introduced with the relay to control the switching frequency of the converters, which depends upon the hysteresis band (h), system parameters, and the feedback gains. Accurate estimation of the switching frequency is the important design requirement for the closed-loop control of power converters. In this section, a frequency-domain approach is proposed to estimate the switching frequency and switching harmonics in the two- and three-level inverter operation for DSTATCOM. Also, the conditions for constant switching frequency operation for carrier-based modulation are determined. Describing function and Tsypkin's methods are the two main tools used to analyze and design the switching operations.

Consider the state-space description of the system of Fig. 1 as obtained in (1) and (2). Let the switching function $s(x_e)$ as defined by (10) consist of two parts, i.e., s_x and s_r such that

$$s_x = k_{e1}x_2 + k_{e2}x_3 \tag{13}$$

$$s_r = k_{e1}x_{2ref} + k_{e2}x_{3\text{ref}} \tag{14}$$

where

$$s(x_e) = s_r - s_x. \tag{15}$$

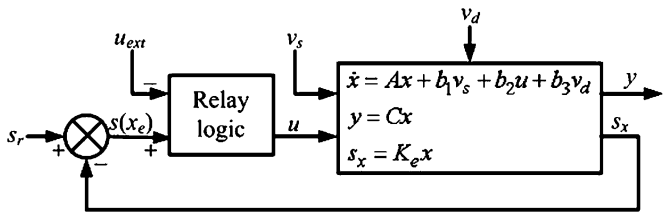

Fig. 5. Sliding-mode-controlled system.

Fig. 5 shows the block diagram of the sliding-mode-controlled system of Fig. 1 with one of the switching schemes discussed in Section III.

A. Steady-State Analysis Using Tsypkin's Method

Both the source voltage v_s and harmonic perturbation v_d due to the nonlinear load are periodic. Then, for an asymptotically stable DSTATCOM converter model (1), let s_s denote the combined steady-state response of feedback function due to the source v_s and v_d. Furthermore, in the steady state, s_r can be subtracted from s_s, yielding net reference s_r' for the DSTATCOM as follows:

$$s_r' = s_r - s_s. \tag{16}$$

Let y_s represent the combined steady-state output due to v_s and v_d. Therefore, the block diagram of Fig. 5 may be redrawn as in Fig. 6, thus eliminating the sources v_s and v_d while retaining the rest of the system.

The describing function method or Tsypkin's method may be used with the model of system shown in Fig. 6. In the describing function approach, it is assumed that the input/output of the nonlinear element is single-frequency sinusoidal input. However, using Tsypkin's method, a more exact analysis may be done by assuming that the input/output of the nonlinear element is a periodic signal [12]. Fig. 7 shows the quasi-linear model for the steady-state analysis of converter switching. For steady-state analysis, the reference s_r' is assumed to be zero, and $N(\mathrm{x})$ represents the describing function of the relay element. The remnant harmonics are added as an external signal at the output of relay. Here, ω_n represents the integer multiple of the switching frequency and γ_n is phase at the nth harmonic

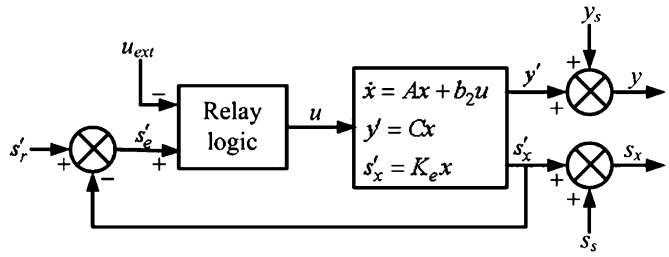

Fig. 6. Decoupling of source voltage and harmonic perturbation.

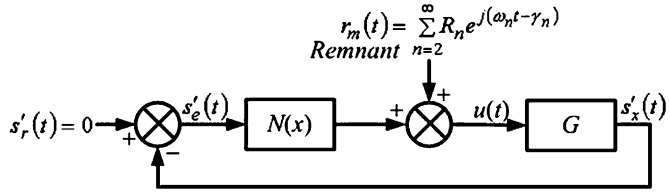

Fig. 7. Quasi-linear model for steady-state analysis.

number. The signals at each point, i.e., $u(t)$, $s'_x(t)$, and $s'_e(t)$, are periodic and may be represented by Fourier series. For self-oscillatory response, the external input to the relay is assumed to be zero, i.e., $u_{\text{ext}} = 0$. The open-loop transfer function $G(s)$ of the quasi-linear model for the DSTATCOM-controlled system is obtained from (1) and (10) as

$$G(s) = K_e(sI - A)^{-1}b_2. \tag{17}$$

Expression for transfer function $G(s)$ is given in Appendix B. The difference between the number of poles and zeros for $G(s)$ is one, and therefore the following will hold:

$$\lim_{s\to\infty} G(s) = 0 \tag{18a}$$

$$\lim_{s\to\infty} sG(s) = \frac{k_1 m V_{dc}}{C_f L_T}. \tag{18b}$$

In the following, Tsypkin's locus is used to determine the frequency and magnitude of oscillation in the switching function. Consider the two-level relay characteristics of Fig. 2(a) with the output level being equal to ± 1. Using Tsypkin's formulation, let us define $T(\omega)$ as [12]

$$\text{Re}\{T(\omega)\} = \frac{4}{\pi}\sum_{n=1(2)}^{\infty} \text{Re}\{G(jn\omega)\} - \frac{1}{\omega}\lim_{s\to\infty} sG(s) \tag{19}$$

$$\text{Im}\{T(\omega)\} = \frac{4}{\pi}\sum_{n=1(2)}^{\infty} \frac{1}{n}\text{Im}\{G(jn\omega)\}. \tag{20}$$

Note that only the odd harmonics are considered in (19) and (20) since the two-level relay characteristic is skew-symmetric. The solution of limit cycle is given by [12]

$$\text{Re}\{T(\omega)\} < 0 \tag{21}$$

$$\text{Im}\{T(\omega)\} = -h. \tag{22}$$

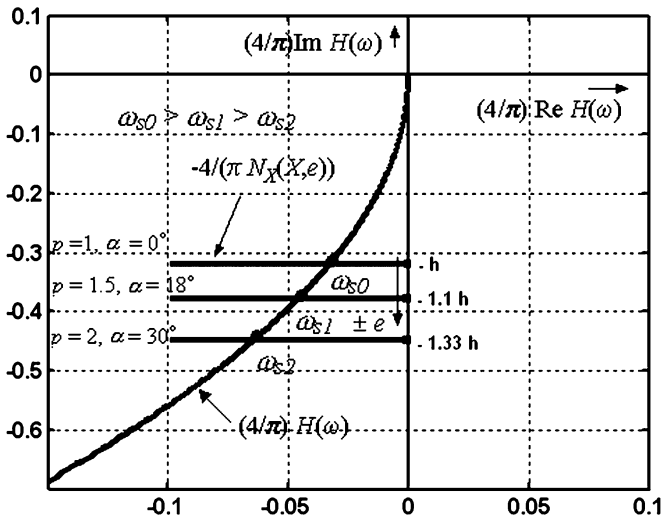

Fig. 8. Tsypkin's locus and describing function.

Now let us define the harmonic summation in (19) and (20) as follows:

$$\sum_{n=1(2)}^{\infty} \text{Re}\{G(jn\omega)\} = \text{Re}\{H(\omega)\} \tag{23}$$

$$\sum_{n=1(2)}^{\infty} \frac{1}{n}\text{Im}\{G(jn\omega)\} = \text{Im}\{H(\omega)\}. \tag{24}$$

The plot of $(4/\pi)\text{Re}\{H(\omega)\}$ versus $(4/\pi)\text{Im}\{H(\omega)\}$ with varying frequency ω is defined here as the Tsypkin's locus. Using (19)-(24), the following equation may be written as:

$$h = -\frac{4}{\pi}\text{Im}\{H(\omega)\} \tag{25}$$

$$\frac{4}{\pi}\text{Re}\{H(\omega)\} < \frac{1}{\omega}\frac{k_1 m V_{dc}}{C_f L_T}. \tag{26}$$

The conditions (25) and (26) can be checked graphically, and the frequency of self-oscillation that is the same as the switching frequency of the inverter may be determined as shown in Fig. 8. Furthermore, the switching frequency ω_s determined is stable if it satisfies the following condition:

$$\frac{d\text{Im}\{T(\omega_s)\}}{d\omega_s} > 0. \tag{27}$$

The magnitude of switching harmonics in the terminal voltage may be calculated from the frequency-domain transfer function of the model in Fig. 6 at the switching frequency ω_s with (2) as its output equation.

Property 1: For a two-level inverter, the switching conditions are variable over one fundamental cycle of switching function at power frequency.

Proof: Let us first assume that the feedback gains in (10) are chosen such that the system has sufficient stability margins. Under this condition, the two-level hysteresis nonlinearity can safely be approximated by a gain through an incremental-input describing function. Assume that the closed-loop frequency response of the system has small error from its unity gain and zero-phase condition at the power frequency. The error

increases for higher order harmonics. Under this condition, the switching function input to the nonlinearity consists of limit cycle at switching frequency and a small error component at power frequency carrying higher order harmonics. Since the switching component is very fast as compared to the low-frequency error, the input to the nonlinearity at any time instant is assumed to be a limit cycle with a bias. Let X be the amplitude of the limit cycle and Y be the constant bias. Then, the signal dual-input describing function is obtained as follows [13]:

$$N_X(X,Y) = \frac{2}{\pi X}\left(e^{-j\sin^{-1}\left(\frac{h-Y}{X}\right)} + e^{-j\sin^{-1}\left(\frac{h+Y}{X}\right)}\right) \quad (28)$$

$$N_Y(X,Y) = \frac{1}{\pi Y}\left(\sin^{-1}\left(\frac{h+Y}{X}\right) - \sin^{-1}\left(\frac{h-Y}{X}\right)\right). \quad (29)$$

The magnitude of bias Y varies between $-e$ to $+e$ through zero along the one cycle of fundamental frequency of the switching function. Consider the positive bias of $+e$ input to the relay of Fig. 2(a). The net input to the relay will now cause more switching duration for $+1$ level than for -1 level. Let the two levels of voltage be in the ratio of p: 1. The average output of the relay is given by $p/(p+1)-1/(p+1) = (p-1)/(p+1)$. Now for $+e$ bias the output of relay may be calculated from incremental input describing function (29) and equated as

$$\frac{1}{\pi}\left(\sin^{-1}\frac{h+e}{X} - \sin^{-1}\frac{h-e}{X}\right) = \frac{p-1}{p+1} \quad (30)$$

Let us define, $\theta_1 = \sin^{-1}(h+e)/X$ *and* $\theta_2 = \sin^{-1}(h-e)/X$. Then, from (30), we obtain

$$\theta_1 - \theta_2 = \pi\frac{p-1}{p+1} = 2\alpha(\text{say}). \quad (31)$$

Also, from (28), we obtain

$$N_X(X,e) = \frac{4}{\pi X}\left(\cos\alpha\cos\frac{\theta_1+\theta_2}{2} - j\frac{2h}{X}\right). \quad (32)$$

Substituting $\cos((\theta_1+\theta_2)/2) = e/(X\sin\alpha)$ and $e\cot\alpha = (X^2\cos^2\alpha - jh^2)^{1/2}$ into (32), the following is obtained:

$$N_X(X,e) = \frac{4}{\pi X^2}\left[(X^2\cos^2\alpha - h^2)^{\frac{1}{2}} - jh\right]. \quad (33)$$

Inverting (33) yields

$$-\frac{1}{N_X(X,e)} = -\frac{\pi}{4\cos^2\alpha}\left[(X^2\cos^2\alpha - h^2)^{\frac{1}{2}} + jh\right]. \quad (34)$$

Note from (34) that the imaginary part is independent of X and the expression for switching frequency may be obtained from (22) by replacing h by $h/\cos^2\alpha$ as

$$\frac{h}{\cos^2\alpha} = -\frac{4}{\pi}\text{Im}\left\{H(\omega)\right\}. \quad (35)$$

Comparing (35) with (25), it is clear that bias $+e$ has the effect of increase in effective hysteresis band and hence reduction in switching frequency. Fig. 8 illustrates this phenomenon for few values of p and α. Also, note from (34) and (35) that the negative bias, i.e., $-e$ has the same effect as positive bias. The only difference is that the switch will remain in the -1 level for a longer duration than will the $+1$ level. Furthermore, the limit cycle magnitude and switching harmonics also increase with the increase in bias on either side. This is due to a reduction in attenuation at lower frequencies. Low-frequency bias may be extracted from the switching function using the low-pass filters.

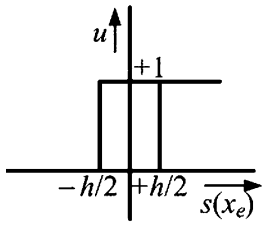

Fig. 9. Asymmetrical relay logic.

Property 2: Switching frequency of the three-level inverter is the same as that of the two-level inverter.

Proof: Consider the three-level-inverter input–output characteristic as shown in Fig. 3(a). First and third quadrants operate for positive and negative half cycle of switching function, respectively. The equivalent characteristic for the half cycle of switching function may be drawn in Fig. 9. The describing function of asymmetrical relay of Fig. 9 is obtained from [13] as

$$N(X) = \frac{1}{\pi X^2}(\sqrt{4X^2 - h^2} - jh). \quad (36)$$

Inverting (36), the following expression is obtained:

$$-\frac{1}{N(X)} = -\frac{\pi}{4}\left(\sqrt{(2X)^2 - h^2} + jh\right). \quad (37)$$

The imaginary part of (37) is the same as that for the two-level inverter, therefore, this leads to the same condition of (25) for switching in the two-level inverter except that the limit cycle is halved at the same switching frequency. Also, since the switching input toggles between $+1$ or -1 and 0, the switching harmonics in output are also halved for the same switching frequency. It is already stated in Section III that the switching losses are also halved approximately.

Remark 1: Since the nonlinearity is not skew-symmetrical for three-level logic, the Tsypkin's formulation of (19) and (20) contains even harmonics terms also. Therefore, the Tsypkin's locus intersects the same $-4/(\pi N(x))$ straight line at a higher frequency as compared to the two-level inverter. Therefore, the switching frequency of the three-level inverter is slightly higher as compared to the two-level inverter.

B. Variable Hysteresis Band

A sensitivity-based approach is proposed here to achieve the constant switching frequency upon the parameter variation. The relation for hysteresis band h for the constant switching frequency ω_s may be determined from (25). The function $\text{Im}\{H(\omega_s)\}$ is a function of DSTATCOM-controlled system parameters and feedback gains. Let P be the vector of parameters, i.e., $P = [p_1\ p_2 \ldots\ p_n]$, and the following parameter function is defined at the constant switching frequency ω_s as:

$$f(P,\omega_s) = \left(\frac{4}{\pi}\right)\text{Im}\left\{H(\omega_s)\right\}. \quad (38)$$

The following cumulative sensitivity is defined upon the variation of parameters:

$$\Delta f(P,\omega_s) = \sum_i \Delta f_i(P,\omega_s) = \sum_i\left(\frac{\partial f(P,\omega_s)}{\partial p_i}\Delta p_i\right). \quad (39)$$

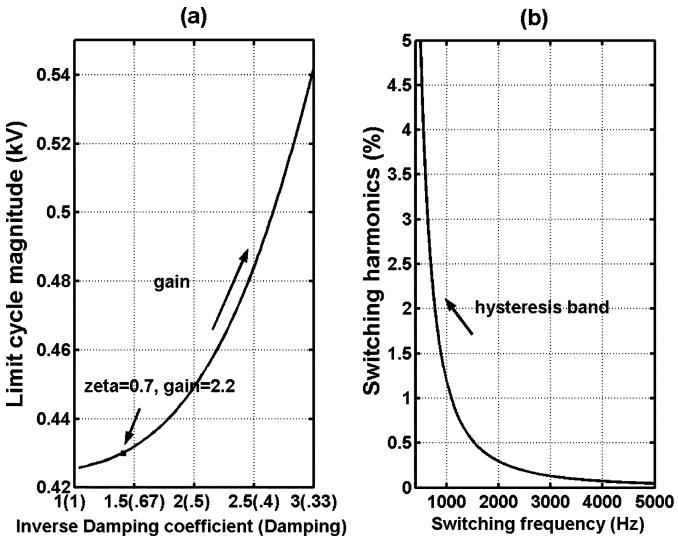

Fig. 10. (a) Variation of gain. (b) Variation of hysteresis band.

The change in hysteresis band Δh required to maintain the constant switching frequency ω_s upon the variation of vector of parameter P is given as

$$\Delta h = -\Delta f(P, \omega_s). \tag{40}$$

However, the determination of function Δp_i in (39) requires some means to monitor the variations of the parameters online.

Example 1: Consider the DSTATCOM-compensated single-phase distribution system shown in Fig. 1 and the parameters given in Appendix A. The nonlinear load consists of a full-bridge diode rectifier with equivalent dc side resistance of 100 Ω and smoothing dc capacitor of 500 μF. The input impedance is $R_l = 1.0\ \Omega$ and $L_l = 0.12$ mH. This also includes leakage impedance of any step-down transformer that may be connected to drive the load. The source voltage has a trapezoidal waveform with a total harmonic distortion (THD) of 5.63% and the total rms voltage of 6.0 kV. The uncompensated PCC voltage drops down to 5 kV (rms) and waveform is distorted with a THD of 21%. It is desired to design a sliding-mode-controlled switching of the inverter such that the PCC voltage v_t has the rms value of 6.35 kV and lags the source voltage by 20°. All of the simulation results in this paper are performed in a PSCAD/EMTDC simulation package (version 3.0.7). The switching element comprises an IGBT with an antiparallel diode.

The following reference values are calculated for a frequency of $f = 50$ Hz:

$$v_t^*(t) = 8.9803\sin(100\pi t - 20^\circ)\text{kV}$$
$$\dot{v}_t^*(t) = 2821.2\sin(100\pi t + 70^\circ)\text{kV/s}.$$

The two design parameters of the quasi-sliding mode, i.e., time constant $(T = k_1/k_2)$ and hysteresis band h are the first to be determined. The time constant has an effect on transient specification and magnitude of limit cycle, whereas the hysteresis band has a conflicting requirement on switching frequency and switching harmonics. For the determination of the time constant, the gain k_1 is fixed to 0.001 s and k_2 is varied to check the damping (ξ) and limit cycle magnitude (X). Fig. 10(a) shows the variation of the inverse of the damping factor $(1/\xi)$ and limit cycle (X) with k_2 varying from 1.1 to 20. Below $k_2 = 1.1$, the system is over-damped. It is observed from the figure that limit cycle magnitude increases and damping factor decreases with the increase of gain k_2. Therefore, this gain should be kept small. The damping factor $\xi = 0.7$ is selected for minimum settling time, and the gain calculated at this value of damping factor is $k_2 = 2.2$ and time constant $T = 0.45$ ms. The above results are under the assumption of unity gain of hysteresis nonlinearity. However, the gain of hysteresis decreases with the increase in the magnitude of the limit cycle. Fig. 10(b) shows the variation of switching frequency and switching harmonics in the terminal voltage with the variation of hysteresis band h. The feasible sets of values are the points lying on the curve. Clearly, a smaller hysteresis band will lead to a high switching frequency and smaller switching harmonics. However, the switching losses increase proportionally with the switching frequency. Hence, the switching frequency has to be limited to a small value depending upon the rating of the semiconductor devices. Let the operating switching frequency of 3 kHz be chosen as a compromise between switching losses and switching harmonics. The terminal voltage v_t and capacitor current i_{cf} being local quantities are measurable and available for feedback. Reference for $i_{\rm cf}$ may be calculated by multiplying C_f with $\dot{v}_t^*$. Therefore, for the evaluation of switching function (10), the feedback gain may be written as $k_1 = 0.001$ s and $k_2 = 2.2$. The transfer function $G(s)$ is determined from the expression given in Appendix B. Tsypkin's locus is plotted (see Fig. 8) and the condition for switching at 3 kHz is obtained. The expression $(4/\pi)\text{Re}\{H(\omega)\}$ is always negative and the expression $(k_1 m V_{dc}/C_f L_T)$ is positive for positive gain k_1 and the realistic values of parameters, therefore, (26) is satisfied for all positive frequencies. Furthermore, $h = 0.3368kV$ obtained from (25) for the switching frequency of 3 kHz and satisfies (27), which leads to the stable switching condition at this frequency. Fig. 11 shows the spectrum of source voltage, uncompensated PCC voltage and compensated PCC voltage. The PCC controlled voltage has an rms value close to 6.35 kV and the THD reduces to 0.5%. The observed switching frequency is variable with the maximum of 3.0 kHz and a minimum of 2.0 kHz. The minimum switching harmonics observed in terminal voltage is 0.16% and the error in tracking terminal voltage is 16.0 V (rms). The voltage tracking error plot and the spectrum of the switching input u is shown at the end of Section IV-C.

It may be noted that, if the analysis is done using the describing function method, the estimated hysteresis band is $h =$ 0.2839 kV, and this leads to the maximum switching frequency of 3.5 kHz. The estimation is not correct because of the presence of a nonsinusoidal limit cycle.

The three-level inverter is used. A small dead zone of 0.1 kV is introduced as discussed in Section III. The switching frequency is near 3 kHz and is slightly higher as compared to its two-level counterpart. The switching harmonics are 0.08%, which is half of the two-level modulation. However, the tracking error is 115.0 V (rms) which is higher than that for the two-level modulation. The THD of PCC voltage is almost the same as that of Fig. 11(c). The voltage tracking error plot and the spectrum of the switching input for three-level modulation is shown at the end of Section IV-C.

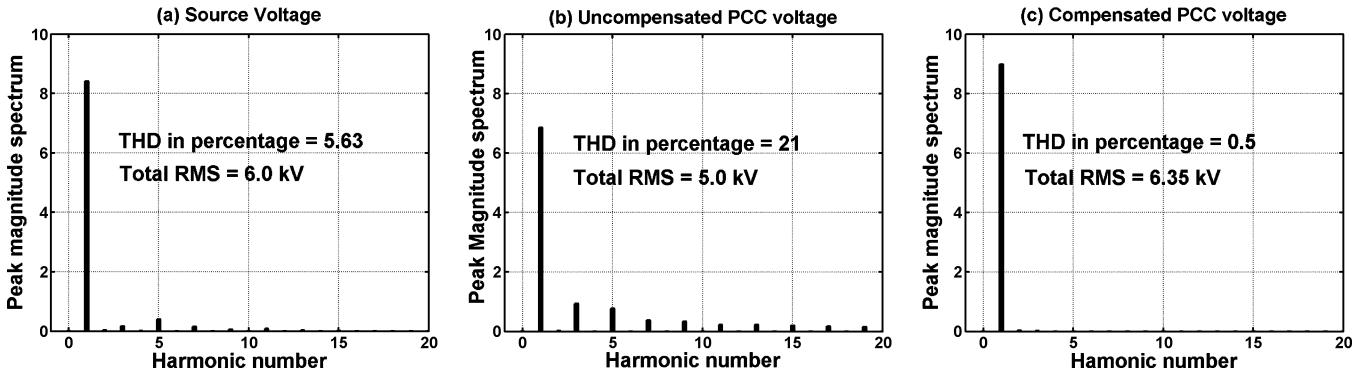

Fig. 11. Peak magnitude spectrum, base frequency 50 Hz. (a) Source voltage. (b) Uncompensated PCC voltage. (c) Compensated PCC voltage.

To verify the variable hysteresis band algorithm, a slowly varying dc link voltage is applied across the transformer. The voltage varies between 400–600 V continuously for the two-level modulation scheme. Using a constant hysteresis band of 0.3368 kV, the maximum switching frequency varies between 2.5–3.5 kHz. In order to obtain a constant switching frequency using (40), the sensitivity function $\partial f/\partial V_{dc} = -0.6725/kV$ is calculated at the switching frequency of 3 kHz. The variable hysteresis band algorithm of Section IV-B is implemented, and a constant maximum switching frequency of 3 kHz is obtained with the hysteresis band varying between 0.269–0.404 kV. The dc link voltage is fed back continuously for the calculation of the change in hysteresis band.

C. Forced Switching

Consider the external periodic carrier signal $u_{\rm ext}$ of frequency $\omega_{\rm ext}$ in Fig. 6. It is desired to determine the minimum magnitude of the carrier that will force the switching of the inverter at the external frequency $\omega_{\rm ext}$. The input to the relay is given by

$$u_{\rm relay}(t) = s'(x_e) - u_{\rm ext}(t). \tag{41}$$

At synchronization, the following conditions are satisfied [12]:

$$\left.\begin{aligned} u_{\rm relay}\left(\tfrac{\pi^-}{\omega}\right) &= -h \\ \dot{u}_{\rm relay}\left(\tfrac{\pi^-}{\omega}\right) &< 0 \end{aligned}\right\}. \tag{42}$$

For sinusoidal carrier signal $u_{\rm ext}(t) = R\sin(\omega_{\rm ext}t + \varphi)$, the condition for forced switching at predefined frequency $\omega_{\rm ext}$ is obtained as

$$R\sin\varphi + \frac{4}{\pi}{\rm Im}\left[H(\omega_{\rm ext})\right] = -h \tag{43}$$

$$R\cos\varphi + \frac{4}{\pi}{\rm Re}\left[H(\omega_{\rm ext})\right] < \frac{k_1 m V_{dc}}{\omega_{\rm ext} C_f L_T}. \tag{44}$$

The graphical technique to find out the solution for (43) is shown in Fig. 12. The minimum amplitude $R_{\rm min}$ required to produce the forced switching at $\omega_{\rm ext}$ is the radius of the circle drawn from the point of $\omega_{\rm ext}$ at $(4/\pi)H(\omega)$ locus, which just touches the inverse describing function of two-level relay $-4/(\pi N(x))$, which is a straight line intersecting the imaginary axis at $(-h)$ and parallel to the real axis. For the input magnitudes, more than $R_{\rm min}$, there is always two solutions A and B with phase angles of φ_A and φ_B, respectively. However, it is shown in [12] that the solution of A is stable whereas B is unstable. Condition (44) can easily be checked analytically.

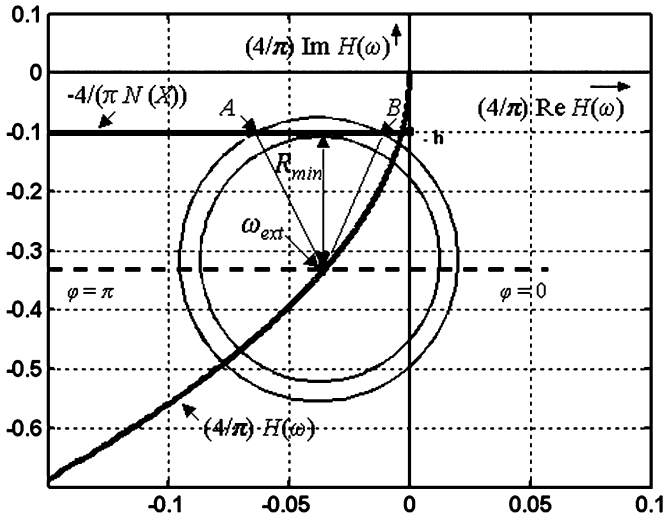

Fig. 12. Carrier magnitude determination.

If the external periodic signal is other than sinusoidal, such as triangular or pulsed, then, for the approximate analysis, the fundamental component of the periodic signal may be considered in (43) and (44). Since the magnitude of the higher order odd-harmonic components of the periodic signal are significantly small, they cannot cause the forced harmonic switching.

Theorem 1: The minimum magnitude of carrier signal required for robust forced switching is given by

$$R_{\rm min} = -{\rm Im}\left[T(\omega_{\rm ext})\right] - \min\left\{0, \sum_i \Delta f_i(P, \omega_{\rm ext})\right\} - h. \tag{45}$$

Proof: It is assumed that the self-oscillation frequency is higher than the desired forced external frequency at the chosen hysteresis band (h). With reference to Fig. 12, $R_{\rm min}$ is the radius of the circle to which the straight line $-4/(\pi N(x))$ is a tangent. Clearly, $\varphi = 90^\circ$ and $R\sin\varphi = R_{\rm min}$. Therefore, the left-hand side (LHS) of (45) will be followed and ${\rm Im}[T(\omega_{\rm ext})] = (4/\pi){\rm Im}[H(\omega_{\rm ext})]$. For robust switching, it is desired that the inverter must be synchronized with the external input frequency $\omega_{\rm ext}$ even with the uncertainty or variation of parameters. As has been shown in Fig. 12, an input magnitude greater than $R_{\rm min}$ will keep the synchronization. Therefore, the positive cumulative sensitivity $\Delta f(P, \omega_{\rm ext})$ in

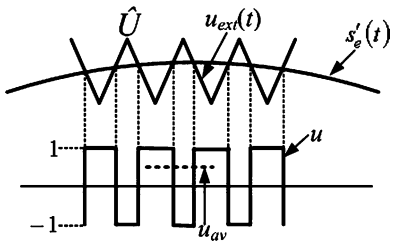

Fig. 13. Switching function modulation.

(39) will not affect the forced oscillation condition. However, if the cumulative sensitivity is negative the choice of $R_{\min}$ is crucial. Small choice of $R_{\min}$ may just pull down the circle to touch the straight line $-4/(\pi N(x))$. Therefore, it is required to determine the net change upon the variation of all of the parameters. Furthermore, this summation is compared with zero to avoid any positive cumulative sensitivity.

Remark 2: Note that, in the literature [5], [9], [10], a point of caution is mentioned that the amplitude of the carrier should not be less than the oscillating magnitude of the switching function and the slope of the control signal should not increase the slope of the carrier. However, under closed-loop operation, it is difficult to test this condition *a priori*. The above theorem is useful to ascertain the condition of constant switching frequency of the inverter.

Property 3: Steady-state error in the switching function increases with the increase in the magnitude of the carrier signal.

Proof: The property is proved for more commonly used triangular carrier in power-converter applications. Let us ignore the oscillating limit cycle component in the switching error function $s'_e(t)$ of Fig. 7. As assumed in Property 1, there will be a steady-state error at the power frequency and its harmonics. Therefore, the input to the relay is considered as the comparison of the low-frequency signal and the high-frequency carrier. Refer to Fig. 13 where the switching error function $s'_e(t)$ is compared with an external carrier signal $u_{\text{ext}}(t)$ and fed to the relay with a small hysteresis width. The carrier frequency is considered to be significantly high so that the switching function $s'_e(t)$ is considered to be constant for one switching time period. From Fig. 13, it can be shown that the instantaneous average output voltage (u_{av}) is proportional to the ratio of control voltage $s'_e(t)$ and peak of triangular voltage $\hat{U}$ [19], which is given by

$$u_{\text{av}} = k_M \left(\frac{s'_e(t)}{\hat{U}} \right) = k_p s'_e(t) \tag{46}$$

where k_M is the constant that depends upon the logic levels and equal to unity for bipolar modulation. The expression $k_p = (k_M/\hat{U})$ in (46) may be considered as the gain in the feed-forward path. The input to the system $u(t)$ is the periodic signal with the fundamental frequency of 50 Hz. From Fig. 6, the sinusoidal transfer function for switching error function $S'_e(jw)$ may be written as

$$S'_e(jw) = \frac{S'_r(jw)}{1 + k_p G(jw)}. \tag{47}$$

Clearly, if the amplitude of the carrier signal increases, then the system gain (k_p) decreases. Since the bandwidth of the system is significantly high as compared to the power frequency, the steady-state magnitude in the frequency response of the switching error function increases with the increase in the amplitude of the carrier signal at low frequency such as at power frequency. This also in effect increases the tracking error in the terminal voltage.

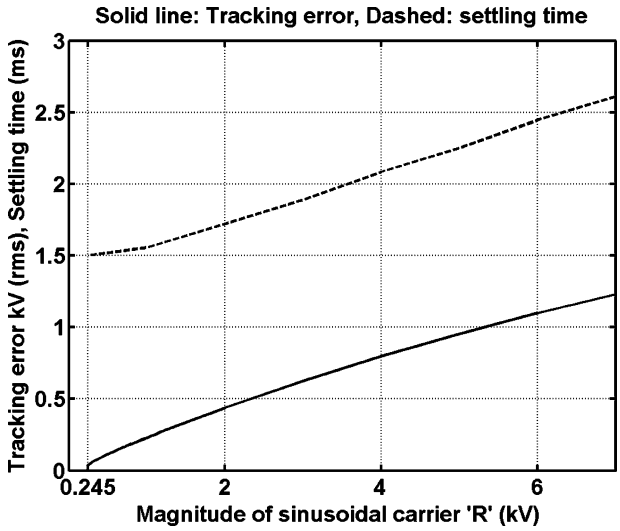

Fig. 14. Variation of tracking error and settling time with carrier magnitude.

Example 2: Consider the system parameters, nonlinear load, and time constant, as discussed in Example 1. In this example, it is illustrated that the constant switching frequency of 3 kHz is achieved using carrier-based modulation.

Carrier modulation allows the choice of a small hysteresis band. However, a very small hysteresis band should be avoided as it may lead to multiple crossing of the carrier and, therefore, the chattering. Let us consider $h = 0.1$ kV. Using the condition (43), the minimum magnitude of sinusoidal carrier required is 0.2368 kV (see Fig. 12) and, for a triangular carrier, this magnitude is 0.2921 kV with same the fundamental value as that of the sinusoidal carrier. The condition (44) is also required to be satisfied as in Example 1. Since the added term $R\cos\varphi$ is always negative for point A in Fig. 12, therefore (44) is satisfied. The actual minimum magnitudes observed from simulation are 0.245 and 0.317 kV for sinusoidal and triangular carriers, respectively. The cause of small error is due to the finite termination of Tsypkin's locus at the 11th harmonic in the estimation of switching frequency. The voltage tracking error and the spectrum of the switching input using sinusoidal carrier is shown at the end of this section. The tracking error is 35 V (rms) and the switching frequency is exactly 3 kHz. The THD of PCC voltage is further improved to 0.1% than that of Fig.11 (c) due to absence of any low frequency switching as in the case of two-level modulation.Fig. 14 shows the variation of the tracking error and settling time with the magnitude of the carrier. It is clear from Fig. 14 that, with the increase in carrier magnitude, both transient and steady-state characteristic deteriorates. Therefore, one must determine the minimum magnitude of the carrier to synchronize the switching at carrier frequency.

Example 3: In this example, the load bus voltage of the three-phase radial distribution is controlled using the DSTATCOM. The configuration of the DSTATCOM as in [15] is considered

where three separate voltage source inverters are supplied from a common dc source. Both feeder and load input impedance are unbalanced with following parameters:

$$\begin{aligned} R_{sa}, L_{sa} &= 6.05\ \Omega,\ 0.1155\ \text{H} \\ R_{sb}, L_{sb} &= 6.05\ \Omega,\ 0.0955\ \text{H} \\ R_{sc}, L_{sc} &= 6.05\ \Omega,\ 0.2155\ \text{H} \\ R_{la}, L_{la} &= 0.1\ \Omega,\ 0.05\ \text{H} \\ R_{lb}, L_{lb} &= 1.0\ \Omega,\ 0.12\ \text{H} \\ R_{lc}, L_{lc} &= 2.0\ \Omega,\ 0.2\ \text{H}. \end{aligned}$$

The supply is also unbalanced with $V_{sa} = 6.0$ kV (rms), $V_{sb} = 8.5$ kV (rms), and $V_{sc} = 5.0$ kV (rms). The shape of the source voltage is trapezoidal, as discussed in Example 1. Furthermore, the dc voltage may vary from 500 to 520 V and the measured value of the capacitance of phase a has an error of 5%. The nonlinear load consists of a three-phase diode rectifier with an equivalent dc side resistance of 30 Ω and smoothing dc capacitor of 500 μF. The remainder of the parameters and design specifications are same as in Example 2. Under these conditions, it is desired to control the PCC load bus voltage to balanced 6.35 kV (rms) using carrier-based modulation with 3 kHz of switching frequency. A sliding mode controller is designed as illustrated in Example 2, however, Theorem 1 is used to determine the minimum magnitude for robust switching. A common minimum magnitude is determined for all three phases considering the worst possible cumulative sensitivity. The following sensitivity functions are calculated numerically:

$$\begin{aligned} S_{\text{dcvolt}} &= -0.6725/\text{kV} \\ S_{\text{filtcapt}} &= 0.0044/\mu\text{F} \\ S_{\text{shuntInd}} &= 0.009\,02/\text{mH} \\ S_{\text{shuntRes}} &= -0.000\,623/\Omega \\ S_{\text{feedInd}} &= 7.54\times10^{-7}/\text{mH} \\ S_{\text{feedRes}} &= -8.28\times10^{-6}/\Omega \\ S_{\text{loadInd}} &= 6.89\times10^{-7}/\text{mH} \\ S_{\text{loadRes}} &= -6.014\times10^{-8}/\Omega \end{aligned}$$

where $S_i = \partial f_i/\partial p_i$. The cumulative sensitivity Δf is calculated as

$$\begin{aligned} \Delta f = [&(-0.6725)\times(0.02) + (0.0044)\times(-3.887) \\ &+ (7.54\times10^{-7})\times(-20.0) + (6.89\times10^{-7}) \\ &\times(-70.0) + (-6.014\times10^{-8})\times(1.0)] \\ = &-0.0306\ \text{kV}. \end{aligned}$$

Therefore, from Theorem 1

$$R_{\min}(\text{sin}) = (0.345 + 0.0306 - 0.1) = 0.2756\ \text{kV}$$

and

$$\begin{aligned} R\text{min}(\text{tri}) &= \left(0.417 + \left(\frac{\pi^2}{8}\right)\times 0.0306 - 0.1\right) \\ &= 0.3548\ \text{kV}. \end{aligned}$$

The error due to Tsypkin's locus is accounted for while calculating the new magnitude of carrier. Rounding off the small fractional part and taking $R_{\min}(\text{tri}) = 0.36$ kV, the simulation is carried out. Fig. 15 shows the controlled three-phase PCC voltage with constant switching frequency of 3 kHz. It is observed that even a small magnitude lesser than the calculated above pushes the system into harmonic switching. Fig. 18(b) shows the presence of harmonic switching in phase a with $R_{\min}(\text{tri}) = 0.35$ kV. Therefore, in practice, a higher value of carrier from its critical value must be used. Fig. 16 (a) and (b) shows the voltage-tracking error for two-level and three-level modulation respectively as discussed in Example 1. Fig. 16 (c) shows the voltage tracking error for the carrier based modulation discussed in Example 2. Fig. 17 shows the magnitude spectrum of the switching input u for the three modulation schemes.

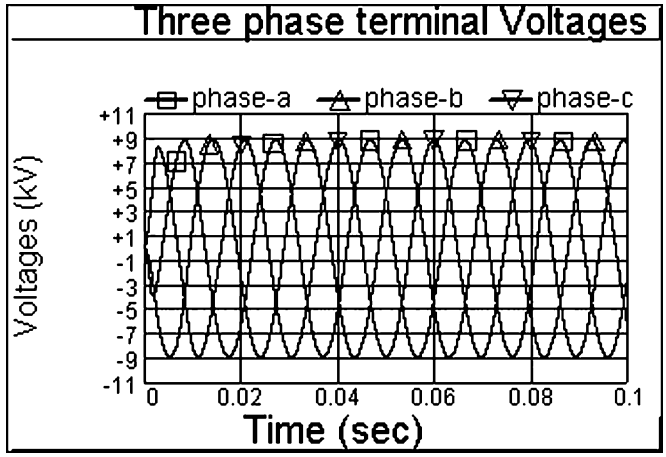

Fig. 15. Three-phase terminal voltage response using a triangular carrier.

D. Border Collision Bifurcation

The border of bifurcation that pushes the system into high-frequency switching must be avoided in order to obtain smooth operation of the inverter with the carrier-based modulation. The design parameters, i.e., hysteresis band and carrier magnitude, must be chosen carefully to avoid chattering and harmonic switching, respectively.

1) Chattering: As has been mentioned in Example 2, an excessively small hysteresis band may cause multiple crossing of the carrier and lead to chattering. With $h = 0.01$ kV, the minimum magnitude required of a triangular carrier is 0.4031 kV. Fig. 18(a) shows the chattering in switching even with 0.45-kV magnitude of the triangular carrier. Therefore, the hysteresis band should not approach zero.

2) Harmonic Switching: Carrier magnitude less than the minimum required from Theorem 1 leads to high-frequency oscillation known as harmonic switching shown in Fig. 18(b). A complex switching is observed near critical magnitude. Therefore, the carrier magnitude must be considerably higher than the minimum calculated in order to avoid any harmonic switching due to parameter variations and uncertainty.

V. Experimental Result

A laboratory scaled model of the single-phase DSTATCOM of Fig. 1 is implemented with the system parameters given in

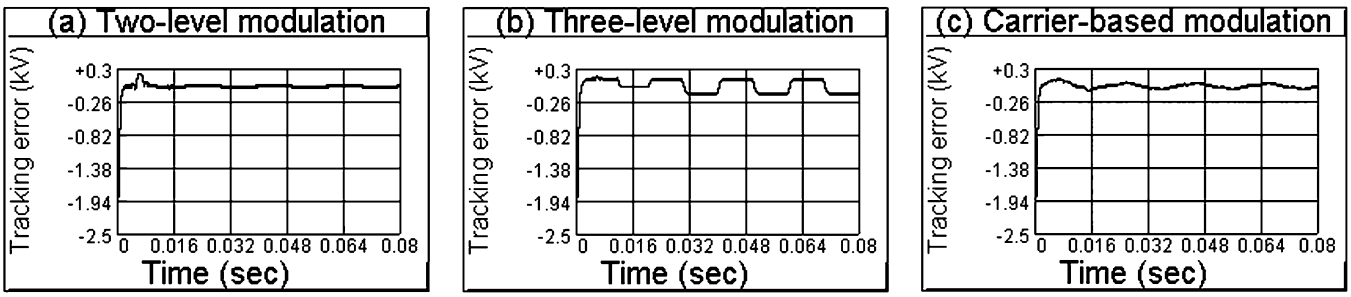

Fig. 16. Voltage tracking error. (a) Two-level, (b) three-level, and (c) carrier-based modulation.

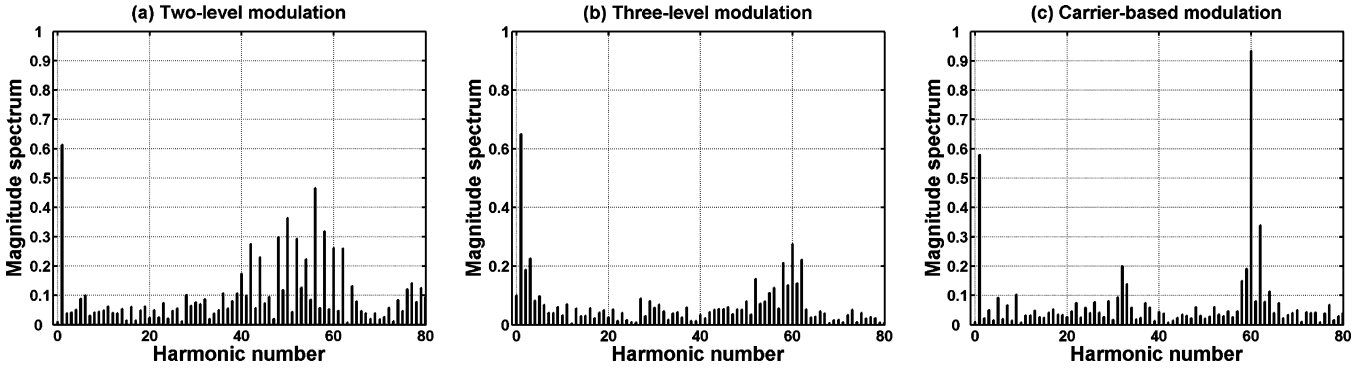

Fig. 17. Magnitude spectrum of switching input, with a base frequency of 50 Hz. (a) Two-level, (b) three-level, and (c) carrier-based modulation.

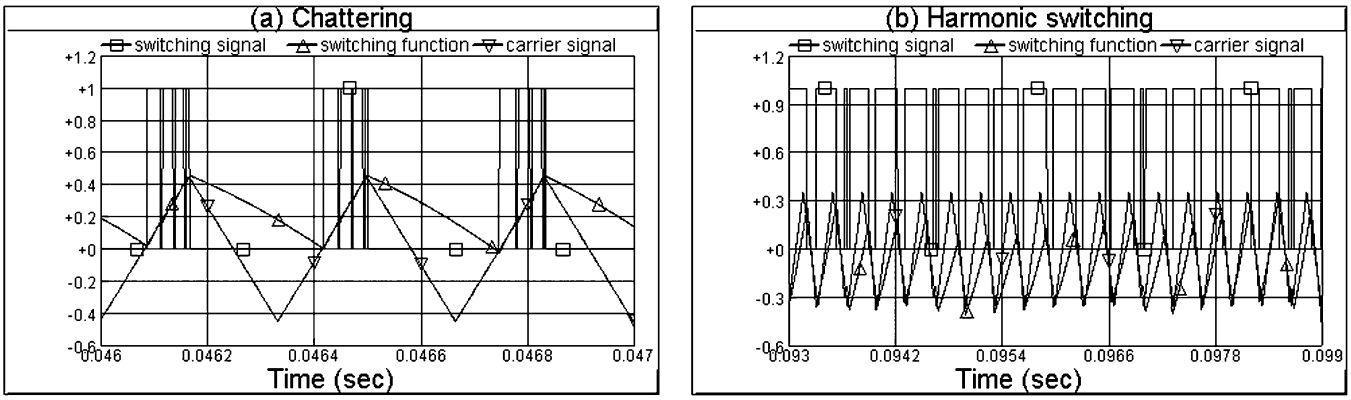

Fig. 18. Border collision bifurcation. (a) Chattering. (b) Harmonic switching.

Appendix A. However, the voltage levels are reduced as compared to kilovolts given in Appendix A. Since the voltage levels are small, the output of the inverter is directly interfaced to the PCC through the inductor with the dc link voltage equivalent to $mV_{\rm dc} = 125.0$ V. The source voltage V_s has the trapezoidal waveform of the same spectrum as shown in Fig. 11(a) with a magnitude of 60.0 V(rms) The inductance L_T is the same as that of the equivalent leakage inductance of the transformer, i.e., 38.5 mH. The nonlinear load connected is a diode bridge rectifier with the parameters the same as those considered in Example 1. The H-bridge of the inverter is implemented using two arms of a Mitsubishi Intelligent Power Module (IPM) PM50CSD120. The sliding mode control and various switching algorithm proposed in this paper are implemented using National Instruments (NI) LabVIEW FPGA module programming that runs on reconfigurable I/O NI 7831R embedded in a remote PXI 8186 processor. The terminal voltage v_t and the filter capacitor current $i_{\rm cf}$ are fed back using the voltage and current transducers LEM LV 25-P and LA 55-P, respectively. They are then fed into the processor through an analog-to-digital (A/D) converter of NI 7831R. The switching logic signals are given to the inverter through the digital output lines of NI 7831R that have the TTL compatible voltage levels of 0.0 and 3.3 V. The switching signals provide the gating signal to the IGBTs of IPM through the isolation and dead-time circuit. The digital processor samples the signal at a rate of 15 μs. Reference signals $v_{\rm tref}$ and $i_{\rm cfref}$ are generated using the software-based phase-locked loop implemented using LabVIEW programming. A discrete FIR low-pass filter is connected across the measured variables v_t and $i_{\rm cf}$ with a cutoff frequency (1/10) of the sampling period to clean up the variables from high-frequency noise signals.

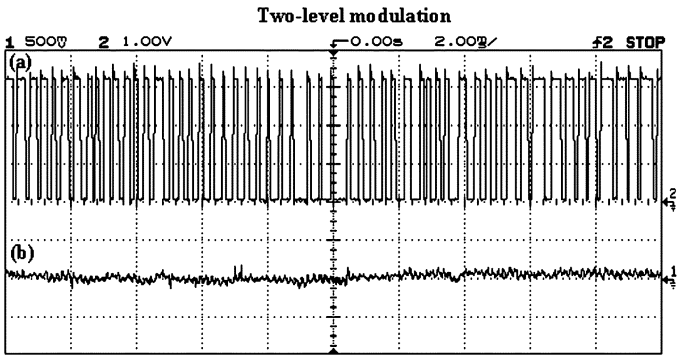

Fig. 19. Two-level modulation. (a) Switching input. (b) Tracking error.

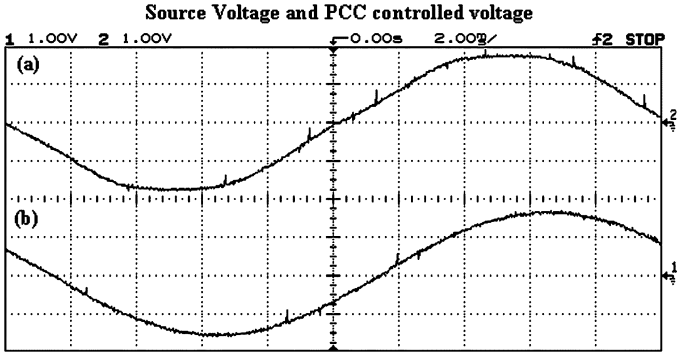

Fig. 20. (a) Source voltage. (b) Controlled voltage.

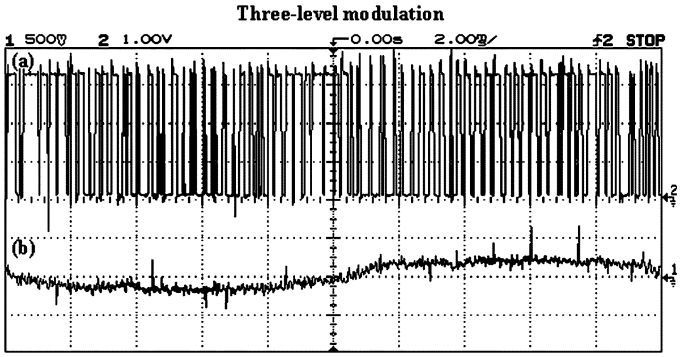

Fig. 21. Three-level modulation. (a) Gating signal for switch S_{w2}. (b) Tracking error.

The load bus voltage is controlled using sliding mode control with the feedback gains as calculated in Example 1. All of the results of previous sections may be scaled by a factor of (1/100). In order to obtain the maximum switching frequency of 3 kHz with two-level modulation, the calculated value of hysteresis band $h = 3.368$ V is used. The required maximum switching frequency of around 3 kHz is obtained as shown by the switching signal for the switch S_{w2} in Fig. 19(a). The steady-state tracking error in the terminal voltage is shown in Fig. 19(b). The tracking error is computed in the processor and is converted into an analog signal through a digital-to-analog (D/A) converter for plotting and shown to the scale of one tenth of the actual value. Fig. 20(a) and (b) shows the waveforms of the source voltage and PCC-controlled voltage, respectively, at the reduced scale of 1/50 of the actual values. Similarly, the

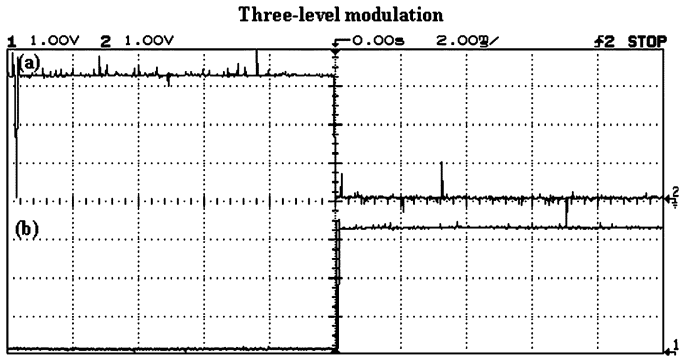

Fig. 22. Three-level modulation. Gating signal for (a) switch S_{w1} and (b) switch S_{w4}.

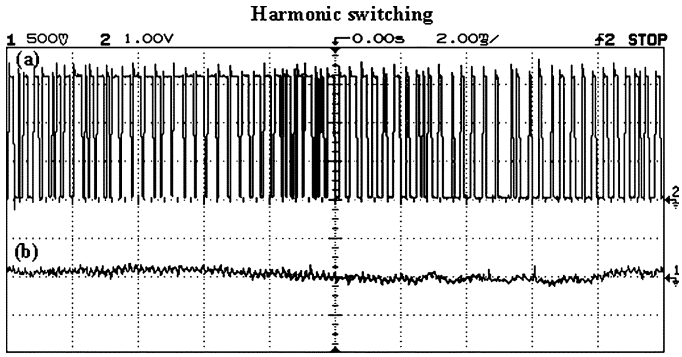

Fig. 23. Harmonic switching. (a) Switching input. (b) Tracking error.

three-level modulation is implemented with the same hysteresis band of $h = 3.368$ V. However, the minimum dead zone required experimentally is $\delta = 3.0$ V to avoid any bipolar modulation. The high value of dead zone is due to the finite sampling delay of digital processor in the feedback signal. Fig. 21(a) shows the switching signal for the switch S_{w2} and the steady-state tracking error is shown in Fig. 21(b). The switching frequency observed is slightly higher as compared to its two-level counterpart as explained in Remark 1. The switch S_{w3} also operates at the same frequency with the complementary logic as that for S_{w2}. The left leg switches S_{w1} and S_{w4} operate at the low frequency as explained in Section III and shown in Fig. 22. The tracking error is significantly high as compared to the two-level inverter.

Carrier-based modulation is implemented with the sinusoidal carrier magnitude of 2.368 V and hysteresis band $h = 1.0$ V as calculated in Example 2. Fig. 23 shows the switching input and tracking error for this magnitude of carrier. The figure illustrates the presence of harmonic switching at this minimum value of carrier magnitude As discussed in Section IV-D, the harmonic switching gets clear if the carrier magnitude is considerably higher than the critical value. Table I is referred in Appendix A. Fig. 24(a) shows the fixed frequency switching at 3 kHz and the tracking error in Fig. 24(b) for the sinusoidal carrier magnitude of 2.8 V. The same result is obtained using the triangular carrier with the magnitude of 3.5 V having approximately same fundamental value as that of sinusoidal carrier. The tracking error characteristics for the three modulation schemes are similar to that shown in Fig. 16.

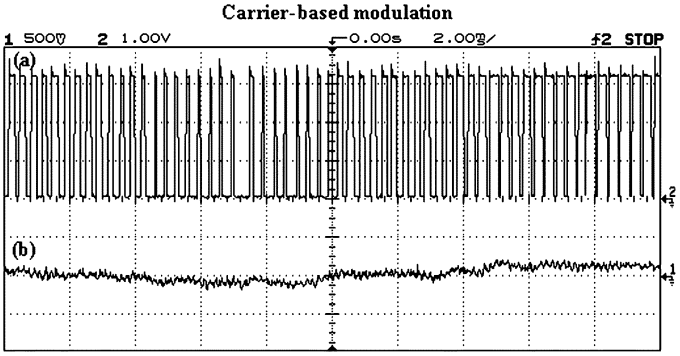

Fig. 24. Carrier-based modulation. (a) Switching input. (b) Tracking error.

TABLE I
SYSTEM PARAMETERS

Parameters	Numerical value
Source voltage (V_s)	6.00 kV (rms)
Feeder impedance (R_s, L_s)	6.05 Ω, 0.1155 H
Filter capacitor (C_f)	77.75 μF
Inverter losses (R_T)	6.05
DC bus voltage (V_{dc})	500V
Transformer (T_1)	1MVA, 440V/11KV, leakage inductance (L_T = 38.5 mH)

VI. CONCLUSION

Sliding mode control of DSTATCOM improves the total harmonic distortion and controls the PCC voltage against the load nonlinearities and nonideal source. Commonly used hysteresis-based switching has good dynamic and tracking properties but suffers from the problem of variable switching frequency. Three-level inverter logic yields half of the switching loss and switching harmonics at the expense of increased tracking error. Tsypkin's method together with the describing function provides good estimation of the switching frequency for power converters. Carrier-based modulation yields robust fixed frequency switching condition with the appropriate design of carrier magnitude. Sinusoidal carrier forms a fundamental signal for the design of any carrier-based modulation. The region of border collision bifurcation should be identified and the complex switching states of the inverter, i.e., chattering and harmonic switching, must be avoided with the proper choice of hysteresis band and carrier magnitude, respectively. Three-phase unbalance load and source parameter have negligible effects on the design of all switching schemes of the sliding mode control. The dc link voltage variation, filter capacitor, and shunt inductance uncertainty provide a high sensitivity for the calculation of switching frequency for two-/three-level modulation and the determination of carrier magnitude for carrier-based modulation. Both simulation studies and experimental results validate the theory proposed in this paper. The design of any state feedback configuration of DSTATCOM control can be extended using the proposed frequency-domain approach.

APPENDIX A

The system parameters are given in Table I.

APPENDIX B

Transfer function for a DSTATCOM controlled system derived in terms of system parameters and feedback gains is given as follows:

$$G(s) = \left(\frac{mV_{dc}}{L_sL_lL_TC_f}\right)\frac{(L_ss+R_s)(L_ls+R_l)(k_1s+k_2)}{D(s)}$$

where

$$\begin{aligned} D(s) = {} & s^4 + \left(\frac{R_s}{L_s}+\frac{R_l}{L_l}+\frac{R_T}{L_T}\right)s^3 \\ & + \left\{\frac{1}{C_f}\left(\frac{1}{L_s}+\frac{1}{L_l}+\frac{1}{L_T}\right) + \frac{R_TR_l}{L_TL_l}+\frac{R_sR_l}{L_sL_l}+\frac{R_TR_s}{L_TL_s}\right\}s^2 \\ & + \left\{\frac{R_s}{C_fL_s}\left(\frac{1}{L_l}+\frac{1}{L_T}\right)+\frac{R_l}{C_fL_l}\left(\frac{1}{L_T}+\frac{1}{L_s}\right) + \frac{R_T}{C_fL_T}\left(\frac{1}{L_l}+\frac{1}{L_s}\right)+\frac{R_sR_lR_T}{L_sL_lL_T}\right\}s \\ & + \frac{R_sR_lR_T}{L_sL_lL_TC_f}\left(\frac{1}{R_s}+\frac{1}{R_l}+\frac{1}{R_T}\right). \end{aligned}$$

ACKNOWLEDGMENT

The authors would like to thank Prof. A. Joshi of the Electrical Engineering Department, IIT Kanpur, for providing helpful suggestions during the preparation of this manuscript.

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