A Scalable Architecture for Multi Millions Frames per Second CMOS Sensor With Digital Storage

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Abstract— **This paper describes a 3D Integrated Circuit (3D-IC) architecture of a burst image sensor (BIS) with embedded digitization and digital storage. This architecture also proposes a new technique to further increase both the frame rate and the stored image capacity at the cost of a spatial resolution reduction. A 2D monolithic demonstrator that takes into account the constraints of a future 3D-IC imager has been fabricated. Experimental results are presented showing that a frame rate from 5 up to 45 Mega frames per second can be achieved. This fully functional approach paves the way to the very first in-focal-plane digital BIS.**

Keywords—CMOS video sensor; ultra fast burst imaging; digital storage; CMOS image sensor; 3D stacking

I. INTRODUCTION

Conventional video systems extract data from the image sensor at each frame and store it into an external memory for post processing or display. The constrained number of Input/Output (I/O) pads of the sensors limits the data rate and consequently the pixel readout rate to about 25 Gpixel/s for the fastest currently available video camera [1]. This bottleneck results in the limitation of the frame rate to a few kfps (kilo frame per second) when the frame resolution is close to 1 million pixel or about 1 Mfps (Mega frames per second) when the frame resolution is reduced to about 1 kpixel. If a higher pixel rate is required, the I/O issue can be circumvented if the data is stored in the sensor at a very high data rate during the acquisition and readout afterward at a relaxed speed.

This approach is known as Burst Image Sensor (BIS) and consists to use an on chip memory to store the video stream. At this time, published BIS use analog CMOS capacitances [2][3] or CCD channel memories [4][5] and are designed in 2D monolithic integrated circuit (IC).

A BIS that stores the recorded data frames within its chip can benefit from a digital storage as the information density can be much higher in the digital domain compared to the analog domain. For instance, in a 28 nm digital process, the surface of respectively a static and a dynamic bit cell are 0.12 µm² and 0.035 µm². As a consequence, while analog BIS can hardly store more than 200 frames in in-focal-plane storage topologies, a digital BIS can easily record respectively more than 1000 or 4000 frames by using a SRAM or a DRAM based memory bank and by assuming a pixel pitch of 50x50 µm and 8 bits dynamic [6]. On the other hand, the surface occupied by the Analog to Digital Converter (ADC) within the pixel will reduce the available area to the memory in a single 2D IC sensor. A 3D stacked IC approach overcomes this limitation by allowing a distribution of electronic functions on dedicated tiers. Top tier photodiodes can benefit from imagery technology and back side illumination for a maximal sensitivity, the ADC gains area and partitioning design flexibility on middle tier, and in the bottom tier almost all the pixel area is available to store the frames thanks to advanced digital node technology.

The paper describes a 3D-IC architecture of a scalable design for burst image sensors with on the fly digitization and embedded digital storage applied to a 3D stack of 3 integrated circuits. In order to demonstrate the benefits of this approach, a 2D monolithic circuit integrating the different electronic parts of the sensor side by side has been designed in a 65 nm CMOS technology. The overall sensor architecture is presented in section II and its different parts are described in section III to VI. The section VII presents the demonstrator and experimental results are shown in section VIII.

II. OVERALL SENSOR ARCHITECTURE

The 3D design allows a better repartition of the electronic parts and the targeted cross-section of the sensor is presented on fig. 1. A first IC is dedicated to the analog pixel array. A second one is devoted to the ADC and the last one is dedicated to the embedded digital memory.

A straight forward implementation of this architecture is to store an ADC and its associated memory in each pixel. This topology is not necessarily optimal in term of frame rate and sequence depth, i.e. the number of storable images. An on-the-fly analog to digital conversion at a targeted frame rate of several tens of Mfps requires a high speed ADC which results in a high silicon area and power consumption as explained in section IV. Likewise, segmenting the memory floorplan into a unit for each pixel is not optimal in term of memory capacity since space is lost for addressing blocks and boundary separations.

For these reasons, a cluster approach has been adopted for the BIS. This line has been recently used with a 2 layers stacked

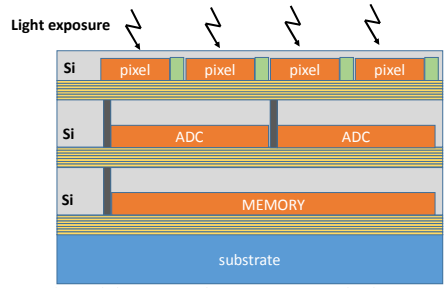

Fig. 1. Cross section of the targeted 3D CMOS stacked

global-shutter image sensor [8]. The detailed architecture of the sensor according to the different tiers is shown on fig. 2. A cluster of pixels is composed of P=10 frontend pixels connected to one ADC. A bloc of L clusters, i.e. LxP pixels, shares the same digital memory for an optimal floorplan configuration that allows embedding the maximal amount of memory.

Furthermore this cluster of pixels approach sharing the same memory unit brings memory addressing flexibility since this feature allows to digitize an adaptable number of pixels. In "full frame" mode an ADC operating at a sampling rate Fs and reading all the P pixels gives an achievable frame rate of Fs/P. But we implemented some modes to improve the frame rate at the cost of a spatial resolution reduction. By assuming a constant data conversion rate, the frame rate increases as the number of read pixels in the cluster is reduced and is given by (1)

$$Fps = \frac{Fs}{P} \cdot \frac{P}{P_{RC}} = \frac{Fs}{P_{RC}} \quad (1)$$

Where P is the number of pixels in the cluster and $P_{RC} \in [1;P]$ is the number of read pixels within the cluster. Meanwhile, the movie length is also increased by a factor P/P_{RC}. Increasing the frame rate is obviously very interesting in high speed imaging to detect faster events whereas expanding the movie length allows the observations of fast and complex event that last for a longer time. While using this feature, the ADC and memory efforts are kept constant whereas the pixel front-end operates at a higher speed. Thus the front-end bandwidth has to be high enough to operate at the highest frame rate or it has to be increased as the frame rate increases to keep the sensor sensitivity constant.

III. Analog Front-end Design

In high speed imaging the analog front-end has to operate at a frame rate of up to several tens of MHz. As a consequence, the exposure time is much less than 1 µs and thus the integrated light energy is potentially very low. Therefore, the front-end must provide both a high bandwidth and a high conversion gain. A Capacitive Trans-Impedance Amplifier (CTIA) provides a very low impedance node, a fixed bias and a very high conversion gain as well as a high bandwidth. The main drawback of a CTIA is the area and the power consumption which both are not critical for this design as the pixel pitch is 50 µm and as a backside illumination is expected for the final sensor. For all this reasons, a CTIA with a transconductance stage based on a cascode differential pair with 2.5V power supply voltage has been implemented in the pixel. In the 2D

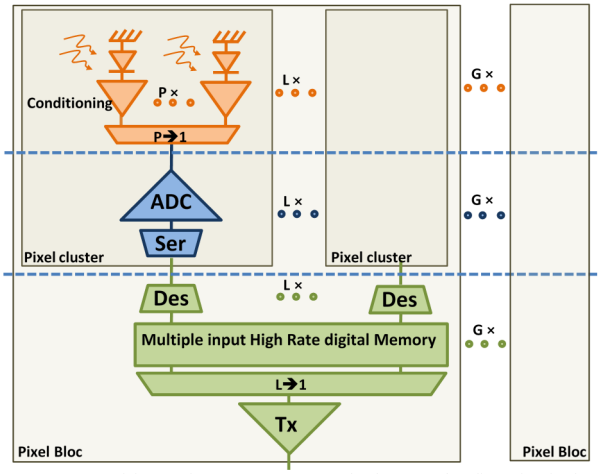

Fig. 2. IC repartition of a 3D CMOS stacked BIS. The first tier is for the pixel frontend, the second tier shares one ADC for one pixel clusters and the third tier is for the deigital memory shared for several ADC clusters.

demonstrator the photodetector is a 35×40 µm P_{Sub}-N_{well} placed beside the CTIA and a buffered analog multiplexer that allows to select one of the pixel output to the shared ADC input. A sample and hold circuitry with a ping pong structure to store the even and odd frames makes possible a pipeline integration, i.e. the odd frames are digitized during the integration of the even frames and vice versa. The CTIA integrating capacitor is 27 fF and the biasing current is 20 µA. An open loop gain of 40 dB and a bandwidth of 30 MHz are achieved. The 10 pixels cluster layout is shown in Fig. 4.

IV. Analog to Digital Converter

In the case of a digital BIS the main bottleneck is the ADC. As the cluster approach allows to use a single ADC shared for several pixels, it can occupy the corresponding silicon surface minus the space required by some Trough Silicon Via (TSV) mandatory to convey signals from the top tier.

Regarding the state of the art from the Murmann data base [9] (Fig. 3), the successive approximation register (SAR) and pipeline architectures seem to be two good candidates for the targeted frame rates between 10 and 100 Mfps with an 8 bits resolution. Pipeline architecture is more subject to missing code error than SAR architecture and delta sigma are too slow for our application. Moreover, the SAR ADC architecture disposes

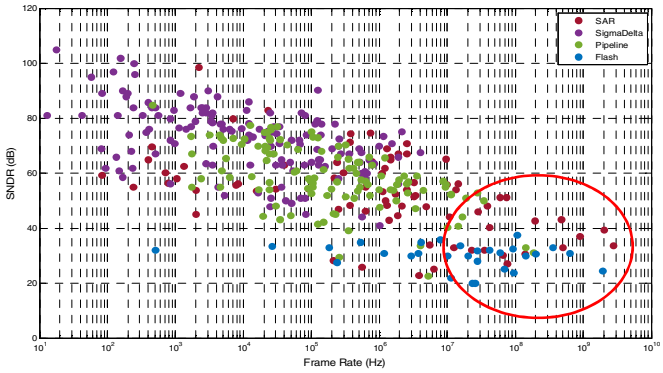

Fig. 3. State of the art of 8-bit ADC from [9]. At the targeted frame rate, SAR architecture offers the best signal to noise ratio.

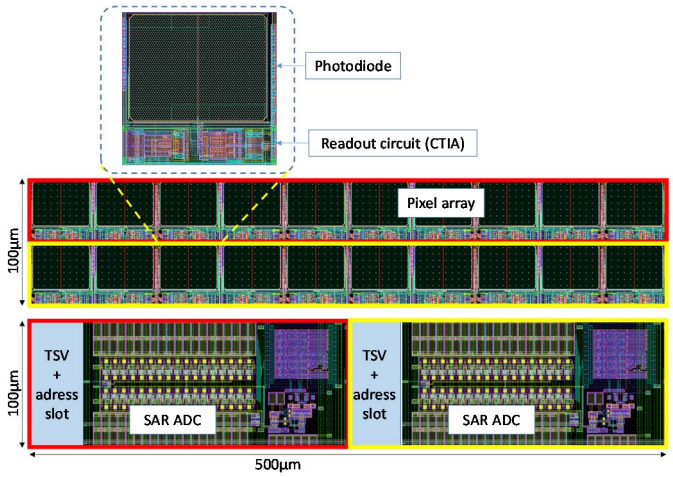

Fig. 4. tier 1 (top) and tier 2 (bottom) floorplan partitionning (100µm×500µm double cluster)

intrinsically of an interesting single bit stream output that limit the number of required TSV to transmit the converted data. Therefore, this architecture is preferred for this range of frame rate. The designed SAR ADC is a single-ended architecture based on a feedforward principle, and is described in detail in [12]. A binary capacitor array segmented by two reduces the total value of the capacitors seen by the input nodes during the sampling phase and also to reduce the total area of the chip. The core's size is about 210×100 µm^2 so that two ADCs fit the area of two clusters, i.e. 500×100 µm², and a space of more than 6000 µm² is available for the TSV required to the 3D stacked version of the final sensor. The post-layout noise simulation shows an effective number of bit (ENOB) of 7.5-b. The total power consumption of this SAR ADC is only 1.55 mW at 100 MS/s.

V. Digital Memory

In the final 3D stacked sensor, the digital memory should be designed with an advanced CMOS process such as a 28 nm technology. In our monolithic demonstrator realized in a 65 nm process, a not optimized SRAM memory bank has been used. The memory receives the single bit stream provided by the ADCs and stores each pixel value into a 16384 bits large memory bank for each cluster. By assuming an 8 bits dynamic, the storable movie length is then 16384/8/10 = 204 frames long.

VI. Sensor Control

The sensor operation is controlled with 4 embedded state machines (SM) that allow to precisely control the fast different unit. These SMs are clocked by a 100 MHz to 1 GHz master clock provided by an external PLL and almost all the timing of these SM are configurable by writing to their specific register. The main SM waits for a "start" signal to initiate the record of a sequence. The integration SM controls the reset signal at each new frame. The write SM controls the ADC operation, in particular the sampling signal and the number of digit of the conversion in the range from 1 to 8 bits. Finally, the pixel read SM allows to choose the pixel to read into the cluster at each frame. Several read modes are available. The first mode, the so called "full frame" mode, consists to read all pixels. The second one, reads out only half of the cluster leading to a 2 × higher frame rate. The third one reads out only 2 pixels of the cluster with a 5 times higher frame rate. The last mode deals with only 1 pixel of the cluster to offer a 10 × higher frame rate. For those different modes biasing adjustments are provided to readout circuits.

VII. Monolithic Demonstrator

The photography of the designed monolithic demonstrator is depicted in Fig. 5. It is composed of 12 clusters of 10 pixels with their 12 associated ADC. Some additional test structure are also included.

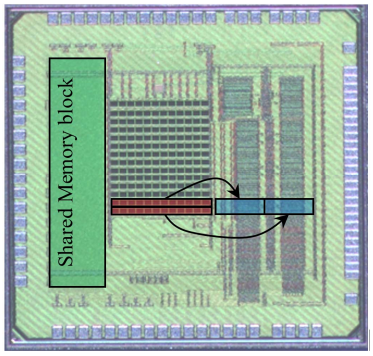

Fig. 5. Demonstrator die photography. Highlighted: two clusters of 10 pixel (pink) and their two associated ADCs (blue) and the shared memory bank for the block of 12 digital clusters.

The memory block merged the 12 clusters data with a total of 12×16384 bits. Two clusters (pink) and their two associated ADCs (blue) are highlighted to show their shape factor and especially the area consumption. The configuration of the sensor and the extraction of the acquired data are passing through a SPI port.

VIII. Experimental Results

The response of the sensor has been tested under a pulsed illumination. A 635 nm laser diode driven by a custom electronic emits a 15 pJ, 100 ps Full Width at Half Maximum (FWHM) long pulse of light that illuminates the whole sensor sensitive area [13]. The acquisition mode is "full frame" and the ADC dynamic is set to 8 bits with a 5 Mfps frame rate. The pulse of light is generated during the frame 4 exposure time.
For clarity reason, only a single cluster is represented over the 7 first frames (Fig. 6). We clearly see that the light pulse is

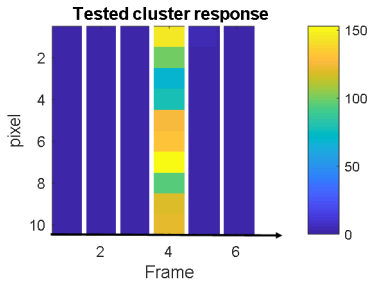

Fig. 6. Time response of a 10 pixels cluster to a 100 ps laser pulse. The pulse is generated during the frame 4 exposure.

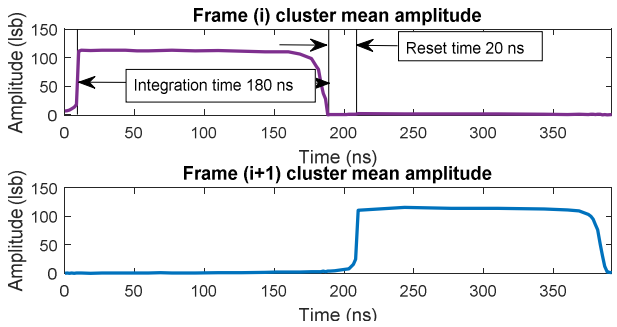

Fig. 7. Aperture of a pixel at 5 Mfps and a reset time of 20 ns

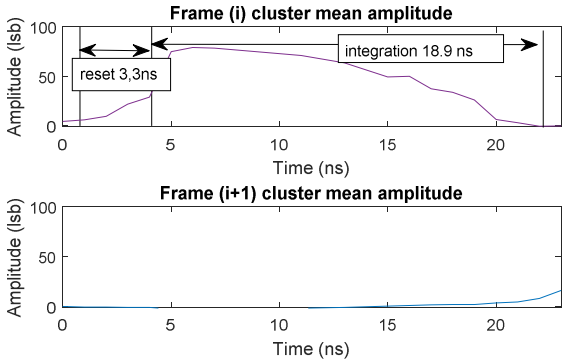

Fig. 8. Aperture of a pixel at 45 Mfps and a reset time of 3.3 ns

detected only on the frame 4. The pixel response non uniformity is meanly due to the speckles pattern of the laser diode.

The pixel aperture against time is precisely measured thanks to the very short 100 ps FWHM light pulse swept across two frame periods. The result (Fig. 7) indicates that the aperture of the pixel is very sharp at the opening and decreases slowly at the end of the integration time. This is because when the laser pulses occurs at the end of the frame, the photodiode and the front-end do not have the time to setup completely before the sampling. When the pulse arises during the reset time of the frame i+1, a few crosstalk of about 1% is still present on the frame i, while the signal of frame i+1 slightly increases. This is due to an incomplete and not fully efficient reset of the CTIA. No influence is observed on the frame i+2 that benefits from a second reset period.

A higher frame rate has been achieved by setting the master clock to 900 MHz, and only 2 pixels of the cluster are read by frame. The resulting frame rate is 900/10/2=45 Mfps. The measured pixel aperture is given in Fig. 8. Measured noise floor is 0.65 lsb rms. Our demonstrator specifications and readout characteristics are summarized in TABLE I.

TABLE I. TECHNICAL SPECIFICATIONS

Scalable Pixel Block specifications		***pixel characteristic***	
technology	7M1P 65nm	Pixel size	50 × 50 µm
Pixel count	40	Fill factor	64%
Area	0.1mm²	***Readout characteristics***	
Fame rate	5Mfps (full frame)	Read noise	2.5 mV rms
	45Mfps (2/10 pixel count)	Dyamic range	1 V
Memory depth	204 full frame 8bit images (1024 in 0.28nm)	Conversion gain	5.9 µV/e-

IX. CONCLUSION

An 3D-IC architecture of a burst imaging CMOS sensor with a digital storage has been presented. A 2D monolithic demonstrator integrating the electronic of the future 3 different tiers has been designed, realized and characterized. The results show that the proposed architecture is fully functional and can operate at the frame rate of 5 Mfps. The used cluster approach allows to increase both the frame rate and the movie length at the cost of a spatial resolution reduction. The CTIA-based high speed pixel allows to reach a frame rate of 45 Mfps. This work paves the way to the very first 3D stacked BIS with digital storage.

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