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# Digitally Controlled Transconductor Based on a Quantum Transconductance

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**Abstract** — A new CMOS digitally controlled negative-transconductance amplifier (DTA) and an application example of a 4-Bits-Digitally Controlled Oscillator (DCO) are presented in this paper. The DTA is based on the traditional Digital CMOS inverter topology. From simulation and under 1.2 volts supply voltage, the proposed DCO oscillates from 375MHz to 475MHz which is compatible with the Medical Implant Communication Service (MICS) frequency band. The maximum total power consumption is about 2.5mW and only 2.5nW in power-off mode. All simulations have been performed using a CMOS 130nm process design kit from STMicroelectronics.

## I. INTRODUCTION

Today Transconductance Amplifiers are used to design several continuous time ‘gm-C’ circuits for analog processing, which are, in several cases, filters and oscillators [1-10]. Transconductance amplifier is also used in numerous analog front-ends based sensors and instrumentation networks. The interest of the gm-C topologies is that they could operate at high frequency [1]; they also give the advantage of using a capacitor as loading impedance that is compatible with the digital supply voltage  $V_{DD}$ . Moreover the transconductance of the amplifier stage can be used to simulate a resistance which is adjustable. High performances radiofrequency and instrumentation front-ends also need high precision filters and oscillators and consequently the cut-off frequency (filters) or the frequency of oscillation (oscillators) must be calibrated. From literature frequency calibration could be done by capacitor switching or by modifying the transconductance values [2,3,4,12]. Amplitude calibration is also often realized by controlled the gain from a transconductance. For all the reasons, discussed below, the controlled transconductance amplifier plays an essential role to process continuous time signals. The amplifier transconductance is traditionally modified from a voltage controlled current source (VCCS) [4,12]. After calibration, the controlled voltage is save analogically in a capacitor [11]. In this case, the system needs to regularly refresh the calibration because of the capacitance discharge [11]. Digitally-controlled-current-source offers the advantage to save and controlled the transconductance from a digital word which can be save in a memory device. In this case the transconductance tuning precision is directly correlate to the current source quantum [4,12]. In this paper we propose to consider directly a transconductance quantum. This idea has been previously proposed by [4] in the design of a CMOS programmable OTA. For a transconductance quantum equal to  $g_0$  the target transconductance ( $g_m$ ) is controlled from a  $n$  bits  $A < n-1:0 >$  digital control number (voltage), we have:

$$g_m = \left[ \sum_{j=1}^n (A_j \cdot 2^j) \right] g_0 = A_{Base10} \cdot g_0 \quad A_j \in [0,1] \quad (1)$$

where  $g_0$  is the *quantum transconductance*. The output of the transconductance amplifier is equivalent to a current source, then it is also easily, by added in parallel a transconductance amplifier (transconductance  $g_H$ ), to obtain:

$$g_m = g_H + \sum_{j=1}^n (A_j \cdot 2^j) g_0 \quad (2)$$

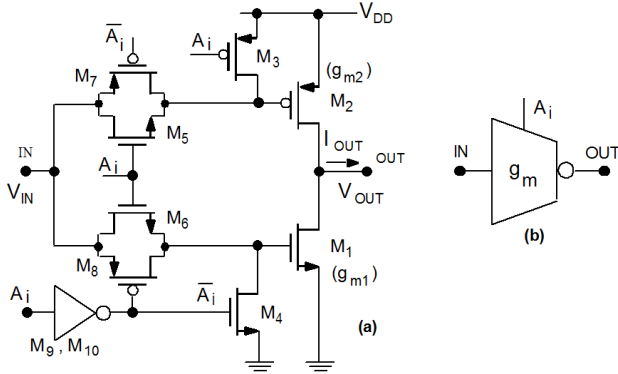
Due to the non-linearity, equations (1) and (2) are generally quasi-valid at small signal amplitude operations only. To maintain a linear relationship between the input and output, i.e. at moderate amplitudes or high amplitude variations, it is necessary that the transconductance remains constant. Literature proposes a large number of solutions to improve the linearity; a number of solutions is based on the source degeneration technique [5,9,13].

Single ended input-output transconductance amplifier using the traditional CMOS two transistors inverter demonstrates interesting properties. These properties are low area, good linearity and the capacity to operate at very high frequency under very low supply voltage [1-3,6-7,10,14]. The main drawback of the traditional CMOS inverter is the relative difficulty to control the bias current in order to modify the transconductance; in this way an elegant solution by acting on the bulk bias voltage is proposed in [3]; however this solution necessitates a relatively complex bulk-control circuitry that increases the silicon area and power consumption. Another classical solution is based on a double CMOS pair source degeneration [2] to control the transconductance; this last solution necessitates to process signal with a relatively low transconductance gains due to the source degeneration. The Idea, presented in this paper concerns a new transconductance amplifier topology based on a “quantum transconductance”  $g_0$  and a multiple of this quantum. In this paper, the proposed transconductance is discussed in session 2 and session 3. In session 4, application based on the design of a digitally controlled oscillator (DCO) is proposed, discussed and simulated using the typical parameters of the CMOS 130nm process from STMicroelectronics [15]. As an example we have choose a frequency range compatible with the Medical Implant Communication Service (MICS) frequency band [16]. Finally a conclusion is given in section V.

## II. ONE BIT DIGITALLY CONTROLLED NEGATIVE TRANSCONDUCTANCE

The proposed one-bit transconductance topology is shown in Fig.1a and its corresponding conventional symbol in Fig.1b. The transistors  $M_1$  and  $M_2$  realize the analog processing [1-2,6] while  $M_3$  to  $M_{10}$  realize the digital operation. Not

represented in Fig.1, all *pmos* bulks are connected to  $V_{DD}$  and all *nmos* bulks to the ground (gnd).



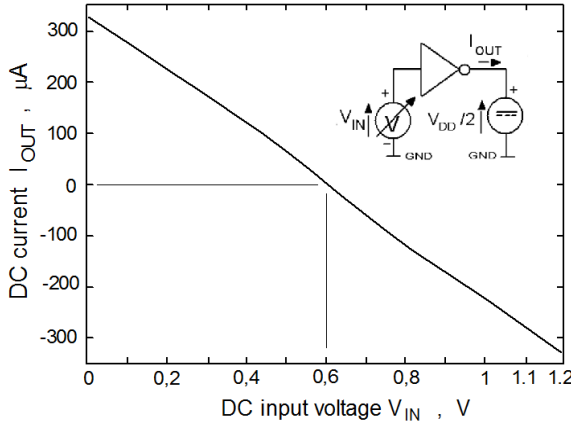
**Fig.1:** Proposed 1bit Negative Transconductor: -a- Transistor configuration -b- proposed symbol

Transistor  $M_1$  and  $M_2$  are sized to be equilibrate [6]; this leads to a common mode DC bias voltage  $V_{DD}/2 = V_{IN0} = V_{OUT0}$ .  $V_{IN0}$ ,  $V_{OUT0}$  correspond to the DC part of  $V_{IN}(t)$ ,  $V_{OUT}(t)$  respectively. In Fig.1a,b the input *digital* voltage  $A_i$  is a 1 bit digit that control the transconductance amplifier. Transistors  $M_3$  to  $M_{10}$  are used to switch-off the amplifier, allowing to manage the power consumption and to provide  $g_m = 0$  when  $A_i = 0$ . From Fig.1a, the transconductance of the proposed amplifier, is given by:

$$g_m = g_{m1} + g_{m2} \quad \text{when } A_i = 1 (V_{DD}) \quad (3a)$$

$$g_m = 0 \quad \text{when } A_i = 0 (\text{gnd}) \quad (3b)$$

Where  $g_{m1}$  and  $g_{m2}$  are the gate-source transconductances of  $M_1$  and  $M_2$  respectively. Note that this amplifier provides a negative transconductance gain for  $A_i = 1$ .



**Fig.2:** Typical DC characteristic of the amplifier output current versus the input voltage when  $A_i = 1$ ; 130nm CMOS process from STMicroelectronics [15],  $g_m = 0.548 \text{m}\Omega^{-1}$

With  $A_i = 1$ , around  $V_{DD}/2$ ,  $M_1$  and  $M_2$  operate in saturation mode for which the drain currents are approximate to [17]:

$$I_{DS1} = (\beta_1 / 2)(V_{GS1} - V_{T1})^n (1 + \lambda_1 V_{DS1}) \quad (4a)$$

$$I_{SD2} = (\beta_2 / 2)(V_{SG2} - |V_{TP2}|)^n (1 + \lambda_2 V_{DS2}) \quad (4b)$$

$$\beta_1 = \mu_1 C_{OX} W_1 / L_1 ; \quad \beta_2 = \mu_2 C_{OX} W_2 / L_2 \quad (5a,b)$$

Where  $n \in (1-2)$ ;  $C_{OX}$  is the thin oxide capacitance by meter square;  $V_{T1}$  and  $V_{T2}$  are the  $M_1$  and  $M_2$  threshold voltages

respectively.  $\mu_1$  and  $\mu_2$  the  $M_1$  and  $M_2$  motilities;  $W_1/L_1$  or  $W_2/L_2$  is the ration between the transistors channel width and length. Considering an equilibrate inverters:  $\beta_1 \cong \beta_2$ , and it will be considered in this paper that  $\beta = \beta_1 = \beta_2$ . Fig.2 shows the typical variation of the output current versus the input voltage  $V_{IN}$ . For  $A_i = 1$ , at small signal amplitude, the transconductance of the proposed DTA using an equilibrate CMOS inverter is:

$$g_m \big|_{V_{IN0}=V_{OUT0}=V_{DD}/2} = -\frac{\delta I_{OUT}}{\delta V_{IN}} \quad (6)$$

In Fig. 1, the output current of a CMOS inverter is:  $I_{OUT} = I_{SD2} - I_{DS1}$ ; where  $I_{DS1}$  and  $I_{SD2}$  are the current through the drain-source of  $M_1$  and  $M_2$  respectively. For  $V_{IN} = (V_{DD}/2) + \Delta V_{IN}$  and neglecting the channel length modulation, the output current  $I_{OUT}$  is given, from equations (4), by [6,8]:

$$I_{OUT} = \frac{\beta}{2} \left[ \left( \frac{V_{DD}}{2} - \Delta V_{IN} - |V_{T1}| \right)^n - \left( \frac{V_{DD}}{2} + \Delta V_{IN} - V_{T2} \right)^n \right] \quad (7)$$

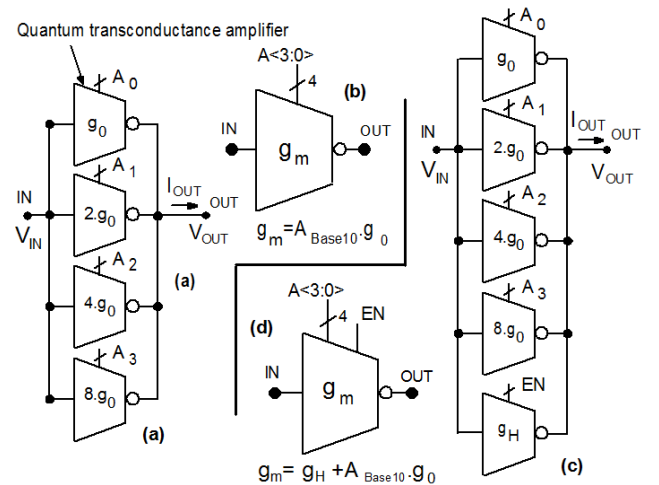
In equation (7) :  $I_{OUT} = I_{OUT0} + \Delta I_{OUT}$ , with  $I_{OUT0} = 0$ . Considering  $V_{T1}$  approximately equal to  $|V_{T2}|$  ( $V_{T1} = |V_{T2}| = V_T$ ), we have [6] for  $n \cong 2$ :

$$\Delta I_{OUT} = -\beta(V_{DD} - 2V_T)\Delta V_{IN} = -g_m \Delta V_{IN} \quad (8)$$

Equation (8) and the simulation proposed in Fig.2 show a good linear relationship between  $\Delta I_{OUT}$  and  $\Delta V_{IN}$ . The CMOS inverter around  $V_{DD}/2$  also provides a very good frequency performance; because the frequency transition of the CMOS equilibrate inverter around  $V_{DD}/2$  is approximately the half of the transition frequency of  $M_1$  (*nmos*) [6,8].

### III. N-BITS DIGGITALLY CONTROLLED TRANSCONDUCTOR AMPLIFIER BASED ON QUANTUM TRANSCONDUCTANCE

The proposed digitally  $N$  Bits controlled transconductance amplifier (DTA) topology is shown in Fig.3a; with an example of a control word  $A <3:0>$ , i.e.  $N=4$ ; In Fig. 3,  $A_0$  is the *less significant bit* (LSB) and  $A_3$  the *most significant bit* (MSB) of  $A <3:0>$ . The equivalent symbol of the proposed DTA in Fig.3a is draw in Fig.3b.



**Fig. 3:** Propose digitally controlled transconductance amplifiers: -a- configuration that verify equation (1) and -b- the proposed equivalent symbol -c- configuration that verify equation (2) and -d- equivalent symbol

The 4-bits DTA is constructed by connecting in parallel 4 identical 1-bit DTAs (Fig.1). The DTA of gain  $g_0$  is the quantum transconductor. The transconductance  $2g_0$  is obtained by doubling the transistor channel widths of  $M_1$  and  $M_2$ . The same sizing operation is done between  $4g_0$  and  $2g_0$  amplifiers and between  $8g_0$  and  $4g_0$  amplifiers; here the length of all transistors are supposed to be equal. The amplifier in Fig. 3 respects the equation (1). To realize a 4bits-DTA that verify equation (2) an additional transconductance amplifier of transconductance  $g_H$  controlled by the digit EN is added in parallel. This derivative amplifier is shown in Fig.3c and its proposed symbol in Fig.3d. Note that the amplifier in Fig.3c,d is powered off for EN=0 and  $A<3:0>=0$ .

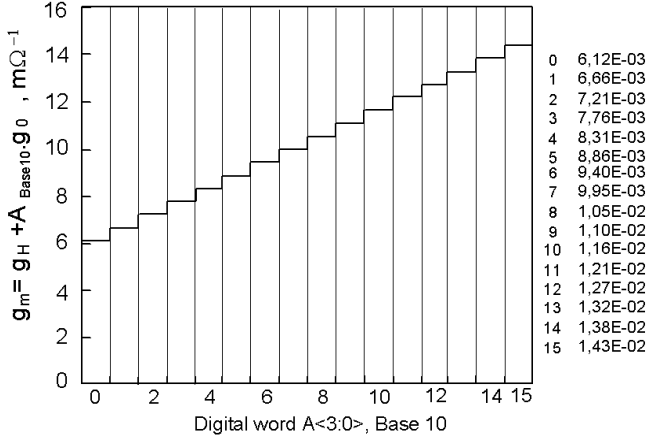


Fig.4: Simulation of the 4Bits DTA in Fig.3c 130nm CMOS process from STMicroelectronics [15], size reported in Table 2 of section IV.

#### IV. MICS-BAND-RADIOFREQUENCY OSCILLATOR BASED DIGITALLY CONTROLLED TRANSCONDUCTORS

To illustrate the capabilities of using *digitally controlled transconductance amplifier* (DTA), simulation results and discussion of a compact active oscillator [8], using the DTA, in section 2 and 3, is proposed in this section. The compact oscillator topology [8] is shown in Fig. 5. The Circuit has been design to be able to operate in the MICS band [16]. Table I resume the transistor channel widths and the circuits transconductances obtained from simulations. Simulation have been performed using typical BSIM4 transistor models and the associated design kit of the CMOS 0.130μm process from STM [15]; the length L of all transistors has been fixed to L=0.2μm.

Table I: Transistors Width in [μm] and equivalent transconductance values in [Ω<sup>-1</sup>], V<sub>DD</sub>=1.2V, L=0.2μm.

| 1bit Amplifiers | $g_m$<br>[Ω <sup>-1</sup> ] | $M_1$<br>[μm] | $M_2$<br>[μm] | $M_{5/6/7/8}$<br>[μm] | $M_{3/9}$<br>[μm] | $M_{4/10}$<br>[μm] |
|-----------------|-----------------------------|---------------|---------------|-----------------------|-------------------|--------------------|
| $g_0$           | 5.48e-4                     | 1             | 2.75          | 0.15                  | 2.75              | 1                  |
| $g_H$           | 6.12e-3                     | 12            | 33            | 18                    | 2.75              | 1                  |
| $g_N$           | 6.02e-4                     | 1.1           | 3.02          | 1.65                  | 2.75              | 1                  |
| $g_P$           | 5.45e-4                     | 1             | 2.75          | 1.5                   | 2.75              | 1                  |
| $g_Q$           | 5.45e-4                     | 1             | 2.75          | 1.5                   | 2.75              | 1                  |

In Fig.5, the DTAs having the transconductance  $g_0$ ,  $g_Q$ ,  $g_N$  and  $g_P$  correspond to the 1bit-DTA topology in Fig. 1a while the DTA having the transconductance  $g_A$  is the 4Bits-DTA architecture of Fig.3c.

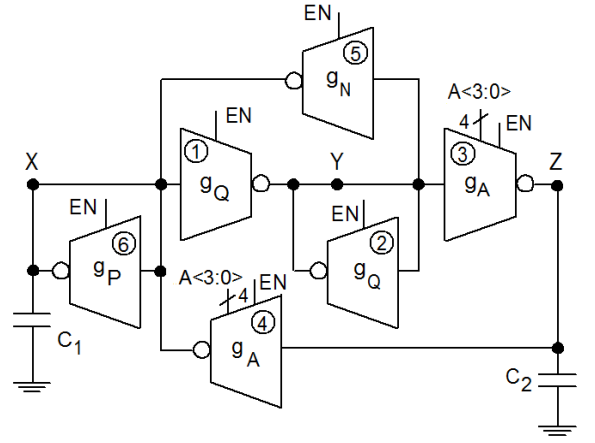


Fig.5: Compact Active RLC oscillator based transconductor [8].

The *Digitally Controlled Oscillator* (DCO) in Fig.5 has only 3 nodes X, Y and Z. At node X: the DTA-⑤ simulates a negative resistance equal to  $R_{NEG} = -1/g_N$ ; The DTA-⑥ simulates a positive resistance  $R_{POS} = 1/g_P$ . Between node X (input) and Z (output), DTA-①, DTA-② and DTA-③ simulate a positive transconductance amplifier. Because DTA-④ is a negative transconductance amplifier, we found that [DTA-①②③], DTA-④ and  $C_2$  form a Gyrator [8]. This gyrator simulate at node X a single ended inductance ( $L_2$ ) which is, from Fig.5, is given by:

$$L_2 = C_2 / g_A^2 \quad (9)$$

The equivalent circuit at X node is shown in Fig.6 [8].

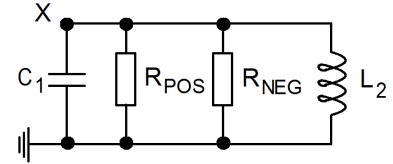


Fig.6: Equivalence of the compact DCO at node X.

Note that when EN=0 and  $A<3:0>=0000$ , the DCO is in standby mode (power off); in oscillation mode EN=V<sub>DD</sub>. The ideal frequency of oscillation of the DCO ( $f_{OSC}$ ) and condition of oscillation (CO) are, EN=V<sub>DD</sub>:

$$CO: g_N \geq g_P; f_0 = \frac{1}{2\pi\sqrt{L_2 C_1}} = \frac{g_A}{2\pi\sqrt{C_1 C_2}} \quad (10,11)$$

Considering equations (2) and (3), it follows that:

$$f_{OSC} = f_{MIN} + A <3:0> \cdot f_0 \quad (12)$$

With  $f_{MIN} = g_H / 2\pi\sqrt{C_1 C_2}$  and  $f_0 = g_0 / 2\pi\sqrt{C_1 C_2}$

$f_{MIN}$  is the minimum frequency of operation;  $f_0$  can be viewed as the quantum frequency and  $A<3:0>f_0$  the tuned frequency in the MICS band [16]. The ideal maximum MICS-band frequency is then:  $f_{MAX} = f_{MIN} + 15 \cdot f_0$ . Fig.7 shows the simulation variation of  $f_{OSC}$  versus the digital 4bits word control  $A<3:0>$ . Including the parasitic effects, an approximation of  $\sqrt{C_1 C_2}$  is  $\sqrt{C_1 C_2} = 2.6\text{pF}$ . A deviation with equation (12) are mainly caused by the variations of the gate-source ( $M_1, M_2$ ) parasitic

capacitances and conductances ( $M_1, M_2$ ) with value varies with  $A < 3:0 >$ . The equivalent parasitic capacitances at node X also introduce some deviation between simulation and the ideal equation (12).

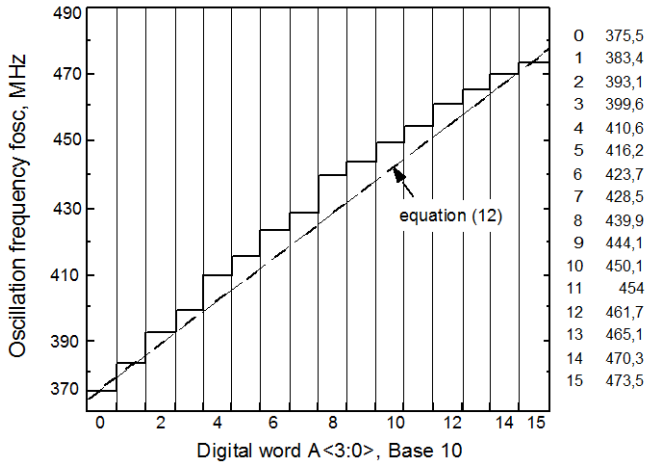


Fig.7: DCO oscillation frequency  $f_{osc}$  versus  $A < 3:0 >$ .

Fig. 8 shows typical oscillation waveforms obtained at X, Y and Z nodes.

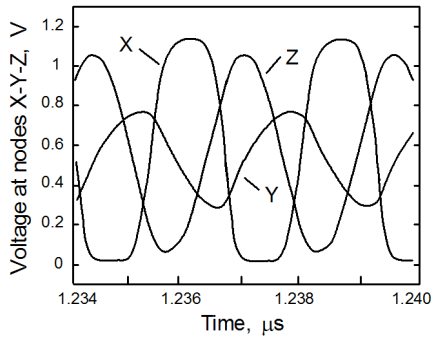


Fig.8: DCO Waveform voltages at X, Y, Z nodes.

Table II resumes the main simulation characteristics of the proposed DCO. The dynamic current consumption through  $V_{DD}$ , for all value of  $A < 3:0 >$  is shown in Fig. 9.

**Table II:** DCO main parameters  
@  $V_{DD}=1.2V$ , 135nm CMOS process STM [15],  $L=0.2\mu m$ .

| parameters                         | values    | scales |
|------------------------------------|-----------|--------|
| Quantum Frequency $f_0$            | 6.5       | [MHz]  |
| Tuning Range $[f_{MIN} - f_{MAX}]$ | 375 - 473 | [MHz]  |
| $I_{off} (EN=0, A=0)$              | 13.1      | [nA]   |
| Total power consumption ( $A=15$ ) | 2.5       | [mW]   |

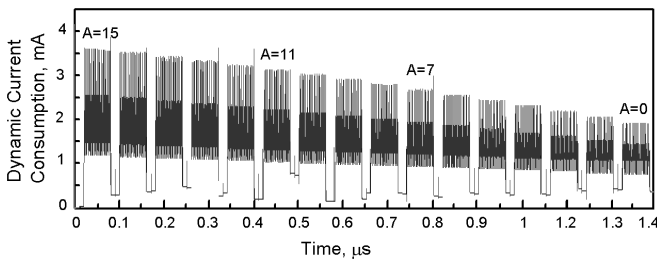


Fig.9: Current consumption versus time for  $A_{Base10}=15$  to  $A_{Base10}=0$

## V. CONCLUSION

Principle and simulation of a new digitally controlled negative transconductance amplifier (DTA) has been proposed in this

paper. The proposed DTA will be a useful design block for several analogue applications that need digital controlled VCCS. The proposed topology can operate at ultra-low voltage supply because the power-off mode is not made from a serial standby-pmos between the supply voltage and the internal circuit; but also because the DTA is based on the simple 2 transistors CMOS inverter. In addition to the advantage of operating at low supply voltage, the transconductor can work at large signal amplitudes and at high signal frequency.

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