Inter-tier Coupling Analysis in Back-illuminated Monolithic 3DSI Image Sensor Pixels

Petros Sideris
IMEP-LAHC
Univ. Grenoble Alpes, Univ. Savoie Mont Blanc, CNRS, Grenoble INP
Grenoble, France
petros.sideris@grenoble-inp.fr

Arnaud Peizerat
DOPT
CEA-LETI,
University Grenoble Alpes,
Grenoble, France
arnaud.peizerat@cea.fr

Perrine Batude
DCOS
CEA-LETI,
University Grenoble Alpes,
Grenoble, France
perrine.batude@cea.fr

Christoforos Theodorou
IMEP-LAHC
Univ. Grenoble Alpes, Univ. Savoie Mont Blanc, CNRS, Grenoble INP
Grenoble, France
christoforos.theodorou@grenoble-inp.fr

Gilles Sicard
DOPT
CEA-LETI,
University Grenoble Alpes,
Grenoble, France
gilles.sicard@cea.fr

***Abstract*—This study investigates the inter-tier coupling, for a Back-Side Illuminated (BSI) 4-Transistor (4T) pixel with its diode and Transfer Gate on the bottom tier and the rest of its circuitry on the top tier of a 3D Sequential Integration (3DSI) process. Variations due to coupling are compared with variations due to temperature, showing that both effects may result in a readout error of the same order of magnitude for the top-tier readout circuit. Nevertheless, we demonstrate that in a typical rolling readout, the sequence of the pixel control signals makes the coupling effect nearly negligible. As a result, we suggest that the fabrication of an inter-tier ground plane for electrical isolation is not strictly necessary for Monolithic 3D pixels when the readout top tier is directly stacked on the photodiode bottom tier.**

Keywords—Image sensors; 3D pixels; 3D sequential integration; 3DSI; Monolithic 3D; M3D; Coupling;

I. Introduction

CMOS Image Sensors (CIS) have been dominating the consumer electronics market over the last decade thanks to the development of Pinned Photodiodes (PPD). This breakthrough invention, in conjunction with a lower cost fabrication, higher data rates as well as a limited power consumption, have made CIS a more appealing choice than the Charge-Coupled Devices (CCD), which were the primary choice for imaging applications in earlier years.

Within the More than Moore context, 3D CMOS Image Sensors enable the possibility of smarter and more advanced sensors through the co-integration of different blocks (Analog, Digital, RF) in various tiers. Although 3D stacking technologies have been used for 3D CIS [1], [2], constraints of traditional 3D stacking alignment capabilities forbid the more aggressive pixel miniaturization required for future generations of CIS [3], [4]. This drawback can be overcome by using 3D sequential integration (3DSI - also named 3D monolithic integration or 3D VLSI), an emerging technology where the stacked tiers are fabricated sequentially on top of each other [5]. This process yields to outstanding high-density-contacts between the tiers (up to 10^8 3D via/mm^2) owing to the high alignment precision obtained with lithography steppers [6], [7], compared to packaging integration schemes (TSV, copper to copper bonding etc.). Therefore, this technology can enable the system partitioning in different processing blocks with high inter-connectivity and low latency.

A major challenge for the sequential processing is the limited thermal budget for the fabrication of the stacked devices. To date, Low Temperature (LT) devices have been successfully processed for Low-Voltage (LV) [7] as well as High-Voltage (HV) [8] applications. In particular, the feasibility of BSI CIS with miniaturized pixels realized in 3DSI has been investigated in [4].

Another important issue concerning the performance of 3DSI circuits is the electrical coupling between the sequential tiers due to the Inter-Layer Dielectric (ILD) that acts as a Back Gate (BG) oxide for the top stacked devices. Consequently, if no inter-tier Ground Plane (GP) is introduced, the top devices behave in fact as asymmetrical SOI MOSFETs, sensitive to the bottom tier electrode voltage variations. The scope of this study is to analyze the immunity of HV analog devices with V_{DD}=2.5V in the top tier when the bottom tier electrode voltage variations can go up to V_{DD}=2.5V, for a BSI 3D pixel. With the aid of TCAD simulations [9], a comparison against the impact of temperature variations on the top-tier stacked devices will be used to draw a conclusion on the necessity to introduce an inter-tier Ground Plane.

II. Inter-tier Coupling at Device Level

A. Simulation Setup

For the TCAD simulation setup we consider the cross-section illustrated in Fig.1(a). It consists of a 4T pixel partitioned in two tiers, the PPD and the Transfer Gate (TG) at the bottom whereas the readout transistors are placed at the top. The two tiers are separated by a 200nm thick ILD, and a 3D contact connects the Sense Node (SN) with the drain of the Reset (RST) transistor and the gate of the Source Follower (SF). In the most critical case of inter-tier coupling, each one of the top devices is placed above the TG electrode as shown in Fig.1(b).

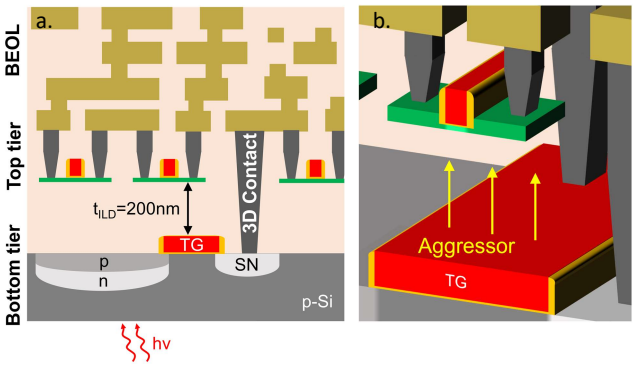

Fig. 1. a) Cross-section of 4T pixel, partitioned in 3D Sequential Integration. (b) In the most critical case, the top device is placed right above the TG electrode carrying a voltage that can go up to V_{DD}=2.5V.

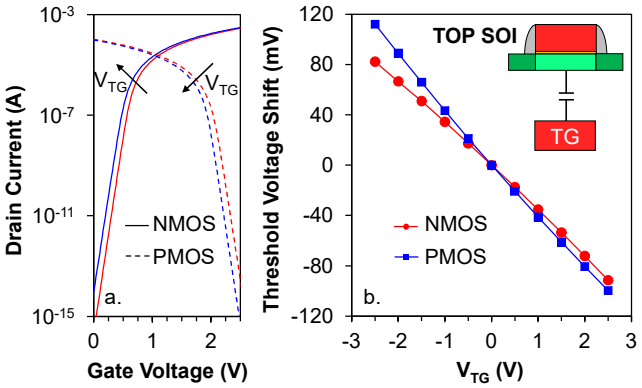

Fig. 2. (a) Impact of TG coupling (VTG=0-2.5V) on the input characteristics for NMOS and PMOS devices (b) Extracted threshold voltage shift versus TG voltage bias (-2.5V to 2.5V with 0.5V step).

B. Impact on electrical parameters

The Transfer Gate placed at the bottom tier toggles from 0V to V_{DD} and vice versa. This voltage node is coupled via a capacitive path to the exposed top device channel resulting in a shift of the I_D-V_G characteristics, as seen in Fig.2(a). This is a non-linear effect that becomes more evident in the sub-threshold region and slightly decreases to a fixed value when the device operates in strong inversion [10]. Extracting the threshold voltage shift due to the TG voltage bias sweep from -2.5V to 2.5V (Fig.2(b)), we obtain the back-bias efficiency γ from the slope, 35mV/V for NMOS and 42mV/V for PMOS.

In order to assess the impact of the TG coupling on the top tier device, we chose to compare it against the temperature dependence of the device electrical characteristics. Unlike the capacitive coupling, the effect of temperature has a complex behavior depending on the gate voltage V_G. As seen in Fig.3(b), increasing the temperature of the device from 253K to 353K (-20°C to 80°C) – extended temperature range in commercial electronics – we observe an increase of the subthreshold conduction current as well as a decrease of the saturation current while there is a gate voltage around threshold for which the drain current remains constant. This behavior is attributed to the increase in carrier concentration with temperature for low gate bias, as opposed to the decrease in carrier mobility for high gate bias [11]. At a specific V_G these two mechanisms are counterbalanced resulting in the Zero Temperature Coefficient (ZTC) point [12].

The impact of both coupling and temperature variations can be expressed through the change in the device electrical

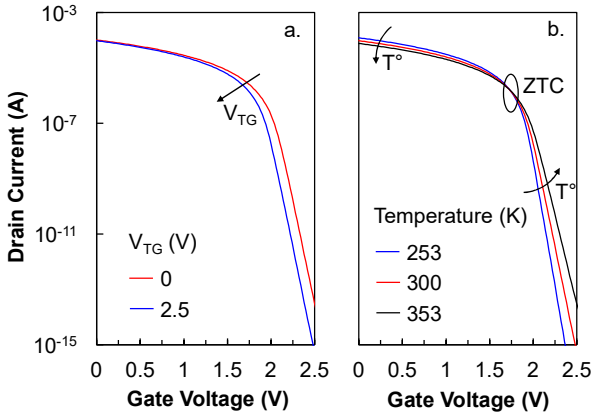

Fig. 3. Impact of coupling (a) and temperature variation (b) on the top-tier SOI input characteristics.

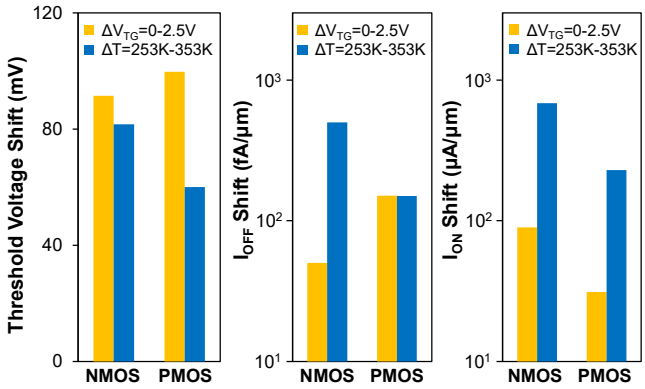

Fig. 4. Comparison of top-tier NMOS and PMOS electrical parameter variations due to TG coupling and due to a 100K temperature increment.

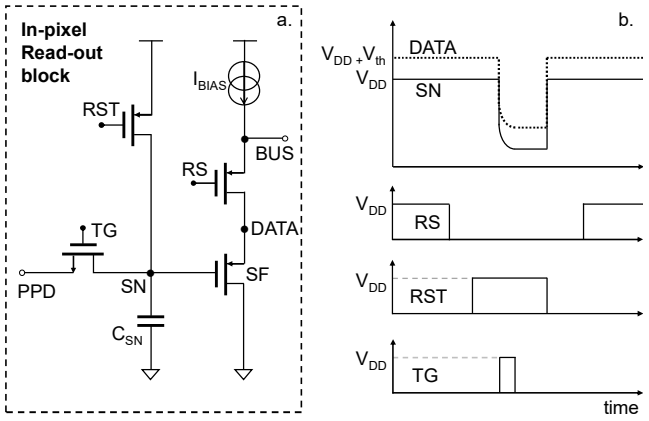

Fig. 5. (a) 4T pixel readout circuit (b) Chronogram of a readout cycle.

parameters, i.e., the Threshold Voltage (V_{TH}), OFF-state current (I_{OFF}) and the ON-state current (I_{ON}).

Fig.4 shows the comparison of the extracted parameters for the two effects. It is evident that they are roughly in the same order of magnitude whereas the slight prominence of the coupling impact regarding the Threshold Voltage Shift is due to the decrease of the temperature impact near the ZTC point at V_{TH}. For switch transistors the most important parameter is the leakage current I_{OFF} which is shifted significantly with the TG coupling. The latter can be critical for memory blocks placed at the top-tier above the TG.

III. Inter-tier Coupling at Pixel Level

A. Simulation Setup

Our 4T pixel contains the NMOS-TG as well as the RST, SF and RS in a PMOS circuit configuration shown in Fig.5(a). The SF is an amplifying transistor connected in common drain configuration with an approximate gain of unity. Fig.5(b) shows the chronogram of the 4T pixel readout operation. During the readout, the Sense Node (SN) is reset, then the TG is switched ON allowing photo-generated electrons to diffuse to the sense node. The accumulated electrons cause a voltage drop at the input of the SF resulting in nearly the same voltage drop at its output.

The Conversion Gain (CG in µV/e$^-$) evaluates the efficiency of this mechanism and is given by [13],

$$CG = \frac{qG_{SF}}{C_{SN} + C_{GD} + (1 - G_{SF})C_{GS}} \quad (1)$$

where q is the elementary charge, G_{SF} is the SF gain, C_{SN} is

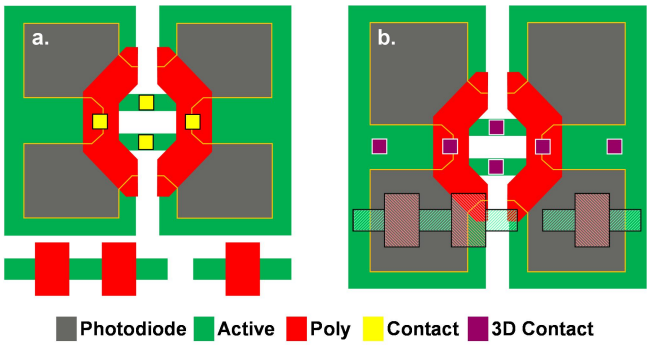

Fig. 6. Shared pixels at photodiode layer: 2D (a.) vs. 3D (b.). Photodiode area (in grey) is increased by 44% when the three readout transistors are placed at the top tier. Courtesy of [4].

the sum of parasitic capacitances at the SN node and C_{GS}, C_{GD} are the gate to source and gate to drain capacitances of the SF.

The gain G_{SF} of the SF is expressed as:

$$G_{SF} = \frac{g_{m,SF}}{g_{ms,SF}} = \frac{1}{n} \quad (2)$$

where $g_{m,SF}$ and $g_{ms,SF}$ are respectively the gate and source transconductances and n is the body factor of the source follower. In the case where the BG of the SF can be tied to the source then the gain is approximately equal to unity, otherwise it is process- dependent and is given by $n=1+\gamma$, where γ is the back-bias efficiency. As the ILD thickness is increased, n approaches unity. In our case, for the γ values extracted in the previous section, the gain G_{SF} of the NMOS device is 0.97 and for a PMOS one is 0.96.

The cutoff frequency (f_c) of the SF is given by [13]:

$$f_c = \frac{g_{m,SF}}{2\pi \cdot C_{out,SF} \cdot G_{SF}} \quad (3)$$

where $C_{out,SF}$ is the capacitance seen at the source of the SF, that is the column-level capacitance if there is no other stage in between.

Parasitic extraction was performed concerning a single-tier (2D) and a two-tier layout (3D) implementation of our pixel as illustrated in Fig. 6, to evaluate the impact of the latter on CG and f_c. The parasitic capacitances contributing to C_{SN}, C_{GD}, C_{GS}, $C_{out,SF}$ and also the CG are presented in Table I. As evaluated, the sum of C_{SN} and C_{GD} as well as C_{GS} are slightly enhanced by 48aF and 44aF respectively. An even smaller increase of 10aF for the column-level capacitance is obtained. This shows a negligible difference in the conversion gain and the AC response of the 3D pixel (yielding in a ΔCG of 0.377µV/e^- and a Δf_c of 0.244Hz) compared to the one processed in planar SOI technology as long as the BOX (equivalently the ILD in 3DSI) thickness is the same. The low 3D impact on the CG also implies that noise performance will not be deteriorated.

B. Impact of TG coupling on pixel electrical parameters

Fig. 7 shows the voltage at the output of the in-pixel SF transistor versus the number of photo generated electrons at the sense node for the voltage bias limits of the bottom tier TG (0V-2.5V). The conversion gain is the slope of the latter and is not altered with the TG coupling. The constant vertical shift can be considered as an offset that can be easily corrected during the readout process.

TABLE I. 2D VS 3D PARASITIC CAPACITANCES & CG

	C_{SN} + C_{GD} [fF]	C_{GS} [fF]	$C_{out,SF}$ [pF]	CG (µV/e^-)
2D	4.432	1.093	2	34.319
3D	4.48	1.137	2	33.942

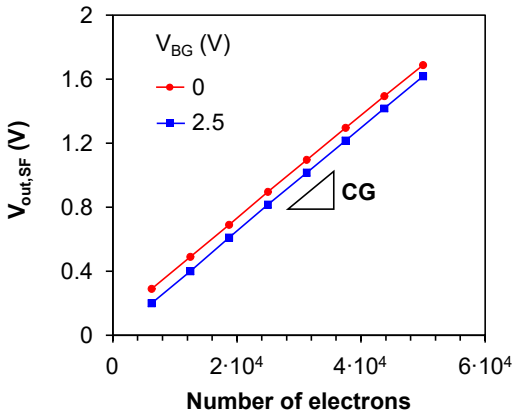

Fig. 7. Output voltage of the in-pixel SF transistor versus the number of photo generated electrons at the sense node for the voltage bias limits of the bottom tier TG (0V-2.5V). The slope gives the conversion gain that is not altered with the TG coupling.

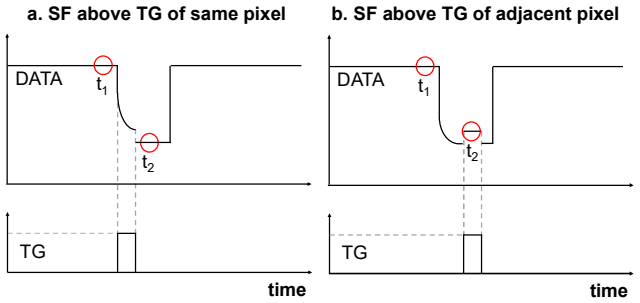

Fig. 8. (a) For SF above a TG of the same pixel, the TG switches ON during the transfer of e- from PPD to the SN. The sampling is thus performed at t_1, t_2 without readout error (b) In the scenario of a SF placed above a TG of an adjacent pixel, the sampling can contain erroneous value due to TG coupling.

To evaluate the impact of the TG coupling on the pixel readout operation, we simulated a readout cycle as the one shown in Fig.5(b). We examined two cases, one where the SF is placed at the top-tier above a TG which belongs to the same pixel as in (Fig.8(a)), and one for which the SF is placed above a TG of an adjacent pixel, illustrated in Fig.8(b). In the first case the TG switches ON during the transfer of e^- from the PPD to the SN and the sampling is thus performed at t_1, t_2 without resulting in a readout error. In the second case, where the TG switching is not synchronized with the top-tier SF device, the sampling value may be compromised due to the TG switched ON.

Fig.9(a) shows the readout error resulting from the non-corresponding TG-SF case versus the number of photo generated electrons at the sense node, for three bias currents of the SF, from low to medium. As expected, a low SF bias current at low light intensity can maximize the readout error at the output of the SF. To assess the strength of this error we compared it with the readout error caused by temperature variations (253K - 353K), with the impact of the latter shown in Fig.9(b). As observed, the temperature effect is in the same order of magnitude and for low SF bias current it can even be worse than the coupling effect. However, because it remains constant with light intensity it is easier to compensate for it later in the circuit.

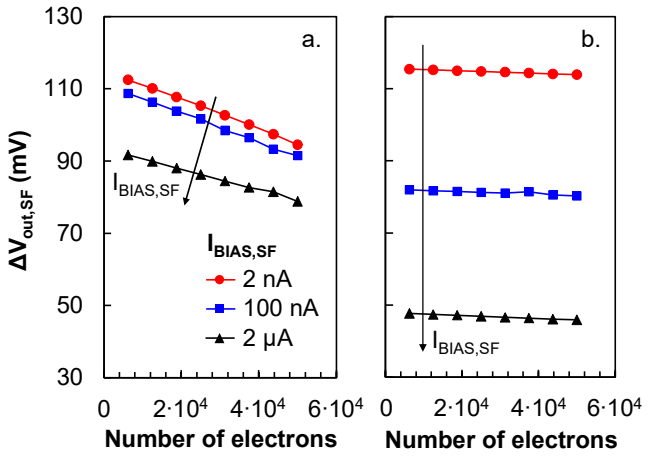

Fig. 9. Readout error of the in-pixel SF transistor versus the number of photo generated electrons at the sense node resulting from (a) the SF-TG coupling of Fig.7(b), and (b) the sensor temperature variation.

C. *Inter-tier Ground Plane necessity*

Recent studies [14], [15] have examined the feasibility of integrating an inter-tier Ground plane in 3DSI that can act as an efficient decoupling layer between sensitive tiers. The necessity for an inter-tier Ground Plane integration results from the specifications targeted for each application and is eventually a trade-off between the process complexity and the inter-tier coupling sensitivity. For example, an inter-tier Ground Plane has been shown to reduce the vertical static coupling by five orders of magnitude [15].

Fortunately, in a typical rolling readout, each row of a pixel array is enabled sequentially, so there is no overlapping of timing diagrams for adjacent pixels. Consequently, there is no probability of a readout error due to TG coupling. Moreover, the Correlated Double Sampling (CDS) stage that exists commonly after the readout circuit, eliminates possible readout errors. This means that even with no intermediate isolating Ground Plane, the Monolithic 3D Imager readout is immune to inter-tier coupling effects. However, if additional blocks are intended to be placed above the photodiode area, like in-pixel frame memory where the leakage current is a significant parameter, then an inter-tier GP is mandatory.

IV. Conclusions

A simulation study of inter-tier coupling-induced effects in a PMOS pixel realized in 3DSI has been presented. At a device level it is shown that the impact of the TG coupling can result in an alteration of the electrical parameters as significant as the one resulting from a temperature variation of 100 degrees, especially for switch transistors for which leakage is a critical parameter. Regarding the in-pixel SF transistor at circuit level, it was shown that there is negligible impact on the conversion gain and the AC performance due to the 3DSI compared to a planar one. Furthermore, the SF-TG coupling can result in a readout error only when the SF is placed above a TG of an adjacent pixel, therefore not synchronized with the pixel readout. However, in a typical rolling readout this is not possible due to the sequential pixel activation. Moreover, possible readout errors are eliminated if a CDS stage in included after the readout circuit. Consequently, we demonstrated that despite the strong electrical coupling and consequently high ΔV_{TH} (~100mV) for top-tier devices, there is an inherent readout error immunity of a sequentially integrated 3D CIS.

Acknowledgement

The authors would like to thank Josep Segura for the fruitful discussion. This work was partially supported by the LabEx Minos ANR-10-LABX-55-01 program and the H2020 3DMUSE European project.

References

[1] L. Millet et al., "A 5500-frames/s 85-GOPS/W 3-D Stacked BSI Vision Chip Based on Parallel In-Focal-Plane Acquisition and Processing," in IEEE Journal of Solid-State Circuits, vol. 54, no. 4, pp. 1096-1105, April 2019, doi: 10.1109/JSSC.2018.2886325.

[2] H. Kim et al., "5.6 A 1/2.65in 44Mpixel CMOS Image Sensor with 0.7µm Pixels Fabricated in Advanced Full-Depth Deep-Trench Isolation Technology," 2020 IEEE International Solid- State Circuits Conference - (ISSCC), San Francisco, CA, USA, 2020, pp. 104-106, doi: 10.1109/ISSCC19947.2020.9062924.

[3] Albert J.P. Theuwissen, CMOS image sensors: State-of-the-art, Solid State Electronics, Volume 52, Issue 9, 2008, Pages 1401-1406, doi: 10.1016/j.sse.2008.04.012.

[4] P. Coudrain et al., " Investigation of a Sequential Three-Dimensional Process for Back-Illuminated CMOS Image Sensors With Miniaturized Pixels," in IEEE Transactions on Electron Devices, vol. 56, no. 11, pp. 2403-2413, Nov. 2009, doi: 10.1109/TED.2009.2030990.

[5] P. Vivet et al., " Advanced 3D Technologies and Architectures for 3D Smart Image Sensors," 2019 Design, Automation & Test in Europe Conference & Exhibition (DATE), Florence, Italy, 2019, pp. 674-679, doi: 10.23919/DATE.2019.8714886.

[6] P. Batude et al., "3D Sequential Integration: Application-driven technological achievements and guidelines," 2017 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, 2017, pp. 3.1.1-3.1.4, doi: 10.1109/IEDM.2017.8268316.

[7] L. Brunet et al., "First demonstration of a CMOS over CMOS 3D VLSI CoolCube™ integration on 300mm wafers," 2016 IEEE Symposium on VLSI Technology, Honolulu, HI, 2016, pp. 1-2, doi: 10.1109/VLSIT.2016.7573428.

[8] C. Cavalcante et al., "Low temperature high voltage analog devices in a 3D sequential integration," 2020 International Symposium on VLSI Technology, Systems and Application (VLSI-TSA), Hsinchu, Taiwan, 2020.

[9] S. International, Atlas user's manual: Device simulation software, 2018.

[10] A. Amara and O. Rozeau, "Planar Double-Gate Transistor from Technology to Circuit", 1st ed., New-York, USA: Springer, 2009, doi: 10.1007/978-1-4020-9341-8.

[11] G. Groeseneken, J. -. Colinge, H. E. Maes, J. C. Alderman and S. Holt, "Temperature dependence of threshold voltage in thin-film SOI MOSFETs," in IEEE Electron Device Letters, vol. 11, no. 8, pp. 329-331, Aug. 1990, doi: 10.1109/55.57923.

[12] V. K. Khanna, "Temperature dependence of electrical characteristics of silicon MOS devices and circuits," in Extreme-Temperature and Harsh-Environment Electronics Physics, technology and applications, IOP Publishing, 2017. doi: 10.1088/978-0-7503-1155-7ch5.

[13] B. Fowler, "Single photon CMOS imaging through noise minimization," in Single-Photon Imaging. Berlin, Germany: Springer-Verlag, 2012. doi: 10.1007/978-3-642-18443-7_8.

[14] A. Vandooren et al., "Buried metal line compatible with 3D sequential integration for top tier planar devices dynamic Vth tuning and RF shielding applications," 2019 Symposium on VLSI Technology, Kyoto, Japan, 2019, pp. T56-T57, doi: 10.23919/VLSIT.2019.8776490.

[15] P. Sideris et al., "Inter-tier Dynamic Coupling and RF Crosstalk in 3D Sequential Integration," 2019 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2019, pp. 3.4.1-3.4.4, doi: 10.1109/IEDM19573.2019.8993493.