An integrated dual-side series/parallel piezoelectric resonator-based 20-to-2.2v DC-DC converter achieving a 310% loss reduction

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An Integrated Dual-side Series/Parallel Piezoelectric Resonator-based 20-to-2.2V DC-DC Converter Achieving a 310% Loss Reduction

Piezoelectric resonators (PRs) have recently emerged as an attractive substitute for inductors to process energy in DC-DC converters, due to their low-volume planar form-factors, superior volume/frequency scaling capabilities, very high *Q*, ability to be batch fabricated at low cost, and integration potential directly into Si (Fig. 1 top left) [1-3]. The baseline PR converter described in the literature [1] (Fig. 1, top right), achieves high efficiency by operating the PR in the inductive region and enabling zero-voltage switching (ZVS) and soft-charging of the PR's junction capacitor, C_P. However, as shown in Fig. 1 (bottom left), the PR's utilization factor, *K*, is maximal at a voltage conversion ratio (VCR) of 0.5, and falls off rapidly at lower VCRs [1]. At the lower VCRs demanded by many modern DC-DC applications (e.g., VCR<0.1), the PR mostly circulates current within itself, leading to a high peak resonant current, $I_{LPR(pk)}$, high PR vibration losses, and poor efficiency. Recent art has suggested adopting a hybrid switched-capacitor (SC) / PR-based structure, where the SC network provides part of the voltage conversion to allow for the PR to operate with a higher *K* and to distribute the voltage drop across low-voltage transistors [4,5]. However, such prior art only includes a single flying capacitor, which limits the optimal conversion ratio to only 0.25-0.33. Importantly, no IC-based PR converter has been demonstrated in the literature to date, and no work has reported operation at low voltage outputs with a high step-down ratio (e.g. V_{in}>10V, V_o<2V).

This paper presents a hybrid Dual-side Series/Parallel PR (DSPPR) converter IC, shown in Fig. 1 (bottom right) that exploits the ability of ICs to offer sophisticated power stages in a small area compared to discrete design, all towards efficient operation at VCRs<0.1. The proposed DSPPR topology: 1) merges 2:1 series/parallel SC networks at both its input (frontside) and output (backside) without causing cascaded losses, resulting in an optimal VCR of 0.125 while reducing active area (switch and driver) thanks to IC integration by 13-23x compared to discrete designs; 2) exploits transistor stacking, popularized by hybrid converters, to reduce voltage stress on power transistors from (V_{in}-V_o) on

S1-S5 to (~$V_{in}/2$) on S1-S4 and ($V_{in}/2$-V_o) in S5, which reduces the cumulative VA (=V_{ds} x I_{rms}) rating across S1-S5 by 67% compared to the baseline PR converter and reduces the transistor area by 60%; 3) positions the PR in the middle of the converter where the equivalent input/output voltage of the PR are respectively lower and higher compared to the baseline PR converter, leading to a 7x PR loss reduction and 2.5x increased output current capability; 4) maintains ZVS of S5-S9 and soft charging of C_P by keeping the same general operating phases as the baseline PR converter [1]; 5) soft-charges the frontside flying capacitor, C_{F1}, via the inductive nature of the PR; and 6) self-balances the backside flying capacitor, C_{F2}, enabling ZVS for S10 and S11. All of these techniques culminate in a loss reduction of 310% and 212% and overall efficiency improvement of 17.1% and 9.9% compared to a co-fabricated discrete baseline PR converter [1] and Frontside SPPR converter (FSPPR) [4], respectively, at 20V-to-2.2V, 0.1A with the same PR.

The operation states, waveforms, and SC modes are shown in Fig. 2. The operation principle of the DSPPR converter is the same as the baseline PR converter in that there is a sequence of 7 phases, yet here phases 1 and 2 alternate their connection (series, S, or parallel, P) to the frontside SC circuit such that control complexity is not increased. Throughout the 7 phases, the PR can be in one of three states: (1) opened PR, (2) connected PR, and (3) shorted PR. Initially, there are no current paths formed by switches in phase 1, and hence, in this opened PR state, the sinusoidal current formed by the PR, $I_{L,PR}$, discharges C_P. In phase 1S, C_{F1} is connected in the up (series) position, while in the subsequent cycle, in phase 1P, C_{F1} is connected in the down (parallel) position. Once V_{P2} reaches $V_{o,PR}$, S6, S7, and S11 are activated with ZVS, and phase 2 begins, connecting the PR to the input and output for energy delivery. Here, C_{F1} is soft-charged in phase 2S and soft-discharged in phase 2P due to $I_{L,PR}$, ensuring charge balance. On the other hand, C_{F2} is in series with the load in both phases 2S and 2P. Phase 3 starts with deactivating switches S1-4, enabling the opened PR state, where $I_{L,PR}$ discharges C_P until V_{P1}=$V_{o,PR}$, enabling ZVS turn-on for S5. Then, phase 4 initiates, forming a shorted loop where $I_{L,PR}$ circulates until its polarity reverses, after which switches S6, S7, and S11 are opened. This brings the PR back to an open PR state in phase 5, discharging V_{P2} until it reaches zero and enabling ZVS turn-on for S8-10. At this point, C_{F2} is in parallel with the load, and the PR is linked to the output, allowing the PR

to release energy to the load. Phase 7 begins when S5 turns off, opening the PR, where $I_{L,PR}$ charges C_P until V_{P1} reaches $V_{in,PR}$, minimizing switching loss across S1,3/S2,4 in the next SC cycle.

All of the power switches of the DSPPR are implemented by on-chip nMOS transistors with carefully optimized voltage ratings (Fig. 1 bottom right) and sizes. Since multiple power transistors are floating relative to ground, a compact yet efficient driving and level shifting scheme is required. Here, a stacked bootstrap driver approach is employed, where the high-side transistor draws power from its neighboring low-side transistor. For instance, consider the frontside SC network in Fig. 3 (left): when $S_{1,3}$ is set, C_{B2} charges from C_{B3}; conversely, when $S_{2,4}$ is set, C_{B1} and C_{B3} charge from C_{B2} and V_{DD}. By repeating this bootstrap operation, all the floating switches can be properly driven from a ground-referenced V_{DD}, and the same logic is applied to the remaining floating transistors. However, the actual driving voltage of the floating transistor is influenced by several factors, including bootstrapping capacitance, time, and power consumption. Fig. 3 (bottom right) illustrates the V_{BTS} and ΔV_{BTS} trade-off with the value of bootstrap capacitance, C_{BTS}, where an acceptable trade-off between 80 to 200nF is observed; 0402 150nF capacitors are selected for this work. Level shifting is accomplished via the circuit in Fig. 3 (top right), based on [6], that is briefly activated only when an edge-triggered pulse is received, resulting in a power of only ~200μW and propagation delay of 2ns. This design consists of two identical level shifters, *PLS* and *NLS*, responsible for positive and negative edge level shifting, respectively. In operation, positive/negative-edge pulses (*PEP* and *NEP*) are generated and fed to their respective level shifters. As *PEP* is set, for example, current flows through the M_n branch and is mirrored by M_{P1} and M_{P2}, charging Out_{PLS} and generating a set pulse for the SR latch. When PEP is reset, M_{nHV2} pulls down Out_{PLS}.

The proposed DSPPR converter IC is fabricated in a 180nm BCD process with a die area of 6mm^2 and operates with 20/0.2mm (diameter/thickness) PIC181 PZT COTS PR , 4x10μF 0603 flying/output capacitors, and 9x150nF 0402 bootstrap capacitors. Owing to the lack of low-voltage PR-based converters in literature, a discrete prototype, reconfigurable between baseline PR and FSPPR converters, is implemented using GaN FETs for direct comparison with prior-art topologies. Steady-state measurements of the DSPPR IC in Fig. 4 (top left), reveal that C_{F1} undergoes

soft-charging/discharging through I_{LPR}, achieving ZVS across S5-S11. In contrast, waveforms for the baseline PR converter (Fig. 4 top right) exhibit shorter energy transfer times and longer current circulation intervals, indicating higher peak resonant current and increased PR vibration losses. Efficiency comparisons among DSPPR, FSPPR, and baseline PR converters under varying input, output, and load conditions are depicted in Fig. 4 (bottom), showcasing 1.7x and 2.5x increased output capability compared to the FSPPR and baseline PR converters thanks to the SC circuits enabling smaller circulating PR currents, ultimately pushing the design towards the current limits allowed by the chosen PR (which was not optimized for power applications) at the given conditions. The proposed DSPPR IC outperforms the other two across all test points, with an up to 310% loss reduction (corresponding to 17% higher efficiency) at 20V-to-2.2V at 0.1A. Fig. 5 shows the efficiency of the DSPPR converter across different input/output ranges at a fixed output current, reaching a peak efficiency of 88.7% at 20V-to-2.2V. The frequency variations are also presented in Fig. 5 (bottom right), showcasing a larger utilization of the region between the resonant and anti-resonant frequencies, which are measured and modeled in Fig. 6 (top left).

A table of comparisons is shown in Fig. 6 (bottom). The DSPPR is the first IC used for PR-based power conversion, and achieves up to 310% loss reduction over prior-art published and co-designed discrete designs for VCRs<0.125. It is also the first PR converter to operate at VCRs<0.1. The theoretically best achievable efficiency assuming 70% die area allocation to power transistors is 90.7% (Fig. 6 top right), which is within 2% of measurements due to imperfections in on/off timing and PR harmonics; using the same assumptions, a baseline PR converter would achieve 67.3% efficiency, representing a 473% loss reduction, which is worse than the discrete prototype due to the higher on-resistance of high-voltage transistors that do not benefit from FCML-like stacking as in the DSPPR in a limited die area. Fig. 7 shows only a 7% extra passive footprint added by the flying capacitors, but a 13-23x active area reduction in the power stage.

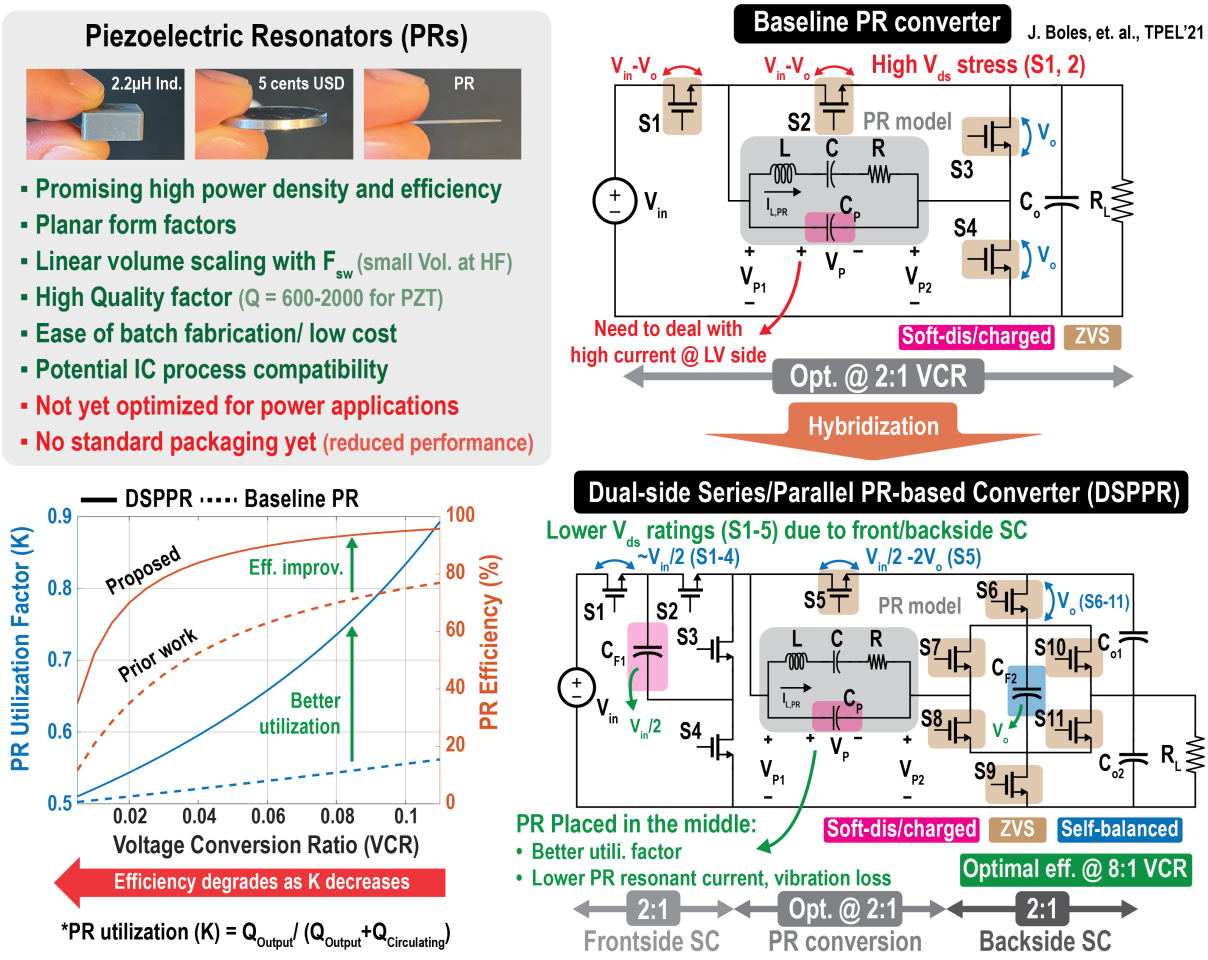


Fig. 1. Introduction to piezoelectric resonators (top left), and comparison of baseline PR (top right) and DSPPR converters (bottom right) along with PR utilization and efficiency analysis (bottom left).

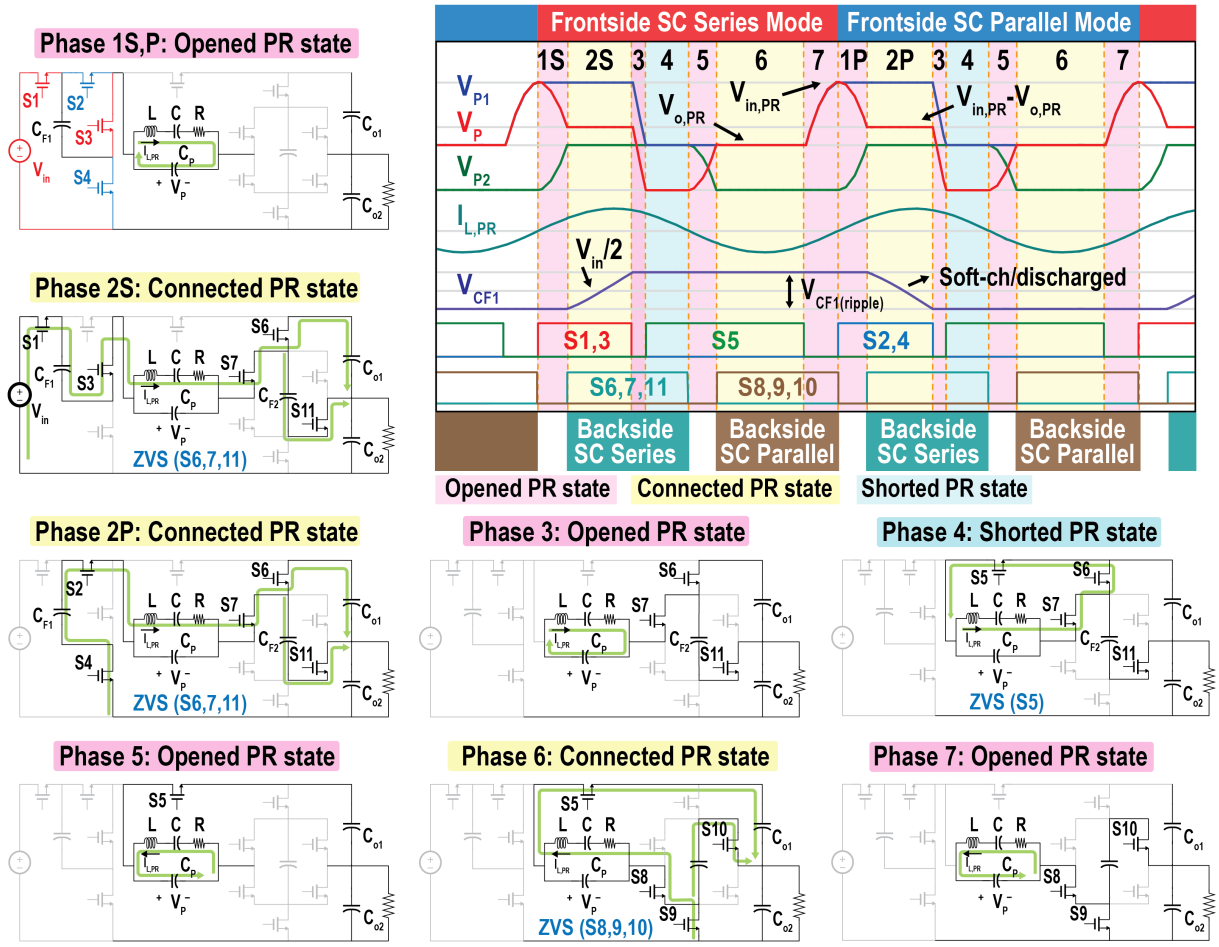


Fig. 2. Operation waveforms and phases of proposed DSPPR converter.

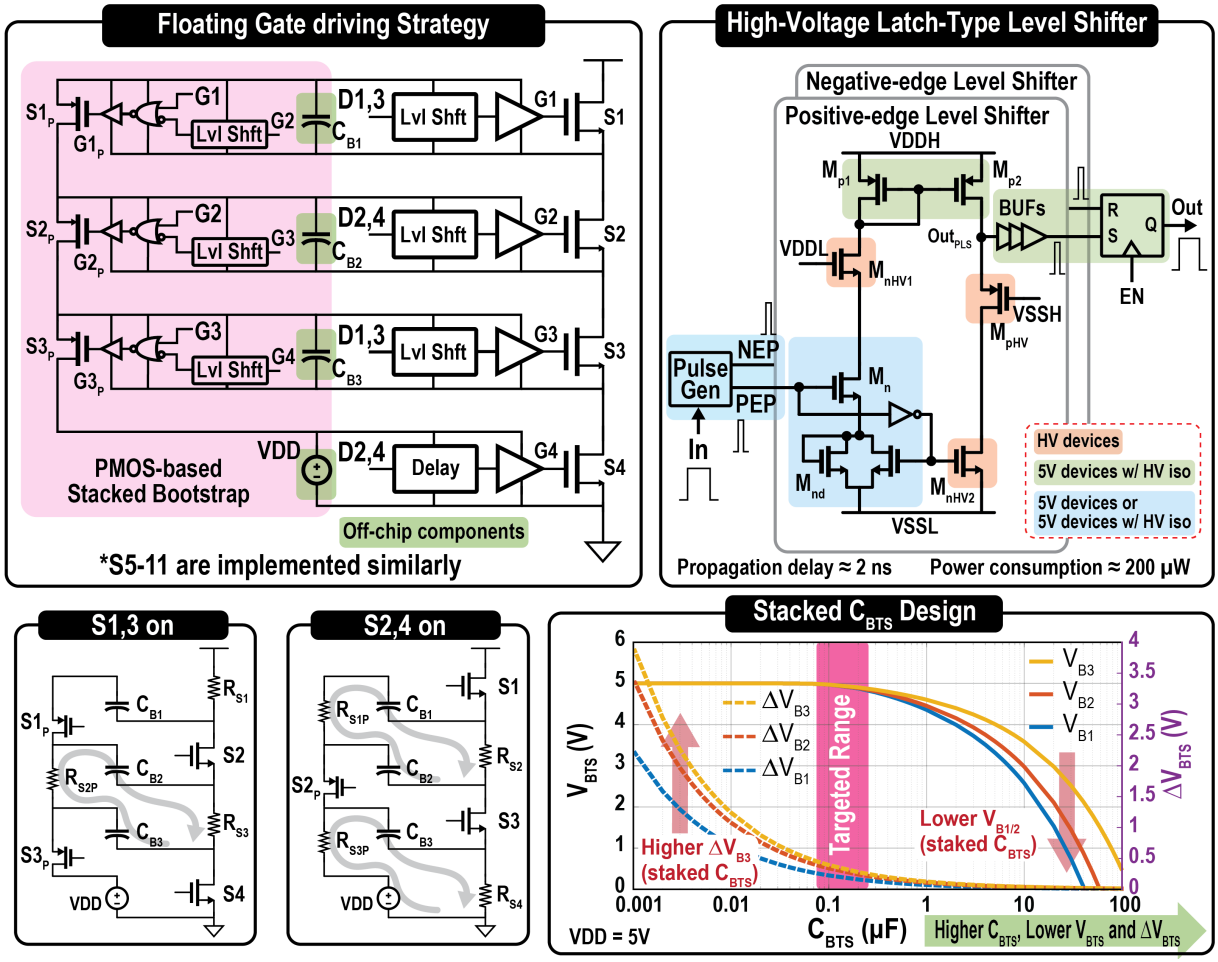


Fig. 3. Stacked bootstrapping strategy (top left), operation (bottom left), bootstrap capacitor design (bottom right), and level-shifter schematic (top right)

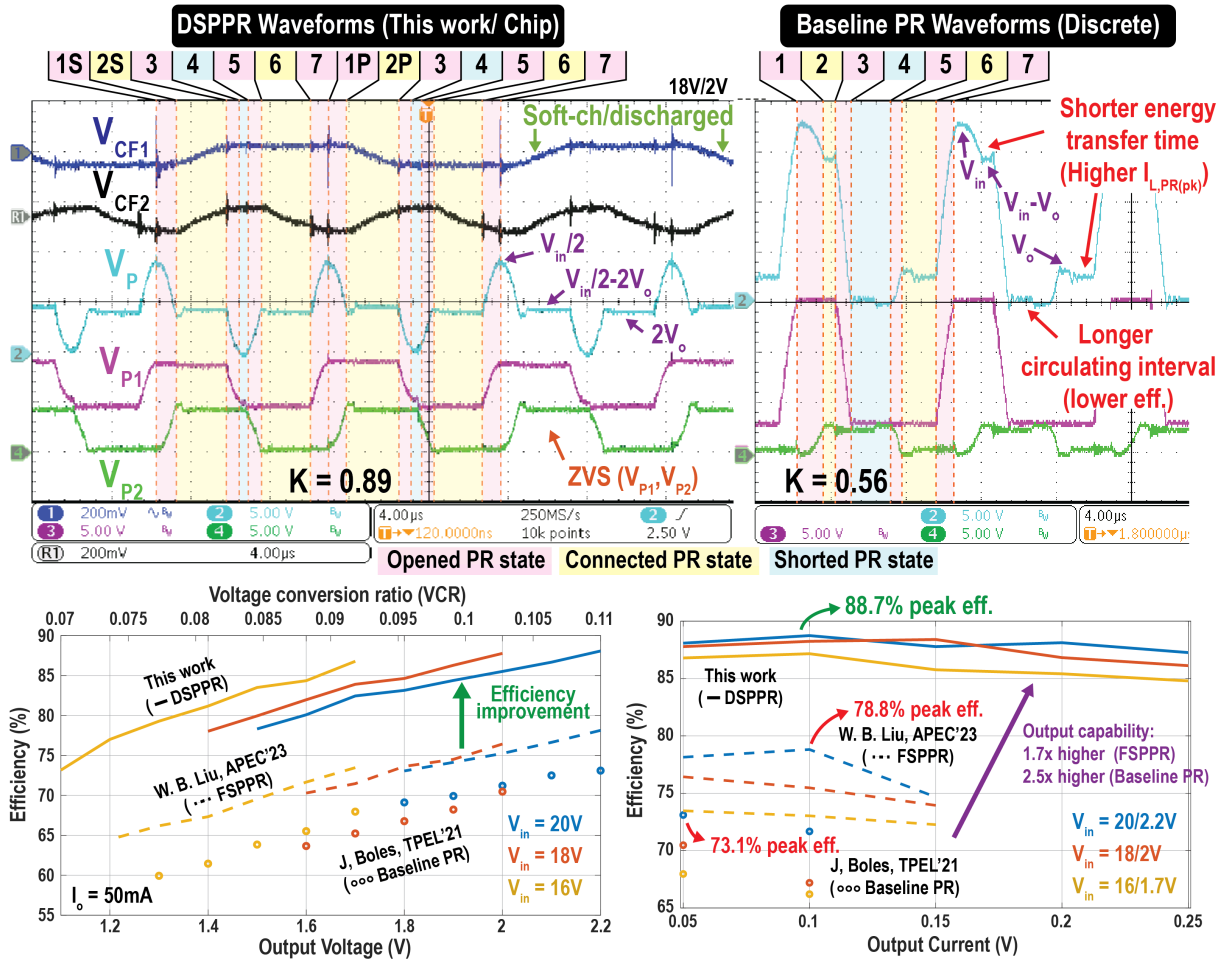


Fig. 4. Measured steady-state waveforms of the DSPPR converter IC (top left) and a baseline discrete converter (top right); measured efficiency compared to FSPPR and baseline discrete co-designs (bottom).

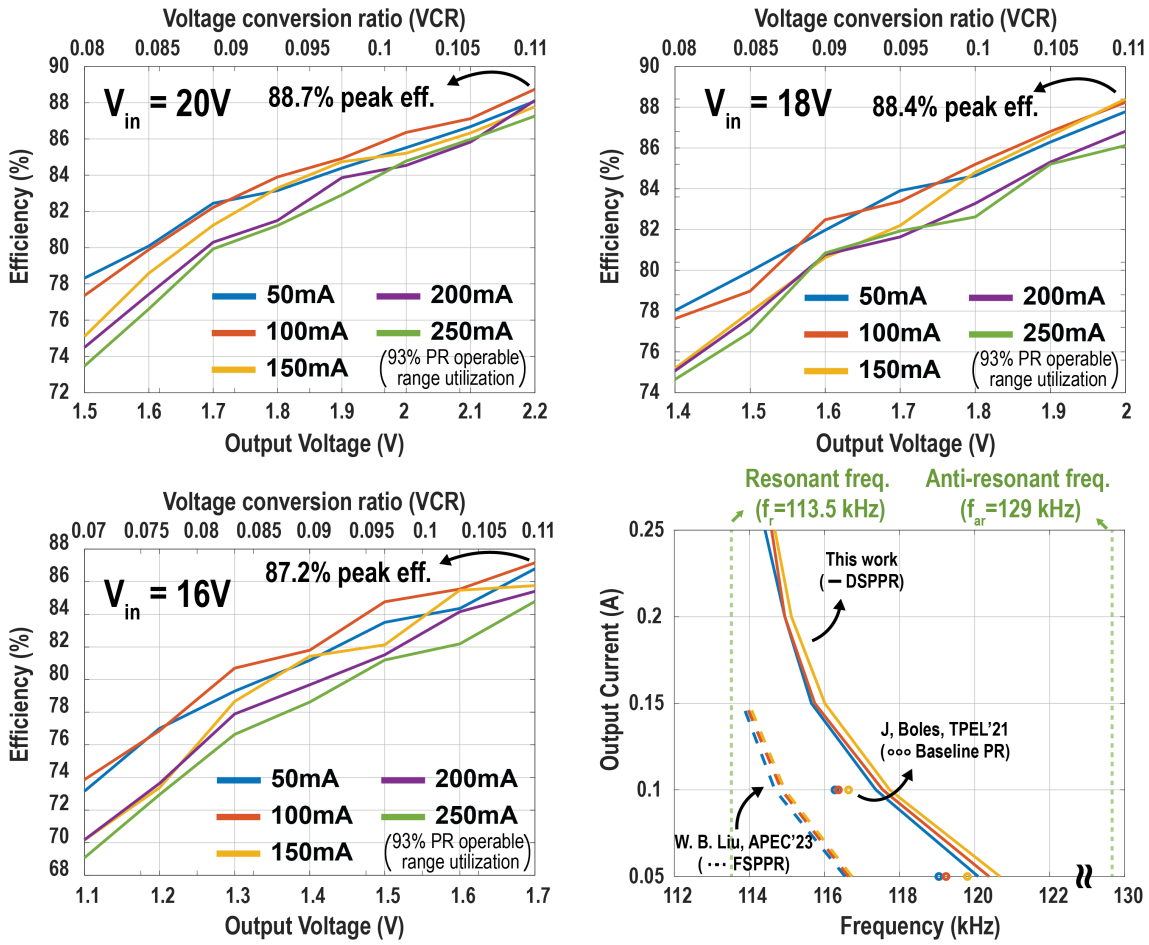
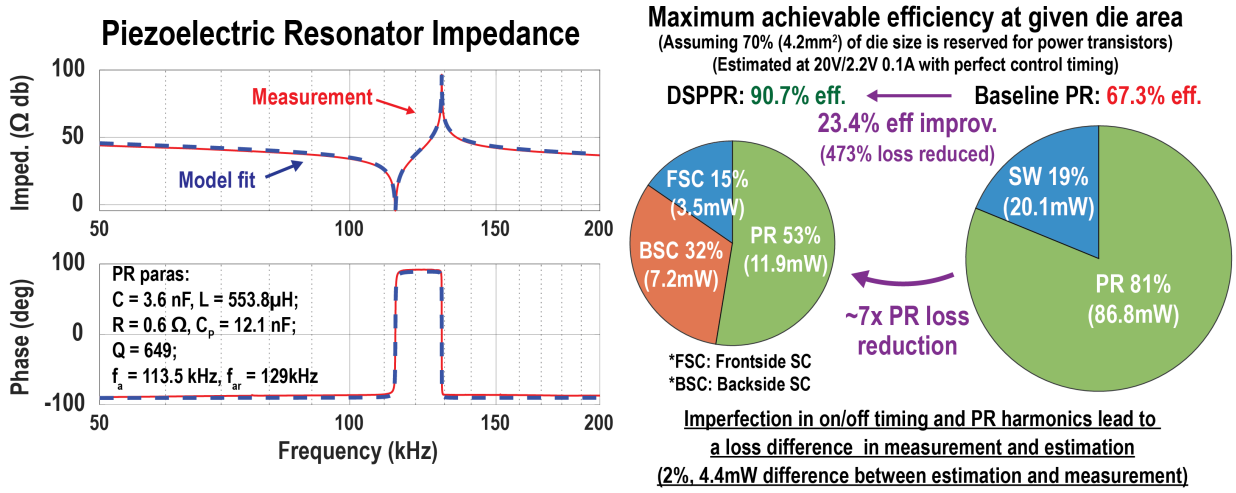


Fig. 5. Measured efficiency and frequency variation of the DSPPR converter over different input/output voltage and load conditions.



	APEC'20 [3]	Discrete test bench		This Work
Technology	Discrete			**180nm HV BCD**
Topology	Baseline PR	Baseline PR	Frontside Series/ Parallal PR (FSPPR)	**Dual-side Series/ Parallal PR (DSPPR)**
PR material	$LiNbO_3$ Y+36° cut	PZT PIC181		**PZT PIC181**
V_{in}/V_o Range	50V/ 10-40V	16-20V/ 1.1-2.2V		**16-20V/ 1.1-2.2V**
Operation frequency	6.3 - 7.1MHz	113-129 kHz		**113-129 kHz**
Die /Power SW Size	GaN (4x 1.74mm²)	GaN (4x 1.82mm²)	GaN (7x 1.82mm²)	**6mm²**
Active PCB area	N.R.	8.16 cm²	14.28 cm²	**0.6cm²**
Peak eff. (@VCR<0.2)	77.5% @ 50/10V (0.2VCR/ 5W)	73.1% @ 20/2.2V (0.11 VCR/ 0.11W)	78.8% @ 20/2.2V (0.11 VCR/ 0.22W)	**88.7% @ 20/2.2V (0.11 VCR/ 0.22W)**
Peak eff. (@20/2.2V, 0.1A)	N.R.	71.7%		

Fig. 6. Piezoelectric resonator impedance characteristics (top left); loss analysis at a given die size (top right), and table of comparisons (bottom).

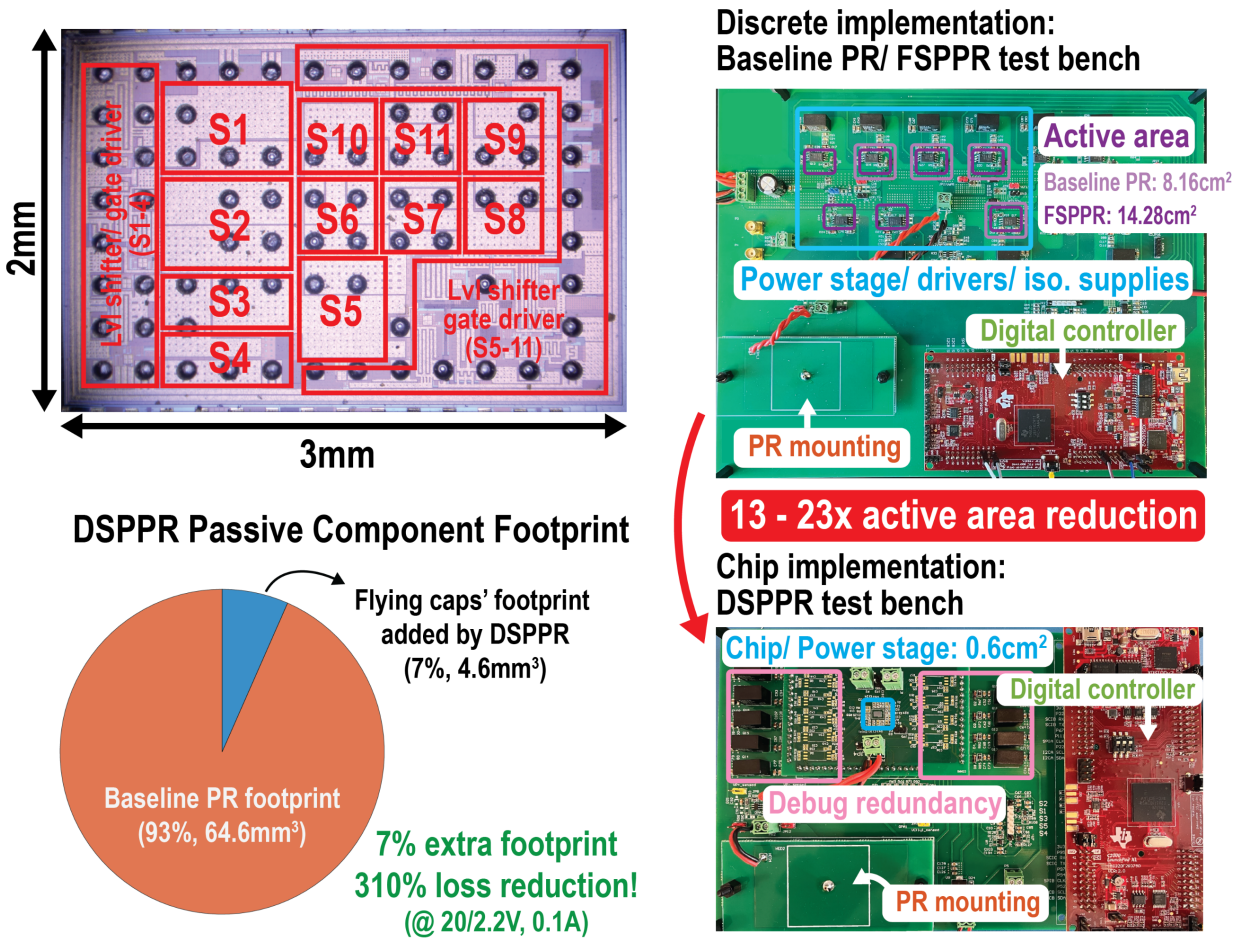
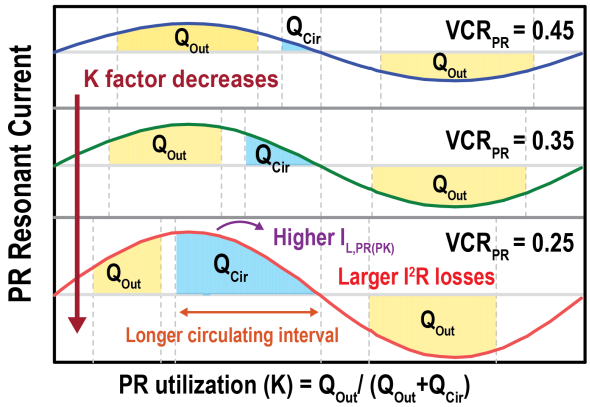


Fig. 7. Die photograph of the proposed DSPPR converter (top left), passive component footprint for the DSPPR converter compared to the baseline PR converter (bottom right), and test bench for chip and discrete designs (right).



Topology	VCR_{PR} (V_o/V_{in}<0.125)	K
Baseline PR	V_o/V_{in}	$\frac{V_{in}}{2(V_{in}-V_o)}$
FSPPR	$2V_o/V_{in}$	$\frac{V_{in}}{2(V_{in}-2V_o)}$
DSPPR	$4V_o/V_{in}$	$\frac{V_{in}}{2(V_{in}-4V_o)}$

Higher PR utilization at low VCR (A lower $I_{L,PR(pk)}$ and I^2R loss)

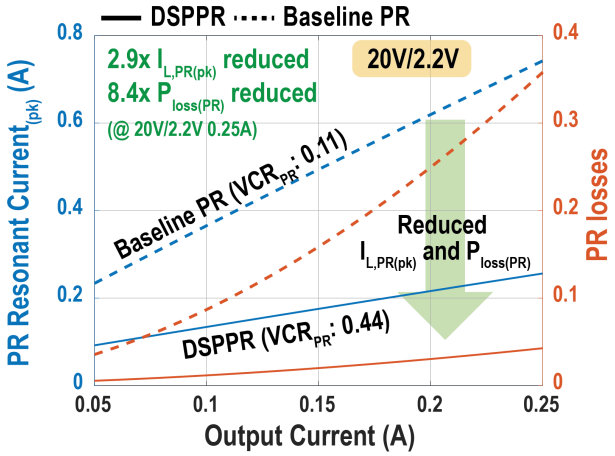


Fig. S1. Relationship of VCR at the PR stage, VCR_{PR}, PR utilization factor, K, and PR resonant current, $I_{L,PR(pk)}$ (top): As VCR_{PR} decreases, the circulating time interval increases, resulting in a higher peak resonant current. At a given VCR(V_o/V_{in}), DSPPR shows the highest VCR_{PR} as well as K, implying superior efficiency. The performance estimation of peak PR resonant current and PR losses for baseline PR and DSPPR converters (bottom left): As per the analysis, the DSPPR converter showcases a 2.9x peak current and 8.4x PR losses reduction due to higher VCR_{PR}.