Session 17 Overview: *DC-DC Converters*

POWER MANAGEMENT SUBCOMMITTEE

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Elegant integrated circuit design techniques are required to further enhance the performance of the next generation of DC-DC converters for various applications such as multi-core microprocessors, energy harvesting, automotive electronics and LED drivers. Novel hybrid combinations of inductors and capacitors, minimizing passive components sizes by operating at GHz, recycling energy from gate drivers using bond wire inductors, and using a single inductor for multiple output power paths for minimal cross-regulation, are some of the techniques presented in this session demonstrating the latest in DC-DC converters at both system and circuit levels.

8:30 AM

17.1 A Two-Stage Cascaded Hybrid Switched-Capacitor DC-DC Converter with 96.9% Peak Efficiency Tolerating 0.6V/µs Input Slew Rate During Startup

Ziyu Xia, Dartmouth College, Hanover, NH

In Paper 17.1, Dartmouth College presents a step-down hybrid switched capacitor converter in a 0.18µm CMOS technology that uses a self-start and self-balance flying capacitor technique and fully integrated drivers. Managing 0-to-5V input transient in less than 10µs, the converter achieves up to 96.9% power efficiency while maintaining <36mV for 1A/µs load step.

8:38 AM

17.2 A Masterless Fault-Tolerant Hybrid Dickson Converter with 95.3% Peak Efficiency 20V-to-60V Input and 3.3V Output for 48V Multi-Phase Automotive Applications

Mojtaba Ashourloo, University of Toronto, Toronto, Canada

In Paper 17.2, the University of Toronto and NXP Semiconductors show a monolithic automotive-grade fault-tolerant 4-to-1 hybrid Dickson PMIC with all the auxiliary circuits on-chip. An integrated mixed-signal quasi-fixed-frequency control and fault-detection scheme enable masterless post-fault operation in a multi-phase configuration. The design is fabricated in a 0.13µm SOI BCD automotive process (SMARTMOS) with 95.3% efficiency at 0.8A load current, 320kHz effective switching frequency, and ⅛ conversion ratio.

8:46 AM

17.3 A 1.25GHz Fully Integrated DC-DC Converter Using Electromagnetically Coupled Class-D LC Oscillators

Alessandro Novello, ETH Zurich, Zurich, Switzerland

In Paper 17.3, ETH Zürich and STMicroelectronics introduce a fully integrated self-oscillating DC-DC topology based on coupled Class-D oscillators delivering up-to 1W/mm^2 at 2.5GHz operating frequency in a 0.18µm CMOS technology.

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8:50 AM

17.4 Peak-Current-Controlled Ganged Integrated High-Frequency Buck Voltage Regulators in 22nm CMOS for Robust Cross-Tile Current Sharing

Nachiket Desai, Intel, Hillsboro, OR

In Paper 17.4, Intel proposes an integrated voltage regulator in a 22nm CMOS technology operating at 60MHz that equilibrates the current sharing between multiple tiles of converters with accuracy as tight as 1.2%. Providing 1A per tile, showing 89.1% power efficiency with down-to 2nH inductor, a peak-current-controlled gang-able buck converter is dedicated to granular power management of multi-core processors.

8:58 AM

17.5 A 98.2%-Efficiency Reciprocal Direct Charge Recycling Inductor-First DC-DC Converter

Abdullah Abdulslam, University of California, San Diego, La Jolla, CA

In Paper 17.5, the University of California, San Diego presents a 3rd-order inductor-first step-down converter in a 0.18µm CMOS technology, achieving 0.72W/mm^2 power density at 98.2% peak efficiency thanks to a reciprocal gate energy recycling. Using only a single 4nH PCB trace inductor, the pragmatic resonant gate driver enables 80% recycling efficiency.

9:06 AM

17.6 A Reconfigurable DC-DC Converter for Maximum TEG Energy Harvesting in a Battery-Powered Wireless Sensor Node

Young-Seok Noh, KAIST, Daejeon, Korea

In Paper 17.6, KAIST shows a reconfigurable DC-DC converter in a 65nm CMOS process with a TEG/battery connection through a SIDO boost and buck structure with a single inductor, achieving 88.5% and 93.3% efficiencies in each mode. The battery TEG pile-up buck and dual-phase buck-boost configuration save up to 44% power from the battery by maximizing the TEG power extraction.

17

9:10 AM

17.7 A 0.03mV/mA Low Crosstalk and 185nA Ultra-Low-Quiescent Single-Inductor Multiple-Output Converter Assisted by 5-Input Operational Amplifier for 94.3% Peak Efficiency and 3.0W Driving Capability

Tzu-Hsien Yang, National Chiao Tung University, Hsinchu, Taiwan

In Paper 17.7, National Chiao Tung University and Realtek Semiconductor propose a single-inductor four-output converter in a 0.153µm CMOS process that includes a shared feedback amplifier to minimize the cross-regulation to 0.03mV/mA and achieve 3W driving capability with 94.3% peak efficiency. A 185nA quiescent mode enables 87.5% power efficiency at light load (10mW).

9:18 AM

17.8 A 90.5%-Efficiency 28.7µV_{RMS}-Noise Bipolar-Output High-Step-Up SC DC-DC Converter with Energy-Recycled Regulation and Post-Filtering for ±15V TFT-Based LAE Sensors

Min-Woo Ko, KAIST, Daejeon, Korea

In Paper 17.8, KAIST shows ±15V bipolar step-up converter from battery with an energy-recycled fine regulation scheme, followed by post linear-regulator with a controlled dropout voltage for reducing the power loss and the switching ripple noise. The chip, fabricated in a 0.18µm BCD process, offers 28.7µV_{rms} output noise and 90.5% peak efficiency.

9:26 AM

17.9 A High-Conversion-Ratio and 97.4% Peak-Efficiency 3-Switch Boost Converter with Duty-Dependent Charge Topology for 1.2A High Driving Current and 20% Reduction of Inductor DC Current in MiniLED Applications

Si-Yi Li, National Chiao Tung University, Hsinchu, Taiwan

In Paper 17.9, National Chiao Tung University and Realtek Semiconductor introduce a 3-switch boost converter to allow 97.4% power efficiency, 7.5 step-up ratio, and 1.2A drive current for driving MiniLED arrays. In this structure, the flying capacitor charging duration increases along the load current, thus expanding the load range and reducing AC and DC inductor currents by 25% and 20%, respectively.