A 2.5μW 0.0067mm 2 automatic back-biasing compensation unit achieving 50% leakage reduction in FDSOI 28nm over 0.35-to-1V VDD range

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A 2.5µW 0.0067mm^2 Automatic Back Biasing Compensation Unit Achieving 50% Leakage Reduction in FDSOI 28nm over 0.35-1V V_{DD} Range

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Worst-case design and post silicon tuning are well-established digital design practices reducing timing violations in presence of process, temperature, aging and voltage variations but they suffer from extra power consumption due to overdesign [1]. Adaptive voltage scaling (AVS) [2] and body bias modulation [1] are well-known strategies to dynamically ensure that the digital core can operate at a targeted frequency, even in the presence of delay degradation due to variations. In a multiple voltage islands context, AVS requires many integrated supply generators such as switched capacitor converters that need to be controlled accurately. Also, for a fine-grain compensation, level shifters are required impacting a lot the circuit performances. As FDSOI technology offers the ability of adjusting the transistor speed through high sensitivity (85mV/V_{BB}) V_{TH} tuning by acting on buried Nwell (NW) and Pwell (PW) voltages, back biasing generators have been investigated [3-5]. However, they require an external controller to reach the optimal Back Bias (BB) voltages (no self-adjustment) [3-4] and [5] has a non-negligible area overhead for sub-mm^2 digital core for a narrow compensation range limited to 0.35-0.45V V_{DD}. We therefore propose a variation-aware BB Compensation unit (BBC) which dynamically self-adjusts the N- and P-MOS transistors BB voltages to maintain the target frequency with low-latency tuning (100µs) across wide ranges of supply voltage (0.35-1V) and temperature (-40-125°C). The very low reported area of 0.0067mm^2 makes it affordable for a small digital core area (0.1-2mm^2). Requiring only a reference frequency signal F_{TGT}, the proposed self-operating BBC exhibits 2.5µW quiescent current without any external component. Compared to worst-case design strategy, BBC brings up to 50% leakage reduction @0.45V_{DD}@120°C and reduces the energy per cycle up to 32% compared to worst case design. Providing a continuous BB voltage adjustment (continuous V_{TH} tuning), the target frequency is maintained within a +3.5% accuracy.

As shown Fig.1, BBC tracks the digital frequency F_{DIG} of on-chip critical path replica (CPR). F_{SENSE}, divided from F_{DIG}, is compared to the target frequency F_{TGT} by using a phase frequency detector (PFD) sending up or down NW voltage commands to an NW driver. A second compensation circuit ensures symmetrical biasing between NW and PW with the use of a Middle Sensor (MS) and a fully-integrated negative switched-capacitor converter able to provide -1.5V@0.6mm^2 digital core area (C_{FLY}=8pF). The chip is composed of the BBC unit compensating a 0.6mm^2 LVT digital core consuming around 50mW. The pull-up/down drivers' resistors are set to allow positive and negative 60mV/µs slew rates and limit the BBC loop gain. The BB drivers is able to load NW and PW equivalent capacitors (1nF each) and 1.2nF PW/NW coupling capacitor. The BBC unit sets a digital flag BB_{OK} when the target frequency is reached by the digital core. The internal sequencing is done by a state machine using an F_{SENSE} clock.

Fig. 2 illustrates the three main compensation configurations where V_{PW} and V_{NW} are adjusted sequentially according to CPR and MS, respectively. First, an N counter from a fractional frequency of F_{DIG} ensures comparison with the divided target frequency F_{TGT2}. If N+ΔN periods are counted before $T_{TGT2}/2$, V_{NW} is decreased by activating pull-down resistors in NW drivers until the next falling edge of F_{TGT2}. On the contrary, NW is decreased until NxT_{SENSE}-$T_{TGT2}/2$ if the N period is not counted before $T_{TGT2}/2$. During the last quarter of the F_{TGT2} period, MS is enabled to compare V_{NW} and $V_{PW,}$ and then V_{PW} is adjusted to be equal to $–V_{NW}$. When a steady state is reached, BBC senses F_{DIG} at the F_{TGT} rate and eventually compensates the drift voltage due to the body leakage (0.28µA/mm^2@125°C/1.4V_{NW}) by activating UP or DOWN signal during T_{SENSE}. Middle Sensor (MS) block, as detailed Fig. 3, ensures an optimal symmetrical well polarization within 20mV V_{MID}. An hysteresis is realized by mismatching the R and R' resistance values. MS is only activated by enabling EN_{MID} during the last quarter of the F_{TGT2} period to decrease the averaged BBC quiescent current.

Fig. 4 depicts the frequency compensation for temperature w/ or w/o BBC. When both Well voltages are set to zero@125°C, F_{DIG} decreases from 9MHz@125°C to 6MHz@-40°C. When the BBC is enabled, V_{NW} increases from 0V@125°C to 0.5V@-40°C to maintain the 9MHz targeted frequency (M=8). The Well voltage resolution is theoretically unlimited as BBC drivers are analogically controlled. Fig. 4 also shows the start-up phase when BBC is turned-on. The

steady state is reached in less than 200µs and BB_{OK} flag is set to be used at system-level. Even if the BBC is not dedicated to power supply droops compensation, Fig. 4 shows the dynamics of BB voltages for an abrupt 100mV V_{DD} step. The NW ramps up from 0.92 to 1.23V in less than 90µs to compensate for the frequency decrease.

Fig. 5 explores BBC energy-efficient ability by showing the normalized leakage current w/ and w/o BBC over -40 to 125°C. By self-adapting V_{NW} from 1.2V@-40°C to 0.9V@125°C (and PW accordingly) while meeting frequency requirement, the leakage current is reduced by 50%@125°C compared to w/o BBC, at near threshold operation ($0.45V_{DD}$). The energy dissipation per cycle is also reduced by 32%@$0.45V_{DD}$ with a 5% activity factor compared to worst case design. F_{SENSE} can be regulated from F_{TGT} set value over x5.4 frequency range at near threshold operation (0.375V) and x1.4@1V, indeed the back biasing effect is proportional to the V_{TH} to V_{DD} ratio. The ratio between F_{TGT} and F_{SENSE} is maintained within two F_{SENSE} cycles which represents a precision of 3.5%.

Fig. 6 compares our variation-aware back biasing system to the most relevant published works. The main benefits are the self-control loop capability, refreshing back biasing at F_{TGT} rate, over a full V_{DD} range (0.35-1V). In addition, the BBC has a negligible power (2.5µW@$0.375V_{DD}$), very small 0.7%/mm^2 area overhead and dynamically compensates variations (process, temperature, aging) because of its 100µs time constant. Even if only FBB is shown in this paper as LVT devices were used, the system is compatible with reverse BB (RBB) polarization with RVT devices. The proved BBC seamless capability enables compensating at near threshold operation for the small-area digital core used for IoT, or at full supply voltage for core-to-core variations in large digital SoC with a sub-mm^2-scale grain due to within-die device parameter variations. It also reduces the need for challenging power supply scaling and/or low efficiency worst-case design strategies.

References:

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microprocessor frequency and leakage," *IEEE Journal of Solid-State Circuits*, pp. 1396–1402, Nov. 2002.

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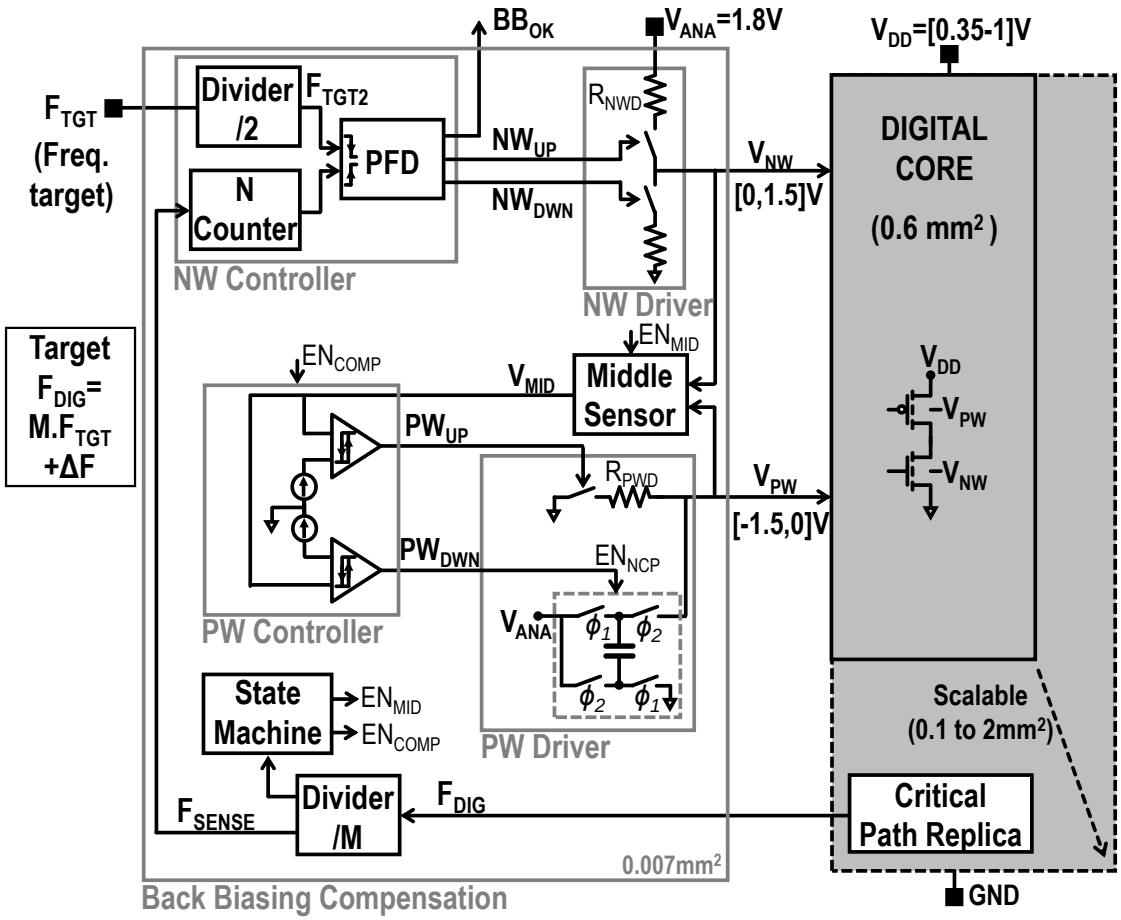

Figure 1: Main building blocks of back biasing compensation unit embedded with a sub-mm² digital core.

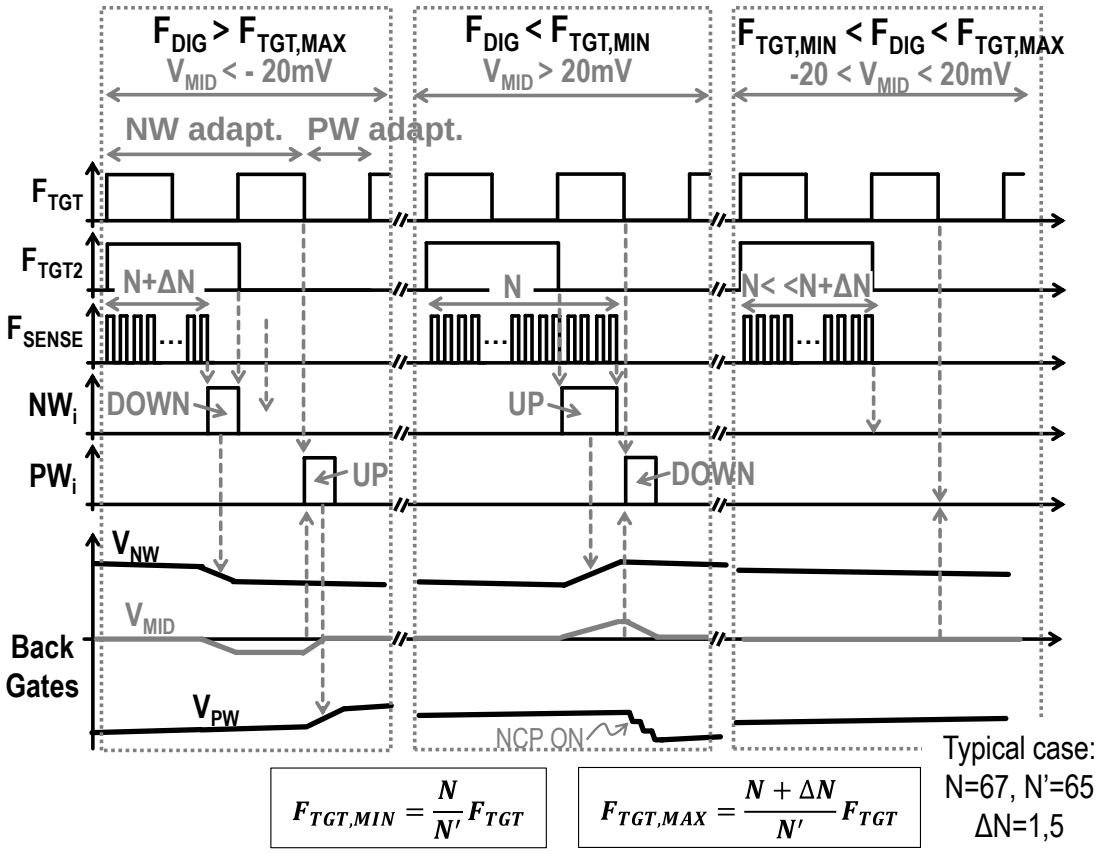

Figure 2: Chronogram in three main biasing configurations.

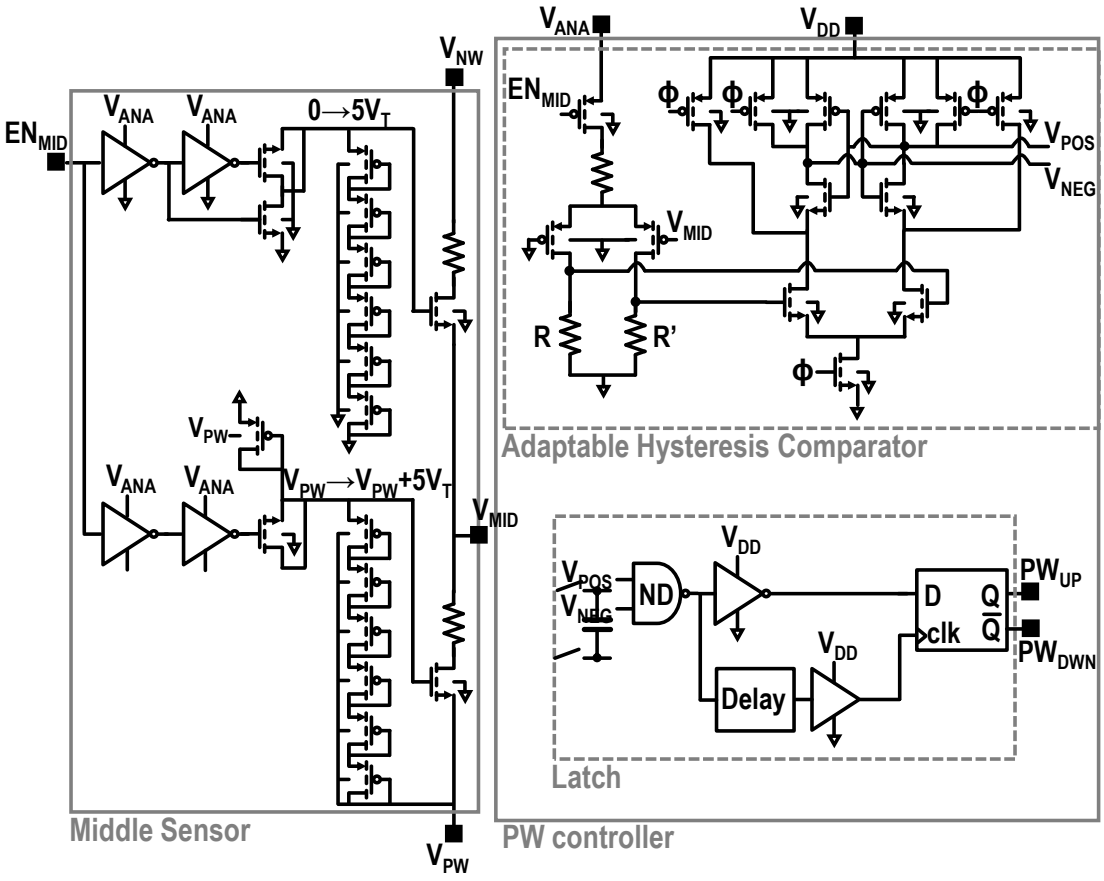

Figure 3: Schematic of middle sensor (MD) including duty-cycled V_{MID} resistive divider and latched hysteresis comparator.

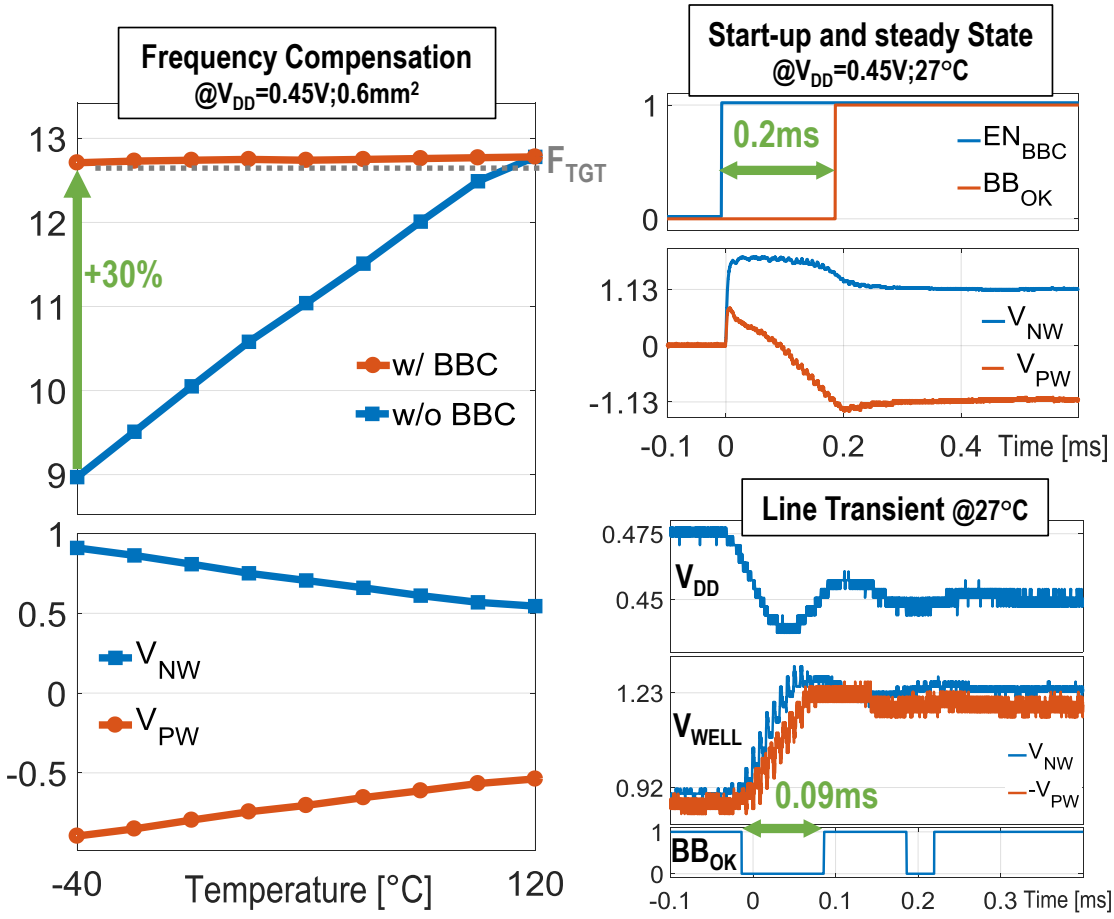

Figure 4: Back biasing profile vs. temperature to maintain targeted frequency; start-up phase timing and biasing dynamics during abrupt power supply transient.

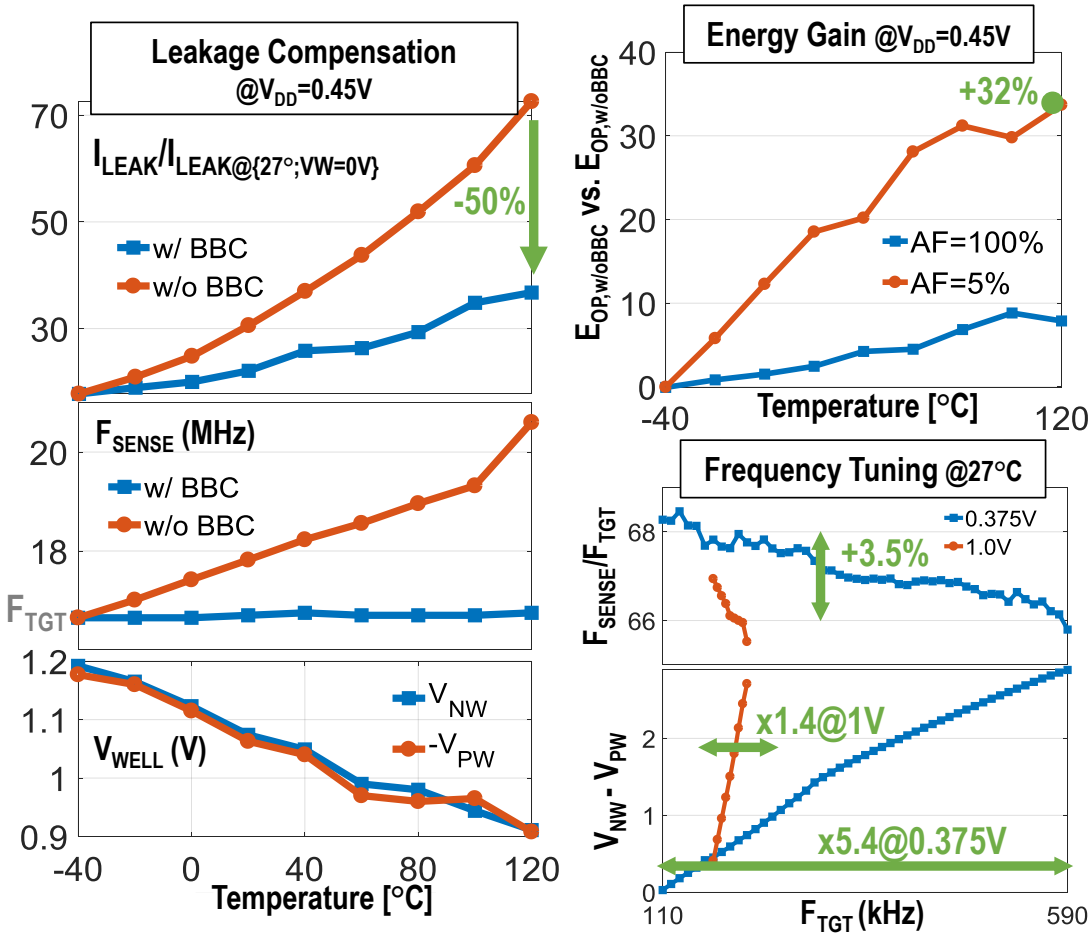

Figure 5: Leakage and energy reduction due to the back biasing compensation unit; frequency compensation and accuracy vs. voltage supply.

Conditions	ASSCC'14 [3]	VLSI'16 [4]	ISSCC'15 [5]	This Work	Unit
Technology	65nm Bulk	28nm FDSOI	28nm FDSOI	28nm FDSOI	-
Onchip compensation	No	No	Yes	Yes	-
Input target	Voltage	Voltage	Freq.	Freq.	-
Frequency accuracy	N.A	N.A	-	3.5	%
Core supply range	0.5-1.2	0.76-0.97	0.33-0.45	**0.35-1**	V
Temperature range	-	-	-40 / 40	**-40 /125**	° C
Quiescent power	600	10	-	**2.5**	µW
Loop time constant	N.A	N.A	-	**0.1**	ms
V_{WELL} min. step	19	58	100	**continuous**	mV
Nwell Pwell	-0.6 / 0.6 -0.6 / 0.6	0 / 1.8 -1.4 / 0	0 / 1.4 -1.4 / 0	**0 / 1.8** **-1.5 / 0**	V
Drivers area	0.0052	0.012	-	**0.0037**	mm^2
System area	N.A	N.A	0.62*	**0.0067**	mm^2
Overhead area	2.3	1.2	-	**0.35**@2mm^2	%

** external capacitance needed (1µF)*

Figure 6: Comparison to state-of-art back biasing generator w/ or w/o feedback loop.

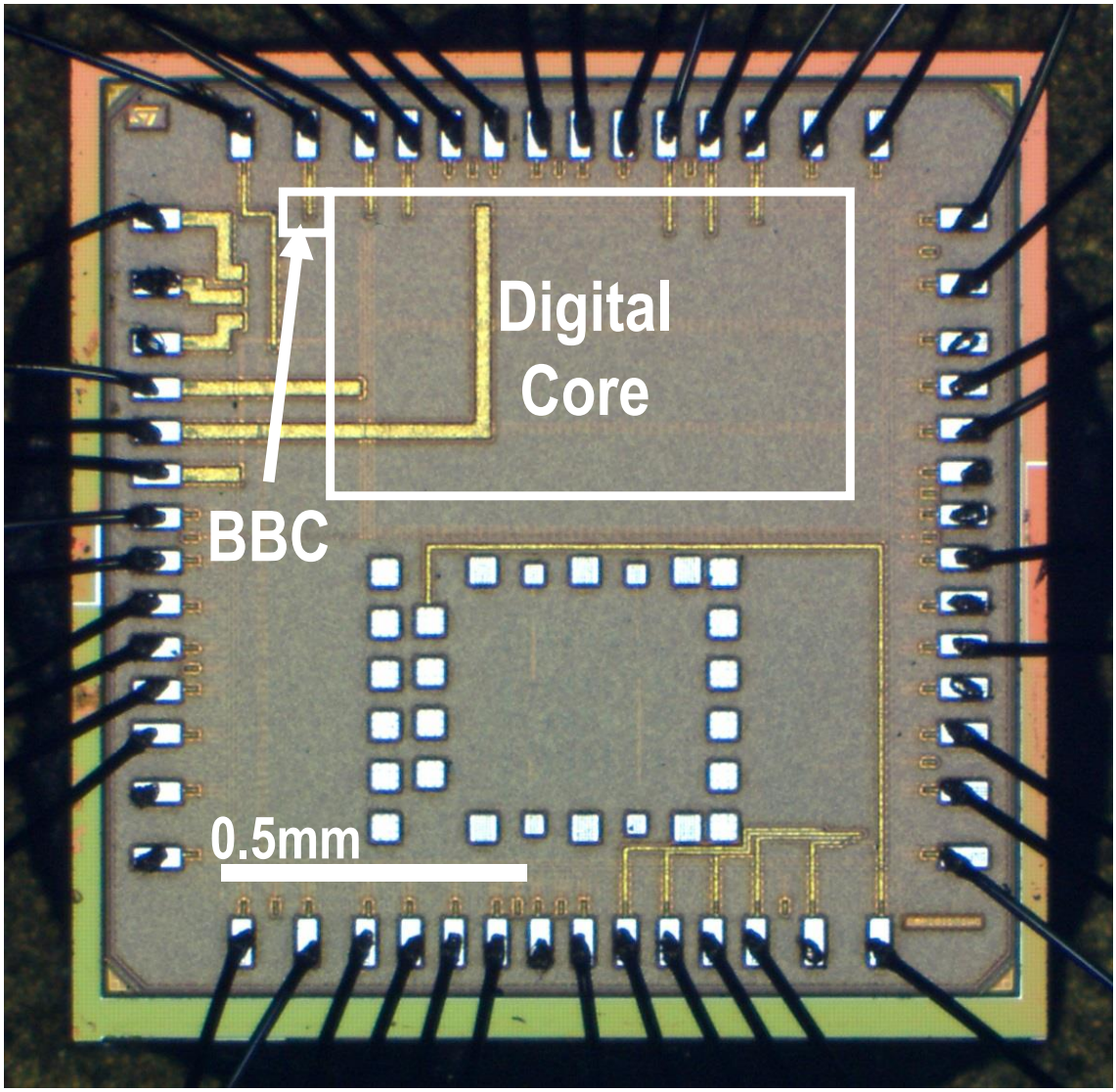

Figure 7: Die micrograph including BBC (0.0067mm^2) and digital core (0.6mm^2) on 1.2x1.2mm^2 die size.