Nonvolatile and SEU-Recoverable Latch Based on FeFET and CMOS for Energy-Harvesting Devices

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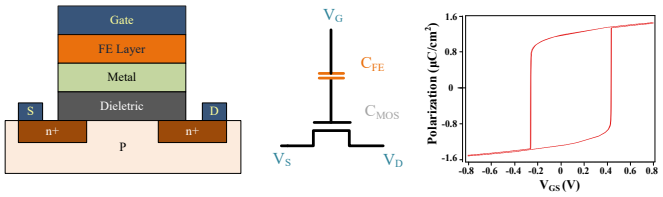
***Abstract*—Nonvolatile memories are widely used in emerging energy-harvesting Internet-of-Things (IoT) applications, and nonvolatile memories constructed from FeFET devices hold great promise. This paper presents a nonvolatile and single-event-upset (SEU)-recoverable latch based on FeFET and CMOS for energy-harvesting devices. The latch uses n-type FeFET devices to provide nonvolatility without any additional control signals. Moreover, since the soft error problem has become increasingly severe, radiation hardening by design gains a great attention as a promising approach to mitigate the reliability issue. The latch uses feedback interlocked loops with n-type FeFETs and C-elements, enabling it to provide nonvolatility and SEU-recovery simultaneously. Simulation results with Candence Virtuoso verifies that the proposed latch design has correct functioning with excellent performance compared to the state-of-the-art designs.**

I. Introduction

In recent years, the continuous advancement of 5G technologies has facilitated the development of the Internet-of-Thing (IoT) industry, with various forms of smart devices being used in a large number of different applications in areas as diverse as healthcare and wellness care, machine building, environmental protection and home automation, among others [1]. These smart devices can be categorized as limited battery capacity and battery-less self-powered [2]. Devices with limited battery capacity often require frequent recharging when operating in a variety of complex and diverse real-world environments [2-3]. Devices in this category are costly to maintain and have significant application limitations. For battery-less self-powered devices, the energy harvesting technology can be used to efficiently capture the energy available in the environment, such as wind energy, solar energy, Wi-Fi, and Radio Frequency (RF) energy, and convert it to ensure the continuous operation of the device [4-5]. However, the energy of these external environments is usually unstable and cannot provide the stable power supply as battery-powered devices, and thus frequent power failures and recovery operations can lead to high energy consumption.

On one hand, as the Complementary Metal Oxide Semiconductor (CMOS) technology continues to advance and transistor feature sizes continue to shrink, soft errors have an increasing impact on the operation of electronic devices [6]. Single-event-upset (SEU) is a typical soft error that occurs when a high-energy particle, such as a neutron, a proton, a heavy ion, an alpha particle, or an electron, impacts a transistor in a storage element [7], and the SEU can be detected at the drain of the affected transistor. Electronic devices without radiation-hardening are prone to soft errors that can lead to data corruption in the storage elements. Therefore, it is also an issue of great concern for safety-critical applications.

On the other hand, many emerging nonvolatile memory (NVM) technologies, such as spin-transfer torque RAMs (STT-RAMs) [8-9], ferroelectric field-effect transistors (FeFETs), magnetic random-access memories (MRAMs) and resistive random-access memories (ReRAMs) [10], have been proposed in recent years. An FeFET is a NVM device with promising applications, which can be categorized into n-type FeFET and p-type FeFET [10]. Figure 1 shows the features of a n-type FeFET device. As shown in Fig. 1-(a), there is a physical representation of the FeFET. An FeFET is essentially a CMOS transistor with a ferroelectric (FE) layer embedded in the gate. Note that the FE layer is integrated by ferroelectric materials. Figure 1(b) shows the equivalent circuit of the FeFET, where the FE capacitance (CFE) couples with the capacitance of the underlying MOSFET (CMOS). As shown in Fig. 1-(c), there is a polarization-voltage (P-V) hysteresis curve. The P-V curve shows the relationship between the VGS and the polarization of the n-type FeFET. V_{GS} is calculated by subtracting the gate voltage from the source voltage. Depending on the V_{GS}, the polarizations of the FE layer in the FeFET can be changed, making the FeFET exhibit different resistance states (HRS, $P < 0$ for a n-type FeFET and $P > 0$ for a p-type FeFET), or low resistance state (LRS, $P > 0$ for a n-type FeFET and $P < 0$ for a p-type FeFET). Note that the difference of resistance between HRS and LRS is almost as high as 10^6.



(a) (b) (c)

Fig. 1. The features of a n-type FeFET device. (a) A physical representation. (b) The equivalent circuit. (c) The P-V hysteresis curve.

It is assumed that logic "1" is stored when the n-type FeFET is in the positive polarization state and logic "0" is stored when it is in the negative polarization state. We refer to the positive polarization state as state "1" and the negative polarization state

as state “0”.

In this paper, FeFET-based latch structures are firstly reviewed, some of which modify conventional CMOS designs by adding several FeFETs to build peripheral nonvolatile modules, but providing nonvolatility in this way often requires additional control signals for backing up and restoring data [10-11]. The design proposed in [12] can provide nonvolatility by improving the structure of conventional inverters to perform backup and restore operations for data without additional control signals. All these designs can provide nonvolatile functionality. However, they cannot effectively provide protection against soft errors.

For the purpose of radiation hardening for basic storage elements, researchers have proposed many solutions, such as those in [13-16]. In [13], the circuit can tolerate SEUs, but it cannot ensure necessary recovery from SEUs. The solutions in [14-16] are SEU-recoverable. However, these designs only take into account the soft error resistance and do not enable nonvolatility.

In this paper, we propose a nonvolatile and SEU-recoverable FeFET-based latch. Eliminating the requirement for additional control signals, the proposed latch can autonomously back up data before the power failure and restore data after the power supply is restored. Moreover, compared to the state-of-the-art designs, the proposed latch provides both nonvolatility and soft error recovery, and also performs low cost in terms of power consumption and latency.

The rest of the paper is organized as follows. Section II describes in detail the proposed FeFET-based latch design. Section III evaluates the proposed design by comparing it with existing designs. Section IV concludes the paper.

II. Proposed FeFET-based Latch Design

Figure 2 shows the structure of the proposed FeFET-based nonvolatile and SEU recovery latch. We propose a hybrid backup circuitry created using FeFET and CMOS technology in each feedback loops, which consists of a conventional nMOS, an inverter and a nonvolatile n-type FeFET. Note that the hybrid backup circuit uses nMOS and FeFET in series to form a voltage divider structure. Depending on the resistance state (HRS or LRS) exhibited by the FeFET in different polarization states, the corresponding storage values can be obtained by the voltage divider principle. A hybrid backup circuitry, a TG, a C-element (CE), and a Clock-gating (CG)-based inverter are used to create each feedback circuit, and the proposed latch consists of a couple of the feedback circuits which forms a symmetrical structure. As shown in Fig. 2, the hybrid backup circuitry, the CE and the CG-based inverter are connected in series in the feedback loop. We use the input of the hybrid backup circuit in a different feedback loop as one of the inputs connected to the CE in another feedback loop. The proposed latch stores values in the feedback loops by the hybrid backup circuitry. Representing an intermediate voltage between VDD and GND, the MVDD in the figure supplies the hybrid backup circuitry as high voltage, so that the output of the hybrid backup circuitry needs to pass through the CE and CG-based inverter in series to re-amplify the voltage to VDD. Note that the two feedback loops have the same values at the same time.

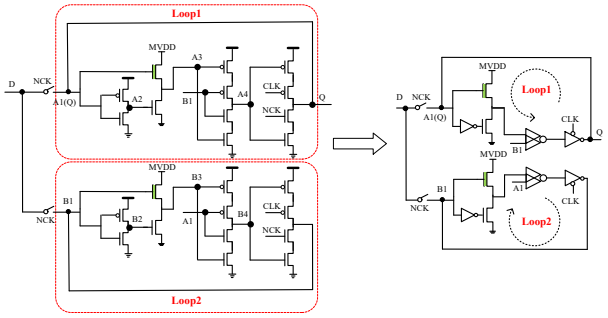


Fig. 2. Structure of the proposed FeFET-based nonvolatile and SEU recovery latch.

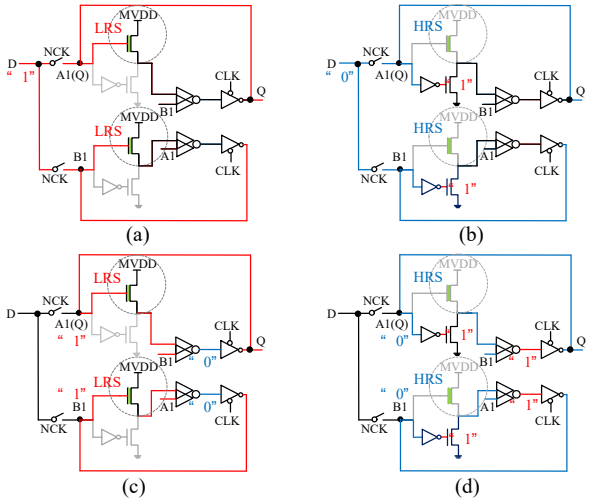


Fig. 3. Schematic of the proposed FeFET-based nonvolatile and SEU recovery latch in normal mode. In transparent mode, (a) FeFET is in LRS and (b) FeFET is in HRS. In hold mode, (c) FeFET is in LRS and (d) FeFET is in HRS. Note that ‘0’ and ‘1’ are used to represent GND and VDD, respectively.

Figure 3 shows the schematic of the proposed FeFET-based nonvolatile and SEU recovery latch in normal mode. In normal mode, the proposed latch works in transparent mode when CLK = 1 and in hold mode when CLK = 0.

In transparent mode (CLK = 1 and NCK= 0), the TGs open, and the values from D directly affects Q. For each feedback loop, the FeFET of the hybrid backup circuitry stores the values and exhibits the corresponding state “0”/“1”. Figure 3-(a) and (b) show the states of the proposed latch in transparent mode, including the states of the latch and the states of the FeFET devices. When CLK = 1, the CG-based inverters of the two symmetrical loops are closed so that the values from D determine Q and B1 completely. As shown in Fig. 3-(a), when D = 1 and CLK = 1, Q is 1 and the FeFET devices are both in LRS. The operation process and corresponding states of the FeFET devices are the same as that described in the previous sub-section. The input voltage of the gate of the FeFET devices are VDD, and the voltage of the source of the FeFET devices both are MVDD. The FeFET devices can get a V_{GS} that reaches a positive threshold to make the FeFET devices go to state “1” and the devices are both in LRS. As shown in Fig. 3-(b), when D = 0 and CLK = 1, Q is 0 and the FeFET devices are in HRS. For each FeFET device in the proposed latch, the input of the gate is GND with the source of the FeFET device being

connected to MVDD, which means that the FeFET device can get a V_{GS} that reaches a negative threshold to make the FeFET go to state "0", and then the FeFET device is able to exhibit HRS.

In hold mode (CLK = 0 and NCK= 1), the TGs connected to D are closed, and the CG-based inverters are opened. The value of the proposed latch is stored in the symmetrical feedback loops. Figure 3-(c) and (d) show the states of the proposed latch in hold mode. As shown in Fig. 3-(c), when the value stored in the proposed latch is 1 and CLK = 0, Q is 1 and the FeFET devices are in LRS. At the gate of the FeFET devices, the inputs are VDD, and the source of the FeFET devices are connected to MVDD, which means that the V_{GS} reaches a positive threshold to make the FeFET go to state "1", and thus the FeFET devices both exhibit LRS. As shown in Fig. 3-(d), when the value stored in the proposed latch is 0 and meanwhile CLK = 0, Q is 0 and the FeFET devices are both in HRS. At the gate of the FeFET devices, the inputs are GND and the source of the FeFET devices are connected to MVDD, which means that the V_{GS} reaches a negative threshold to make the FeFET go to state "0", and then the FeFET devices exhibit HRS.

The proposed latch uses CEs to interlock values in each of the two symmetric feedback loops to robustly maintain correct data. Note that the latch can recover from any possible SEU in hold mode. Let us discuss the principle of SEU-recovery for the proposed latch. For example, when B1 is affected by SEU, the error passes to the CE of the hybrid backup circuit in series as well as another feedback loop in symmetry. Note that the erroneous values of B1 and MVDD work together to obtain the V_{GS}, which here reaches the threshold voltage and changes the state of the FeFET device. The hybrid backup circuit then passes the erroneous values out to the CE in the current feedback loop. Since the CE's output still has the previous value when the two inputs are different, and the value of A1, which is in the different feedback loop, is not affected by the SEU, the CE receives the correct value of A1 as well as the erroneous value of the hybrid backup circuit and thus it outputs the original correct value. The correct output of the CE is returned to B1, restoring the value of the node and re-affects the V_{GS} of the FeFET device, restoring it to the correct state.

In nonvolatile mode, the states of the FeFETs can determine the state of the proposed latch when recovering from a power failure. If Q is low before power failure, the FeFET devices store value "0", which means that the devices are both in state "0". For each FeFET device, which is in the HRS, the resistance is much larger than that of the nMOS connected in series with it. We can approximate the FeFET to be disconnected and the resistance of the nMOS to be neglected. Based on the principle of voltage division, Q finally returns to the low voltage. If Q is high before power failure, the FeFET devices store value "1". For each FeFET device, it is in state "1" and exhibits LRS, with the resistance of the device much larger than the nMOS which is connected in series with it. We can approximate the FeFET as having negligible resistance and the nMOS is disconnected. After the output of the backup circuits has been amplified by the CEs and CG-based inverters, Q returns to high voltage. Finally, Q can restore to the previous state correctly.

III. Latch Comparison and Evaluation

Extensive simulations were performed using Cadence Virtuoso to verify the functioning of the proposed FeFET-based latch under a 65 nm CMOS technology as well as a FeFET model based on the Landau-Khalatnikov equation [17]. The thickness of the ferroelectric layer was set to 6.5 nm and the supply voltage was 0.8 V. Note that the same models and simulation parameters were used in the comparison of the state-of-the-art CMOS-based and/or FeFET-based latch designs for the purpose of a fair comparison.

A. Simulations of the Proposed Latch

Figure 4 shows the simulations of power failures and normal operations of the proposed latch. We assume that VDD and MVDD are powered off at the power failures.

When suffering from power failures, the description of Section II regarding the nonvolatile mode of the proposed latch is still consistent with the current latch's state. As shown in Fig. 4, when it is in the first power failure (CLK = 0 and Q = 1), the FeFET devices keep state "1". If the power recovers from the power failure, the output can recover to 1 at a short time. When it is in the second power failure (CLK = 0 and Q = 0), the FeFET devices keep state "0". If the power recovers from power failure, the output can recover to 0. Note that the proposed latch can also perform the normal operations correctly, which is similar to a conventional latch.

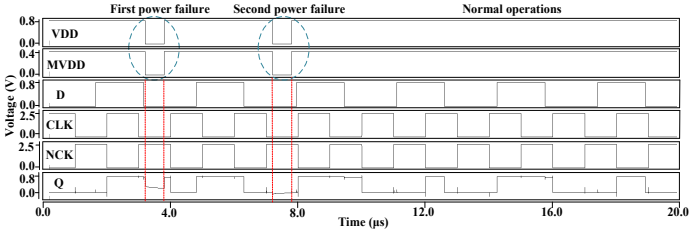


Fig. 4. Simulations of power failures and normal operations of the proposed latch.

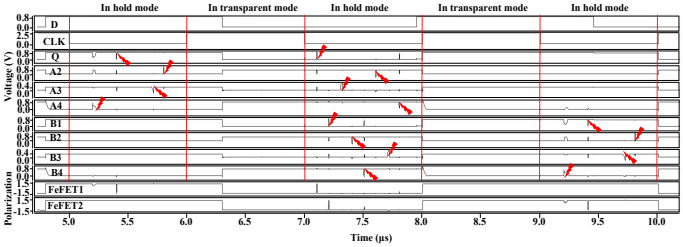


Fig. 5. Simulations of SEU injections of the proposed latch.

Figure 5 shows the simulation results of SEU injections of the proposed latch. We selected all of the possible SEUs (see Cases 1 to 2 below) for simulations.

Case 1: Each node in the top feedback loop, including Q(A1), A2, A3, and A4 suffers from an SEU, respectively. The SEUs were injected at Q at time 5.4 µs and 7.1 µs. As shown in Fig. 5, Q can recover from the SEUs. Similarly, SEUs were injected at A2, A3 and A4 at time sequences of (5.8 µs, 7.6 µs), (5.7 µs, 7.3 µs) and (5.2 µs, 7.8 µs), respectively. Clearly, all these nodes can completely recover from the injected SEUs.

Case 2: Each node in the bottom feedback loop, including B1, B2, B3, and B4 suffers from an SEU, respectively. The

TABLE I
COMPARISON RESULTS FOR ALTERNATIVE SEU/NONVOLATILE LATCH DESIGNS

Latch	Technology	Number of Transistors/Devices	SEU Tol.	SEU Rec.	NV.	Addi Ctrl	D-Q Delay (ps)	CLK-Q Delay (ps)	Power (nW)
Latch [13]	CMOS	20MOS	√	×	×		3.31	4.11	240.4
DICE [14]	CMOS	12MOS	√	√	×		4.86	4.89	352.9
SHLR [15]	CMOS	22MOS	√	√	×		5.12	5.19	193.0
RFC [16]	CMOS	24MOS	√	√	×		5.64	5.58	193.3
FeFET-in NVFF [10]	FeFET	12MOS+1FeFET	×	×	√	√	508.79	499.44	174.1
FeFET-in NVFF [11]	FeFET	11MOS+1FeFET	×	×	√	√	179.11	174.45	149.7
NCFET NV-Latch-NC [12]	FeFET	12MOS+2FeFETs	×	×	√	×	277.32	270.01	190.0
Proposed Latch (SEU+NV)	FeFET	26MOS+2FeFETs	√	√	√	×	5.65	7.38	247.0

SEUs were injected at B1 at time 7.2 μs and 9.4 μs. As shown in Fig. 5, B1 can recover from the SEUs. Similarly, SEUs were injected at B2, B3 and B4 at time sequences of (7.4 μs, 9.8μs), (7.7 μs, 9.7 μs) and (7.5 μs, 9.2 μs). Clearly, all these nodes can completely recover from the injected SEUs. Therefore, the simulations clearly demonstrate that the proposed latch can provide recovery from any possible SEUs.

B. Comparison Results with Alternative Designs

Table I illustrates the reliability and overhead comparison results for alternative SEU recovery and/or nonvolatile latches. Note that, in the table, "Tol." means "tolerant", "Rec." means "recoverable", "NV." means "nonvolatile", "Addi Ctrl" means whether a nonvolatile latch needs additional control signals, "D-Q Delay" is the average of the transmission delays (rise and fall) from D to Q, "CLK-Q Delay" means the average of the delays (rise and fall) from CLK to Q, and "Power" means the average of the power dissipation (dynamic and static).

For latch reliability comparisons, it can be seen from Table I that, the latch based on CMOS in [13] is SEU-tolerant but it cannot offer SEU-recovery and nonvolatility. The other CMOS-based latches, such as DICE [14], SHLR [15] and RFC [16], are SEU-recoverable, but they also cannot offer nonvolatility. The FeFET-based latches, including FeFET-in NVFF [10], FeFET-in NVFF [11], NCFET NV-Latch-NC [12], can only offer nonvolatility and cannot be SEU-recoverable (even non-SEU-tolerant). It can be seen that the proposed latch can simultaneously provide SEU-tolerance, SEU-recovery and nonvolatility. Note that, the proposed latch design does not need additional control signals, which is better than the nonvolatile latches that need additional control signals (including FeFET-in NVFF [10], and FeFET-in NVFF [11]).

Since the compared designs include CMOS-based as well as FeFET-based latches, we indicate the area overhead of the designs by comparing the number of transistors/devices. Note that the FeFET device is made by embedding ferroelectric material on the basis of CMOS and has excellent compatibility with CMOS, and thus we can approximate that an FeFET and a CMOS have the same area overhead and define it as a standard area. With regard to the number of transistors/devices, it can be seen from Table I that DICE is the latch having the minimum standard areas among the SEU-recoverable or SEU-tolerant latches (however, it cannot provide nonvolatility). It can also be seen that FeFET-in NVFF in [11] uses the smallest number of transistors and devices but the latch can only offer nonvolatility without tolerance and recovery from SEUs. Clearly, the existing designs consist of 12 to 24 standard area. To provide more functionalities, such as SEU-tolerance, SEU-recovery, and nonvolatility, more area has to be introduced. That is the reason why 28 standard areas are used for the proposed latch, so as to integrates more functionalities.

With regard to the D-Q delay, for the proposed latch and some existing latches, such as SHLR, RFC, and the latch in [13], their D-Q delay is small because of the high-speed transmission path from D to Q. In contrast, the latches, such as FeFET-in NVFF in [10], FeFET-in NVFF in [11], and NV-Latch-NC, have a large D-Q delay because they use extra devices from D to Q. Note that the FeFET-based circuits tend to require more delay overhead than the CMOS-based circuits [18].

With regard to the CLK-Q delay, it can be seen from Table I that it is close to the D-Q delay because they are both related to the devices on the path from D to Q. The proposed latch has a moderate CLK-Q delay. The latches, such as the proposed latch, DICE, RFC, and the latch in [13], have a small CLK-Q delay, because they have a small D-Q delay. In contrast, FeFET-in NVFF in [10], FeFET-in NVFF in [11], and NV-Latch-NC, have a large D-Q delay, so that they have a large CLK-Q delay.

With regard to the power dissipation, DICE consumes the highest power, because of the high competition for current between nodes inside the latch and the fact that the latch does not use the CG technique. Note that, when a latch has a large area and/or does not use the CG technique, its power dissipation is high. Since the proposed latch uses redundant area to provide more functioning, it consumes extra but moderate power.

IV. CONCLUSIONS

In this paper, we have proposed a nonvolatile and SEU-recoverable latch based on FeFET and CMOS for energy-harvesting devices. Simulation results has demonstrated that the proposed design is SEU-recoverable and nonvolatile with moderate overhead compared to the state-of-the-art latch designs. Additionally, the proposed latch does not require additional control signals, making it applicable to energy harvesting and safety-critical applications.

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