Optimizing RRAM performance: A comparative analysis of forming strategies

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***Abstract*— This paper investigates the impact of various forming strategies on resistive random access memory (RRAM) device performance, focusing on conductance distribution and failure rates. Through experimental characterization and the introduction of a new figure of merit for failure rate, we analyze Progressive I-Mode with and without Current Limiter (I-PCL/I-P), Single-Pulse I-Mode (I-SPCL), and Voltage-Mode forming methods. Our findings reveal that I-PCL significantly enhances device reliability and performance by optimizing conductance distribution and minimizing failure rates post-cycling, offering critical insights for the development and application of RRAM technologies.**

Keywords*— *RRAM, forming

I. Introduction

Resistive random access memories (RRAMs) are rapidly emerging as a next-generation non-volatile memory (NVM) technology, attracting significant attention from memory manufacturers for integration into embedded applications [1, 2]. These oxide-based RRAMs exploit the resistance state of their metal/oxide/metal structure to store information. However, before operational use, each memory cell requires an initial "forming" process to transition from its high-resistance insulating state (R_0) to a low-resistance conducting state (LRS). This crucial step typically involves applying a controlled voltage to induce partial breakdown of the oxide layer, creating conductive paths through oxygen vacancy formation. The forming process needs careful control to ensure device integrity and prevent complete oxide breakdown.

Extensive research has focused on understanding the impact of forming methods on device characteristics such as cycling endurance, retention, and read/write margin. Traditional approaches rely on applying a constant voltage while limiting current with a series transistor [3]. Recent studies have explored more progressive forming techniques, such as utilizing trains of increasing-amplitude voltage pulses interspersed with read operations to detect device readiness and halt the process early [4, 5]. Additionally, current-driven forming methodologies have been presented in literature [6, 7, 8]. However, consensus on the actual impact of forming strategies remains elusive; research [9] indicates it does not significantly affect long-term device performance, whereas [10] demonstrates that high-temperature forming procedures enhance retention.

This paper delves into the forming process influence on RRAM performance. We explore various forming methods and analyze their impact on RRAM conductance distribution.

II. Material

The experiments is based on a chip fabricated using an industrial 130 nm CMOS technology with BEOL RRAM as illustrated in Fig. 1. This platform offers key features tailored for comprehensive characterization of hafnium-based RRAMs. The IC includes a co-integrated programmable current sources alongside the RRAM array. Notably, this seamless integration mitigates the impact of parallel parasitic capacitance (C_p) present in current programming [11]. The implemented current source utilizes a thermometric DAC architecture, enabling a wide output current range spanning from 63 nA to 992 µA through its logarithmic scaling. While the testchip provides on-chip current control, voltage driving and read-out functionalities are implemented externally on the accompanying test board. This configuration grants flexibility and modularity for exploring diverse forming procedures.

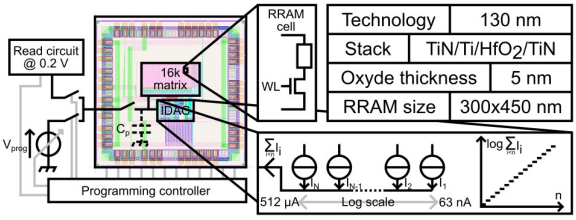

Fig. 1. Diagram of our testing setup, with the integrated memory matrix and the integrated programmable current source. Table of details on the technology of memory used.

III. Method

A. Current Mode Forming

Forming OxRAM devices using a current source is challenging due to the initially high resistance (R_0) of RRAM devices, typically in the hundreds of megaohms. Careful selection of the current source value is essential to prevent excessive voltage across the device, ideally limited by the voltage power supply (V_{DD}). In practice, the current source and the device are connected through a bit line, introducing an interconnection capacitance (C_p), resulting in a time constant of R_0C_p for establishing the voltage across the device. Additionally, after the first filament formation, when RRAM resistance drops, C_p is rapidly discharged through the device, creating an additional energy packet. This extra energy, independent of current value, also influences filament formation. Current programming offers inherent write termination capabilities, automatically adjusting the voltage well below the critical SET voltage when resistance drops, limiting overprogramming compared to voltage-mode patterns (V-mode). As no RRAM models are available for simulating forming mechanisms, this paper focuses on experimental characterization of the effect of current pulses on the initial SET resistance distribution and subsequent RESET/SET cycling.

To achieve device formation in current mode (I-mode) while avoiding excessive voltage and current surges, we explore three current-based forming techniques (Fig. 2):

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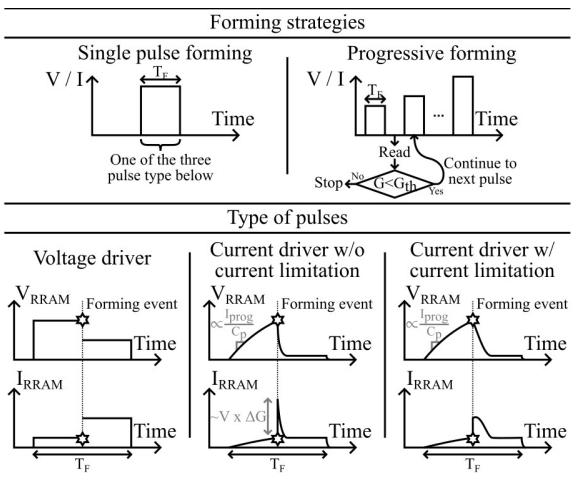

Fig. 2. Description of the forming strategies.

Progressive I-Mode without Current Limiter (I-P): In this approach, the current is incrementally increased step by step, starting from a very low current level (63 nA). The RRAM selector, represented by an NMOS, is biased at $WL = V_{DD}$ and does not act as a current limiter. At each step, the current source is connected to the device for time T_F (1 µs when not specified), ensuring that the programming current flows through the device. After each pulse, the device conductance is read. If its conductance is above a given threshold (G_{TH}), the forming process is stopped, and the device will not receive any stronger pulse. This approach offers the potential advantage of spending more time at lower voltages to promote forming at lower voltage levels, potentially reducing the current spike resulting from C_p discharge.

Progressive I-Mode with Current Limiter (I-PCL): Similar to the I-P method, the current is progressively increased step by step. Additionally, a transistor-based selector within the RRAM is utilized as a current limiter (CL), resembling the approach used in voltage mode (V-mode). The CL's purpose is to prevent current surges by extending the discharge time. This method offers the potential advantage of further preventing excessive forming due to high voltage and current.

Single-Pulse I-Mode with Current Limiter (I-SPCL): In this method, only one current step is applied. To prevent current surges, a transistor-based selector within the RRAM is employed as a CL. The potential advantage of this approach is achieving faster forming, potentially in a collective manner, with all devices exposed to the same excitation.

B. Voltage Mode Forming

In addition to I-mode, we propose to benchmark two voltage-based forming methods (V-mode). The CL, based on adapted gate voltage biasing of the selector, is used to prevent any excessive current through the cell in both cases:

Single-Pulse V-Mode with Current Limiter (V-SPCL): In this method, a single voltage step is applied from an external source to the selected RRAM device with CL. This method is conventional and has been studied in prior art.

Progressive V-Mode with Current Limiter (V-PCL): Similar to the I-PCL method, the voltage is progressively increased gradually by pulses. As highlighted in prior research, this method offers an advantageous forming process, as each cell is formed at the lowest voltage it could form under the chosen time constraint, reducing over-forming.

IV. Results and Discusion

A. Conductance distribution after forming

We provide an analysis of the outcomes from employing the five forming strategies for RRAM cells detailed in Section III. The cumulative distribution function in Fig. 3 (a, b) demonstrates the conductance of devices immediately after forming, revealing key insights into each strategy's efficacy.

V-SPCL Limitations: The Single-Pulse Voltage Mode with Current Limiter (V-SPCL) strategy is shown to be ineffective in fully forming all RRAM cells, with a significant number of devices exhibiting insufficient conductance. While applying higher voltage programming could potentially address this issue, it risks overprogramming some cells, leading to failures in the RESET process, as evidenced by the omitted data in Fig. 3 (a).

Advantages of V-PCL: The Progressive Voltage Mode with Current Limiter (V-PCL) is highlighted as a more reliable method, capable of forming devices at lower voltages. This results in a tighter conductance distribution, particularly at a CL level (by setting the *WL* value) of 1.3 V, as depicted by the blue curve in Fig 3 (a). When the current limiter setting is increased to $WL = 1.55$ V, the average conductance rises, validating the current limiter's effectiveness. As described in Section II, read verify after each pulse efficiently bounds the lowest values of the distribution to G_{TH}.

Comparison of I-Mode Forming: The I-Mode forming strategies offer a comparison to V-Mode, showcasing a generally narrower distribution of conductance. However, the Single-Pulse I-Mode with Current Limiter (I-SPCL) also faces challenges with incomplete cell formation at 304 µA, akin to V-SPCL. Adjusting the current influences the conductance distribution, reducing the lower tail at the expense of enlarging the upper tail, which could lead to overprogramming.

Benefits of Progressive I-Mode: Implementing a progressive forming approach without a current limiter (I-P) enhances the formation of the lower tail, allowing cells to form under optimal conditions. Despite this improvement, a significant number of cells become over-formed, indicating that merely extending the current pulse duration to 1 ms to promote forming at low current does not sufficiently mitigate excessive forming due to the additional energy from C_p.

Optimization with I-PCL: Introducing a Current Limiter (CL) in the I-Mode forming, particularly with I-PCL at $WL = 1.3$ V, emerges as the most effective strategy. It outperforms other methods by achieving a well-balanced conductance distribution and preventing over-forming.

The analysis concludes that the Progressive I-Mode with Current Limiter (I-PCL) yields the best conductance distribution among the tested strategies, establishing it as the preferred method for forming RRAM devices.

B. Conductance state after cycling

We investigate the impact of various forming methods, as previously described, on the conductance distribution of RRAM devices after 1000 cycles. Both the Set and Reset operations were performed using voltage-mode by applying a single 1 µs pulse at 2 V with $WL = 1.55$ V and 1.3 V, respectively (the Reset does not use CL). Fig. 3 (c, d) present the distribution of the High Resistance State (HRS) and Low Resistance State (LRS) after these cycles. It was observed that cells subjected to over-forming, particularly noticeable in the I-P forming method, resulted in a population of cells with high conductance, which in turn, reduced the read margin between the binary states. This complicates multi-level programming

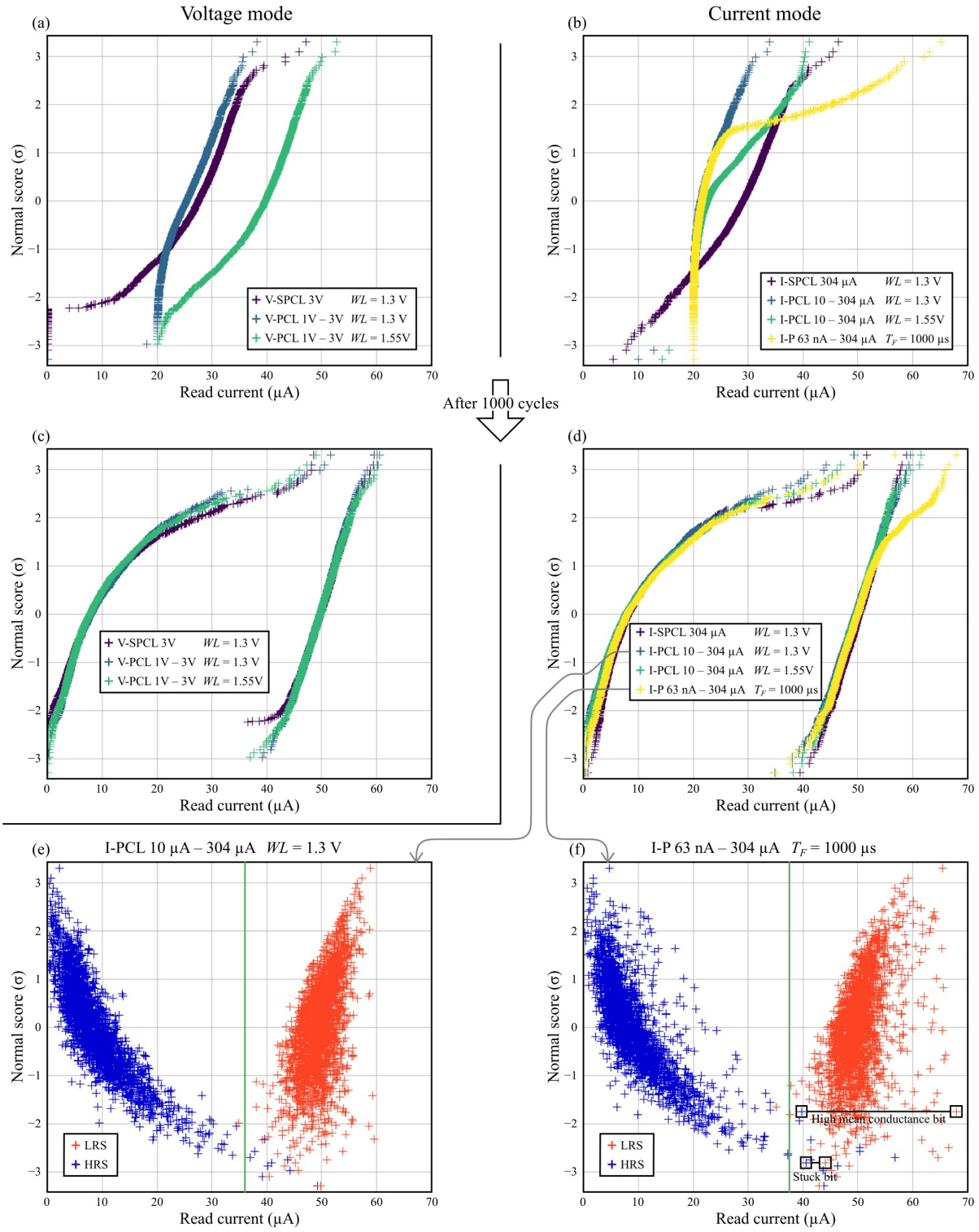

Fig. 3. (a) Cumulative ditribution function of the conductance of the devices just after forming with a voltage driver for: V-SPCL at 3 V with WL = 1.3 V (purple); V-PCL from 1 V to 3 V with G_{TH} = 20 μA and WL = 1.3 V (blue); same with WL = 1.55 V (cyan). (b) Cumulative ditribution function of the conductance of the devices just after forming with a current driver for: I-SPCL at 304 μA with WL = 1.3 V (purple); I-PCL from 10 μA to 304 μA with G_{TH} = 20 μA and WL = 1.3 V (blue); same with WL = 1.55 V (cyan); I-P from 63 nA to 304 μA with G_{TH} = 20 μA and T_F = 1000 μs (yellow). (c) Same as (a) but after the cells were cycled 1000 times. HRS is the left trace and LRS the right one. (d) Same as (b) but after the cells were cycled 1000 times. HRS is the left trace and LRS the right one. (e) Consecutive HRS and LRS conductance on the devices ranked by window margin size formed with I-PCL from 10 μA to 304 μA with G_{TH} = 20 μA and WL = 1.3 V. Both the HRS and LRS forms two coherent clumps. (f) Same as (e) for the devices formed with I-P from 63 nA to 304 μA with G_{TH} = 20 μA and T_F = 1000 μs. Two extra sparse clumps appears, one in HRS and one in LRS. These correspond to devices that have a mean conductance higher than the bulk of the devices. When not specified, T_F = 1 μs.

due to the extended high conductive tail in the LRS state. Interestingly, if forming is executed through progressive forming in either V-mode or I-mode, the post-cycling conductance distributions are quite similar. This finding lends support to the assertion made in [9]. However, when using single-pulse forming or omitting a CL, the forming can have a significant impact. To further refine the comparison of forming methods, given the difficulty of directly comparing distributions, we introduce a new visualization technique and a figure of merit to more thoroughly evaluate the different forming approaches.

C. HRS-LRS pairs distribution

Cumulative distribution graphs serve as an effective means to present large datasets in a concise and understandable manner. However, they fall short in differentiating between High Resistance State (HRS) and Low Resistance State (LRS) for the same device when these states are superimposed, complicating the analysis of distribution tails. For instance, it remains unclear whether devices with high conductance in HRS are malfunctioning or are simply operating at a higher average conductance than the majority. To shed light on these nuances, we have developed a novel graph type, showcased in Fig. 3 (e, f). This graph maintains the association between successive LRS and HRS conductance for each device. The device conductance pairs are ordered by their window margin, the conductance difference between successive HRS and LRS, and plotted with conductance on the x-axis (each pair has two points) and their rank (based on window margin) on the y-axis. Consequently, devices with minimal window margin, indicative of malfunction, are positioned lower on the graph. Fig. 3 (e) reveals that in the case of I-PCL, the majority of read errors stem from such stuck devices, forming the high conductance HRS tail observed in Fig. 3 (d). Conversely, Fig. 3 (f) illustrates that with I-P, a significant number of devices exhibit high HRS conductance while having a wide windows margin. This suggests that the prominent high conductance tail in HRS results from overprogrammed devices, correlating with the high conductance LRS tail and parts of the HRS tail seen in Fig. 3 (d). This innovative data visualization method enables the identification of distinct types of degradation, which were not readily discernible through cumulative distribution plots alone.

D. Write Failure Rate

To enhance our comparison of forming methods, we introduce a new figure of merit (FoM) termed "write failure rate", which quantifies the proportion of devices that failed to write properly and subsequently failed to be read against a universal conductance threshold. This threshold is optimized for each forming method to minimize the failure rate, representing an ideal scenario for reading. Fig. 4 displays the peak failure rate observed in the final 100 cycles, along with the conductance threshold selected for each forming method. This new FoM effectively highlights the distinction between Single-Pulse forming in both I-mode and V-mode, a differentiation that isn't readily apparent from the conductance distributions in Fig. 3 (c) and (d). According to this FoM analysis, I-PCL emerges as the superior forming strategy, achieving 3.5 times less write fails compared to the least effective method (V-SPCL). Notably, while an increase in the CL threshold (through *WL*) in V-mode leads to a lower failure rate, an inverse trend is seen with I-mode forming, where increasing *WL* increase the failure rate.

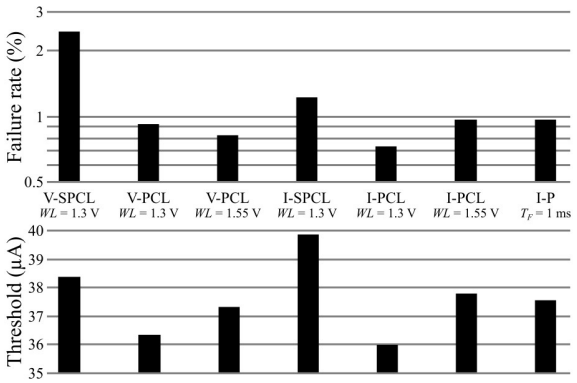

Fig. 4. Histogramme of the write failure rate and associated read threshold current for each of the studied cases.

V. Conclusion

In conclusion, our study investigates the effects of various forming strategies on the performance of RRAM devices, employing experimental analysis complemented by innovative data visualization and a novel write failure rate figure of merit. We demonstrate that the Progressive I-Mode with Current Limiter (I-PCL) method outperforms other strategies by minimizing failure rates and optimizing conductance distribution after 1000 cycles. These findings underscore the impact of forming process selection providing valuable insights for future RRAM adoption.

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