Dual Output Regulating Rectifier for an Implantable Neural Interface

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***Abstract*— This paper presents the design of a power management circuit consisting of a dual output regulating rectifier configuration featuring pulse width modulation (PWM) and pulse frequency modulation (PFM) to control the regulated output of 1.8 V, and 3.3 V from a single input ac voltage. The PFM control feedback consists of feedback-driven regulation to adjust the driving frequency of the power transistors through the buffers in the active rectifier. The PWM mode control provides a feedback loop to accurately adjust the conduction duration. The design also includes an adiabatic charge pump (CP) to power stimulators in an implantable neural interface. The adiabatic CP consists of latch up and power saving topologies to enhance its energy efficiency. Simulation results show that the dual regulating rectifier has a voltage conversion efficiency 94.3% with an ac input magnitude of 3.5 Vp. The power transfer efficiency of the regulated 3.3 V output voltage is 82.3%. The dual output regulating rectifier topology is suitable for multi-functional implantable devices. The adiabatic CP has an overall efficiency of 92.9% with an overall on-chip capacitance of 60 pF. The circuit was designed in a 180-nm CMOS technology.**

Keywords—Adiabatic charge pump, biomedical implant, inductive wireless power transfer, pulse frequency modulation, pulse width modulation, regulating rectifier.

I. Introduction

Neural stimulators are used in a range of applications to treat neural disorders and diseases. Due to the high voltage requirement of stimulators, an efficient power management unit (PMU) is required as batteries have limitations on miniaturisation and require periodic surgical replacement. Inductive wireless power transfer (WPT) addresses the requirements of implantable applications and obviates the need of implanted batteries [1]. To deliver biosafe output power there are limitations on MHz range of operation frequencies. In a WPT system a PMU consists of a rectifier and regulator required to convert an input ac voltage delivered by the link to multiple regulated dc supply voltages. A PMU using power-saving and a power optimization strategy, can provide an overall system efficiency making WPT a viable and reliable powering solution.

State-of-the-art PMUs are designed with several stages including a voltage rectification and voltage regulation (requiring several low-dropout (LDOs) voltage regulators). Combining the two-stages rectification and regulation, into a single-stage can improve the overall system efficiency and eliminate the need for a large off chip capacitor between the two-stages. However, with the advancement of multifunctional biomedical implantable devices there is a need for efficient multiple output PMUs to generate various supply voltages from a single input ac voltage while using maximum power system efficiency. Having several regulation blocks within a PMU can degrade the overall power efficiency. For the case of dual outputs, a single-stage dual output regulating rectifier can improve the overall system efficiency and avoid the need for power hungry LDOs.

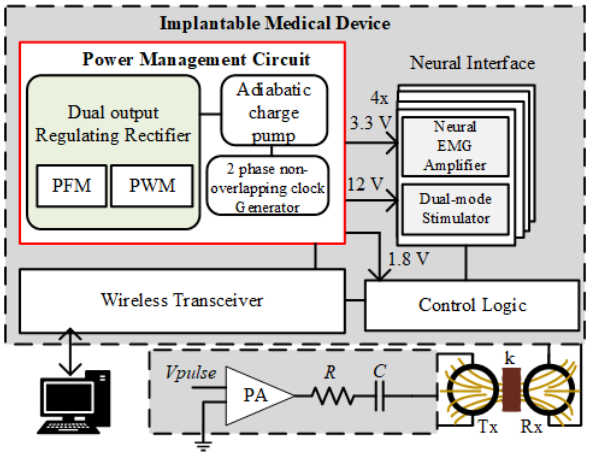


Fig. 1 Proposed power system design of a neural interface.

State-of-the-art designs of regulating rectifiers generate a single voltage output [2], [3]. Using a voltage doubler for a high output can generate a higher output voltage compared to an active rectifier, but its power conversion efficiency (PCE) is generally lower than that of an active rectifier. Therefore, it is better to eliminate the reverse leakage current of an active rectifier by reducing conduction time, especially when the system operates at high frequency. Minimizing the charge loss per cycle, and the reverse leakage current is important as the ac frequency will affect the dc output ripple. In this design, the carrier frequency is limited to 13.56 MHz as a trade-off of the power transfer efficiency and data telemetry. The implant stimulator diagram shown in Fig. 1 consists of a PMU, inductive wireless transfer, and control logic connected to a wireless transceiver.

This paper describes a novel design of an integrated PMU for an implantable neural interface. It features a dual output active rectifier with pulse width modulation (PWM) regulation and pulse frequency modulation (PFM) to generate both 1.8 V and 3.3 V regulated outputs from a 3.5 Vp ac supply. It also describes a novel adiabatic three stage latch charge pump (CP) that generates a 12 V output from the regulated 3.3 V input, and a two-phase non-overlapping clock generator to control switching. The paper is organized as follows. Section II describes the system overview of the dual output regulating rectifier and the adiabatic CP. Section III shows the simulated results. Conclusions are in Section IV.

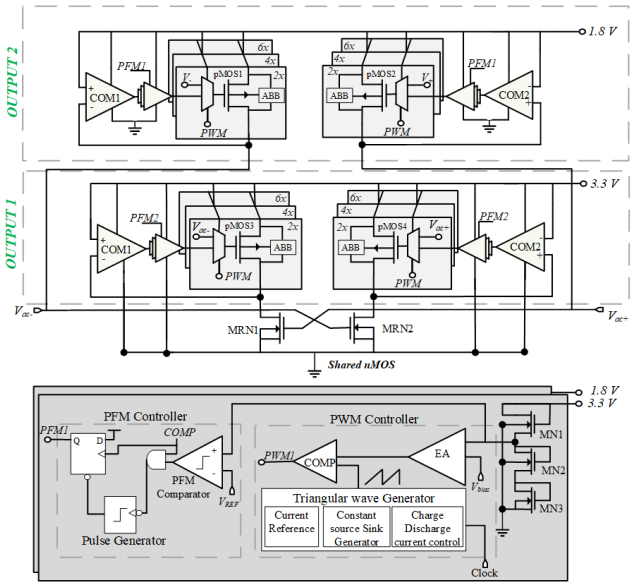


Fig. 2 Design of the proposed dual output regulating rectifier with controller topology for generating 1.8V and 3.3 V outputs. The '2x,4x,6x' refer to transistor sizes.

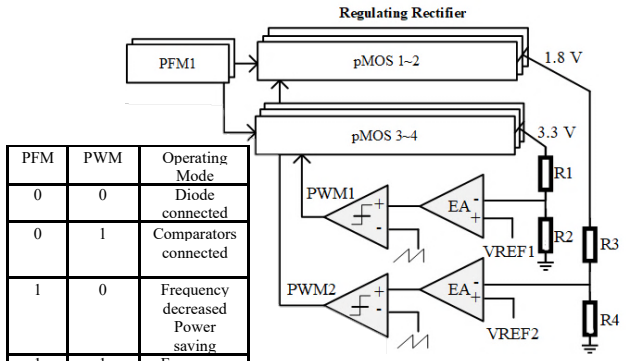
II. System Overview

The design of a dual output regulating rectifier includes PWM and PFM control feedback loops to provide feedback-driven dual voltage output regulation. The PMU also consists of an adiabatic CP to power a dual-mode stimulator within the neural interface. The design of the dual output regulating rectifier consists of: 1) different size of pMOS transistors and adaptive body biasing (ABB) to improve the power conversion efficiency; 2) a body biased high-speed comparator [4]; 3) ABB to decrease leakage current; and 4) dual voltage outputs of 1.8 V and 3.3 V.

A. Dual Output Regulating Rectifier

As shown in Fig. 2, the dual output regulating rectifier has an ac input voltage of (V_{ac+} and V_{ac-}) connected to both *OUTPUT 1* of 1.8 V and *OUTPUT 2* of 3.3 V. The outputs of the two multiplexers are connected to several sizes of pMOS 2x,4x,6x connected in parallel. Adaptive sizing of the pMOS power transistors [2] provides a tradeoff between the conduction and switching losses to optimize the PCE over a wide range of load values. The active rectifier controllers feature a body biased high-speed comparator and a PFM dynamic buffer that can support several speed operation modes to decrease power losses. The active rectifier controllers feature ABB so that the power pMOS transistors are always connected to the highest terminal between the input terminals (V_{ac+} and V_{ac-}), and the output 1.8 V and 3.3 V.

The design principle is shown in Fig. 3 which includes the operating mode logic in different stages of the PFM and PWM. The outputs of the active rectifier controllers are fed to a PFM controller to trigger regulation speed of the dynamic buffers. PFM only operates when required for power saving optimization. The PWM controller consists of an error amplifier, a rail-to-rail static comparator, and a triangular wave



PFM	PWM	Operating Mode
0	0	Diode connected
0	1	Comparators connected
1	0	Frequency decreased Power saving
1	1	Frequency decreased

Fig. 3 The design principal topology with the regulation principle. Resistors implemented with diode connected nMOS transistors.

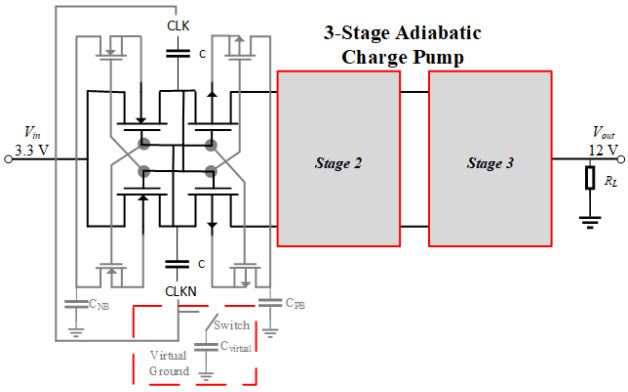


Fig. 4 Proposed three stage adiabatic charge pump with dynamic body biasing.

generator required for generating the PWM signals. The triangular wave generator consists of a current reference, constant source sink generator, and charge discharge current control.

B. Adiabatic charge pump

The design of a two branch latch CP was first adopted in [5] providing a solution for a reliability issue due to gate oxide stress by providing a non-overlap clock, and ensuring the gate and source do not exceed the input voltage. The design has a high efficiency pumping operation, and minimizes the voltage drop while charging. A charge sharing topology was proposed in [6] for a linear charge pump in which a two-step waveform is applied on the gates of the transistors to reduce current peaking and improve the PCE. As the output current requirement increases the PCE decreases significantly and addressing the current peaking issue can improve the PCE.

The proposed CP design in Fig. 4 has three identical stages. It reconfigures the latch CP design to decrease the overall power consumption by implementing a virtual ground, and bulk biasing. The adiabatic technique reduces energy dissipation by reducing the voltage swing and peak current which halves the power dissipation, improving the PCE of the charge pump.

This topology minimizes the voltage drop across the current source by having an adiabatic CP slowly ramping up the supply

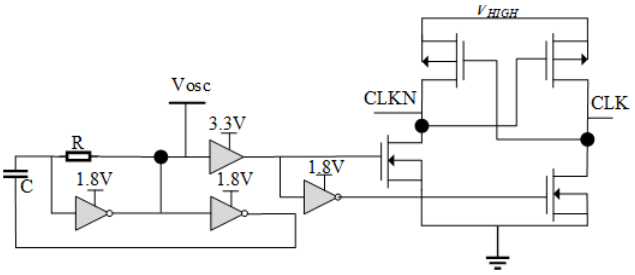


Fig. 5 Clock generator operating at 20 MHz for the adiabatic charge pump.

voltage. Making use of the charge dissipated and recycling can help in energy reduction by implementing a virtual ground-bound charge in a capacitor, and then reusing it for an internal feed of the virtual input. The use of virtual ground bound charge can pump up the capacitors' virtual input; this topology is mostly used in pipelined logic blocks. The bulk biasing circuit for each CP stage is required to ensure that the pMOS bulk is connected to the highest potential and the nMOS bulk is connect to the lowest potential. This reduces the threshold voltage at forward bias and increases the threshold voltage at reverse bias to ensure that the transistors within their limits. The bulking capacitors are the minimum size to avoid an increase in the parasitic capacitance. The proposed 20 MHz clock generator in Fig. 5 consists of a level shifter and an oscillator with clock pairing to be used for the adiabatic charge pump.

III. Simulated Results and Analysis

The PMU was designed and implemented in a CMOS 180 nm process. Table I compares the performance of the dual output regulating rectifier with other designs. The current work has a higher PCE and VCE without requiring an inductor [7].

A. Dual Output Regulating Rectifier

The simulated results were carried out with a 13.56 MHz input frequency. Fig. 6 shows simulated output waveforms of the dual output regulating rectifier for *OUTPUT 1* = 1.8V and *OUTPUT 2* = 3.3 V with loads of 200 Ω and 1 KΩ respectively. The overall PCE of the dual output regulating rectifier is defined as

$$\eta(dual) = \frac{P_{out1}+P_{out2}}{P_{IN}} = \frac{P_{out1}+P_{out2}}{V_{AC,rms}\times I_{AC,rms}} \quad (1)$$

Where P_{out1} , P_{out2} , P_{IN}, are the first output power, second output power, and the input power, respectively. The measured PCE is dependent on the output of both terminals with an average peak of PCE of 82.3% at output power of 40.5 mW. The VCE is

$$VCE = \frac{V_{dc}}{\max(|V_{in\_ac}|)} \times 100\% \quad (2)$$

Fig. 7 shows the simulated VCE of the regulating rectifier with a peak value of 94.3%. The proposed design supports a wide strategy to monitor and adaptively regulate the output voltage levels.

B. Three Stage Adiabatic Charge Pump

The proposed technique for saving energy during the charging of capacitances C in Fig. 4 uses some voltage steps

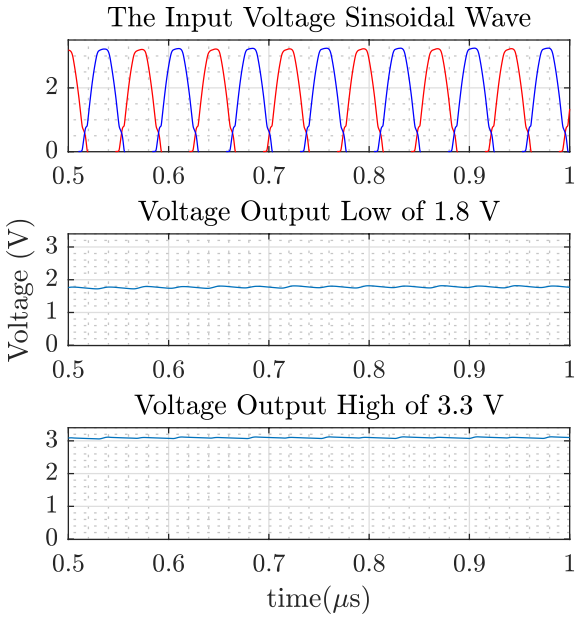


Fig. 6 Simulated performance of the regulating rectifier showing the rectified 3.5Vp sinusoidal voltage input and the two voltage outputs of 1.8 V nominal (load 200Ω)*, and 3.3 V nominal* (load 1KΩ)*.*

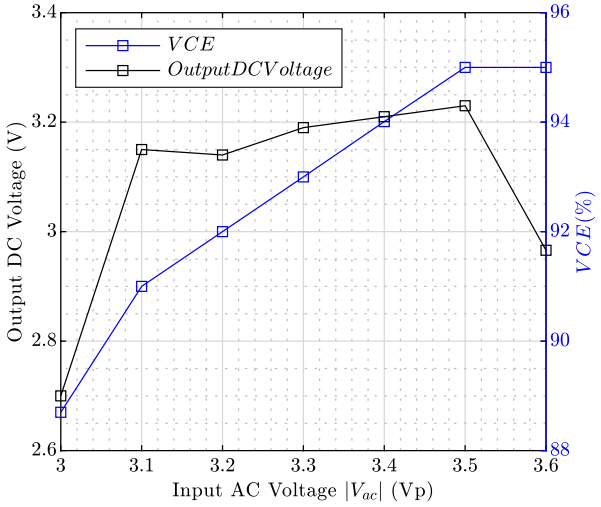


Fig. 7 Simulated startup performances of the VCE of the 3.3V regulating rectifier for a range of inputs.

when charge Q is transferred. When the capacitor is charging, the energy delivered by the voltage source is

$$E_{source} = Q \times V_{in}. \quad (3)$$

During the discharge of the upper and lower capacitors, C, are connected in parallel to a smaller virtual capacitor to be reused. This helps to decrease power dissipation. In several steps, the energy transferred E_T is given by

$$E_T = \frac{1}{2} C \left(\frac{V_f}{2} - V_i\right)^2 + \frac{1}{2} C \left(V_f - \left(\frac{V_f}{2} - V_i\right)\right)^2 \quad (4)$$

where V_i and V_f are the initial and final capacitor voltage levels. Combining power reduction with several step charging and charge sharing can provide a 50% reduction in energy compared

Table I Comparison of Dual Output Regulating Rectifier Topology

	CICC Conf. 2018 [8]	***TCSI 2019*** [9]	***TBCAS 2019*** [7]	***TBCAS 2020*** [10]	***This Work***
Process	0.18-µm CMOS	0.18-µm CMOS	0.18-µm 1P8M CMOS SOI	0.18-µm TSMC 1P/6M	**0.18-µm CMOS**
Freq. (MHz)	13.56	0.0125	1	1-10	**13.56**
$V_{in\ ac}$ (V), peak	1.35~1.8, 2.15~2.8	1.6~2	NA	1.5~2.5	**3.5**
Regulation Topology	Delay-based Regulation	SSDO Tri-mode	Voltage power reg.	Regulator Rectifier	**Regulating Rectifier**
V_{dc} (V)	3.12	3.6	1	1.5-2.5	**1.8 - 3.3**
R_{load} (kΩ)	0.5	0.2,1	8	0.1	**0.33-1**
$P_{out,Max}$ (mW)	10	114	4.7	65	**40.5**
VCE (%)	82.2	NA	92	75.8	**94.3**
PCE Peak (%)	79	91.7	75.3	90.75	**82.3**

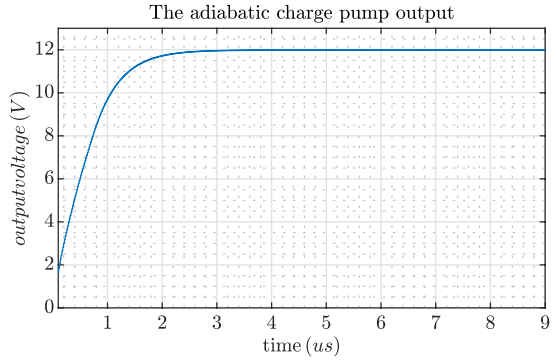


Fig. 8 Simulated output voltage response of the proposed adiabatic charge Pump, Vin = 3.3 V and R_{load} = 50 KΩ at 90 us.

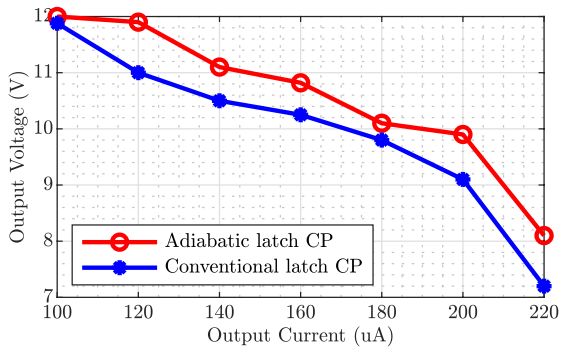


Fig. 9 The output characteristics of the charge pumps as a function of the output current comparing proposed charge pump with conventional latch.

to single step charging. Output is shown in Fig. 8. The power efficiency η_{PCE} of the CP is:

$$\eta_{PCE} = \frac{P_{out}}{P_{in}+P_{clock}} \times 100\% \quad (5)$$

where $P_{out}, P_{in}, P_{clock}$ are the output power, input power, and the power consumed by the clocks. The output current of the CP is shown in Fig. 9 for different input currents comparing the conventional latch CP [5] with the proposed adiabatic latch CP design. The maximum power efficiency is 92.9% at an output current of 102 μA. The output is restricted to below 12 V to ensure that the deep n-well in the transistors is not damaged when the load is increased.

IV. Conclusion

This paper has presented a dual output regulating rectifier from a single stage ac to dc conversion. The circuit has been designed to provide two regulated supply voltages from an input ac voltage using the PWM and PFM control modes to power an neural interface. A new design of an adiabatic charge pump to improve the overall energy usage while working at a high efficiency has also been proposed. This design of PMU can be utilized for different biomedical applications to improve overall system efficiency. A maximum total output power of 40.5 mW can be delivered with a PCE of 82.3%.

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