Enhanced Dual-Transition Probabilistic Power Estimation with Selective Supergate Analysis

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Abstract

Consideration of pairs of transition in probabilistic simulation allows power estimation for digital circuits in which inertial delays can filter glitches [5]. However, the merit of the method is not fully realized because of the way probabilistic simulation approximates spatial correlations of signals in the presence of delays. In this paper, we use supergate partitions (enclosing reconvergent fanouts) and timed Boolean functions (TBF) to obtain the dual-transition probabilities that correctly deal with glitches and filtering as they affect power estimation. Experimental results on ISCAS'85 benchmarks show significant improvements in estimation accuracy as the average estimation error on total power consumption remains under 5%.

1. Introduction

Most existing probabilistic approaches of dynamic power estimation [1], [2], [4], [6], [7], [13] assume a zero-delay model and neglect the transient signal transitions, namely, glitches or hazards. In [15], the method of [7] has been extended to include real delays so as to consider glitch power. *Transition density* approach [11] included glitch power assuming that no two signals transit simultaneously. *Probabilistic simulation* (CREST) [9], [10] and *tagged probabilistic simulation* (TPS) [3] use *probability waveforms* to statistically model the signal activity that also includes the glitch activity. A major weakness in these approaches is that although glitches are considered, the *glitch filtering effect* is seldom considered, which refers to the fact that glitches with pulse width less than the gate inertial delay will be "filtered" out by the gate. Glitch filtering effect can change the node activity dramatically and has significant impact on the power estimation. Recently, a new measure of dual-transition probability was proposed [5], leading to a more accurate glitch filtering method in the tagged probabilistic simulation (TPS). However, it was also shown that the merit of the new method was not fully realized due to the limitation of the underlying probabilistic simulation techniques.

We observe that for circuits with reconvergent fanouts, strong correlation among signals can lead to errors in the probability waveform of a node. Such errors will be propagated through the glitch filtering stage and to fanout nodes, eventually constraining the overall estimation accuracy. In this paper, we propose the use of *supergate* partitions [14] and *timed Boolean functions* (TBF) [8] for handling the spatial correlation at reconvergent fanouts and thereby improve the estimation accuracy. Our technique is applied to the TPS [3], with the dual-transition glitch filtering model [5]. Experimental results show that the new method further improves the accuracy and the consistency of power estimation over a variety of circuits and delay assignments. The average accuracy for total power estimation (in terms of transition density and with respect to logic simulation) is within 5% for ISCAS'85 benchmark circuits.

2. Background

Probability waveform [10] represents the transition waveforms of a signal node collectively for a set of input vectors. A probability waveform w is a sequence of *signal probabilities* and *transition probabilities* over time. A tagged probability waveform [3] can be viewed as a partitioning of a probability waveform according to the four possible initial and final steady state signal values. In this paper, we adopt the same notations as that in [5]. Tagged probability waveforms defined for a node n are w_n^{xy} ($x, y \in \{0,1\}$). *Tagged waveform probability* is denoted as $P(w_n^{xy})$. Signal probability and transition probability at time t in waveform w_n^{xy} are denoted as $sp_n^{xy}(t)$ and $P_{n,xy}^{s}(t)$ ($s \in \{00,01,10,11\}$). In TPS, the *macroscopic spatial correlations* between steady state signal values ($\omega_{a,b}^{xy,wz}$) are used to approximate the exact spatial correlations. *Dual-transition probability* [5] $P_{n,xy}^{sn1,sn2}(t_1,t_2)$ is defined as the probability of a joint event that node n is in state *sn1* at time t_1 and in state *sn2* at t_2 on the xy tagged probability waveform, where $sn1, sn2 \in \{00,01,10,11\}$ and $x, y \in \{0,1\}$.

3. Supergate enhancement of TPS

3.1 Motivation

According to the results in [5] the effectiveness of dual-transition glitch filtering is strictly bounded by the underlying probabilistic simulation method. It is just because that TPS takes spatial correlation of signals into account, the application of dual-transition glitch filtering to TPS leads to a better estimation accuracy compared to that obtained by the probabilistic simulation. Therefore, in order to improve the estimation accuracy under the same architecture, the enhancements in the underlying probabilistic simulation method are needed.

3.2 Application of supergate

It has been shown [14] that to reduce the error caused by the strong correlation at the reconvergent fanouts, circuits can be partitioned in such a way that all inputs to a partition are externally independent. These partitions, known as *supergates*, provide a convenient way to reduce errors due to spatial correlations in the circuit. Although supergate is not a new concept in power estimation [12], its application to TPS has never

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been attempted. More importantly, by incorporating supergate technique into TPS, the effectiveness of dual-transition glitch filtering can be further enhanced. As a result, we are able to obtain better estimation accuracy when compared to both of previous approaches [3], [5].

Since a supergate can be very large in an extreme case and the complexity of TPS increases exponentially with the number of inputs of the supergate, we limit the supergate to three levels and at most three inputs are allowed for a supergate partition. After the supergate is built for a node, the TPS waveform at the output is derived from the inputs and the function of the supergate. The approximation method of spatial correlation in TPS is then applied for correlated input case. Figure 1 shows an example.

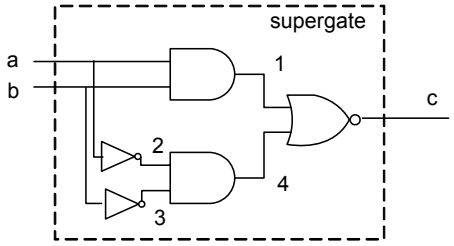

Figure 1. Illustration of a supergate.

4. Timed Boolean function (TBF)

4.1 TBF for a supergate

Since probability waveform describes the transient signal activity of a node and there are multiple propagation delay paths inside a supergate, we could not use conventional Boolean function to describe a supergate. Therefore, we adopt the *timed Boolean function* (TBF) [8] in our analysis. With TBF, we are able to propagate probability waveform through a supergate accurately and efficiently when inputs are independent and no inertial filtering effect exists.

For the example supergate shown in Figure 1 we assume that every gate has the same delay τ. The TBF of output *c* can be expressed in terms of inputs *a* and *b* as follows,

$$c(t) = \overline{a(t-2\tau)b(t-2\tau) + \overline{a(t-3\tau)}\ \overline{b(t-3\tau)}} \qquad (1)$$

which shows the current state of node *c* as determined by the values on inputs *a* and *b* at times $t-2\tau$ and $t-3\tau$. The propagation delay of sub-paths *a-1-c and b-1-c* is 2τ and that of *a-2-4-c and b-3-4-c* is 3τ.

4.2 Modification of TPS propagation

For the example supergate in Figure 1, the up transition condition can be expressed as

$$ut_c(t) = \overline{c(t^-)}\ c(t^+) = \sum_{i=1}^{n} uterm_i \qquad (2)$$

where each $uterm_i$ is a product term containing $a(t^- - 2\tau)$, $a(t^+ - 2\tau)$, $b(t^- - 2\tau)$, $b(t^+ - 2\tau)$, $a(t^- - 3\tau)$, $a(t^+ - 3\tau)$, $b(t^- - 3\tau)$, $b(t^+ - 3\tau)$. Here t^-, t^+ represent the time instance before and after the time *t*. Each product term indicates the transition state on inputs *a* and *b* at time $t-2\tau$ and $t-3\tau$, the up transition probability of *c* at time *t* is then as follows,

$$P^{01}_{c,(xy,wz)}(t) = \sum_{i=1}^{n} P^{sa1_i, sa2_i}_{a,xy}(t-2\tau, t-3\tau) P^{sb1_i sb2_i}_{b,wz}(t-2\tau, t-3\tau) \omega^{xy,wz}_{a,b} \qquad (3)$$

where $sa1_i, sb1_i, sa2_i, sb2_i$ are 2-bits representations of the transition state at times $t-2\tau$ and $t-3\tau$ corresponding to the $uterm_i$ in Equation (2). We extend the possible state for $sa1_i, sb1_i, sa2_i$, and $sb2_i$ as compared to that in [5]. Each bit of $sa1_i, sb1_i, sa2_i, sb2_i$ can be either *1*, *0* or *X* (don't care). For example, $sa1_i$=11 if $uterm_i$ contains $a(t^- - 2\tau)$ and $a(t^+ - 2\tau)$, $\underline{sa1_i = 1X}$ if $uterm_i$ contains $a(t^- - 2\tau)$ but not $a(t^+ - 2\tau)$ or $a(t^+ - 2\tau)$. The dual-transition probabilities used in Equation (3) can be obtained as a simple sum of individual dual-transition probabilities with definite states. In case that transition state for one time instant is *XX*, the dual-transition probability equals the simple transition probability for the other time instant two. If transition state for both time instants is *XX*, the dual-transition probability equals the tagged waveform probability $P(w_n^{xy})$. The spatial correlation between *a* and *b* (if they are not independent) is approximated by their steady state correlation coefficient $\omega^{xy,wz}_{a,b}$.

Similarly, the down transition condition can be expressed as

$$dt_c(t) = c(t^+)\overline{c(t^-)} = \sum_{j=1}^{n} dterm_j \qquad (4)$$

and the down transition probability of *c* at time *t* is then,

$$P^{10}_{c,(xy,wz)}(t) = \sum_{j=1}^{n} P^{sa1_j, sa2_j}_{a,xy}(t-2\tau, t-3\tau) P^{sb1_j sb2_j}_{b,wz}(t-2\tau, t-3\tau) \omega^{xy,wz}_{a,b} \qquad (5)$$

where $sa1_j, sa2_j, sb1_j, sb2_j$ correspond to the $dterm_j$ in Equation (4).

4.3 Modification to dual-transition probability

The original propagation of dual-transition probabilities according to [5] needs to be augmented for the presence of supergates. After the probability waveform is propagated to the output of a supergate, the inertial delay of the ending node is used for the glitch filtering process. For the example shown in Figure 1, $P^{sc1,sc2}_{c,xy}(t_1, t_2)$ represents the joint probability that node *c* is in state *sc1* at time t_1 and in state *sc2* at t_2 on the tagged waveform w_c^{xy}. Assuming *sc1=01, sc2=10*, the corresponding TBF for this joint event will be

$$F^{01,10}_c(t_1, t_2) = \overline{c(t_1^-)} c(t_1^+) c(t_2^-) \overline{c(t_2^+)} = \sum_{i=1}^{n} term_i \qquad (6)$$

which is a sum of products form. The corresponding dual-transition probability will then be

$$P^{01,10}_{c,(xy,wz)}(t_1, t_2) = \sum_{i=1}^{n} (P^{sa1_i, sa2_i, sa3_i, sa4_i}_{a,xy}(t_1-3\tau, t_1-2\tau, t_2-3\tau, t_2-2\tau) \cdot P^{sb1_i, sb2_i, sb3_i, sb4_i}_{b,wz}(t_1-3\tau, t_1-2\tau, t_2-3\tau, t_2-2\tau)) \omega^{xy,wz}_{a,b} \qquad (7)$$

where $sa1_i, sb1_i, sa2_i, sb2_i, sa3_i, sb3_i, sa4_i, sb4_i$ are 2-bit representations of transition states at times $t_1-3\tau$, $t_1-2\tau$, $t_2-3\tau$ and $t_2-2\tau$ corresponding to the $term_i$ in Equation (6). Spatial correlation between *a* and *b* is still approximated by $\omega^{xy,wz}_{a,b}$. Different from the dual-transition probability [5], the joint probability of transition states for up to four different time instants, e.g., $P^{sa1_i, sa2_i, sa3_i, sa4_i}_{a,xy}(t_1-3\tau, t_1-2\tau, t_2-3\tau, t_2-2\tau)$, is needed in Equation (7). Since we do not maintain such joint probabilities to avoid an exponential increase of computation

complexity, we use pair-wise dual-transition probabilities as approximations. By ignoring the higher order correlations between transitions, we have

$$P_{t_a t_b t_c t_d} = \frac{P_{t_a t_b} P_{t_a t_c} P_{t_a t_d} P_{t_b t_c} P_{t_b t_d} P_{t_c t_d}}{P_{t_a}^2 P_{t_b}^2 P_{t_c}^2 P_{t_d}^2} \quad (8)$$

where $P_{t_a t_b t_c t_d}$ is the simplified representation of the joint probabilities of transition states at four time instants (t_a, t_b, t_c, t_d), e.g., $P_{a,xy}^{sa1_i, sa2_i, sa3_i, sa4_i}(t_1 - 3\tau, t_1 - 2\tau, t_2 - 3\tau, t_2 - 2\tau)$ and $P_{t_i t_j}$ ($i, j \in \{a,b,c,d\}$ $i \neq j$) are the corresponding dual-transition probabilities for each pair of time instants, e.g., $P_{a,xy}^{sa1_i, sa2_i}(t_1 - 3\tau, t_1 - 2\tau)$. The joint probability of transitions at three different times can be approximated similarly as

$$P_{t_a t_b t_c} = \frac{P_{t_a t_b} P_{t_a t_c} P_{t_b t_c}}{P_{t_a} P_{t_b} P_{t_c}} \quad (9)$$

Note that the above approximation can lead to a large error in some cases. Therefore, we examine a boundary condition to help control the error. This boundary condition states that the joint transition probability cannot be larger than the maximum of the individual dual-transition probabilities, that is, $P_{t_a t_b t_c t_d} < Max(P_{t_a t_b}, P_{t_a t_c}, P_{t_a t_d}, P_{t_b t_c}, P_{t_b t_d}, P_{t_c t_d})$. Also, in our implementation, the Boolean expression is first minimized algebraically leading to a set of disjoint product terms that cannot be further reduced. Therefore, the major product terms are short and not subjected to further approximation. The error introduced by these approximations is generally limited.

4.4 Selective application of supergate

In our analysis, the timed Boolean function represents a supergate accurately only when glitch filtering inside the supergate can be neglected. In reality, sometimes this assumption can cause an error, as shown by the example of Figure 2. This is a supergate with two inputs *a* and *b* and output *c*. Assuming *b* remains 0 all the time, the TBF for *c* is then obtained as $c(t) = a(t - d_1)a(t - (d_1 + d_2))$. However, when $d_1 < w < d_2$, the output waveform by the TBF deviates from the actual waveform due to the inertial filtering effect.

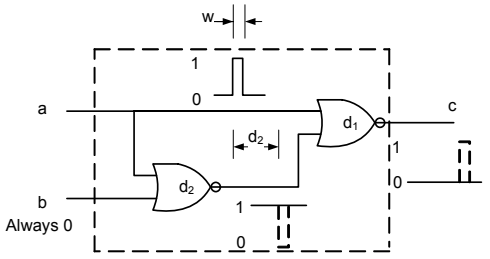

Figure 2. Illustration of a supergate where neglecting of inside glitch filtering causes an error. Dashed line represents the waveform obtained by timed Boolean function. Solid line represents the actual waveform.

From the preceding example, it is clear that the application of the supergate analysis should be such that the error caused by the inside filtering is minimized. In our analysis, we make the decision on whether or not a node should be considered as a supergate based on the time instances that it is subject to glitch filtering. For each internal node of a supergate, first we list all the time instants at which transitions could occur $t_1,..,t_n$ by static analysis of propagation delays inside the circuit. Then for each time instant, the numbers of neighboring time instants subject to glitch filtering N_i are summed up. Finally, the average number of time instants requiring glitch filtering is calculated as

$$D = \frac{1}{n}\sum_{i=1}^{n} N_i \quad (10)$$

where the parameter *D* represents the density of the probability waveform and the possible glitch filtering effect, approximately. A node can be considered for a supergate analysis if $D > D_T$, where D_T is an experimentally determined threshold. The advantage of this approach is that such a static analysis can be done very quickly.

5. Experimental results

The proposed algorithm has been implemented with TPS [3] and the dual-transition glitch filtering method [5] as a stand-alone software tool using C++. It takes the circuit netlist and estimates the switching activity for each node. The default input signal probabilities are assumed to be 0.5, but can be changed as required. The estimation is compared with the results obtained by event-driven simulation with 40,000 randomly generated vectors (assuming spatial-temporal independence). As in [3], [5], the transition probabilities and macroscopic correlations for steady state signals are first generated using a zero-delay logic simulator and then fed into our power estimation software. Previous methods are referred to as TPS [3] and DualTrans [5] (TPS with dual-transition glitch filtering). In all experiments, the threshold D_T is set as 0.9.

5.1 Estimation Accuracy

Experimental evaluation was done for ISCAS'85 benchmark circuits. Both fanout delay and unit delay assignments were used. For fanout delay assignment, gate delay is set as the number of its fanouts. For unit delay assignment, every gate has the same delay of 1 unit. Note that our method works under any real-delay assignment as well, although only two delay assignment schemes are examined. For each circuit, average node error (E_{avg}), standard deviation of node errors (σ), and the error for total power (E_{tot}) are shown in Table 1. Here, node errors and the total error are percentages with respect to the average node power obtained from logic simulation.

Table 1. Power estimation for benchmark circuit under fanout delay assignment. All errors are in percentage.

Circuit	TPS [3]			DualTrans [5]			Supergate method		
	E_{avg}	σ	E_{tot}	E_{avg}	σ	E_{tot}	E_{avg}	σ	E_{tot}
c17	2.3	2.6	0.1	2.3	2.6	0.1	2.3	2.6	0.1
c432	29.9	38.8	35.8	9.5	11.8	6.5	11.5	16.6	11.5
c499	6.8	14.0	7.0	3.6	8.2	0.6	2.3	3.0	3.0
c880	8.3	15.3	1.6	8.0	15.7	5.2	4.8	9.0	0.0
c1355	24.2	31.6	32.9	5.8	11.2	5.4	5.0	9.5	0.5
c1908	15.0	23.1	4.1	17.7	27.9	11.2	7.0	16.3	2.0
c2670	16.6	29.8	7.2	16.7	28.3	9.9	13.2	23.6	6.2
c3540	13.8	26.3	9.8	10.3	25.6	2.4	10.5	26.4	3.7
c5315	11.8	24.4	2.3	13.4	31.5	10.1	11.3	27.0	3.4
c6288	27.4	27.5	32.1	15.7	18.8	4.1	12.7	15.4	0.2
c7552	14.5	27.5	3.2	14.8	31.4	7.8	14.1	27.6	1.3
Avg.	15.5	23.7	12.4	10.7	19.4	5.7	8.6	16.1	2.9

As shown in Table 1, the supergate method is able to reduce the estimation error on most circuit where estimation error has already been quite small. Both total power estimation and node power estimation are improved. The overall average estimation error for total power is under 3%. Only one circuit that leads to a significantly larger error in Table 1 is c432, which is due to the limitation of our adaptive supergate application scheme. Since our decision on selective application of supergate relies on the approximated internal filtering criterion $D > D_T$, the application of supergate analysis in c432 is not optimum.

For circuits with unit delay assignment, the results are shown in Table 2. The power dissipation for circuits with unit delay assignment can differ from that of fanout delay assignment by as much as 40%. Results show that our supergate method is able to further reduce the estimation errors that were already quite small. It also proves that this method works consistently under different delay assignments. For the unit delay assignment, DualTrans has almost the same estimation error as that of TPS.

Table 2. Power estimation for benchmark circuits with unit delay assignment (errors shown as percentages.)

Circuits	TPS [3]			DualTrans [5]			Supergate method		
	E_{avg}	σ	E_{tot}	E_{avg}	σ	E_{tot}	E_{avg}	σ	E_{tot}
c17	0.6	0.4	0.1	0.6	0.4	0.1	0.6	0.4	0.9
c432	7.9	9.6	9.0	5.6	8.7	4.8	3.4	6.3	2.2
c499	11.1	26.9	16.0	11.1	26.6	16.1	1.0	2.1	0.8
c880	7.8	15.3	4.7	7.7	15.3	4.7	4.0	6.8	2.6
c1355	10.0	20.8	9.9	10.0	20.6	10.1	10.3	24.2	12.7
c1908	21.6	31.5	18.6	21.5	31.5	18.7	6.0	13.7	2.0
c2670	11.2	32.4	7.0	8.8	30.7	1.0	7.3	29.4	1.8
c3540	9.5	25.0	3.0	9.9	27.0	4.8	9.5	26.8	4.3
c5315	18.0	44.7	14.0	18.5	45.5	15.6	13.6	40.4	9.2
c6288	27.9	36.3	15.4	28.5	36.9	16.4	27.6	37.3	15.0
c7552	15.5	39.5	8.8	15.8	39.9	9.4	13.9	36.0	3.8
Avg.	12.8	25.7	9.7	12.5	25.7	9.2	8.8	20.3	5.0

5.2 Computation cost

As reported in [5], DualTrans is about 2 to 3 times faster than logic simulation over 40,000 vectors. TPS is about 2 orders of magnitude faster than logic simulation. Although our method has a higher complexity for the propagation of the probability waveform and the dual-transition probability for supergates, the total computation cost does not scale up exponentially due to two factors. First, the size of supergate is not large for a typical circuit. Second, in our implementation, we find the exact time interval requiring the dual-transition probability for each node, which eliminates redundant computation. Our method results in a 2 to 25 times faster evaluation than logic simulation. The computer time is not so constant because we have adaptive application of supergate and the variable time-interval requiring dual-transition probability calculation. The average speed up over all benchmark circuits is 6 to 8 times for both fanout delay and unit delay assignments.

6. Conclusion

The effectiveness of dual-transition glitch filtering method [5] has been limited by the underlying probabilistic simulation techniques [3]. In this paper, we propose an enhanced dual-transition power estimation incorporating the concept of supergate in the previous techniques [3], [5] to handle the spatial correlation at reconvergent fanouts. Consequently, the effectiveness of dual-transition glitch filtering can be enhanced. Each supergate is described using timed Boolean function to better represent signal input output relationships at the transient stage. To avoid the possible error due to filtering of glitches internal to supergates, we selectively apply supergate analysis depending on an estimated possibility of the occurrence of such filtering. Experiments show that our method provides improved accuracy over both of previous approaches [3], [5]. The average estimation accuracy of total power is within 5% with respect to logic simulation for ISCAS'85 benchmark circuits. An optimized implementation of our algorithm also results in a relatively lower computation cost.

From the experimental results, further improvements in the estimation accuracy under the constraint of computation complexity will be challenging. However, tradeoffs between computational cost and accuracy can be provided to a designer through options of various analysis methods.

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