Constructing Hardware/software Interface Using Protocol Converters

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Abstract

Hardware/software partition is a critical phase in hardware/software co-design. This paper proposes a hybrid partitioning framework, in which we design a set of protocol converters to construct the interface component between the hardware and software components, and reuse the formerly well-built partitioning rules by introducing protocol converters and rewriting them for this hybrid framework. The hardware components generated by our partitioning process are coded directly in Verilog HDL, which will greatly facilitate the further compilation from it down to netlists.

Keywords: *Hardware/software partition, protocol converter, program algebra*

1. Introduction

Hardware/software co-design is a design technique which delivers computer systems comprising hardware and software components. A critical phase of co-design process is to partition the specification into hardware and software parts. Meanwhile, an interface component should be adopted to deal with the interactions between these parts.

Recently, some works have suggested the use of formal methods for the partitioning process [1, 3, 15]. Balboni *et al* ([1]) adopt Occam as an internal model for the system exploration and partitioning strategy. Cheung ([3]) pursues the structural transformation and verification within the functional programming framework. However, neither has provided a formal proof for the correctness of the partitioning process. In [15], Silva *et al* provide a formal strategy for carrying out the splitting phase automatically, and presents an correctness proof. However, their splitting phase delivers many simple processes, and it's rather difficult to cluster and join these small processes into the target hardware and software components. Furthermore, additional channels and local variables introduced in the splitting to accommodate huge number of parallel processes actually increase the data flow between the hardware and software components.

Our former work ([13]) proposes a formal partitioning approach to hardware/software partition within a high-level communicating language, where both the hardware and software components are coded in the language. Due to this fact, an obvious gap exists in compiling the hardware specification down to netlists. In this paper, we'll bridge this gap by partitioning the system's specification into a software component coded in a high-level communicating language, a hardware component coded in a hardware description language (such as, Verilog), and as well an interface component to manage the interactions between hardware and software. A hardware component of this form will facilitate hardware compilation. Rather than construct all these components and the partitioning rules from scratch and then verify them in program algebra, we define a set of protocol converters (inspired by [2]), from which we obtain the interface component. Moreover, we derive new partitioning rules directly from those ones in [13] by introducing protocol converters and rewriting them. We prove the correctness of the protocol converters by the algebra for hybrid programming languages ([4]), which ensures the correctness of all the new partitioning rules.

[*] Partially supported by NNSFC No. 69873003
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The algebraic approach advocated in this paper has been successfully employed in the **ProCoS** project on "Provably Correct Systems" [8, 6]. Sampaio showed how to reduce the compiler design task to one of program transformation by program algebra [14]. Ian Page *et al* made rapid advance in the development of hardware compilation technique using an Occam-like language targeted towards Field Programmable Gate Arrays [12], and He Jifeng *et al* provided a formal verification of the hardware compilation scheme within the algebra of Occam programs [5].

The remainder of this paper is organized as follows. Section 2 retrospects the original hardware/software partitioning framework and points out those parts that can be reused in the work presented here. Section 3 proposes the hybrid partitioning framework and poses the underlying architecture. In section 4, we define the protocol converters and provide the theoretical foundation for them. Section 5 shows how to gain the new partitioning rules from the original ones. A simple conclusion is presented in section 6.

2. Original Framework for Hardware/software Partitioning

This section is a brief introduction to our approach on hardware/software partitioning proposed in [13], which provides shades of results that can be reused, and can be regarded as a starting point of this work.

The hardware/software partitioning approach is pursued within a parallel communicating language, denoted by $\mathcal{L}$, which contains the following syntactic elements:

1. Sequential Process:

$$\begin{aligned} S \;::=\;& PC \text{ (primitive command)} \\ \mid\;& S; S \text{ (sequential composition)} \\ \mid\;& \mathit{if}\; b\, S\; \mathit{else}\; S \text{ (conditional)} \\ \mid\;& S \sqcap S \text{ (non-deterministic choice)} \\ \mid\;& \mathit{while}\; b\, S \text{ (iteration)} \\ \mid\;& (g\ S) \,[\!]\, (g\ S) \text{ (guarded choice)} \end{aligned}$$

where $PC \;::=\; (x := e) \mid \mathit{skip} \mid \mathit{chaos} \mid c!e \mid c?x$ and g is *skip* or a communication event $c!e$ or $d?x$.

2. Parallel Program:

$$P \;::=\; S \mid P \parallel P \mid \mathbf{var}\; x \bullet P$$

In later discussions, we adopt $Var(P)$ and $Chan(P)$ to denote the set of variables and channels employed by P, respectively.

Our former hardware/software partitioning process is illustrated in Figure 1. The specification to be partitioned is a

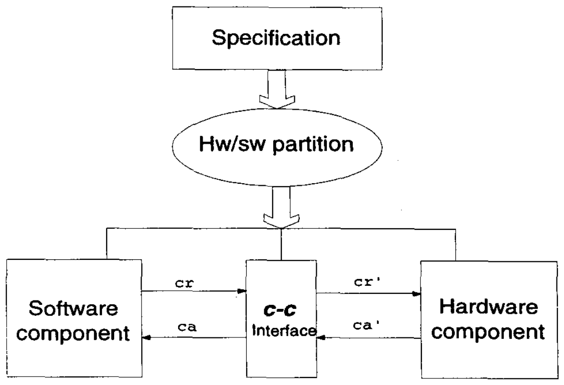

Figure 1. The original hardware/software partitioning process

sequential program within the language $\mathcal{L}$. A collection of syntax-based partitioning rules has been developed to partition the specification into hardware and software components.

It is required that both the hardware and software components satisfy the handshaking protocol [9, 10] and enjoy specially-chosen forms of our language $\mathcal{L}$.

The software component is chosen from the sequential subset of $\mathcal{L}$. It is a member of the set of processes $CP(B)$, for a given set of channels $B = \{cr_j, ca_j \mid j \in I\}$, where the set $CP(B)$ is the minimal set generated by following rules:

(1). a communicating process C, which does not use any channel in B, but $Chan(C) \supseteq B$.

(2). $cr_j!e;\ C;\ ca_j?x$, where C is a member of $CP(B)$ not interacting via any channel in B.

(3). $C_1; C_2$, or $C_1 \sqcap C_2$, or $\mathit{if}\; b\, C_1\; \mathit{else}\; C_2$, or $(g_1\ C_1)[\!](g_2\ C_2)$, where both g_i and C_i lie in $CP(B)$, for $i = 1, 2$.

(4). $\mathit{while}\; b\, C$, where C is a member of $CP(B)$.

The hardware component is chosen from the set of processes $H_V(B')$, for a given set of channels $B' = \{cr'_j, ca'_j \mid j \in I\}$, and the set of data variables $V = \{x_j, y_j \mid j \in I\}$. The set $H_V(B')$ is composed by the processes of the form:

$$D_V^{B'} \;=\; \mu X \bullet ([\!]_{j\in I}(cr'_j?x_j; M_j; ca'_j!y_j; X)[\!]\mathit{skip})$$

where none of M_j mentions channels in B'. The communicating process $D_V^{B'}$ represents a digital device which offers a set of services, each of which responds to a request from its environment on an input channel cr'_j by running the corresponding program M_j and delivering the result to the output channel ca'_j afterwards.

To simplify the interface design, in [13], we confined the interactions between the hardware and software components to the communications along the channels from the set B. However, in general, the hardware component is chosen from $H_V(B')$, which employs a different set of channels B'. Thus, an explicit interface component is needed to deal with the interaction between hardware and software. Such an interface is of the form

$$\begin{array}{l} c\text{-}c(B, B') =_{df} \\ \mu X \bullet ([\!]_{i \in I}(cr_i \,?\, x_i; cr'_i \,!\, x_i; ca'_i \,?\, y_i; ca_i \,!\, y_i; X) \,[\!]\, skip) \end{array}$$

which passes the request along a channel cr_i into the corresponding channel cr'_i, then delivers the acknowledgement from a channel ca'_i back into ca_i. The notion *c–c* means "from channel-based to channel-based".

The syntax-based hardware/software partitioning rules were developed in two different styles: the bottom-up and top-down one. We illustrate some as follows.

Bottom-up Rule for Sequential Composition

$$\frac{\begin{array}{c} Split_B(S_i,\ C_i,\ D),\ i = 1,2 \\ Var(S_1) = Var(S_2) \\ Chan(C_1) = Chan(C_2) \end{array}}{Split_B(S_1; S_2,\ C_1; C_2,\ D)}$$

Bottom-up Rule for Conditional

$$\frac{\begin{array}{c} Split_B(S_i,\ C_i,\ D),\ i = 1,2 \\ Var(S_1) = Var(S_2) \\ Chan(C_1) = Chan(C_2) \\ Var(b) \subseteq Var(C_1) \end{array}}{Split_B(if\ b\, S_1\ else\, S_2,\ if\ b\, C_1\ else\, C_2,\ D)}$$

Bottom-up Rule for Iteration

$$\frac{\begin{array}{c} Split_B(S,\ C,\ D) \\ Var(b) \subseteq Var(C) \end{array}}{Split_B(while\ b\, S,\ while\ b\, C,\ D)}$$

Bottom-up Rule for Non-deterministic Choice

$$\frac{\begin{array}{c} Split_B(S_i,\ C_i,\ D),\ i = 1,2 \\ Var(S_1) = Var(S_2) \\ Chan(C_1) = Chan(C_2) \end{array}}{Split_B(S_1 \sqcap S_2,\ C_1 \sqcap C_2,\ D)}$$

Top-down Rule for Sequential Composition

$$\frac{\begin{array}{c} Split_{B_i}(S_i,\ C_i,\ D_i),\ i = 1,2 \\ Var(S_1) = Var(S_2) \\ Chan(S_1) = Chan(S_2) \\ consist(D_1, D_2) \end{array}}{Split_{B_1 \cup B_2}(S_1; S_2,\ C_1; C_2,\ union(D_1, D_2))}$$

Top-down Rule for Conditional

$$\frac{\begin{array}{c} Split_{B_i}(S_i,\ C_i,\ D_i),\ i = 1,2 \\ Var(S_1) = Var(S_2),\ Chan(S_1) = Chan(S_2) \\ consist(D_1, D_2),\ Var(b) \subseteq Var(C_1) \end{array}}{Split_{B_1 \cup B_2}(if\ b\, S_1\ else\, S_2,\ if\ b\, C_1\ else\, C_2,\ union(D_1, D_2))}$$

where the predicate $Split_B(S,\ C,\ D)$ is defined in [13], which specifies that the process with C and D in parallel is a refinement of the specification S, the predicate $consist(D_1, D_2)$ indicates that D_1 and D_2 employ the same set of variables and the same set of external channels, i.e., the channels not used for communications with the software component. $union(D_1, D_2)$ represents a digital device providing the union set of services supplied by both D_1 and D_2.

The complete set of rules can be reached in [13]. Based on those rules and the new interface we will construct, we can generate the new partitioning rules within a hybrid parallel language framework, where the software component is written in a high level communicating language as above, however, the hardware component is coded within a hardware description language (HDL) as Verilog, which will facilitate the hardware synthesis.

3. The Hybrid Partitioning Architecture

This section presents our hybrid partitioning framework, in which we will partition a specification coded in the sequential subset of $\mathcal{L}$ into three components: a software component owning the same form as that in our former work, a hardware component written in the Verilog HDL, and an interface component to tackle the interactions between hardware and software.

It is worth noting that the hardware and software component will adopt different communicating mechanisms, the signal-based communicating mechanism and the channel-based one respectively. Due to this fact, the partitioning framework is called hybrid([4]), and the interface component proves to be critical in the sense that it transforms information between two processes under different protocols.

For ease of understanding, we give the source language and the target ones separately, instead of the whole framework. Our source language is the sequential subset of the language $\mathcal{L}$ defined in Section 2.

The software component generated by our partitioning process will own the same form as that in the original framework, i.e, will be a member of the set of communicating processes $CP(B)$, for the given channel set B as defined earlier, which communicates with the environment via communications on channels.

However, the hardware component delivered by our partitioning process will enjoy a quite different form from that in the approach described in Section 2. It will be a specially chosen process from Verilog HDL, rather than a process in $\mathcal{L}$.

Given a set of signal variables $E = \{er_i, ea_i \mid i \in I\} \cup \{ter\}$, and a set of data variables $V = \{x_i, y_i \mid i \in I\}$, we define a set of processes $\mathcal{D}(E, V)$, which is composed by processes of the following form:

$$D_V^E =_{df}$$
$$\mu X \bullet (\|_{i \in I}(@er_i; M_i(x_i, y_i); \rightarrow ea_i; X) \,\|\, (@ter; skip))$$

where $@er_i$ and $\rightarrow ea_i$ are respectively an input signal and an output signal in Verilog. The signal ter is used for synchronized termination. Each $M_i(x_i, y_i)$ has input parameter x_i and output parameter y_i, and is a member of the set of Verilog processes $MP(V)$, which is constructed by the following rules:

(1). $v := e$, or *skip*, or *chaos*, where no signal variables from E occur in v or e;

(2). $M; M'$, or *if* $b\, M$ *else* M', or *while* $b\, M$, where $M, M' \in MP(V)$.

The signal-driven process D_V^E represents a digital device which offers a set of services to its environment, each of them responds to a request from its environment via an input signal er_j by running the corresponding program M_j, then putting the result to variable y_j and delivering an acknowledgement through the output signal ea_j afterwards.

Since the hardware and software components adopt different communication mechanisms, the interface component to tackle their interactions should enjoy a hybrid form and convert information between these two levels.

4. The Interface Component as a Protocol Converter

This section pursues the construction of the interface component. From the hybrid architecture mentioned above, we know that the interface component plays an essential role between the hardware and software as a protocol converter ([2]). Rather than construct the interface straightforwardly, we derive it indirectly from our original work by splitting the interface process into two parallel ones, which as well inspires us to obtain the complete set of partitioning rules from that in [13] without redefining them from scratch.

4.1. Protocol Converters

We define several protocol converters in this subsection, one of which will be adopted as the interface component between hardware and software within our partition framework.

First of all, we denote six sets that will be used frequently in following discussions:

sets of channel names: $B = \{cr_i, ca_i \mid i \in I\}$, and $B' = \{cr'_i, ca'_i \mid i \in I\}$;

sets of signal variables: $E = \{er_i, ea_i \mid i \in I\} \cup \{ter\}$, and $E' = \{er'_i, ea'_i \mid i \in I\} \cup \{ter'\}$;

sets of data variables: $V = \{x_i, y_i \mid i \in I\}$, and $V' = \{x'_i, y'_i \mid i \in I\}$.

The protocol converters are defined as follows.

Definition 4.1 (Protocol Converters) *The process $c\text{–}c(B, B')$ is a converter between two communicating protocols on B and B', respectively:*

$$c\text{–}c(B, B') =_{df}$$
$$\mu X \bullet \begin{pmatrix} \|_{i \in I}(cr_i\,?\,x_i; cr'_i\,!\,x_i; ca'_i\,?\,y_i; ca_i\,!\,y_i; X) \\ \|\, skip \end{pmatrix}$$

Similarly, the process $s\text{–}s(E, E')$ converts a signal-driven protocol concerned with signals on E into that with respect to signals on E':

$$s\text{–}s(E, E') =_{df}$$
$$\mu X \bullet \begin{pmatrix} \|_{i \in I}(@er_i; \rightarrow er'_i; @ea'_i; \rightarrow ea_i; X) \\ \|\, (@ter; \rightarrow ter') \end{pmatrix}$$

The two protocol converters to appear convert between protocols on two different levels. The process $c\text{–}s_V(B, E)$ converts a communicating protocol on B into a signal-driven protocol on E, whereas the process $s\text{–}c_V(E, B)$ is the reverse. The data variables from V are used to hold the information delivered by communication events:

$$c\text{–}s_V(B, E) =_{df}$$
$$\mu X \bullet \begin{pmatrix} \|_{i \in I}(cr_i\,?\,x_i; \rightarrow er_i; @ea_i; ca_i\,!\,y_i; X) \\ \|\, (skip; \rightarrow ter) \end{pmatrix}$$

$$s\text{–}c_V(E, B) =_{df}$$
$$\mu X \bullet \begin{pmatrix} \|_{i \in I}(@er_i; cr_i\,!\,x_i; ca_i\,?\,y_i; \rightarrow ea_i; X) \\ \|\, (@ter; skip) \end{pmatrix} \quad \square$$

Theorem 4.2 (Compositionality of Protocol Converters) *Each of the protocol converters mentioned above is a parallel composition of other two.*

(1). $c\text{–}c(B, B') = c\text{–}s_V(B, E) \parallel s\text{–}c_V(E, B')$, provided all variables in E and V are local ones only shared by $c\text{–}s_V(B, E)$ and $s\text{–}c_V(E, B')$;

(2). $s\text{–}s(E, E') = s\text{–}c_V(E, B) \parallel c\text{–}s_V(B, E')$, provided all channels in B are local ones only shared by $s\text{–}c_V(E, B)$ and $c\text{–}s_V(B, E')$;

(3). $c\text{–}s_V(B, E) = c\text{–}c(B, B') \parallel c\text{–}s_V(B', E)$, provided channels in B' are only used to perform communication between $c\text{–}c(B, B')$ and $c\text{–}s_V(B', E)$;

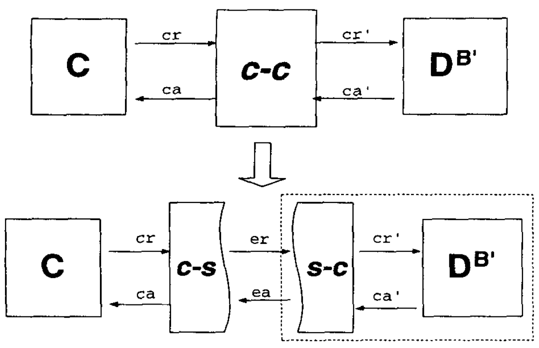

Figure 2. Protocol converter and interface derivation

(4). $s\text{-}c_V(E,B) = s\text{-}s(E,E') \parallel s\text{-}c_V(E',B)$, provided variables in E' are only shared by $s\text{-}s(E,E')$ and $s\text{-}c_V(E',B)$. $\square$

Theorem 4.2 explores the compositionality of protocol converters. As a by-product, it inspires us the way to derive the hybrid interface from the original one, and as well to compose the new hardware component under Verilog from that under $\mathcal{L}$.

Theorem 4.3 (Hardware Derivation) *The hardware component on different levels (defined in last two sections) can be derived from one another by protocol converters.*

(1). $D_V^B = c\text{-}s_V(B,E) \parallel D_V^E$, provided signal variables from E are local ones only shared by $c\text{-}s_V(B,E)$ and D_V^E;

(2). $D_{V'}^E = s\text{-}c_V(E,B') \parallel D_{V'}^{B'}$, provided channels in B' are only used by $s\text{-}c_V(E,B')$ and $D_{V'}^{B'}$ to arrange their interactions. $\square$

Theorem 4.3 shows that the new hardware component $D_{V'}^E$ in Verilog HDL can be constructed from the communicating one $D_{V'}^{B'}$ and a protocol converter. As well it reveals the way to generate the partitioning rules directly from the original ones. The interface and hardware derivation process is shown in Figure 2, where *c–s* denotes the new interface component, the dotted-box represents the new hardware component which hides those channels from B'.

4.2. Algebraic Proofs

We present the proofs for theorem 4.2 and 4.3 using program algebra in this subsection.

In addition to the algebraic laws mentioned in [13, 7, 4], we investigate the following laws, which will be used in the proofs later on.

The first law is an expansion law for the hybrid programming language([4]).

HL1 (*hgc-expan*, hybrid guarded choice expansion)

Let $G_1 = [\!]_{i\in I}(g_i; P_i)$, and $G_2 = [\!]_{j\in J}(h_j; Q_j)$, where g_i and h_j are of the form $ch\,!\,e$, or $ch\,?\,x$, or *skip*, or output event $\rightarrow ev$, or input event $@ev$, for all $i \in I$ and $j \in J$.

Let g and h denote the disjunction of all input event guards in G_1 and G_2, respectively. Then

$G_1 \parallel G_2 = [\!]_{r=1}^{n}(k_r; R_r)$, where the pairs $\langle k_r, R_r\rangle$ are precisely all possibilities from the following:

(1) $R_r = P_i \parallel G_2$, and
$k_r = g_i = skip$ or $k_r = g_i = ch\,!\,e$ or $k_r = g_i = ch\,?\,x$, where $ch \notin Chan(G_2)$, or
$k_r = g_i = \rightarrow ev$, or
$k_r = g_i \wedge \neg h$, and $g_i = @ev$

(2) $R_r = G_1 \parallel Q_j$, and
$k_r = h_j = skip$ or $k_r = h_j = ch\,!\,e$ or $k_r = h_j = ch\,?\,x$, where $ch \notin Chan(G_1)$, or
$k_r = h_j = \rightarrow ev$, or
$k_r = h_j \wedge \neg g$, and $h_j = @ev$

(3) $R_r = P_i \parallel Q_j$, and
$k_r = g_i \wedge h_j$, and $g_i = @ev$ and $h_j = @eu$

(4) $R_r = x := e; (P_i \parallel Q_j)$, and $k_r = skip$, and
$g_i = ch\,!\,e$, and $h_j = ch\,?\,x$, or
$g_i = ch\,?\,x$, and $h_j = ch\,!\,e$ $\square$

The second and third laws deal with two special cases with regard to signals .

HL2 (*eg-elim*, event guards elimination)

Let $P = G\,[\!]\,(@ev; Q)$, where G is a guarded choice, and ev is not a shared variable between P and its environment, then $P = G$. $\square$

HL3 (*self-trig*)

Let $P = \rightarrow ev; ((@ev; Q)\,[\!]\,G)$, where ev is not shared by the environment of P, and none of guards in G mentions ev, then $P = skip; Q$. $\square$

The following lemma is needed later in the proof of theorem 4.3.

Lemma 4.4 *Let $P = M; P_1$, where $M \in MP(V)$, and G be a guarded choice construct not containing output guards of the kind $\rightarrow e$, where all guards in G are only shared by*

P and G, then we have

$$P \parallel G \;=\; M; (P_1 \parallel G). \qquad \square$$

It can be proved by a simple structural induction on M.

Now we can prove the theorems mentioned in last subsection.

The proof of theorem 4.2

(1). For brevity, we denote $c\text{–}s_V(B,E)$ as $c\text{–}s$ and $s\text{–}c_V(E,B')$ as $s\text{–}c$.

RHS

$\{(hgc\text{-}expan),\ (eg\text{-}elim)\}$

$= [\!]_{i\in I}\,(cr_i\,?\,x_i; ((\rightarrow er_i; @ea_i; ca_i\,!\,y_i;\ c\text{–}s \parallel s\text{–}c))\,[\!]\,skip$

$\{(hgc\text{-}expan),\ (eg\text{-}elim),\ (self\text{-}trig)\}$

$= [\!]_{i\in I}\,(cr_i\,?\,x_i; skip;\ ((@ea_i; ca_i\,!\,y_i; c\text{–}s) \parallel (cr'_i\,!\,x_i; ca'_i\,?\,y_i; \rightarrow ea_i; s\text{–}c)))\,[\!]\,skip$

$\{(hgc\text{-}expan),\ (eg\text{-}elim)\}$

$= [\!]_{i\in I}\,(cr_i\,?\,x_i; skip; cr'_i\,!\,x_i;\ ((@ea_i; ca_i\,!\,y_i; c\text{–}s) \parallel (ca'_i\,?\,y_i; \rightarrow ea_i; s\text{–}c)))\,[\!]\,skip$

$\{(hgc\text{-}expan),\ (eg\text{-}elim)\}$

$= [\!]_{i\in I}\,(cr_i\,?\,x_i; cr'_i\,!\,x_i; ca'_i\,?\,y_i;\ ((@ea_i; ca_i\,!\,y_i; c\text{–}s) \parallel (\rightarrow ea_i; s\text{–}c)))\,[\!]\,skip$

$\{(hgc\text{-}expan),\ (eg\text{-}elim),\ (self\text{-}trig)\}$

$= [\!]_{i\in I}\,(cr_i\,?\,x_i; cr'_i\,!\,x_i; ca'_i\,?\,y_i; skip;\ ((ca_i\,!\,y_i; c\text{–}s) \parallel s\text{–}c))\,[\!]\,skip$

$\{(hgc\text{-}expan),\ (eg\text{-}elim)\}$

$= [\!]_{i\in I}\,(cr_i\,?\,x_i; cr'_i\,!\,x_i; ca'_i\,?\,y_i; skip; ca_i\,!\,y_i;\ (c\text{–}s \parallel s\text{–}c))\,[\!]\,skip$

$\{unique\ fixed\ point\ for\ guarded\ recursion\}$

$= LHS$

(2)-(4). Similar to (1). $\square$

The proof of theorem 4.3

(1). For brevity, we denote $c\text{–}s_V(B,E)$ as $c\text{–}s$.

RHS

$\{(hgc\text{-}expan),\ (eg\text{-}elim)\}$

$= [\!]_{i\in I}\,(cr_i\,?\,x_i;\ ((\rightarrow er_i; @ea_i; ca_i!y_i; c\text{–}s) \parallel D^E_V))\,[\!]\,(skip; (\rightarrow ter \parallel D^E_V)))$

$\{(hgc\text{-}expan),\ (eg\text{-}elim),\ (self\text{-}trig)\}$

$= [\!]_{i\in I}\,(cr_i\,?\,x_i; skip;\ ((@ea_i; ca_i!y_i; c\text{–}s) \parallel (M_i(x_i,y_i); \rightarrow ea_i; D^E_V)))\,[\!]\,(skip; skip)$

$\{Lemma\ 4.4\}$

$= [\!]_{i\in I}\,(cr_i\,?\,x_i; skip; M_i(x_i,y_i);\ ((@ea_i; ca_i!y_i; c\text{–}s) \parallel (\rightarrow ea_i; D^E_V)))\,[\!]\,skip$

$\{(hgc\text{-}expan),\ (eg\text{-}elim),\ (self\text{-}trig)\}$

$= [\!]_{i\in I}\,(cr_i\,?\,x_i; M_i(x_i,y_i); skip;\ ((ca_i!y_i; c\text{–}s) \parallel D^E_V))\,[\!]\,skip$

$\{(hgc\text{-}expan),\ (eg\text{-}elim)\}$

$= [\!]_{i\in I}\,(cr_i\,?\,x_i; M_i(x_i,y_i); skip; ca_i!y_i;\ (c\text{–}s \parallel D^E_V))\,[\!]\,skip$

$\{unique\ fixed\ point\ for\ guarded\ recursion\}$

$= LHS$

(2). Similar to (1). $\square$

5. Partitioning Rules in the Hybrid Framework

This section aims to generate hardware/software partitioning rules within the hybrid framework from those ones in [13] by using protocol converters.

To specify the partitioning rules, we introduce a new predicate $Split^E_B(S, C, c\text{–}s_V, D^E_V)$ which is defined by:

$$\begin{array}{l} Split^E_B(S, C, c\text{–}s_V, D^E_V) =_{df} \\ \quad Split_B(S, C, (c\text{–}s_V(B,E) \parallel D^E_V)) \end{array}$$

where the predicate $Split_B$ is defined in [13] and is explained in section 2.

The following lemma is directly from theorem 4.3.

Lemma 5.1 *We have*

$Split_B(S, C, D^B_V)$ **implies** $Split^E_B(S, C, c\text{–}s_V, D^E_V)$. $\square$

Based on this lemma, we generate all *bottom-up* rules straightforwardly as follows.

Bottom-up Rule for Sequential Composition

$$\frac{\begin{array}{c} Split^E_B(S_i,\ C_i,\ c\text{–}s_V,\ D^E_V),\ i = 1,2 \\ Var(S_1) = Var(S_2) \\ Chan(C_1) = Chan(C_2) \end{array}}{Split^E_B(S_1; S_2,\ C_1; C_2,\ c\text{–}s_V,\ D^E_V)}$$

Bottom-up Rule for Conditional

$$\frac{\begin{array}{c} Split^E_B(S_i,\ C_i,\ c\text{–}s_V,\ D^E_V),\ i = 1,2 \\ Var(S_1) = Var(S_2) \\ Chan(C_1) = Chan(C_2) \\ Var(b) \subseteq Var(C_1) \end{array}}{Split^E_B(if\ b\ S_1\ else\ S_2,\ if\ b\ C_1\ else\ C_2,\ c\text{–}s_V,\ D^E_V)}$$

Bottom-up Rule for Iteration

$$\frac{Split^E_B(S,\ C,\ c\text{–}s_V,\ D^E_V),\ Var(b) \subseteq Var(C)}{Split^E_B(while\ b\ S,\ while\ b\ C,\ c\text{–}s_V,\ D^E_V)}$$

When $Var(b) \cap Var(D) \neq \emptyset$, we will introduce a local variable lb, and rewrite the conditional and iteration into the forms

$\textbf{var}\ lb \bullet (lb := b;\ if\ lb\, S_1\ else\, S_2)$, and

$\textbf{var}\ lb \bullet (lb := b;\ while\ lb\,(S;\ lb := b))$

respectively by the laws in [13].

Bottom-up Rule for Non-deterministic Choice

$$\frac{\begin{array}{c} Split_B^E(S_i,\ C_i,\ c\text{–}s_V,\ D_V^E),\ i = 1,2 \\ Var(S_1) = Var(S_2) \\ Chan(C_1) = Chan(C_2) \end{array}}{Split_B^E(S_1 \sqcap S_2,\ C_1 \sqcap C_2,\ c\text{–}s_V,\ D_V^E)}$$

Bottom-up Rule for Guarded Choice

$$\frac{\begin{array}{c} Split_B^E(S_i,\ C_i,\ c\text{–}s_V,\ D_V^E),\ i = 1,2 \\ Var(S_1) = Var(S_2) \\ Chan(C_1) = Chan(C_2) \\ Var(g_i) \subseteq Var(C_1),\ Chan(g_i) \subseteq Chan(C_1),\ i = 1,2 \end{array}}{Split_B^E((g_1\ S_1)[\!](g_2\ S_2),\ (g_1\ C_1)[\!](g_2\ C_2),\ c\text{–}s_V,\ D_V^E)}$$

Before presenting the *top-down* partitioning rules, we introduce some notations and abbreviations which will be frequently used in the forthcoming rules.

Let

$E_i =_{df} \{er_j, ea_j \mid j \in I_i\} \cup \{ter\},\ i = 1,2$

$B_i =_{df} \{cr_j, ca_j \mid j \in I_i\},\ i = 1,2$

$V_i =_{df} \{x_j, y_j \mid j \in I_i\},\ i = 1,2$

For simplicity, from now on, we will always assume that

$E_1 \cap E_2 = \{ter\}, B_1 \cap B_2 = \emptyset, V_1 \cap V_2 = \emptyset.$

Given $c\text{–}s_{V_i}(B_i, E_i)$, for $i = 1,2$, we define

$c\text{–}s =_{df} c\text{–}s_{V_1 \cup V_2}(B_1 \cup B_2, E_1 \cup E_2).$

Given

$$D_{V_i}^{E_i} = \mu X \bullet \left(\begin{array}{l} [\!]_{j \in I_i}(@er_j; M_j(x_j, y_j); \rightarrow ea_j; X) \\ [\!]\,(@ter; skip) \end{array} \right),$$

for $i = 1,2$, we define

$ExlVar(D_{V_i}^{E_i}) =_{df} Var(D_{V_i}^{E_i}) \backslash (E_i \cup V_i),$

$D = merge(D_{V_1}^{E_1}, D_{V_2}^{E_2}) =_{df}$

$$\mu X \bullet \left(\begin{array}{l} [\!]_{i \in I_1 \cup I_2}(@er_i; M_i(x_i, y_i); \rightarrow ea_i; X) \\ [\!]\,(@ter; skip) \end{array} \right).$$

Now it's time to present the *top-down* rules in our new partitioning framework.

Top-down Rule for Sequential Composition

$$\frac{\begin{array}{c} Split_B^E(S_i,\ C_i,\ c\text{–}s_{V_i},\ D_{V_i}^{E_i}),\ i = 1,2 \\ Var(S_1) = Var(S_2) \\ Chan(C_1) = Chan(C_2) \\ ExlVar(D_{V_1}^{E_1}) = ExlVar(D_{V_2}^{E_2}) \end{array}}{Split_{B_1 \cup B_2}^{E_1 \cup E_2}(S_1; S_2,\ C_1; C_2,\ c\text{–}s,\ D)}$$

Top-down Rule for Conditional

$$\frac{\begin{array}{c} Split_B^E(S_i,\ C_i,\ c\text{–}s_{V_i},\ D_{V_i}^{E_i}),\ i = 1,2 \\ Var(S_1) = Var(S_2) \\ Chan(C_1) = Chan(C_2) \\ ExlVar(D_{V_1}^{E_1}) = ExlVar(D_{V_2}^{E_2}) \\ Var(b) \subseteq Var(C_1) \end{array}}{Split_{B_1 \cup B_2}^{E_1 \cup E_2}(if\ b\, S_1\ else\, S_2,\ if\ b\, C_1\ else\, C_2,\ c\text{–}s,\ D)}$$

Top-down Rule for Non-deterministic Choice

$$\frac{\begin{array}{c} Split_B^E(S_i,\ C_i,\ c\text{–}s_{V_i},\ D_{V_i}^{E_i}),\ i = 1,2 \\ Var(S_1) = Var(S_2) \\ Chan(C_1) = Chan(C_2) \\ ExlVar(D_{V_1}^{E_1}) = ExlVar(D_{V_2}^{E_2}) \end{array}}{Split_{B_1 \cup B_2}^{E_1 \cup E_2}(S_1 \sqcap S_2,\ C_1 \sqcap C_2,\ c\text{–}s,\ D)}$$

Top-down Rule for Guarded Choice

$$\frac{\begin{array}{c} Split_B^E(S_i,\ C_i,\ c\text{–}s_{V_i},\ D_{V_i}^{E_i}),\ i = 1,2 \\ Var(S_1) = Var(S_2) \\ Chan(C_1) = Chan(C_2) \\ ExlVar(D_{V_1}^{E_1}) = ExlVar(D_{V_2}^{E_2}) \\ Var(g_i) \subseteq Var(C_1),\ Chan(g_i) \subseteq Chan(C_1),\ i = 1,2 \end{array}}{Split_{B_1 \cup B_2}^{E_1 \cup E_2}((g_1\ S_1)[\!](g_2\ S_2),\ (g_1\ C_1)[\!](g_2\ C_2),\ c\text{–}s,\ D)}$$

6 Conclusion

Hardware/software partition is a critical phase, and as well a challenging issue in hardware/software co-design process. One possible way is to cope with the specification of hardware, software and the interface between them separately, but this approach can hardly ensure that the composition of the three separate specifications satisfy the original requirement. In this sense, the co-specification of hardware, software and their interface has its superiority. In [13], we proposed a formal model for hardware/software partition within Occam algebra, in which a collection of provable partitioning rules have been explored. In that model, the interactions between hardware and software components appear very simple, due to the fact that they are both coded within the same high level communication language, which, on the other hand, reflects there exists a wide gap between our hardware component and the low level hardware description needed in later hardware synthesis phase.

In this paper, we refine the original partition approach and try to produce the hardware component coded directly in Verilog HDL. We adopt a hybrid partitioning framework, in which our partitioning process generates from the original system specification (a high level source program) three components: the software component in the high level communication language, the hardware component coded in Verilog HDL, and a hybrid interface component to cope with their interactions. Rather than construct partitioning rules in the new framework from scratch and then verify them, we introduce a set of protocol converters, from which we derive the new rules directly from the well-built ones in [13], and generate the new interface component together with the new hardware component.

Such an approach owns at least two merits: firstly, the original proved partitioning rules in our former model can be reused, and the proofs for the new rules become straightforward; secondly, the new hardware component is directly coded in Verilog HDL, which will facilitate the compilation from it down to the low level synthesizable description. However, the further synthesis of the interface component is still a challenging issue, which should be part of our future work. As other future work, we shall reconfigure and reorganize the hardware component so as to optimize it and reuse its sub-components. Certain algebraic transformations shall be conducted to link our hardware component with the hardware specification to be compiled in [11] using Verilog algebra.

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