Phasor Measurement Unit and Sampled Values: Measurement and Implementation Challenges

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***Abstract*—In recent years, the electrical substations are experiencing a rapid transition towards a fully digital measurement infrastructure, in terms of data acquisition, storage and processing. The IEC Std 61850-9-2 defines the data format, also known as Sampled Value (SV), to be employed by instrument transformers, merging units, and controller devices. In this scenario, it is reasonable to expect that also Phasor Measurement Units (PMUs) will be directly connected with digital instrument transformers and will be required to process directly the SV data stream. In this paper, we present the design and development of a stand-alone PMU based on digital inputs. The prototype has been characterized in terms of estimation accuracy and computational requirements, by means of a dedicated IEC Std 61850-9-2 calibration system. The preliminary results prove the potential of SV-based PMUs, but also reveal some implementation bottlenecks that have to be properly addressed before an effective deployment on the field.**

I. Introduction

Modern power systems are characterized by an ever-increasing penetration of distributed generation and renewable energy sources [1], [2]. Due to their inherent volatility and lack of rotating inertia, such resources are likely to produce faster dynamics and high distortion levels, that might interfere with the traditional monitoring and control schemes [3]–[5].

In order to address these issues, electrical substations are experiencing a rapid transition towards a fully digital measurement infrastructure, that promises to guarantee higher levels of control, responsiveness, cost management and safety. In this context, the IEC Std 61850 defines the substation communication protocols and the need for interoperability between systems from different vendors [6]–[8].

Such communication protocol includes different message types, specifically designed for applications like device synchronization, actuators' control, measurement data, etc. In this regard, the IEC Std 61850-9-2 [9] and its recent amendment [10] (IEC Std) introduces the Sampled Values (SV) protocol as a publisher/subscriber communication for information exchange between Stand Alone Merging Units (SAMUs) and Intelligent Electronic Devices (IEDs) over the Ethernet.

Among the different fields that compose the SV message, the Application Protocol Data Unit (APDU) is the actual payload: up to eight Application Specific Data Units (ASDUs), each consisting of a three-phase current and voltage measurement (16-bit resolution). Each measurement is time-stamped by means of a counter that is reset to zero at each new second occurrence. As the IEC Std relies on the Ethernet, the most common synchronization source is represented by the Precision Time Protocol (PTP) [11]. In the SV protocol, the publisher sends messages (typically, the digitized values of an instrument transformer secondary circuit) with a fixed rate that depends on the nominal system rate (i.e. 50 or 60 Hz) and the number of samples per cycle (i.e. 80 or 256), divided by the number of ASDUs (i.e. from 1 to 8).

The SV protocol was originally conceived to efficiently store and transmit the output of non-conventional instrument transformers (NCITs) and SAMUs. In recent years, though, the ever-increasing deployment of Phasor Measurement Units also at distribution level is pushing for an integration between phasor estimation and digital data stream [12]. In this way, the data stream transmitted from the substation to the control room would be twofold: on one side, the real-time digitized output of NCITs and SAMUs; on the other side, a more *compressed* format consisting of the synchrophasor, frequency and Rate-Of-Change-Of-Frequency (ROCOF) associated to the fundamental component.

A PMU that processes directly the SV data stream, briefly a SV-PMU, could benefit of the following advantages. The SVs are already time-stamped, so there is no need for internal synchronization units. Moreover, the data format is standardized and the SV-PMU could be easily deployed in any substation compliant with the IEC Std.

On the other hand, the SVs are transmitted as User Datagram Protocol (UDP) packets: the absence of re-transmissions might result in packet losses. Furthermore, the PMU should be able to deal with a fixed-rate data steam in terms of communication interface and processing capabilities, whereas the traditional scheme with analog inputs and digitizers allows for much more flexible solutions.

The recent project FutureGrid II has been investigating the measurement needs and potential of SVs in modern electrical substations. In this context, the recent literature has proposed a new calibration infrastructure for transmitting and receiving SVs [13], [14], and software libraries have been developed to facilitate the implementation of this communication protocol also in low-cost real-time controllers [15].

In this paper, we present the design, development and preliminary characterization of a SV-PMU. To the best of the Authors' knowledge, it represents the first attempt of realizing a stand-alone PMU that relies only on digital inputs. First, we discuss the main challenges in terms of hardware implemen-

tation and measurement procedure. Then, we characterize the SV-PMU performance against the IEC Std calibrator.

The paper is organized as follows. In Section II, we introduce the hardware architecture of the SV-PMU. Section III describes the software libraries for the efficient management of SV data streams. In Section IV, we characterize the performance of the SV-PMU in terms of estimation accuracy and computational requirements. Finally, Section V provides some closing remarks and outlines the research following steps.

II. Hardware Implementation

The SV-PMU relies on a NI cRIO-9068 (National Instruments, Austin, US-TX), i.e. an embedded industrial controller equipped with a Linux Real-Time (RT) Operative System (OS) and a re-configurable Field Programmable Gate Array (FPGA) board. More precisely, the cRIO-9068 relies on a 667-MHz dual-core ARM Cortex-A9 (Arm Holdings, Cambridge, GBR) processor, and a Xilinx Artix-7 (Xilinx, San Jose, US-CA) FPGA board. In principle, the RT controller is responsible for capturing the SV data stream, whereas the second one can be used to expedite the processing of the current and voltage measurements.[1] For this analysis, the cRIO-9068 has been programmed in LabVIEW 2020 Real-Time, with the addition of Shared Object libraries, specifically developed for the Linux RT OS (further details in Section III).

As shown in Fig. 1, the cRIO-9068 is equipped with two independent Ethernet boards, compatible with the IEEE Std 802.3 (Gigabit Ethernet) and characterized by a communication rate of 100 Mbps (if auto-negotiated, up to 1000 Mbps). The fist board (Ethernet 0) is reserved for the bi-directional communication with the host computer, and allows for programming the controller and retrieving in real-time the measurement results. The second board (Ethernet 1), instead, is responsible of capturing the SV data stream. The Ethernet tranceivers communicate with the RT by means of a Reduced Gigabit Media-Independent Interface (RGMII). Once received the SV messages, the RT extracts the ASDUs, stores the current and voltage measurements, and processes them in order to extract the parameters of interest. In this sense, it is worth noticing that the volatile and non-volatile memory are limited to 512 MB of Double Data Rate 3 Synchronous Dynamic Random-Access Memory, and 1 GB of NAND flash drive.

For the characterization of the SV-PMU, the measurement setup in Fig. 2 has been employed. A Meinberg LANTIME M600 Time Server (Meinberg Funkuhren, Bad Pyrmont, DEU) provides the time reference in terms of a Pulse-Per-Second signal that is aligned with UTC-CH by means of PTP synchronization protocol. A NI PXIe 1062Q hosts the IEC Std calibrator that consists of three main units [13], [14]:

[1]As further discussed in the following Section, at this stage of the research, all the operations are carried out by the RT controller, also for the sake of easier debugging. Nevertheless, the envisioned final implementation envisions the exploitation of the FPGA, aiming at the minimization of computational costs and reporting latencies.

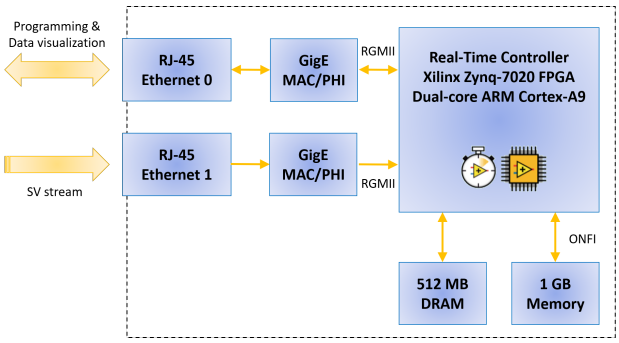

Fig. 1. Block scheme of the data communication and processing paths within the NI cRIO-9068 employed for the implementation of the SV-PMU.

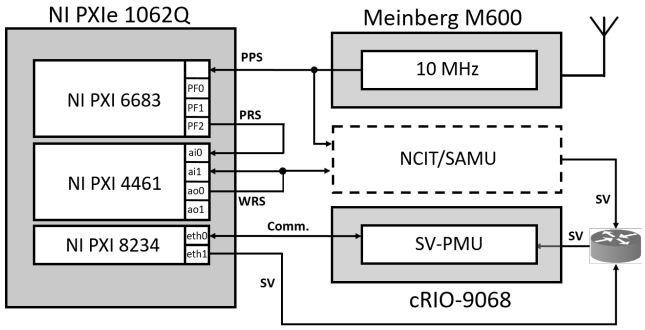

Fig. 2. Measurement setup.

- a synchronization board (NI PXI 6683) that is disciplined by the reference clock PPS and provides the trigger signals (PRS) for the other boards;
- a data acquisition board (NI PXI 4461) that generates the analog test waveforms (WRS) and re-acquires them (along with the PRS) for defining the reference values;
- an Ethernet interface module (NI PXI 8234) that is responsible for the communication with the SV-PMU and generates the SV data stream, synchronously with the analog output WRS signal.

In the typical calibration setup, the device under test is represented by a NCIT or a SAMU that receives the analog test waveform and converts it into an equivalent SV data stream. In this context, the SV-PMU can receive its digital input either from the IEC Std calibrator or the DUT (in Fig. 2, both are connected to a network transparent switch.

In this paper, we consider the first option. In order to characterize the SV-PMU performance, the IEC Std calibrator allows for a perfect knowledge of the SV data stream and facilitates the debugging process. Once validated the prototype, it will be possible to test it in real-world conditions, i.e. directly connected to a NCIT supplied with a known analog input.

III. Software Implementation

The NI Linux Real Time version 8.0 is the operative system which manages the tasks of the RT controller. This guarantees that the time constraints of each process are respected in a deterministic manner, conferring the device great reliability

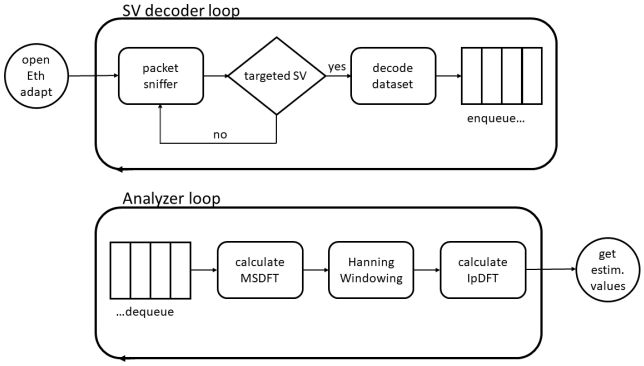

Fig. 3. Logical blocks of the digital PMU with SV input code.

in terms of time execution. The SV-PMU software has been developed in the LabVIEW 2020 Real-Time programming environment by means of a point-to-point Ethernet connection between the cRIO-9068 and a host computer (in our case the NI PXIe 1062Q, see Fig. 2).

The SV-PMU code is structured in two main parts, running in parallel on the RT OS, as illustrated in the flowchart of Fig. 3. The first part, named *SV decoder*, consists of a packet sniffer functionality, which is able to capture the targeted SV data stream as fast as possible, and a decoding functionality, which extracts the measurement data from the APDU and stores them into a First-In-First-Out (FIFO) queue. The second one, named *Analyzer*, reads the current and voltage values from the FIFO queue and process them in order to define the corresponding synchrophasor, frequency and ROCOF associated to the fundamental component. In particular, a simple algorithm that combines a Modulated Sliding DFT (MSDFT) [16] and a two-point interpolation (IpDFT) [17] has been implemented.

A. The SV decoder

The SV decoder code is responsible for three main tasks: the packet sniffing of the Ethenet traffic on Ethernet 1 port, the selection of streams compatible with the IEC Std communication protocol, as well as the decoding and storing of the APDU field. To this end, an *ad hoc* Shared Object library has been deployed in the cRIO-9068. It is worth noticing that the library has been derived from a C/C++ code, previously employed for producing an equivalent Dynamic Linked Library for Windows OS [13], [18]. More precisely, the C/C++ source code has been suitably modified and cross-compiled in such a way as to be compatible with the Linux RT OS. Moreover, since the packet sniffer relies on some functions of the library for packet capture `pcap` [19], also the corresponding Shared Object library has to be correctly installed in the cRIO-9068 and its path has to be accordingly included in the source code cross-compilation.

First, the code opens the adapter associated to the MAC destination address of the SV data stream. The sniffer is initialized in promiscuous mode, i.e. all the received messages are transmitted to the Central Processing Unit (CPU), independently from the adopted communication protocol. At CPU level, the SV messages are identified as the ones whose Ether Type field has a hexadecimal value equal to 88BA. In case of multiple SV data streams, a further refinement is possible by selecting just the messages with a specific MAC source address and SV ID.

Once captured a SV message, the *SV decoder* extracts from the APDU the informative fields, namely the sample counter index and the measured values of the three-phase current and voltage for each ASDU. These values are clustered and stored in a FIFO queue. In this way, it is possible to access in real-time the same data also from the parallel *Analyzer* cycle.

B. The Analyzer

As soon as a new element enters the queue, a dedicated notifier triggers the *Analyzer*. Without loss of generality, it is reasonable to introduce a further starting criterion, namely to start the analysis in correspondence of a SV counter index equal to 0, i.e. in correspondence of a PPS rising edge.

The cluster is extracted from the queue and each current and voltage channel is treated separately and independently. A first subtask performs the MSDFT, a recursive sliding algorithm that allows for efficiently computing a limited set of DFT coefficients. Being interested on the fundamental component only, we consider just the DFT bins in the range from 0 to 100 Hz (i.e. the second harmonic of the nominal system rate). Differently from the traditional DFT that process sample windows, the MSDFT adopts a sample-by-sample procedure. The convergence of this approach depends on the target frequency resolution. For instance, a frequency resolution corresponds to a window length of three nominal cycles, i.e. 240 samples at 4000 Hz. The MSDFT converges to the same results of a traditional DFT after exactly 240 samples. On the other hand, the MSDFT allows for drastically reducing the computational complexity of the DFT bin computation by efficiently exploiting its inherent recursive structure.

At each new sample, the MSDFT invokes a second subtask, named Twiddle Factor, that defines the complex exponential kernel, based on the selected DFT bin, frequency resolution and SV counter index. It is worth noticing that both MSDFT and Twiddle Factor tasks can be easily parallelized for each current and voltage channel and for each DFT bin of interest. In view of an optimized implementation, these operations can be efficiently performed on the FPGA and save further processing power in the RT controller for the other tasks.

Given the DFT bins between 0 and 100 Hz, the estimation of the synchrophasor, frequency and ROCOF associated to the fundamental component is performed by the IpDFT task. First, it invokes the Hanning subtask that combines the consecutive DFT bins in order to apply a Hanning weighing function, that is meant to reduce the spectral leakage contributions from the negative image components. Then, a two-point interpolation routine is applied to the DFT bins around 50 Hz. Finally, the IpDFT estimates are stored in a queue. In correspondence of the selected PMU reporting interval (e.g., every 20 ms at 50 fps), the IpDFT estimates are encapsulated in a measurement

packet compatible with the PMU Std and transmitted over the Ethernet 0 communication channel. This last operation is beyond the scope of the present paper and will be investigated in the following steps of the research.

IV. Performance Characterization

The performance assessment of the SV-PMU has been carried out in the following configuration. The SV message contains a single ASDU, with nominal system rate f_0 and number of sample per cycle N_c equal to 50 Hz and 80, respectively. This corresponds to a set of three-phase current and voltage signals, sampled at F_s = 4000 Hz and with a 16-bit resolution. Given the considered calibration scenario, the following figures and tables refer to a single-phase signal, but similar results hold for the other phases.

Without loss of generality, A and φ are fixed to 1 pu and 0 rad, respectively, whereas f is varied between 45 and 55 Hz, that corresponds to the signal frequency range for the M-class compliance requirements in the most recent PMU standard (PMU Std), namely the IEC/IEEE Std 60255-118-1 [20].

Unless otherwise stated, the test duration is set equal to 3 s, and the PMU reporting rate is set equal to the sampling rate[2], apart for the ROCOF that is computed as the finite difference between frequency values spaced by 20 ms. In this way, we can get a statistically relevant set of estimates and evaluate the SV-PMU performance as function of the initial phase.

The test signals $x(t)$ refer to a purely sinusoidal model:

$$x(t) = A \cdot \cos(2\pi f t + \varphi_0) \tag{1}$$

where A, f and φ are the amplitude, frequency and initial phase of the fundamental component. As digital input to the SV-PMU, the test signals consist of a sample series $x[n]$:

$$\begin{aligned} x[n] &:= x(t = nT_s) + \varepsilon, \\ T_s = 1/F_s, &\quad n = 0, 1, \ldots (f_0 \cdot N_c - 1) \end{aligned} \tag{2}$$

where T_s is the sampling period, i.e. 250 μs, and n is the SV counter index that accounts for the time shift with respect to the PPS, i.e. the second occurrence. The additive term ε accounts for any distortion introduced by the SV conversion and should consists of quantization noise only.

A. Test waveform quality

First of all, we have verified the validity of the modeling assumptions. To this end, for each considered frequency value, we have fitted the SVs against the model (1) and evaluated the goodness of fit in terms of sum of squared residuals (SSR): in the worst case, SSR was equal to $2.943 \cdot 10^{-4}$ pu. In this context, Fig. 4 shows the residuals' distribution in the time- and frequency-domain for f = 51 Hz. In the time-domain, the residual follows the typical quantization error trend. In the frequency domain (1-Hz spectral resolution), it is noticeable how the energy is spread uniformly from DC to Nyquist rate

[2]The IEC/IEEE Std 60255-118-1 defines a maximum reporting rate of 100 fps for a nominal system rate of 50 Hz. Nevertheless, a high reporting rate is here employed just for metrological characterization purposes.

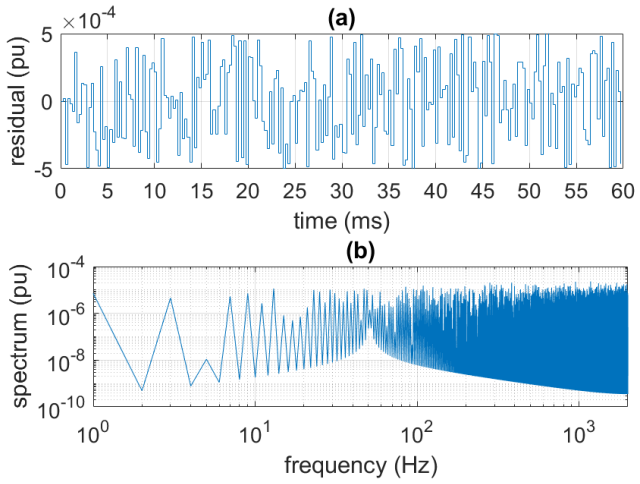

Fig. 4. Test waveform residuals when fitted against an ideal sinusoidal model in time- and frequency-domain in (a) and (b), respectively.

and the leakage effects (suggested by the Dirichlet kernel-like trend around 51 Hz) is practically negligible.

Over the same dataset, we have also evaluated the purity of the test waveforms in terms of Total Harmonic Distortion (THD) and Signal-to-Noise Ratio (SNR). In the worst case, THD and SNR are equal to -95.624 and 96.348 dB, respectively. It can be noticed how both these values are consistent with an equivalent number of 16 bits.

B. Estimation accuracy

The estimation accuracy of the SV-PMU has been characterized in the Signal Frequency Range test of the PMU Std. For this analysis, we varied the frequency between 45 to 55 Hz, with a step of 1 Hz. In order to evaluate the dependence on the frequency resolution, the window length for the MSDFT has been set equal to 3 and 5 nominal cycles, corresponding to 240 and 400 samples, respectively.

For each considered frequency, Fig. 5 shows the maximum value of TVE, FE, and RFE for both the selected window lengths. The performance indices correspond to the performance of the IpDFT estimator already published in the literature [21], as further proof of the correct implementation of the processing routine. It is well-known that such estimator is significantly affected by the leakage contributions from the negative image components. This phenomenon is particularly evident with a 3-cycle window length, as the reduced frequency resolution cause the side-lobes of the negative image component to interfere with the DFT bins considered in the interpolation.

In this sense, the IpDFT represents a preliminary attempt of synchrophasor and frequency estimator, valuable for verification testing, rather than for actual measurement campaigns. On the other hand, the future steps of the research will involve its extension in view of a minimization of the leakage contributions [22] and/or the computation of a dynamic phasor that accounts also for a time-varying parameters [23].

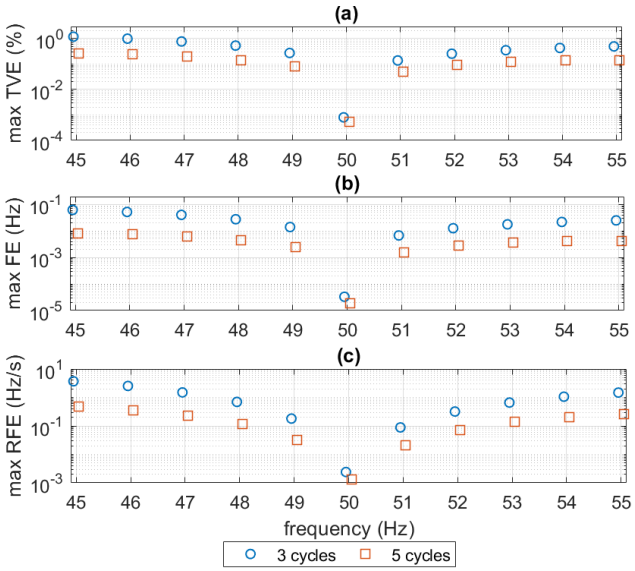

Fig. 5. Estimation accuracy in terms of maximum TVE (a), FE (b), and RFE (c) for a window length of 3 and 5 nominal cycles in blue circles and red squares, respectively.

C. Computational requirements

The monitoring of the computational requirements of both hardware and software activities allow for assessing possible room for enhancement or identifying architectural limits in the design of the instrument or of the measurement procedure. For this analysis, we have employed the LabVIEW RT Tracer Viewer function, that records the execution time of different tasks and subtasks running on the RT processor.

Fig. 6 shows the execution time on the two Ethernet boards (Ethernet 0 and Ethernet 1) to accomplish their respective tasks during the capturing and processing of a SV data stream. On the bottom, the swapper functionality highlights the time intervals where neither board is active. Based on the recorded execution time profiles, it is interesting to notice that the two boards cannot operate simultaneously. When Ethernet 0 is inactive, i.e. when no communication between the cRIO-9068 and the host computer is ongoing, the packet capturing on Ethernet 1 has a stable duration and starts regularly every 250 μs, compatibly with the publishing rate of 4000 Hz. Conversely, as soon as a communication takes place on Ethernet 0, the packet capturing is suspended and takes place as soon as Ethernet 0 ceases its activity. This might represent a bottleneck, especially if higher publisher rates are taken into account. On the other hand, it is worth noting that, even in the presence of these *interruptions*, no packet is lost and the correct rate of packet capturing is recovered very rapidly. Moreover, in its final implementation, the SV-PMU would be a purely stand-alone device, without any need of communicating with the host computer, and would use the Ethernet 0 only to transmit PMU packets (i.e., every tens of ms).

In Fig. 7, we present the execution times of all the different tasks and subtasks involved in a single iteration of the *Analyzer* cycle. In total, the overall duration is equal to 1.232 ms as

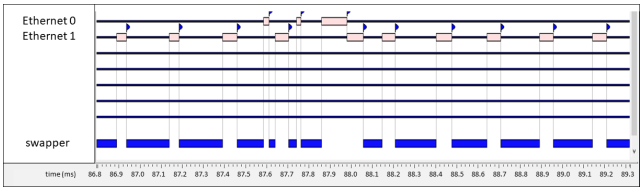

Fig. 6. Monitored activity of the two Ethernet boards as function of time during the capturing and processing of a SV stream.

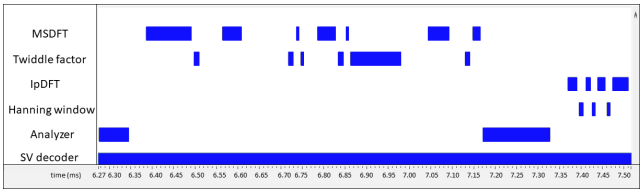

Fig. 7. Execution time diagram for the Analyzer routine.

given by the cumulative contribution of each task and subtask: 783.94 μs for the MSDFT, 170.41 μs for the Twiddle Factor, 141.92 μs for the IpDFT, and 23.28 μs for the Hanning. In this regard, two aspects can be noticed. On one side, the overall execution time is significantly lower than the typical latency requirements for PMU measurements (typically, in the order of tens ms). On the other side, the contribution from the tasks devoted to the actual estimation of synchrophasor, frequency and ROCOF is almost negligible. As a consequence, more computation resources can be devoted to the implementation of more sophisticated (and more accurate) estimation algorithms.

V. Conclusions

In this paper, a novel design for a PMU operating with digital inputs based on the SV communication protocol is presented. We described in detail the hardware and software architecture of the instrument, and we discussed the possible bottlenecks in terms of measurement procedure and computational requirements.

The performance of the proposed SV-PMU was assessed by means of a calibration system for IEC Std 61850-9-2. In this context, we evaluated the quality of the SV data streams in terms of quantization noise and harmonic distortion. The SV-PMU estimation accuracy was characterized in terms of TVE, FE and RFE in the Signal Frequency Range test of the IEC Std 60255-118-1. Finally, we quantified the execution times associated to each task and subtask of the measurement procedure.

The results confirm the potential of the proposed architecture and prove that there is still significant room for improvement from the estimation point of view.

The future steps of the research will involve the implementation of more sophisticated estimation algorithms and the characterization of the device performance when directly connected to a non-conventional instrument transformer.

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