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Abstract

Radiation-induced soft error is an ever-increasing concern in the microelectronic industry in order to provide reliable VLSI systems at advanced technology nodes. Most of the redundancy-based methodologies adopt majority voters to ensure the fault masking. This paper presents a comparative analysis of different Majority Voter designs in 7nm FinFET under radiation effects. The MUSCA SEP3 tool is used to estimate the SER of each circuit. Results show that NOR voter is less sensitive than the NAND voter. However, the SET pulse width is larger for the NOR voter than NAND voter.

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1. Introduction

Within the advancement in microelectronics, a growth in the susceptibility to variability and radiation effects of integrated circuits is observed at advanced nodes [1]-[4]. Some main contributors to this high susceptibility can be pointed as: the high complexity of manufacturing processes; the reduction of size dimension and supply voltage; and, the increase in circuit density and operating frequency [1][2].

Then, to overcome some of these problems, new device architectures and novel materials are being used. For instance, metal gate and high-k gate dielectrics, as well as multigate devices have allowed the further scaling of transistors by alleviating the Short-Channel Effects (SCE) and variability effects [1]-[8]. The FinFET is a tri-gate technology and it has shown a better response to radiation effects due to its limited sensitivity volume compared to planar devices [1]-[7]. The proper estimation of Soft Error Rates (SER) is of utmost importance for error mitigation and radiation-tolerant circuit design. However, the lack of experimental data of radiation campaigns on such advanced technologies nodes prevents the exploration of circuit design robustness to these effects [9].

In this context, this work investigates the radiation robustness of majority voter designs in 7nm FinFET technology [8]. For it, this work adopts a Monte-Carlo tool that calculates both cross section and SER based on modeling of physical and electrical mechanisms associated to a radiation event, MUSCA SEP3 [9]-[16]. For this purpose, the 3D radial distribution of generated charges and the charge collection process are calculated based on Back-End of Line (BEOL) and Front-End of Line (FEOL), obtained directly from layout design files in Graphic Data System (GDS) format.

The goal of this work is to determine the SEE sensitivity trends of majority voters depending on the use of various gates designed in 7nm FinFET (ASAP7) technology at ground level [8]. The atmospheric radiation environment (neutron, protons and muons) and the alpha constrain are investigated. The impact of the voltage scaling on the soft error (SE) occurrence is also studied with the aim to anticipate the use of such technology for embedded applications.

2. Majority Voters in 7nm FinFET (ASAP7)

2.1 Principle of majority voter

Hardware redundancy is the most commonly fault-tolerant technique used to increase the robustness of a given design or application. Triple-Modular Redundancy (TMR) technique is widely explored in a variety of strategies implementation [17][18]. The concept of TMR relies on three identical copies processing data and a majority voter (MJV) unit voting the triplicated outputs to mask single faults in one of the copies [17]. The logical function that translates the MJV circuitry in a TMR scheme is represented by Eq. (1), where A, B and C constitute the signal data provided by the triplicated modules in the TMR scheme (see Fig.1).

$$\text{MJV output} = A \times B + B \times C + C \times A \qquad (1)$$

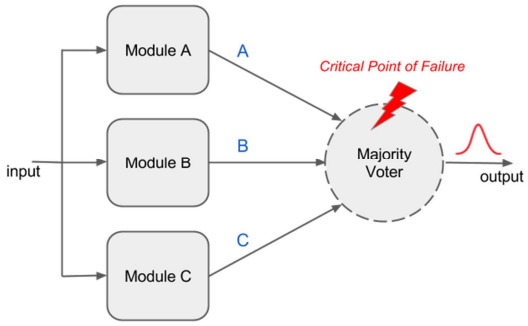


Fig. 1. TMR Scheme – The voter circuit constitutes the critical point of failure in the technique.

TMR can be implemented in hardware at gate level, for instance, where each module is triplicated and voters are added [17]. According to the granularity of the TMR, the majority voters do not need to be placed only at the outputs, but also in the designs after some combinational logic or flip-flops [18]. The majority voter is able to mask the occurrence of a single fault in any of the triplicated circuit modules. Therefore, the voter circuit constitutes the critical point of failure for the TMR scheme, i.e., a soft error in the voter circuit leads to a faulty output as can be seen in Fig. 1.

Based on Boolean function described in Eq. 1, the majority voting function can be implemented in a plurality of circuit topologies. For instance, one common approach is the use of a Standard Cells Library. Accordingly, this work analyzes two different majority voter circuits against radiation effects: the NOR-based and NAND-based majority voters.

2.2 Description of the 7nm FinFET technology

The MJV circuits were designed using the 7-nm FinFET Predictive Process Design Kit (ASAP7) developed at Arizona State University in partnership with ARM Ltd [8]. Based on current assumptions regarding the lithography and manufacturing processes, ASAP7 is a realistic and predictive PDK that allows exploring circuit designs at a not yet available technology node (7-nm FinFET). The Extreme Ultra-violet (EUV) lithography was assumed for the major layers due to its cost-effectiveness, by not requiring multiple patterning (MP), and also to provide simpler layout design rules [8][20]. Table 1 summarizes some of the layers and design rules adopted in the PDK development.

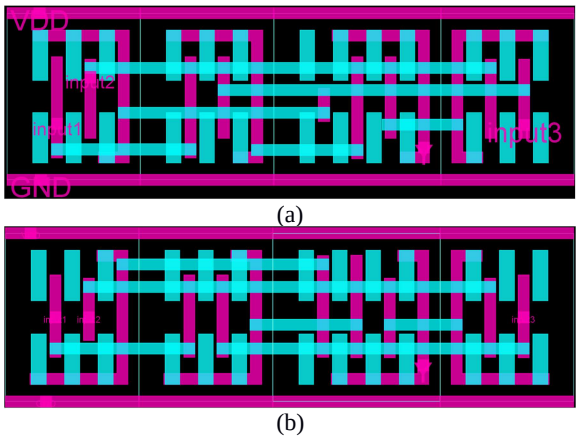
Middle-Of-Line (MOL) metal layers are introduced in this technology to provide better cell connectivity while applying multiple patterning (MP) approaches. The Local-Interconnect Gate (LIG), Local-Interconnect Source-Drain (LISD) and VIA0 compose the MOL layers for this PDK [8]. These layers are used as metal local interconnect layers connected by shape overlap without need of a cut layer. The MP techniques are named to some of the design layers as self-aligned quadruple patterning (SAQP) and self-aligned double patterning (SADP).

TABLE I
KEY LAYERS AND ITS WIDTHS AND PITCHES [8]

Layer	Lithography	Width/drawn (nm)	Pitch (nm)
Fin	SAQP	6.5/7	27
Active	EUV	54/16	108
Gate	SADP	21/20	54
SDT/LISD	EUV	25/24	54
LIG	EUV	16/16	54
VIA0-VIA3	EUV	18/18	25
M1-M3	EUV	18/18	36

2.3 Design of the Majority Voters (MJV)

The layout design of the Majority Voters was conducted based on the Standard Cell methodology assumed for a Design/Technology Co-Optimization (DTCO) approach [21]. The cell height is set to 7.5 tracks of M2 (0.27µm) and double diffusion breaks with dummy gates are used to provide better quality diffusion growth. With a 27nm fin pitch, a high-density layout design is achieved with three fins for each PFET and NFET devices [8][21]. As silicon-based channel and strain engineering are assumed for this PDK, the obtained NFET/PFET drive ratio is approximately 10:9 [8]. For this reason, the cells are designed with symmetric sizing of NFET and PFET transistors. The designs of the two majority voters, i.e., NAND-based voter and NOR-based voter, are presented in Fig. 2 (a) and Fig. 2 (b) respectively.



(a)

(b)

Fig. 2. Layout of (a) NAND and (b) NOR gate with Active implants, M1 and M2 metal layers based on design rules of the 7nm FinFET technology (ASAP7).

The active implants (for source and drain), and Metal 1 and Metal 2 layers are depicted in pink and blue respectively. The gate area of the both designs is exactly the same. The NOR-based MJV is composed of three NOR gates with 2 inputs (called NOR2) and one NOR gate with 3 inputs (called NOR3). While the NAND-based MJV is composed of three NAND gates with 2 inputs (called NAND2) and one NAND gate with 3 inputs (called NAND3).

3. SEE prediction tool

MUSCA SEP3 is a single event effects prediction tool based on a Monte-Carlo approach, and developed at ONERA since 2007 [16]. The prediction tool allow for performing a full flow of simulations from the interaction of the radiation particles with the device down to the occurrence of the soft error in the circuit (in this work the majority voters). The tool was extensively validated for different devices and technology nodes [10][11], including SOI FinFET technology [5] and bulk FinFET technology [6].

The complete principle of the modeling is reported in previous works [10][11][19]. These simulations use GEANT-4 database for a complete description of free carrier generation (nuclear interaction, ionization, etc.). The 3D radial distribution of generated charges in the silicon (taking into account all parallel fins [6]) is calculated for each incident particle considering the Back-End Of Line (BEOL) [10]. The modeling of the charge diffusion accounts for the ambipolar diffusion mechanisms and recombination processes [16]. The modeling of the charge collection accounts for the dynamic transport and the multi-charge collection mechanisms (charge sharing, pulse quenching [13] [16]), the bias voltage, the layout, the bipolar amplification, the shallow trench isolation (STI) and the fabrication process. In the case of this work, the low substrate coupling effect induced by the bulk FinFET technology is taking into account at electrical level.

The bipolar amplification model depends on two mechanisms. First, the model uses the equivalent access resistances of the FinFET transistor to determine the triggering of the bipolar transistor. Second, the model takes into account the variability of the amplification of charge collection as a function of LET [5]. These simulations allow to build a SET currents database. Next this SET current database is used as current generator on each relevant node of the studied cell at transistor level for an electrical transient simulation using SPICE (Simulation Program with Integrated Circuit Emphasis) simulator with the aim to estimate the soft error response of the majority voter cell.

4. Results of SEE sensitivity of majority voters

4.1 Identification of critical areas

One of the interests of SEE prediction tool is the ability to determine the critical areas of device/gate. In this work, the critical area of NOR-based and NAND-based voters has been obtained from a simulation of heavy ion irradiation with an average LET of 10MeV.cm^2.mg^{-1}. Fig. 3 presents the SET sensitivity mapping of the NOR-based majority voter in its most sensitive state, as reported in previous works [14][15]: the three inputs have been set at state “on”. The red area indicates the sensitive areas of the majority voter. A first interesting point is that most of the critical transistors are NFET transistors. Second, it is also interesting to note that the sensitive NFET transistors are issued from the NOR3 gate or from the adjacent NOR2 gates.

Fig. 4 presents the SET sensitivity mapping of the NAND-based majority voter in its most sensitive

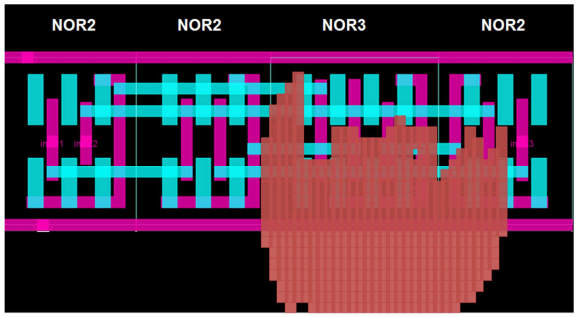


Fig. 3. SET mapping of NOR majority voter obtained by simulation for a heavy ion at normal incidence with an average LET of about 10MeV.cm^2.mg^{-1}

state: the three inputs have been set at state “off”. The red area indicates the sensitive areas of the majority voter. Different from the observations for the NOR-based MJV, for this design most of the critical transistors are the NFET transistors. Additionally, it is also interesting to note that the sensitive PFET transistors are issued from the NAND3 gate or from the adjacent NAND2 gates.

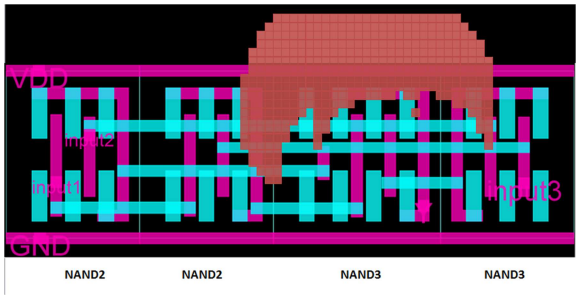


Fig. 4. SET mapping of NAND majority voter obtained by simulation for a heavy ion at normal incidence with an average LET of about 10MeV.cm^2.mg^{-1}

These results are consistent with electrical simulations and are mainly induced by the strong multi-collection allowed by the bulk technology. The bulk substrate leads the diffusion of free carrier in the gate, which induces multiple SET pulses in the nodes of the majority voter. This effect is illustrated in the Fig. 5, where the signals of internal and output nodes of the NOR-based majority voter can be observed. The majority voter is under a heavy ion at normal incidence with an average LET of about 15MeV.cm^2.mg^{-1}. The SET event is observed in the output node (yellow curve). The multi-collection allowed by the bulk technology has induced the voltage drop of the two floating nodes of the NAND3 gate in the majority voter. The criticality of the SET pulse width will be discussed in the final section of this work.

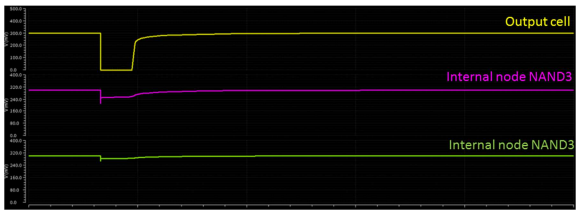


Fig. 5. SET waveform of internal and output nodes of majority voter based on NOR gate for a heavy ion at normal incidence with an average LET of about 15MeV.cm^2.mg^{-1}

4.2 Soft error sensitivity of majority voters at ground level

The goal of this section is to determine the SET sensitivity trends at ground level for the NAND and NOR-based majority voters. The atmospheric radiation environment (neutron, protons and muons) and the alpha constrain are investigated.

As mentioned, one of the constraints is the alpha particle. Alpha-emitting impurities can be found in some packaging materials, chemicals and materials used in the fabrication process of the chip. This alpha constraint can have a significant impact on the soft error rate (SER) [9][19]. The emission rate can strongly vary depending on the quantity and purification grade of these materials. The α-emitter contamination effect is considered here as the sum of the package and wafer contributions. Four alpha emission categories can be considered for the package as summarized in Table II.

TABLE II
Alpha emissivity of the package in VLSI devices

Alpha emissivity Category	Alpha emissivity (α/cm²/hr)
Standard	~10^{-2}
Low Alpha	~ 5.10^{-3}
Ultra Low Alpha	~ 5.10^{-4}
Hyper Low Alpha	~ 5.10^{-5}

Fig. 6 shows the evolution of SER induced by the atmospheric radiation environment at ground level, for the two voter designs as a function of core voltage. The error bars correspond the standard deviation. The simulations highlight the higher soft error rate of the NAND gate. The SER ratio between the NOR and NAND voter reaches 40X for the lowest core voltage, at 0.2V. At the threshold occurrence (0.5V), one SET has been considered and depicted by an arrow on the Fig. 6. Note that the two majority voters are not sensitive to soft error at

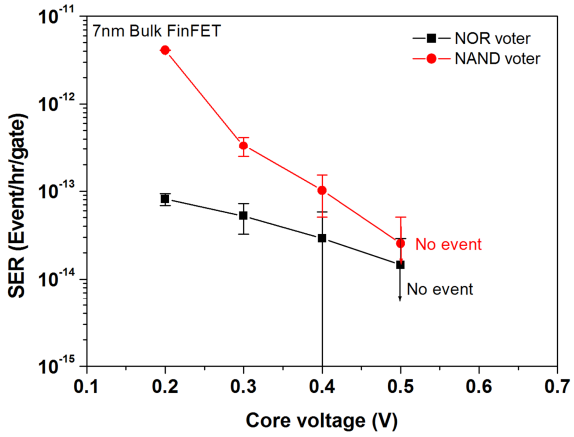


Fig. 6. SER simulated for the NOR (black squares) and NAND (red dots) voter for the atmospheric constraint as a function of core voltage

nominal voltage, 0.7V, considering operation at ground level. As future work, a stronger statistic analysis coupled with experimental irradiations with very high fluence, could be done in order to find rare events for this core voltage range.

Fig. 7 shows the SER obtained for the NAND-based voter simulated for various alpha emissivity rate of the package and for the atmospheric environment at ground level. Fig. 8 shows the SER obtained for the NOR-based voter simulated for various alpha emissivity rate of the package and for the atmospheric environment at ground level. The atmospheric environment takes into account neutron, proton, and muon energy spectra. The SER has been calculated for a range of core voltage: from 0.7V down to 0.2V.

First, it is interesting to note the strong robustness

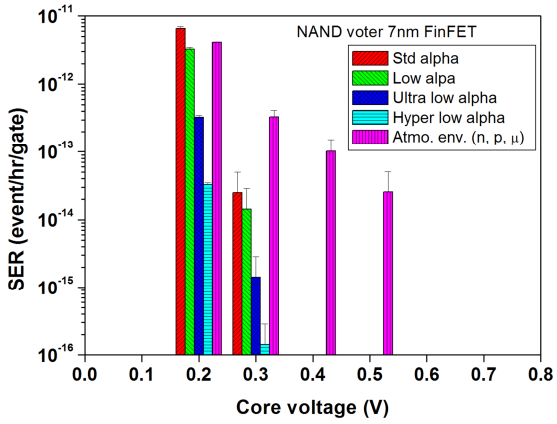


Fig. 7. SER simulated for the NAND voter for the atmospheric constraint and for various alpha emissivity rate of the package as a function of core voltage

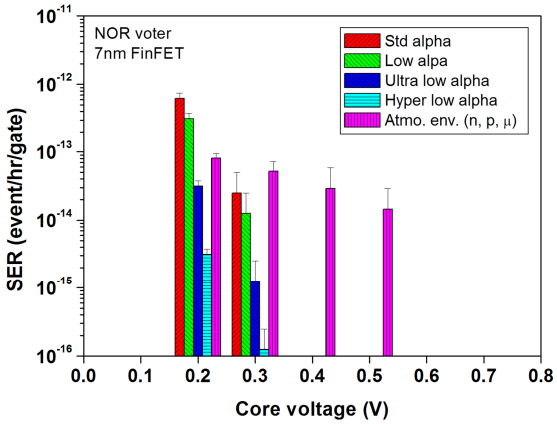


Fig. 5. SER simulated for the NOR voter for the atmospheric constraint and for various alpha emissivity rate of the package as a function of core voltage

of both majority voters. At nominal core voltage, i.e., 0.7V, no event has been observed even with alpha constraint. The error bars correspond the standard deviation. Note that one event has been considered with an error bar of 100%. Second, note that for higher core voltage than 0.3V, neutron, protons and muons particles are more critical than the alpha constraint. While at 0.2V the alpha constraint is significant in the SER for the two majority voters. Further, the NOR-based voter seems to be slightly less sensitive than the NAND-based voter as it provides lower SER. This point was not expected considering the higher sensitivity of standalone NOR gate observed in previous works [5]. However, these previous simulation results have been obtained for an asymmetric design of NFET and PFET transistors [5]. The asymmetric design performed in previous works has been done by a lower number of fins for NFET transistor of the NOR gate. It is not the case in this work. The elementary NOR and NAND gates have been designed with the same number of fins for NFET and PFET transistors. The symmetric design of majority voters induced a higher drive current. This improves the SEU robustness of the two majority voters and decrease the difference in the SER between the NOR and NAND gates.

4.3 Analysis of SET worst-case occurrences of majority voters at ground level

The final discussion of this work is focused on the worst case of soft error occurrence in the two majority voters at ground level. The point is discussed by the analysis of the worst case of SET pulse width induced directly or indirectly by alpha and atmospheric particles. Fig. 9 shows the widest SET pulse observed by simulation under atmospheric and alpha environment as a function of core voltage for the two majority voters.

The simulations show a strong increase in the SET pulse width with the decrease in the core voltage for the two majority voters. This trend is in good correlation with previous worked done on FinFET technologies [6]. Note that, the largest SET pulse are observed for the NOR voter while its SER is lower than the NAND voter. This point is confirmed for the core voltages, excepted at 0.2V.

This metric is very important because of its utility to define the most relevant timing of clock tree used with the Flip-Flops system.

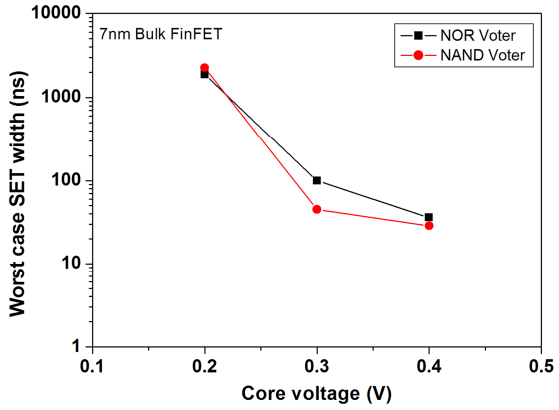


Fig. 9. Worst case of SET pulse width induced in atmospheric and alpha environment of NOR (red squares) and NAND (red dots) voter as a function of core voltage

5. Conclusions

This paper presents a comparative analysis of Majority Voters designed at 7nm FinFET devices against radiation effects. The MUSCA SEP3 tool is used to estimate the SER of each circuit depending on the core voltage and the radiation constraint, alpha, atmospheric environment. The predictive tool was extensively validated and used in previous works, exhibiting a good agreement with the TCAD mixed-mode simulation analysis [5][6][10][11]. Two designs based on NOR and NAND gates have been evaluated. A strong SEU robustness of the two majority voters is determined. The NOR voter seems to be less sensitive than the NAND voter as it provides lower SER. However, the SET pulse width is larger for the NOR voter than NAND voter. This point should be considered during the design of an embedded circuit such as PLL.

At nominal core voltage, i.e. 0.7V, no event has been observed for alpha and atmospheric environment. In the future, a stronger statistic analysis coupled with experimental irradiations with very high fluence, could be done in order to find rare events for this core voltage range.

Acknowledgments

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