

Scheme & Syllabus of
UNDERGRADUATE DEGREE COURSE
B.Tech. VII & VIII Semester

Electronics & Communication Engineering



Rajasthan Technical University, Kota
Effective from session: 2020 – 2021



RAJASTHAN TECHNICAL UNIVERSITY, KOTA

Scheme & Syllabus

IV Year- VII & VIII Semester: B. Tech. (Electronics & Communication Engineering)

Teaching & Examination Scheme B.Tech. : Electronics & Communication Engineering 4th Year - VII Semester

THEORY											
SN	Category	Course		Contact hrs/week			Marks			Cr	
		Code	Title	L	T	P	Exm Hrs	IA	ETE		Total
1	PEC	Program Elective		3	0	0	3	30	120	150	3
		7EC5-11	VLSI Design								
		7EC5-12	Mixed Signal Design								
		7EC5-13	CMOS design								
2	OE		Open Elective-I	3	0	0	3	30	120	150	3
			Sub Total	6	0	0		60	240	300	6
PRACTICAL & SESSIONAL											
3	PCC	7EC4-21	VLSI Design Lab	0	0	4	2	60	40	100	2
4		7EC4-22	Advance communication lab (MATLAB Simulation)	0	0	2	2	30	20	50	1
5		7EC4-23	Optical Communication Lab	0	0	2	2	30	20	50	1
6	PSIT	7EC7-30	Industrial Training	1	0	0		75	50	125	2.5
7		7EC7-40	Seminar	2	0	0		60	40	100	2
8	SODECA	7EC8-00	Social Outreach, Discipline & Extra Curricular Activities					0	25	25	0.5
			Sub Total	3	0	8		255	195	450	9
			TOTAL of VII SEMESTER	9	0	8		315	435	750	15

L: Lecture, **T:** Tutorial, **P:** Practical, **Cr:** Credits

ETE: End Term Exam, **IA:** Internal Assessment



RAJASTHAN TECHNICAL UNIVERSITY, KOTA

Scheme & Syllabus

IV Year- VII & VIII Semester: B. Tech. (Electronics & Communication Engineering)

Teaching & Examination Scheme B.Tech. : Electronics & Communication Engineering 4th Year - VIII Semester

THEORY											
SN	Category	Course Code	Course Title	Contact hrs/week			Marks			Cr	
				L	T	P	Exm Hrs	IA	ETE		Total
1	PEC	Program Elective		3	0	0	3	30	120	150	3
		8EC5-11	Artificial Intelligence And Expert Systems								
		8EC5-12	Digital Image and Video Processing								
		8EC5-13	Adaptive Signal Processing								
2	OE		Open Elective-II	3	0	0	3	30	120	150	3
Sub Total				6	0	0		60	240	300	6
PRACTICAL & SESSIONAL											
3	PCC	8EC4-21	Internet of Things (IOT) Lab	0	0	2	2	30	20	50	1
4		8EC4-22	Skill Development Lab	0	0	2	2	30	20	50	1
5	PSIT	8EC7-50	Project	3	0	0		210	140	350	7
6	SODECA	8EC8-00	Social Outreach, Discipline & Extra Curricular Activities						25	25	0.5
Sub Total				3	0	4		270	205	475	9.5
TOTAL of VIII SEMESTER				9	0	4		330	445	775	15.5

L: Lecture, **T:** Tutorial, **P:** Practical, **Cr:** Credits

ETE: End Term Exam, **IA:** Internal Assessment



RAJASTHAN TECHNICAL UNIVERSITY, KOTA

Scheme & Syllabus

IV Year- VII & VIII Semester: B. Tech. (Electronics & Communication Engineering)

List of Open Electives for Electronics & Communication Engineering			
Subject Code	Title	Subject Code	Title
Open Elective - I		Open Elective - II	
7AG6-60.1	Human Engineering and Safety	8AG6-60.1	Energy Management
7AG6-60.2	Environmental Engineering and Disaster Management	8AG6-60.2	Waste and By-product Utilization
7AN6-60.1	Aircraft Avionic System	8AN6-60.1	Finite Element Methods
7AN6-60.2	Non-Destructive Testing	8AN6-60.2	Factor of Human Interactions
7CH6-60.1	Optimization Techniques	8CH6-60.1	Refinery Engineering Design
7CH6-60.2	Sustainable Engineering	8CH6-60.2	Fertilizer Technology
7CR6-60.1	Introduction to Ceramic Science & Technology	8CR6-60.1	Electrical and Electronic Ceramics
7CR6-60.2	Plant, Equipment and Furnace Design	8CR6-60.2	Biomaterials
7CE6-60.1	Environmental Impact Analysis	8CE6-60.1	Composite Materials
7CE6-60.2	Disaster Management	8CE6-60.2	Fire and Safety Engineering
7CS6-60.1	Quality Management/ISO 9000	8CS6-60.1	Big Data Analytics
7CS6-60.2	Cyber Security	8CS6-60.2	IPR, Copyright and Cyber Law of India
7EE6-60.1	Electrical Machines and Drives	8EE6-60.1	Energy Audit and Demand side Management
7EE6-60.2	Power Generation Sources.	8EE6-60.2	Soft Computing
7ME6-60.1	Finite Element Analysis	8ME6-60.1	Operations Research
7ME6-60.2	Quality Management	8ME6-60.2	Simulation Modeling and Analysis
7MI6-60.1	Rock Engineering	8MI6-60.1	Experimental Stress Analysis
7MI6-60.2	Mineral Processing	8MI6-60.2	Maintenance Management
7PE6-60.1	Pipeline Engineering	8PE6-60.1	Unconventional Hydrocarbon Resources
7PE6-60.2	Water Pollution control Engineering	8PE6-60.2	Energy Management & Policy
7TT6-60.1	Technical Textiles	8TT6-60.1	Material and Human Resource Management
7TT6-60.2	Garment Manufacturing Technology	8TT6-60.2	Disaster Management



RAJASTHAN TECHNICAL UNIVERSITY, KOTA

Scheme & Syllabus

IV Year- VII & VIII Semester: B. Tech. (Electronics & Communication Engineering)

7EC5-11: VLSI Design (program elective-3)

Credit: 3
3L+0T+0P

Max. Marks: 150(IA:30, ETE:120)
End Term Exam: 3 Hours

SN	Contents	Hours
1	Introduction: Objective, scope and outcome of the course.	01
2	INTRODUCTION TO MOSFET- Basic MOS transistors, Enhancement Mode transistor action, Depletion Mode transistor action, NMOS and CMOS fabrication. Aspects of threshold voltage, threshold voltage with body effect. I_{ds} versus V_{ds} relationship, channel length modulation. Transistor Trans-conductance g_m . MOS transistor circuit Model, Model parameter (oxide and junction capacitor, channel resistance) variation with scaling and biasing. High order effects (i.e. sub threshold conduction, hot electron effect, narrow channel effect and punch through effect.	12
3	CMOS LOGIC CIRCUITS- NMOS inverter (resistive and active load), Pull up to Pull-down ratio (β_p/β_n) for a NMOS Inverter and CMOS Inverter, determination of inverter parameter (V_{IL} , V_{IH} , V_{OL} , V_{OH}) and Noise Margin. Speed and power dissipation analysis of CMOS inverter. Combinational Logic, NAND Gate, NOR gate, XOR gate, Compound Gates, 2 input CMOS Multiplexer, Memory latches and registers, Transmission Gate (TG), estimation of Gate delays, Power dissipation and Transistor sizing. Basic physical design of simple Gates and Layout issues. Layout issues for CMOS inverter, Layout for NAND, NOR and Complex Logic gates, Layout of TG, Layout optimization using Euler path. DRC rules for layout and issues of interconnects, Latch up problem.	11
4	Dynamic CMOS circuits- Clocked CMOS (C^2 MOS) logic, DOMINO logic, NORA logic, NP(ZIPPER) logic, PE (pre-charge and Evaluation) Logic. Basic Memory circuits, SRAM and DRAM.	08
5	Physical Design- Introduction to ECAD tools for front and back end design of VLSI circuits. Custom /ASIC design, Design using FPGA and VHDL. VHDL Code for simple Logic gates, flip-flops, shift registers.	08
	Total	40



RAJASTHAN TECHNICAL UNIVERSITY, KOTA

Scheme & Syllabus

IV Year- VII & VIII Semester: B. Tech. (Electronics & Communication Engineering)

Text/Reference Books:

1	Cmos Digital Integrated Circuits Analysis And Design. Sung-Mo (Steve) Kang, Yusuf Leblebici, McGraw Hill (2008)
2	N.Weste and K. Eshraghian, Principles of CMOS VLSI, 2e, Pearson Education, 2011
3	VLSI Design, P PSahu , , McGraw, 2013
4	VLSI Design, D.P. Das, Oxford, 2011
5	Chip Design for Submicron VLSI: CMOS Layout & Simulation, Uyemura, cengage learning, 2009



RAJASTHAN TECHNICAL UNIVERSITY, KOTA

Scheme & Syllabus

IV Year- VII & VIII Semester: B. Tech. (Electronics & Communication Engineering)

7EC5-12: Mixed Signal Design(program elective-3)

Credit: 3
3L+0T+0P

Max. Marks: 150(IA:30, ETE:120)
End Term Exam: 3 Hours

SN	Contents	Hours
1	Introduction: Objective, scope and outcome of the course.	01
2	Analog and discrete-time signal processing, introduction to sampling theory; Analog continuous time filters: passive and active filters; Basics of analog discrete-time filters and Z-transform.	10
3	Basic logic gates with BJT and MOSFET combination, Switched-capacitor filters- Non idealities in switched-capacitor filters; Switched-capacitor filter architectures; Switched-capacitor filter applications.	07
4	Basics of data converters; Successive approximation ADCs, Dual slope ADCs, Flash ADCs, Pipeline ADCs, Hybrid ADC structures, High-resolution ADCs, DACs.	08
5	Mixed-signal layout, Interconnects and data transmission; Voltage-mode signal aligned data transmission; Current-mode signaling and data transmission.	08
6	Introduction to frequency synthesizers and synchronization; Basics of PLL, Analog PLLs; Digital PLLs; DLLs	06
	Total	40

Text/Reference Books:

1.	R. Jacob Baker, CMOS mixed-signal circuit design, Wiley India, IEEE press, reprint 2008.
2.	Behzad Razavi, Design of analog CMOS integrated circuits, McGraw-Hill, 2003.
3.	R. Jacob Baker, CMOS circuit design, layout and simulation, Revised second edition, IEEE press, 2008.
4.	Rudy V. de Plassche, CMOS Integrated ADCs and DACs, Springer, Indian edition, 2005.
5.	Arthur B. Williams, Electronic Filter Design Handbook, McGraw-Hill, 1981.
6.	R. Schauman, Design of analog filters by, Prentice-Hall 1990 (or newer additions).
7.	M. Burns et al., An introduction to mixed-signal IC test and measurement by, Oxford university press, first Indian edition, 2008.



RAJASTHAN TECHNICAL UNIVERSITY, KOTA

Scheme & Syllabus

IV Year- VII & VIII Semester: B. Tech. (Electronics & Communication Engineering)

7EC5-13: CMOS Design (program elective-3)

Credit: 3

Max. Marks: 150(IA:30, ETE:120)

3L+0T+0P

End Term Exam: 3 Hours

SN	Contents	Hours
1	Introduction: Objective, scope and outcome of the course.	01
2	Review of MOS transistor models, Non-ideal behavior of the MOS Transistor, Transistor as a switch, Inverter characteristics	08
3	Integrated Circuit Layout: Design Rules, Parasitic, Delay: RC Delay model, linear delay model, logical path efforts, Power, interconnect and Robustness in CMOS circuit layout	07
4	Combinational Circuit Design: CMOS logic families including static, dynamic and dual rail logic. NAND Gate, NOR gate, XOR gate, Compound Gates, 2 input CMOS Multiplexer, Memory latches and registers, Transmission Gate, estimation of Gate delays, Power dissipation and Transistor sizing. Basic physical design of simple Gates and Layout issues. Layout issues for CMOS inverter, Layout for NAND, NOR and Complex Logic gates,	10
5	Dynamic CMOS circuits- Clocked CMOS (C ² MOS) logic, DOMINO logic, NORA logic, NP(ZIPPER) logic, PE (pre-charge and Evaluation) Logic. Basic Memory circuits, SRAM and DRAM.	08
6	Physical Design- Introduction to ECAD tools for first and back end design of VLSI circuits. Custom /ASIC design, Design using FPGA and VHDL. VHDL Code for simple Logic gates, flip-flops, shift registers.	06
	Total	40

Text/Reference Books:

1.	N.H.E. Weste and D.M. Harris, CMOS VLSI design: A Circuits and Systems Perspective, 4th Edition, Pearson Education India, 2011.
2.	Sung-Mo-Kang and Yusuf Leblebici, CMOS Digital Integrated Circuits Analysis & Design, McGraw Hill
3.	C.Mead and L. Conway, Introduction to VLSI Systems, Addison Wesley, 1979.
4.	J. Rabaey, Digital Integrated Circuits: A Design Perspective, Prentice Hall India, 1997.
5.	P. Douglas, VHDL: programming by example, McGraw Hill, 2013.
6.	L. Glaser and D. Dobberpuhl, The Design and Analysis of VLSI Circuits, Addison Wesley, 1985.



RAJASTHAN TECHNICAL UNIVERSITY, KOTA

Scheme & Syllabus

IV Year- VII & VIII Semester: B. Tech. (Electronics & Communication Engineering)

7EC4-21: VLSI Design Lab

Credit:

Max. Marks: 100(IA:60, ETE:40)

OL+OT+4P

SN	Contents
1	Introduction: Objective, scope and outcome of the course.
PART-A	Step1 Write the VHDL/Verilog code using VHDL software for following experiment and simulate them. Step 2. Burn the Written code in Xilling Board and test the output with real input signal
1	Design and simulate all the logic gates with 2 inputs using VHDL/Verilog.
2	Design and simulate 2-to-4 decoder,3-to-8 encoder and 8X1 multiplexer using VHDL/Verilog.
3	Design and simulate half adder and full adder using VHDL (data flow method)/Verilog.
4	Design and simulate D, T and J-K flip flop using VHDL/Verilog.
5	Design a 4bit binary Asynchronous and synchronous counter. Obtain its number of gates, area, and speed and power dissipation.
6	Design a 4- bit Serial in-serial out shift register. Obtain its number of gates, area, and speed and power dissipation.
PART-B	Step-1 Design and simulate following experiment using ECAD software Viz. Mentor graphics, Orcade Pspice, Cadence etc. Step-2 Draw the layout (without any DRC error)of the schematic obtain in step 1 and obtain post layout simulation using appropriate ECAD software.
1	Design and simulate all the logic gates (NOT, NAND and NOR) with 2 inputs in CMOS Technology.
2	Design and simulate $Y = AB(C+D)$, $Y = A+B(C+D)$ and 4X1 multiplexer using CMOS Technology.
3	Design and simulate half adder and full adder using CMOS Technology.
4	Design and simulate SR flip flop using CMOS Technology.
5	Design and Simulate any DRAM cell.



RAJASTHAN TECHNICAL UNIVERSITY, KOTA

Scheme & Syllabus

IV Year- VII & VIII Semester: B. Tech. (Electronics & Communication Engineering)

7EC4-22: Advance Communication Lab (MATLAB Simulation)

Credit: 1

Max. Marks: 50 (IA:30, ETE:20)

0L+0T+2P

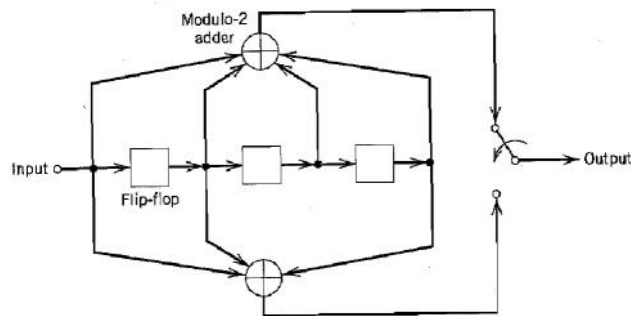
SN	Contents
1	Introduction: Objective, scope and outcome of the course.
Part-A	Analog-to-digital conversion <ol style="list-style-type: none">1. Generate a sinusoidal signal. Sample and reconstruct a signal through interpolation. Vary the sampling rate below and above the Nyquist rate and hence verify the Sampling theorem.2. Generate a sequence of length 500 of zero-mean, unit variance Gaussian random variables. Using a uniform PCM scheme, quantize this sequence to 16, 64 and 128 levels.<ol style="list-style-type: none">(a). Find and compare the resulting signal-to-quantization noise ratios.(b). Find the first ten values of the sequence, the corresponding quantized values and the corresponding code words for each case.(c). Plot the quantization error and the quantized value as a function of the input value for each case. Digital modulation techniques <ol style="list-style-type: none">3. Simulate the transmitter and receiver for QPSK. Plot the signal and signal constellation diagram. Plot the average probability of symbol error as a function of SNR E_b/N_o, where E_b is the transmitted energy per bit and $N_o/2$ is the double sided power spectral density of additive white Gaussian noise (AWGN) with zero mean.4. Simulate the transmitter and receiver for 16-QAM. Plot the signal and signal constellation diagram. Plot the average probability of symbol error as a function of SNR E_b/N_o, where E_b is the transmitted energy per bit and $N_o/2$ is the double sided power spectral density of additive white Gaussian noise (AWGN) with zero mean.
PART-B Attempt any four experiment	<ol style="list-style-type: none">1. Find all the code words of the (15,11) Hamming code and verify that its minimum distance is equal to 3.2. Generate an equiprobable random binary information sequence of length 15. Determine the output of the convolutional encoder shown below for this sequence.



RAJASTHAN TECHNICAL UNIVERSITY, KOTA

Scheme & Syllabus

IV Year- VII & VIII Semester: B. Tech. (Electronics & Communication Engineering)



3. Generate the $L=31$ Gold sequences. Consider a time-synchronous CDMA system (direct sequence spread spectrum) having four users, each employing a distinct Gold sequence of length $L=31$ and the binary (± 1) modulation of their representative Gold sequences. The receiver for each user correlates the composite CDMA received signal, which is corrupted by AWGN (added on a chip-by-chip basis) with each user's respective sequence. Using 10000 information bits, estimate and plot the probability of error for each user as a function of SNR.
4. Consider a MIMO (multiple-input, multiple-output) system with $N_T = 2$ transmit antennas and $N_R = 2$ receive antennas. Generate the elements of the channel matrix \mathbf{H} for a Rayleigh fading (frequency nonselective) AWGN channel and the corresponding inputs to the detectors for the two receive antennas.
5. Perform feature extraction from a given Image and use Principal Components as image descriptors.
6. By using an image dataset, train a Neural Network to recognize a given Image. Apply this in context to face/object recognition and calculate recognition accuracy of the training set.
7. Develop a Fuzzy Inference System (FIS) by using a set of fuzzy rule base between some key image parameters and calculate output after defuzzification.
8. Design a Fuzzy PID controller using Matlab for a Dc Motor.
9. Classify ECG signals using Neural networks.



RAJASTHAN TECHNICAL UNIVERSITY, KOTA

Scheme & Syllabus

IV Year- VII & VIII Semester: B. Tech. (Electronics & Communication Engineering)

7EC4-23: Optical Communication Lab

Credit: 1

Max. Marks: 50 (IA:30, ETE:20)

OL+OT+2P

SN	Contents
1	Introduction: Objective, scope and outcome of the course.
	Hardware based experiment;
1	To set up Fiber Optic Analog and fiber Optic Digital link.
2	Measurement of Propagation loss and numerical aperture.
3	Measurement of optical power bending loss in a plastic optical fiber.
4	Study and measure characteristics of fiber optic LED's, LDR and Laser diode.
5	OTDR Measurement of Fiber Length, Attenuation and Dispersion Loss.
	Software based experiment;
6	Design and simulate of single and multimode transmission in optical fiber system.
7	Show and simulate the optical system performance analysis using Eye diagram and measure the value of Q-factor & BER of optical signals.
8	Study and simulate the linear and parabolic waveguide structure use in optical fiber communication.
9	Design and simulate the Dispersion compensators for fiber optic communication.
10	Design and calculate the power budget for optical communication link.
11	Design and simulate the DWDM and WDM techniques use in optical communication.
12	Design and simulate the Fiber Bragg grating and find its transmission characteristics and optical band-gap.



RAJASTHAN TECHNICAL UNIVERSITY, KOTA

Scheme & Syllabus

IV Year- VII & VIII Semester: B. Tech. (Electronics & Communication Engineering)

SEC5-11: ARTIFICIAL INTELLIGENCE AND EXPERT SYSTEMS (program elective-4)

Credit: 3

Max. Marks: 150(IA:30, ETE:120)

3L+0T+0P

End Term Exam: 3 Hours

SN	Contents	Hours
1	Introduction: Objective, scope and outcome of the course.	01
2	Introduction to Artificial Intelligence: Intelligent Agents, State Space Search, Uninformed Search, Informed Search, Two Players Games, Constraint Satisfaction Problems.	08
3	Knowledge Representation: Knowledge Representation And Logic, Interface in Propositional Logic, First Order Logic, Reasoning Using First Order Logic, Resolution in FOPL.	07
4	KNOWLEDGE ORGANIZATION: Rule based System, Semantic Net, Reasoning in Semantic Net Frames, Planning	08
5	KNOWLEDGE SYSTEMS: Rule Based Expert System, Reasoning with Uncertainty, Fuzzy Reasoning.	08
6	KNOWLEDGE ACQUISITION: Introduction to Learning, Rule Induction and Decision Trees, Learning Using neural Networks, Probabilistic Learning Natural Language Processing.	08
	Total	40

Text/Reference Books:

1.	Elaine Rich and Kevin Knight, Artificial Intelligence 3/e, TMH (1991)
2.	PADHY: ARTIFICIAL INTELLIGENCE & INTELLIGENT SYSTEMS, Oxford (2005)
3.	James A Anderson, An introduction to Neural Networks. Bradford Books 1995
4.	Dan. W Patterson, Artificial Intelligence and Expert Systems, PHI 1990
5.	Kumar Satish, "Neural Networks" Tata Mc Graw Hill 2004
6.	S. Rajsekarand G.A. Vijayalakshmi Pai, "Neural Networks, Fuzzy Logic and Genetic Algorithm: Synthesis and Applications" Prentice Hall of India. 2006
7.	SimanHaykin, "Neural Netowrks" Prentice Hall of India 1990
8.	Artificial Intelligence, Kaushik, cengage learning 1997



RAJASTHAN TECHNICAL UNIVERSITY, KOTA

Scheme & Syllabus

IV Year- VII & VIII Semester: B. Tech. (Electronics & Communication Engineering)

SEC5-12: Digital Image and Video Processing (program elective-4)

Credit: 3

Max. Marks: 150(IA:30, ETE:120)

3L+0T+0P

End Term Exam: 3 Hours

SN	Contents	Hours
1	Introduction: Objective, scope and outcome of the course.	01
2	Digital Image Fundamentals-Elements of visual perception, image sensing and acquisition, image sampling and quantization, basic relationships between pixels neighborhood, adjacency, connectivity, distance measures.	04
3	Image Enhancements and Filtering-Gray level transformations, histogram equalization and specifications, pixel-domain smoothing filters – linear and order-statistics, pixel-domain sharpening filters – first and second derivative, two-dimensional DFT and its inverse, frequency domain filters – low-pass and high-pass.	03
4	Color Image Processing-Color models–RGB, YUV, HSI; Color transformations-formulation, color complements, color slicing, tone and color corrections; Color image smoothing and sharpening; Color Segmentation.	04
5	Image Segmentation- Detection of discontinuities, edge linking and boundary detection, Thresholding – global and adaptive, region-based segmentation.	04
6	Wavelets and Multi-resolution image processing- Uncertainty principles of Fourier Transform, Time-frequency localization, continuous wavelet transforms, wavelet bases and multi-resolution analysis, wavelets and Sub-band filter banks, wavelet packets.	06
7	Image Compression-Redundancy–inter-pixel and psycho-visual; Lossless compression – predictive, entropy; Lossy compression–predictive and transform coding; Discrete Cosine Transform; Still image compression standards – JPEG and JPEG-2000.	06
8	Fundamentals of Video Coding- Inter-frame redundancy, motion estimation techniques – full search, fast search strategies, forward and backward motion prediction, frame classification – I, P and B; Video sequence hierarchy – Group of pictures, frames, slices, macro-blocks and blocks; Elements of a video encoder and decoder; Video coding standards – MPEG and H.26X.	06
9	Video Segmentation- Temporal segmentation–shot boundary detection, hard-cuts and soft-cuts; spatial segmentation – motion-based; Video object detection and tracking.	06
	Total	40



RAJASTHAN TECHNICAL UNIVERSITY, KOTA

Scheme & Syllabus

IV Year- VII & VIII Semester: B. Tech. (Electronics & Communication Engineering)

Text/Reference Books:

1.	R.C. Gonzalez and R.E. Woods, Digital Image Processing, Second Edition, Pearson Education 3rd edition 2008
2.	R.C. Gonzalez, R.E. Woods and S.L. Eddins, Digital Image Processing using Matlab, McGraw Hill, 2 nd Edition
3.	Anil Kumar Jain, Fundamentals of Digital Image Processing, Prentice Hall of India, 2 nd edition 2004
4.	Murat Tekalp, Digital Video Processing" Prentice Hall, 2nd edition 2015



RAJASTHAN TECHNICAL UNIVERSITY, KOTA

Scheme & Syllabus

IV Year- VII & VIII Semester: B. Tech. (Electronics & Communication Engineering)

SEC5-13: Adaptive Signal Processing (program elective-4)

Credit: 3

Max. Marks: 150(IA:30, ETE:120)

3L+0T+0P

End Term Exam: 3 Hours

SN	Contents	Hours
1	Introduction: Objective, scope and outcome of the course.	01
2	General concept of adaptive filtering and estimation, applications and motivation, Review of probability, random variables and stationary random processes, Correlation structures, properties of correlation matrices.	08
3	Optimal FIR (Wiener) filter, Method of steepest descent, extension to complex valued The LMS algorithm (real, complex), convergence analysis, weight error correlation matrix, excess mean square error and mis-adjustment Variants of the LMS algorithm: the sign LMS family, normalized LMS algorithm, block LMS and FFT based realization, frequency domain adaptive filters, Sub-band adaptive filtering.	07
4	Signal space concepts - introduction to finite dimensional vector space theory, subspace, basis, dimension, linear operators, rank and nullity, inner product space, orthogonality, Gram-Schmidt orthogonalization, concepts of orthogonal projection, orthogonal decomposition of vector spaces.	08
5	Vector space of random variables, correlation as inner product, forward and backward projections, Stochastic lattice filters, recursive updating of forward and backward prediction errors, relationship with AR modeling, joint process estimator, gradient adaptive lattice.	08
6	Introduction to recursive least squares (RLS), vector space formulation of RLS estimation, pseudo-inverse of a matrix, time updating of inner products, development of RLS lattice filters, RLS transversal adaptive filters. Advanced topics: affine projection and subspace based adaptive filters, partial update algorithms, QR decomposition and systolic array.	08
	Total	40

Text/Reference Books:

1. S. Haykin, Adaptive filter theory, Prentice Hall, 1986.
2. C.Widrow and S.D. Stearns, Adaptive signal processing, Prentice Hall, 1984.



RAJASTHAN TECHNICAL UNIVERSITY, KOTA

Scheme & Syllabus

IV Year- VII & VIII Semester: B. Tech. (Electronics & Communication Engineering)

SEC4-21: IOT Lab

Credit: 1

Max. Marks: 50 (IA:30, ETE:20)

OL+OT+2P

LIST OF PRACTICALS	
1.	Study the fundamental of IOT softwares and components.
2.	Familiarization with Arduino/Raspberry Pi and perform necessary software installation.
3.	To interface LED/Buzzer with Arduino/Raspberry Pi and write a program to turn ON LED for 1 sec after every 2 seconds.
4.	To interface Push button/Digital sensor (IR/LDR) with Arduino/Raspberry Pi and write a program to turn ON LED when push button is pressed or at sensor detection.
5.	To interface DHT11 sensor with Arduino/Raspberry Pi and write a program to print temperature and humidity readings.
6.	To interface motor using relay with Arduino/Raspberry Pi and write a program to turn ON motor when push button is pressed.
7.	To interface OLED with Arduino/Raspberry Pi and write a program to print temperature and humidity readings on it.
8.	To interface Bluetooth with Arduino/Raspberry Pi and write a program to send sensor data to smartphone using Bluetooth.
9.	To interface Bluetooth with Arduino/Raspberry Pi and write a program to turn LED ON/OFF when '1'/'0' is received from smartphone using Bluetooth.
10.	Write a program on Arduino/Raspberry Pi to upload temperature and humidity data to thingspeak cloud.
11.	Write a program on Arduino/Raspberry Pi to retrieve temperature and humidity data from thingspeak cloud.
12.	To install MySQL database on Raspberry Pi and perform basic SQL queries.
13.	Write a program to create UDP server on Arduino/Raspberry Pi and respond with humidity data to UDP client when requested.
14.	Write a program to create TCP server on Arduino/Raspberry Pi and respond with humidity data to TCP client when requested.

LIST OF SUGGESTED BOOKS:

1.	Vijay Madiseti, Arshdeep Bahga, Internet of Things, "A Hands on Approach", University Press.
2.	Dr. SRN Reddy, Rachit Thukral and Manasi Mishra, "Introduction to Internet of Things: A practical Approach", ETI Labs.
3.	Pethuru Raj and Anupama C. Raman, "The Internet of Things: Enabling Technologies, Platforms, and Use Cases", CRC Press
4.	Jeeva Jose, "Internet of Things", Khanna Publishing House, Delhi
5.	Adrian McEwen, "Designing the Internet of Things", Wiley
6.	Raj Kamal, "Internet of Things: Architecture and Design", McGraw Hill



RAJASTHAN TECHNICAL UNIVERSITY, KOTA

Scheme & Syllabus

IV Year- VII & VIII Semester: B. Tech. (Electronics & Communication Engineering)

8EC4- 22 Skill Development Lab

Credit: 1

Max. Marks : 50 (IA:30,ETE:20)

0L+0T+2P

Part A: Training	
SN	Contents
1	Introduction: Objective, scope and outcome of the lab.
	Every student has to learn any two software from the following list, with consultation of their lab in charge. Students may get online certification or is advised to learn these from available freeware. Students may register online training courses from institutes of repute i.e. IITs/NITs/AICTE/MHRD, etc. Industrial experts /professional may be deputed to train the students in department.
1	Network simulator (NS ₂)
2	Lab view
3	Software for Robotics/Artificial intelligence (AI) /machine learning
4	Java
5	Python

PART B: Implementation	
SN	Contents
1	Student has to complete any one assignment with detailed project report based on the software/tool learn in part A.
2	Student can select any Social engineering project: Any problem of the society can be taken which can be solved with the help of electronics engineering software and gadgets.
3	Student can select Startup for innovation/entrepreneurship.
4	Engineering solution of any Industrial problem. Sufficient number of such problem may be identified by the department from nearby industry and may be given to the student for innovative solutions under guidance of faculty.
	This lab may be evaluated by an external examiner from industry along with internal faculty.