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Effect of Relative Humidity and Temperature on the Stability of DNTT Transistors: A Density of States Investigation

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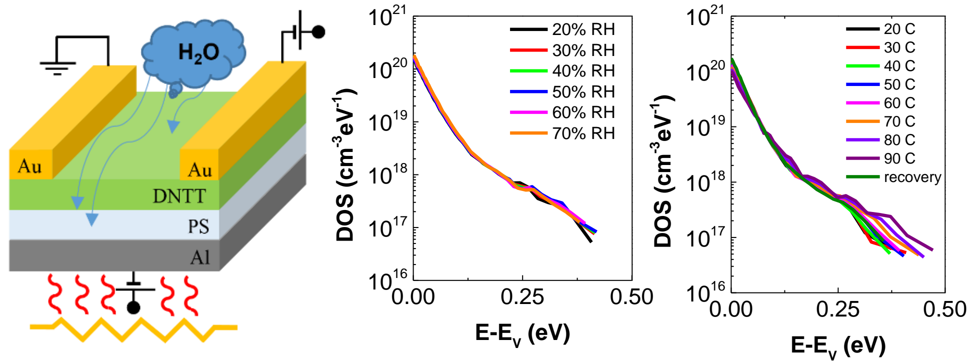
Abstract

Exposure to moisture and elevated temperatures usually results in significant degradation of organic thin film transistor (OTFT) performance. Typical observations include reduced mobility, unstable threshold voltage and the appearance of hysteresis in electrical characteristics. In this contribution we investigate the effects of environmental conditions on OTFTs based on DNTT, a high-mobility, small-molecule, organic semiconductor, with polystyrene (PS) as the gate insulator. Device characteristics were measured after consecutive 30-minute exposures to a relative humidity (RH) that was gradually increased from 20% to 80% with temperature fixed at 20ºC and for temperatures increasing from 20ºC to 90ºC with RH held at 10%. Despite significant negative shifts in turn-on and threshold voltages, only slight changes in the hole mobility were observed at the highest RH and temperature. The DNTT density of states (DoS) extracted from transfer characteristics in the linear regime using the Grünewald approach showed little change with environmental conditions. In all cases, the DoS decreased from ~1 x 10^{20} down to ~1 x 10^{17} cm^{-3} eV^{-1} in the 0.45 eV energy range above the hole mobility edge. Some evidence was obtained for a weak trap feature between ~0.25 and 0.35 eV above the mobility edge. These results confirm the high stability of DNTT as a semiconducting material and that OTFT instability observed here is associated almost entirely with a flatband voltage shift caused by hole trapping in the polystyrene gate dielectric or at the polystyrene/DNTT interface.

Key Words: OTFT, DNTT, Density of States, Environmental Effects

Graphical Abstract:



Highlights:

- Effect of relative humidity and temperature on DNTT transistors.
- Grünewald approach used to determine DNTT Density of States (DoS).
- DoS insensitive to relative humidity.
- Slight increase in DoS ~0.3 eV above mobility edge with increasing temperature.
- Instability in V_{ON} and V_T associated with hole trapping in the gate insulator.

1. Introduction

Recent reports have demonstrated that organic thin film transistors (TFTs) based on the fused heteroarene small molecule dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNTT) meet performance criteria required for application in electronic circuits [1-7]. Carrier mobility is comparable to amorphous silicon, typically μ ~ 1 cm^2/Vs, and higher than that of pentacene films, turn-on voltage is close to zero and on-off ratio exceeds 10^6. Importantly, DNTT is more resistant to oxidation by atmospheric oxygen than pentacene due to its higher ionization potential [1,2]. Taking these factors together, DNTT-based TFTs have the potential to make significant impact on the future development of large-area organic electronic circuits and considerable research effort has already been devoted to the development of functioning circuits [3,8,9] and improving OTFT performance by device engineering [9].

For practical applications, both material and operational stability are required. Not surprisingly, therefore, the effects of environmental factors on the electrical stability of organic TFTs have been extensively studied. Oxygen was recognized to be a reversible dopant of polythiophenes as long ago as 1991 [10]. Later, it was suggested that ozone played a role in shifting the onset voltage in polythiophene [11]. Previous reports [12,13] had highlighted the degrading effects of atmospheric moisture on a number of different organic semiconductors with high moisture levels resulting in significant deterioration in transistor performance [14]. Most recently, Risteska et al [15] studied the effects of oxygen and moisture on the bias stress effect in pentacene TFTs. They found that exposure to oxygen during bias stress gave rise to acceptor-like states while exposure to moisture gave rise to both acceptor- and donor-like states.

Absorbed moisture can induce charge traps either in the semiconductor or at the semiconductor/dielectric interface, causing deleterious changes in charge transport and/or threshold voltage. The field-effect mobility of several molecular organic semiconductors has been shown to decrease with increasing humidity [13]. However, this is not the case for DNTT-based TFTs. A recent study showed that moisture led to negative shifts of threshold and turn-on voltages, and an increase in off-current [16]. The measured mobility appeared to be unaffected. The observed changes were ascribed to charged states either at the insulator-semiconductor interface or in the semiconductor itself. In either case, measurement of the semiconductor density of states (DoS) should provide evidence for the presence of any new, moisture-related states.

Measuring the DoS in organic semiconductors has been important for understanding the nature of carrier transport phenomena in these materials and several methods have been suggested

for extracting the DoS from TFT transfer characteristics. In a comparative study [17], Kalb and Batlogg analysed and discussed the advantages and drawbacks of the various methods. Some require measurements to be made over a range of temperatures but also require knowledge of the temperature dependence of the band mobility for accurate results. Other approaches assume a fixed width for the accumulation channel, which can lead to significant errors. A simple approach is one introduced by Grünewald et al [18] in which the form of the DoS relative to the Fermi level is extracted from a single transfer characteristic measured in the linear regime of operation. No assumption is made about the form of the DoS, although Boltzmann rather than Fermi-Dirac statistics are used to describe the dependence of transistor current on the gate induced potential within the semiconductor. Errors associated with this assumption will be negligible until the Fermi level approaches the mobility/band edge. The method, therefore, provides a useful tool for investigating trends caused by external agencies including process variables. It has been adopted for both inorganic [19,20] and organic [21-24] semiconductors. It is based on relating the gate-induced incremental increases in device current to the band-bending resulting from the accumulation of charge carriers at the semiconductor/insulator interface. Importantly, it does not rely on iterative fits of the transfer curve with a gradually optimized, pre-determined form for the DoS. Such an approach can be time-consuming and can lead to ambiguous results owing to the insensitivity of the transfer plot to any fine detail in the DoS [18].

While many studies involving the DoS in pentacene [22,23,25-27] and other small molecules have been reported [24], to date little attention has been given to the DoS in DNTT. In one report [25], the computer model developed by Oberhoff et al [26] was applied to transfer characteristics obtained from DNTT single crystal devices. More recently, Yogev et al [28] derived the DoS from changes in contact potential difference between the tip of a scanning Kelvin probe microscope (SKPM) and the semiconductor surface on changing the gate voltage in a thin film DNTT transistor. In the present contribution, we extend measurements to evaporated DNTT thin film transistors exposed to a range of relative humidities (20% $\leq$ RH $\leq$ 80%) and temperatures (10°C $\leq$ T $\leq$ 90°C) and use the Grünewald et al [18] approach to extract the DoS under the various conditions.

2. Experimental

As previously reported [7] DNTT was synthesised following a published route [29] from 2-naphthaldehyde with an overall yield of 35%. The iodine-catalysed ring closure was followed by two recrystallisations from o-dichlorobenzene, yielding yellow microcrystals of high purity DNTT.

Full details of the purification steps are given in section S.1 of the Supplementary Information. Polystyrene (PS), M_W = 350,000, for the gate insulator was purchased from Sigma Aldrich and used without further purification.

Bottom-gate top-contact TFTs were fabricated using our previously reported 90-device arrays [6] following procedures reported in [7]. Briefly, a ~1.0 μm thick film of polystyrene was spin-coated from 8 wt% toluene solution onto aluminium gate electrodes previously evaporated through a shadow mask onto a polyethylene naphthalate (PEN) substrate. After heating for 10 mins at 100°C to remove residual solvent, the substrate was moved into an evaporator for deposition of a DNTT film ~70 nm thick with the substrate held at room temperature. Topographical AFM images of our DNTT films on polystyrene were indistinguishable from those presented in an earlier report [7] and show grain sizes in the range 50 – 500 nm. Without breaking the vacuum, gold source/drain electrodes were evaporated through a shadow mask to define the channel dimensions. In the measurements reported here, transistors had a channel width W = 2 mm with channel length, L, either 150 μm or 200 μm.

Test devices were placed in an artificial climate chamber (CLIMACELL) set to a RH in the range 10% to 80% and temperatures between 20°C and 90°C. Prior to each measurement, the test device was held at the set conditions for 30 minutes to come into equilibrium with the test environment. Transistor characteristics were obtained using a Keithley source/measure unit (model 2636B).

3. Results and Discussion

3.1 Effect of Relative Humidity

To investigate the effect of RH the test device was held at 20°C while RH was incremented in 10% steps from 20% to 80%. Figure 1(a) shows the output characteristics obtained for both the forward (0 to -60 V) and reverse sweeps of drain voltage, V_{DS}. The linear increase in device current, I_D, at low V_{DS} follows the predicted behaviour for the linear regime, $V_{DS} < (V_{GS} - V_T)$, that is

$$I_D = \frac{W}{L}\mu C_i (V_{GS} - V_T) V_{DS} \tag{1}$$

where, μ is the carrier mobility, C_i the capacitance per unit area of the gate dielectric and V_{GS} the gate voltage. At higher V_{DS} clear saturation occurs and on reducing V_{DS} no hysteresis was observed between forward and reverse sweeps at any RH. The corresponding transfer characteristics are given in Figure 1(b). Again little hysteresis was observed between forward and reverse sweeps of the gate voltage. The only other notable feature in the transfer plots is the rapid increase in off-

current as RH increases above 70% due to parasitic currents through water films on the device surface and/or increased gate leakage current. At lower RH the off-currents were determined by the displacement current of a few pA charging the gate capacitance.

The transfer data obtained during the forward sweep (+20 V to -60 V) are replotted using linear scales in the inset of Figure 1(b). Based on equation (1) and a measured C_i = 2.37 nF/cm^2, the slope of the linear section of such plots yields the carrier mobility while extrapolation to the V_{GS} axis yields V_T. These are given in Table 1 for the different values of RH, together with V_{ON}, subthreshold slope, SS, and on-off ratio extracted from the main plot in Figure 1(b). The reduction of ~16% in I_D seen in Figure 1(a) as RH increased is now seen to have arisen almost entirely from the shifts in V_{ON} and V_T as reported in [16]. The contribution from the reduction in mobility is only ~1%. The on-off ratio, defined here as the ratio of the current flowing at V_{GS} = -60 V to that at V_{ON}, is significantly affected by the rapidly increasing off-currrent at the highest humidity. This same high off-current also results in an overestimate of the negative shift in V_{ON}. The relatively high values of SS (3.7 to 4.1 V/decade) are mainly the consequence of the relatively thick and hence low C_i gate dielectric used in our OTFTs. Simple scaling to the much thinner C_{14}-phosphonic acid treated AlO_x (C_i = 800 nF/cm^2) used by Zschieschang et al [30] in their DNTT transistors would result in an SS ~12 mV/decade compared with 90 mV/decade reported by these authors.

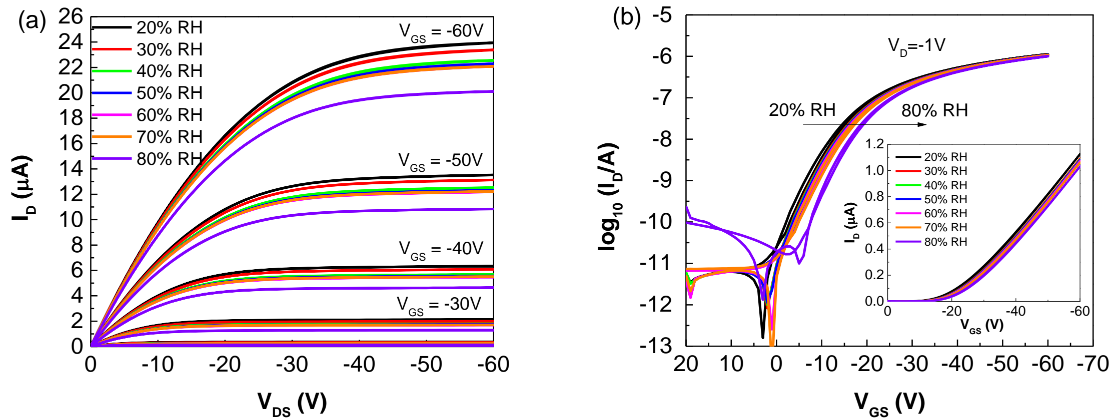


Figure 1. Effect of increasing relative humidity at 20°C on (a) output and (b) transfer characteristics of a DNTT TFT (W = 2 mm, L = 150 μm) with polystyrene gate insulator. The transfer plots were obtained in the linear regime with drain voltage, V_{DS} = -1V. The inset in (b) shows the data for the forward sweep (+20V to -60V) plotted on linear axes.

Table 1 Device parameters extracted from the transfer characteristics measured with V_D = -1V, T = 20ºC and RH increasing from 20% to 80%. The values in brackets are for decreasing RH.

RH	20%	30%	40%	50%	60%	70%	80%
***μ* (cm²/V.s)**	0.95 (0.94)	0.95 (0.93)	0.95 (0.93)	0.95 (0.93)	0.94 (0.93)	0. 94 (0.93)	0. 94 (0.94)
V_{ON} (V)	3 (0)	2 (0)	2 (-1)	2 (-1)	1 (-2)	1 (-5)	-6 (-6)
V_T (V)	-22 (-24)	-23 (-24)	-23 (-25)	-24 (-25)	-24 (-25)	-24 (-25)	-26 (-25)
I_{ON}/I_{OFF}	1.8x10⁵ (1.6x10⁵)	1.7x10⁵ (1.6x10⁵)	1.7x10⁵ (1.6x10⁵)	1.7x10⁵ (1.6x10⁵)	1.7x10⁵ (1.7x10⁵)	1.6x10⁵ (5.8x10⁴)	1.5 x10⁴ (1.6x10⁴)
SS (V/decade)	3.67 (3.56)	3.71 (3.65)	3.75 (3.71)	3.83 (3.72)	3.85 (3.84)	3.92 (3.91)	4.09 (3.90)

When RH was reduced back to 20% in stages over a period of 3 hours, device characteristics remained well-behaved but only partial recovery occurred. For decreasing RH, the output and transfer characteristics corresponding to Figure 1 are given in Figure S1 in the Supplementary Information with extracted parameter values appearing in brackets in Table 1. While mobility remained virtually unchanged throughout the RH cycle, long-term shifts occurred in V_{ON} and V_T. Transfer plots measured after returning to the initial conditions show a translation of around -2.5 V along the V_{GS} axis while maintaining the same profile. This is readily explained by a shift, ΔV_{FB}, in the flatband voltage arising from hole trapping in the PS film or at the PS/DNTT interface. For an effective interface trapped charge density Q_{it}, which includes also the influence of charges in the insulator, $\Delta V_{FB} = -Q_{it}/C_i$. Thus a -2.5 V shift in the post-RH exposure transfer plots corresponds to an effective hole density of ~3.7 x 10^{10} cm^{-2} trapped on water-related states.

The relative constancy of mobility and subthreshold slope are mirrored in Figure 2, where the gate-voltage dependent mobility, extracted from the local slope of the transfer characteristics using the relation

$$\mu = \frac{L}{WC_i V_{DS}} \frac{\partial I_D}{\partial V_{GS}}, \qquad (2)$$

is plotted as a function of gate voltage for increasing values of RH. The rate of mobility increase and the final values reached, which correspond to those extracted using equation (1) and given in Table 1, show only slight reductions over the RH range. The main effect of increasing RH, therefore, is a systematic shift of the transfer plot to negative voltages which, as indicated above, is caused by additional hole trapping at water-related defects at the PS/DNTT interface or in the bulk PS. Such defects will not contribute to the semiconductor DoS.

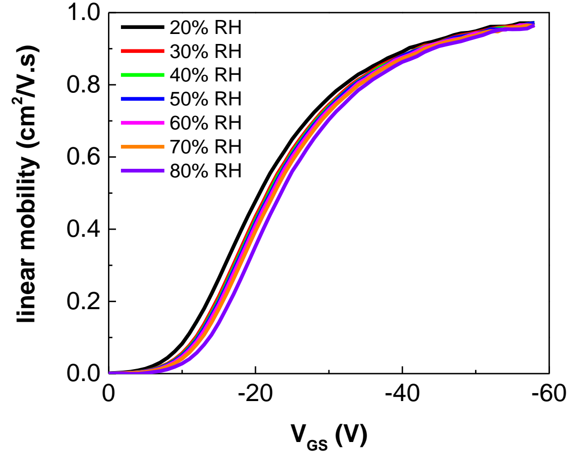


Figure 2. Gate-voltage-dependent mobility extracted by applying equation (2) to transfer characteristics obtained in the linear regime.

3.2 Effect of Temperature

To investigate the effect of temperature, RH was held constant at 10% while temperature was increased from 20ºC to 90ºC. As before, measurements were made 30 minutes after attaining the new conditions. On the timescale of the measurements, the output characteristics given in Figure 3(a) were stable, showing no hysteresis between forward and reverse voltage sweeps. The transfer characteristics in Figure 3(b) again show that the decreasing currents at higher temperatures were caused by shifts in V_{ON} and V_T to more negative values. As seen from the dash plots in Figure 3, even after holding the device open-circuited overnight at 20ºC and 10% RH very little recovery occurred.

Device parameters extracted from the transfer plots in Figure 3 are given in Table 2. As before, mobility and threshold voltages were extracted using equation (1), but now with a measured C_i = 2.54 nF/cm^2, to the linear sections of the transfer characteristics shown in the inset of Figure 3(b). As temperature increased up to 90ºC, mobility increased slightly from 1.00 to 1.25 cm^2/Vs. The shifts in V_{ON}, V_T and SS are similar to the changes caused by increasing RH. On-off current ratios remain ~10^5 at all temperatures. The only significant change observed after conditioning of the device overnight at 20ºC and RH=10% was a reduction of the mobility almost to its previous room temperature value and a reduction in the subthreshold slope below its initial value, both of which would be consistent with slight improvements in the morphology of the DNTT layer.

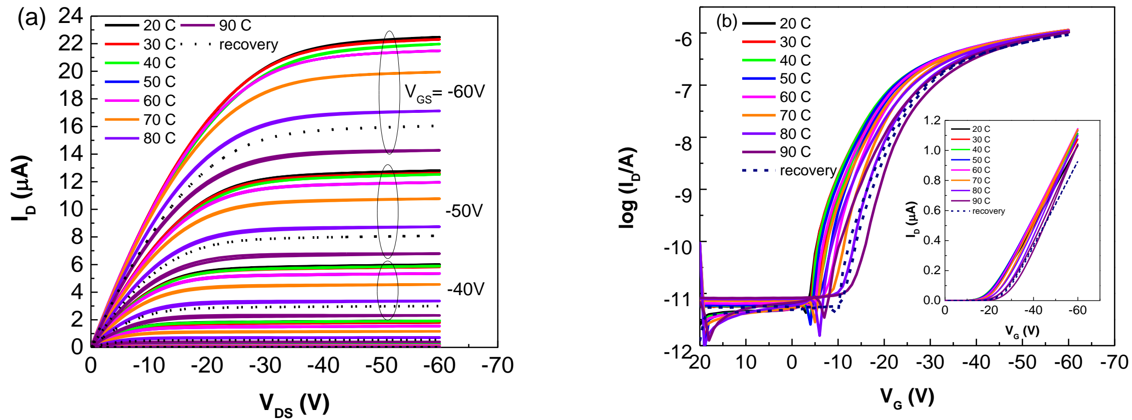


Figure 3. Effect of increasing temperature at RH = 10% on (a) output and (b) transfer (V_{DS} = -1 V) characteristics of a DNTT TFT (W = 2mm, L = 200 μm) with polystyrene gate insulator. The inset in (b) shows the data from the main figure obtained during the forward voltage sweep (+20 V to -60 V) replotted on a linear scale. The dashed plots were obtained after holding the device at 20ºC and 10% RH overnight.

Table 2 Device parameters extracted from the transfer characteristics in Figure 3(b) obtained during the forward voltage sweep with temperature increasing from 20ºC to 90ºC, RH = 10% and V_{DS} = -1V. Values in the final column were obtained subsequently at 20ºC after holding the device overnight at 20ºC and 10% RH.

Temperature	20 ºC	30 ºC	40 ºC	50 ºC	60 ºC	70 ºC	80 ºC	90 ºC	20 ºC
μ (cm^2/V.s)	1.00	1.07	1.10	1.13	1.16	1.19	1.22	1.25	1.10
V_{ON} (V)	-3	-3	-4	-4	-5	-5	-6	-7	-10
V_T (V)	-18	-20	-21	-21	-21	-23	-24	-27	-27
I_{ON}/I_{OFF}	2.18x10^5	2.33x10^5	2.38x10^5	2.47x10^5	2.50x10^5	2.33x10^5	2.03x10^5	1.65x10^5	2.00x10^5
SS (V/decade)	4.19	4.10	4.15	4.22	4.41	4.37	4.40	4.62	3.53

The post-heating transfer characteristic at 20ºC shows a displacement of about -8 V from the original plots, corresponding to an effective interface trapped hole density of ~9 x 10^{10} cm^{-2} arising from heating the device to 90ºC.

Figure 4 shows the gate-voltage dependence of the mobility, extracted by applying equation (2) to the forward sweep of each gate-voltage cycle in Figure 3(b). The initial rate of rise is similar at all temperatures albeit that the plots are shifted to more negative values consistent with a shift in flat-band voltage. As seen in the inset to Figure 4, the mobility saturates at values consistent with

those given in Table 2. Interestingly, and not unexpectedly for transport through an accumulation layer, the temperature dependence fits the model for hopping conduction in a 2-dimensional sheet [31] i.e. $\mu = \mu_0 \exp - (T_0 / T)^{1/3}$ with $T_0 = 288$ K. Since the mobility measured subsequently at 20ºC is slightly higher than measured initially, we assume that this is linked to the higher than expected increase in mobility that occurred at ~90ºC, which may be the result of morphological changes induced in the DNTT by increased molecular motion in the polystyrene which has a glass transition temperature at ~100ºC.

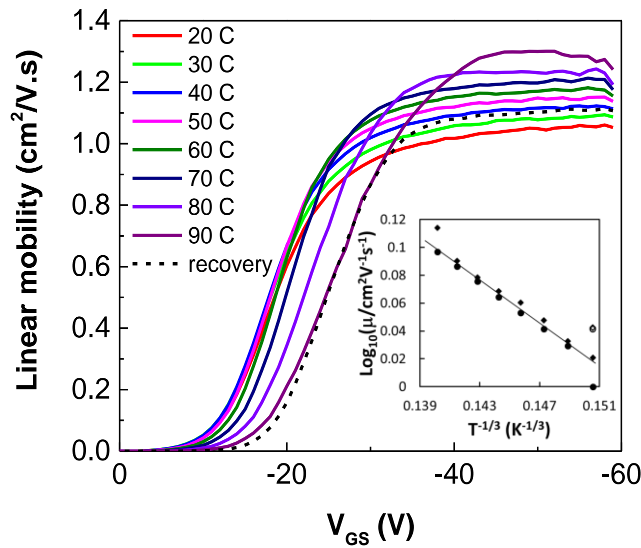


Figure 4 Gate-voltage-dependent mobility extracted by applying equation (2) to the transfer characteristics obtained for increasing temperatures during the forward voltage sweep (+20 V to -60 V) together with the post-heating plot at 20ºC (dotted curve). The inset shows the temperature dependence of the mobility from Table 2 (dots) and values corresponding to V_{GS} = -50V in the main figure (diamonds). The open data points were obtained at 20ºC post-heating.

3.3 Density of States

The Grünewald et al model [18] for extracting the DoS from the transfer characteristic of a thin film transistor assumes that V_{ON} corresponds to the flatband condition at the semiconductor/insulator interface. In the absence of parasitic effects the corresponding current, I_O, then measured is the true off-current flowing between source and drain through the bulk semiconductor. The model further assumes that the transfer characteristic reflects the accumulation of charge carriers at the semiconductor/insulator interface. Trapped insulator and interface charges are accounted for by a flatband voltage shift. Implicit in the approach is that the semiconductor is

not doped, thereby avoiding complicating features that would arise from the need to consider the effect of a conventional depletion region on the subthreshold slope. In the latter case, for example, the measured V_{ON} and I_O may not correspond to the flatband condition.

Distortion of the transfer characteristic caused by a gated Schottky contact [32] at low V_{GS} and series resistances at the source and drain at higher V_{GS} [33] will also lead to erroneous values for the DoS. No evidence for the last two effects is present in the transfer or mobility data presented here. This is confirmed also by the well-behaved increases in the slopes of the linear sections of the output characteristics at low V_{DS} when V_{GS} increases. Furthermore, in a previous report [7], we have shown that the mobility extracted from PS/DNTT transistors such as those investigated here is independent of channel length in the range 50 – 200 μm. Both the linear and saturation regimes yielded values ~ 1 cm^2/Vs as seen here. Therefore, we may safely ignore contact effects in our DoS calculations.

Within the above framework, and assuming Boltzmann statistics apply, the dependence of device current on gate voltage is written as

$$I_D(V_F) = I_{OFF}\,\frac{1}{l}\int_0^l e^{\beta V(x)}dx \tag{3}$$

where $V_F = (V_{GS}\text{-}V_{ON})$, l the thickness of the semiconductor, $V(x)$ the potential profile through the accumulation channel measured relative to that deep into the semiconductor and $\beta = q/kT$ with q the electronic charge, k Boltzmann's constant and T the absolute temperature. The Poisson equation

$$\frac{d^2V(x)}{dx^2} = -\frac{qp(V(x))}{\varepsilon_S\varepsilon_0} \tag{4}$$

where $p(V(x))$ is the concentration of accumulated holes at distance x from the interface, ε_S the relative permittivity of the semiconductor and ε_0 the permittivity of free space, is then solved subject to appropriate boundary conditions. This leads to an expression relating the interface potential, V_0, to V_F, namely

$$\exp(\beta V_0) + \beta V_0 - 1 = \beta\frac{C_i l}{\varepsilon_S\varepsilon_0 I_0}\left[V_F I(V_F) - \int_0^{V_F} I(\tilde{V}_F)d\tilde{V}_F\right]. \tag{5}$$

The right hand side of equation (5) may be calculated numerically from the experimental transfer characteristic. With suitable choice of units for β, the dependence of V_0 (in eV) on V_F is then determined. Following further manipulation, the total hole density $p(V_0)$ may be obtained from

$$p(V_0) = \frac{C_i^2}{\varepsilon_S \varepsilon_0 q^2} V_F \left(\frac{dV_0}{dV_F} \right)^{-1} \quad . \tag{6}$$

Assuming the zero Kelvin approximation for the Fermi function, Kalb [34] shows that the density of states *N(E)* may be extracted from

$$N(E) \approx \frac{dp(V_0)}{dV_0} \, . \tag{7}$$

It will be immediately obvious from the need to undertake two numerical differentiating steps in equations (6) and (7) that any extraneous noise in the transfer characteristic will be amplified significantly. Accordingly, limited smoothing was undertaken by utilizing values at $V_{GS}+\delta V$ and $V_{GS}-\delta V$ for effecting the differentiation at V_{GS}, where δV represents the sweep voltage step size (= 1 V).

Plots of V_0 versus V_F obtained using the procedure outlined above are given in Figure 5 showing the effect of (a) RH and (b) temperature. As RH increases, the plots of V_0 rise more slowly with V_F. Increasing temperature has the opposite effect with V_0 rising more rapidly. Using these plots together with equations (6) and (7), allows the DoS to be calculated as a function of V_0 (= E -E_F). The profiles for different RH appear in Figure 6(a) and for different temperatures in Figure 7(a).

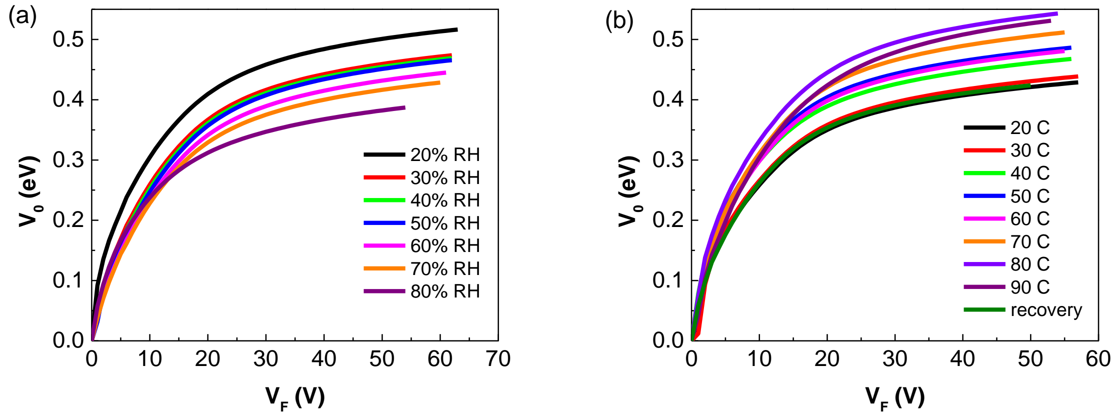


Figure 5 Plots of V_0 versus V_F showing the effect of (a) relative humidity and (b) temperature.

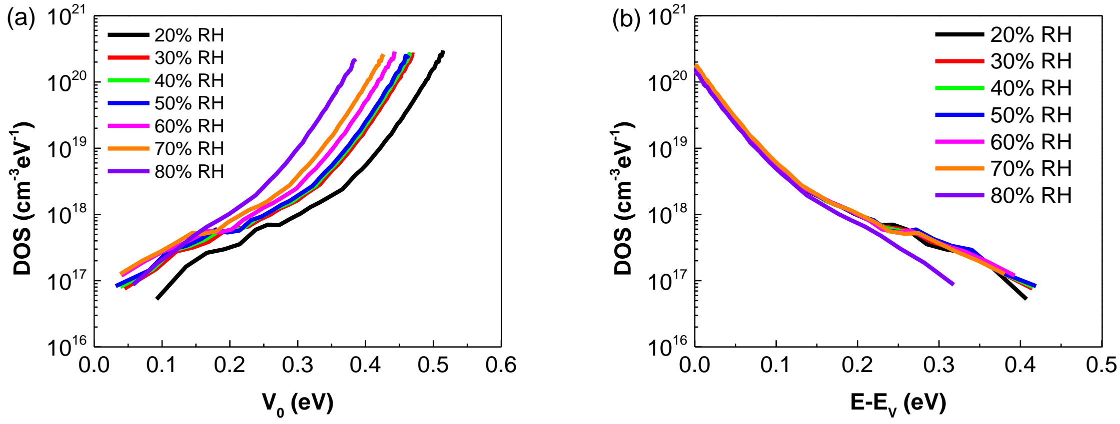


Figure 6 Density of states for different values of RH plotted relative to (a) V_0 (=E-E_F) and (b) the mobility edge assumed to coincide with ~E_V.

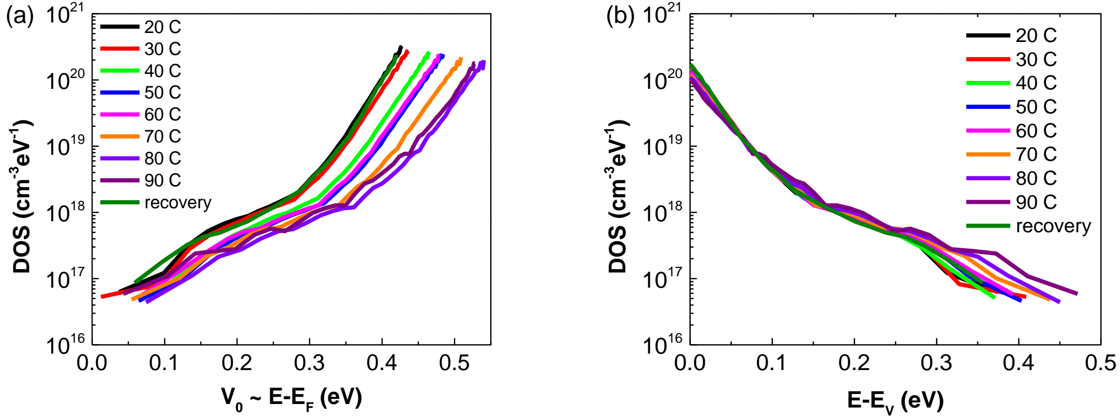


Figure 7 Density of states for different values of temperature plotted relative to (a) V_0 (=E-E_F) and (b) the mobility edge assumed to coincide with E_V.

Ideally, we wish to plot the DoS relative to the valence band edge, E_V. For CuSCN [20] and a small molecule/polymer blend [24], a sharp rise was observed in the DoS at high V_0 attributed to a band edge. Except in a very small number of plots, we do not see such a rise. V_0 vs V_F plots continue to rise steadily. However, a sharp rise in DoS at high V_0 in [20] and [24] implies saturation of the V_0 vs V_F plot. It is readily shown from equation (5) that if the carrier mobility becomes constant and equation (1) applies, then such a plot never saturates (see section S.3 in Supplementary Information). Rather, it continues to rise following the relation

$$\beta V_0 = \ln \alpha_1 \left(V_F^2 + \alpha_2 \right) \tag{8}$$

where α_1 and α_2 are constants determined by device and materials parameters and in the case of α_2 also dependent on the form of the transfer curve in the subthreshold region. To obviate the need to identify the location of E_F in the bandgap, some authors simply assume a value for (E_F-E_V) e.g. ~0.5 eV in pentacene [17].

In the present case, values of V_{GS}, and hence V_F and V_O, can be identified at which the effective mobility becomes constant at ~1 cm^2/Vs. We now assume that this occurs at a mobility shoulder coinciding with a transport band edge [23,35] (E_V in the case of a p-type semiconductor). Our method for determining the mobility edge is shown in section S.4 in the Supplementary Information. Upon evaluating the relevant energy, the DoS may be replotted as a function of (E-E_V).

In Figure 6(b) we see that the effect of RH on the DoS is minimal with the plots obtained for all relative humidities coalescing to a single curve over most of the range. (The departure from the general trend seen at 80% RH arises from the effect of the parasitic leakage current on the transfer characteristic at low device currents). Over the initial 0.1 eV above E_V, the DoS decreases exponentially from ~10^{20} $cm^{-3}eV^{-1}$ with a characteristic energy ~0.027 eV. Thereafter the DoS shows a broad, weak feature before decreasing to ~10^{17} $cm^{-3}eV^{-1}$ at ~0.4 eV above E_V. The plots for different temperatures (Figure7(b)) also coalesce to a common curve over most of the range, decreasing from ~10^{20} $cm^{-3}eV^{-1}$ with similar initial characteristic energy. These plots, however, show a slight increase in deeper states at higher temperatures, which eventually mask the weak feature lying between ~0.25 and ~0.35 eV above E_V.

A feature with similar energy (0.28 eV above the mobility edge) was observed in pentacene [36] and attributed to oxygen related defects. A sharp peak, even higher than in thin film pentacene, was observed in the DoS of rubrene single crystals when exposed to oxygen and light [37]. This could be expected based on the lower ionization potential of rubrene, ~4.75 eV [38] compared with that of pentacene, ~5.0 eV [2]. The ionization potential of DNTT (~5.4 eV [28]) is significantly higher than that of pentacene, so the concentration of any oxidation-related species in DNTT is expected to be lower. This is consistent with a peak amplitude here of ~2 x 10^{17} $cm^{-3}eV^{-1}$ above the background, which is significantly lower than observed in pentacene [23, 36]. While oxidation of the sulphur atoms to disulphones is possible in DNTT, this requires exposure to strong oxidizing agents. In the unlikely event that oxidized forms of DNTT were produced as by-products of synthesis, these would be more soluble than the parent molecule in dichlorobenzene and would be removed during recrystallization. Without further detailed studies,

we do not believe that the weak feature in DNTT can be attributed to an oxidation product of DNTT.

Another possible reason given for a peak in the DoS of organic semiconductors is a packing mismatch due to the presence of isomers. For example, in 2,8-difluoro-5,11-bis(triethylsilylethynyl) anthradithiophene (diF-TES ADT), a mixture of sys- and anti-isomers gave rise to strong peaks in the DoS at ~0.4 eV above the valence band [39]. The molecular structure of DNTT does not allow for this possibility.

In Figure 8 we compare the DoS obtained here with those obtained (a) by applying the Oberhoff computer model to transistor characteristics of single-crystals of DNTT placed over vacuum gaps defined by PDMS or silicon spacers [25] and (b) by SKPM on thin film transistors formed from evaporated films of DNTT on SAM-treated AlOx [28].

Xie et al [25] modelled the transfer data from single-crystal DNTT transistors, assuming *a priori* that it followed a double exponential profile. The best fit DoS showed a rapid decrease from ~10^{22} $cm^{-3}eV^{-1}$ to 10^{18} $cm^{-3}eV^{-1}$ followed by a slower decrease to below 10^{17} $cm^{-3}eV^{-1}$. In their analysis of SKPM data from pentacene thin film transistors formed on HMDS-treated SiO_2, Yogev et al [27] assume that the steep fall is the Gaussian tail of the occupied molecular orbitals. SKPM measurements by the same group on DNTT films evaporated onto SAM-modified AlO_x [28] gave a similar profile to those reported by Xie et al [25] for single crystal DNTT but displaced by ~0.1 eV to deeper states (Figure 8). This probably reflects measurements made over a polycrystalline grain, thus excluding states related to traps at intergrain boundaries. We conclude therefore that, while the method seems appropriate, an unaccounted for systematic error is present in their estimate of the energy range of the DoS spectrum and possibly E_F.

In our case, the DoS shows a more gradual decrease from ~10^{20} $cm^{-3}eV^{-1}$ but asymptoting to the same concentration (~10^{17} $cm^{-3}eV^{-1}$) of deeper states seen in [28]. Since V_{ON}, in our case coincides with flatband conditions, we locate E_F for DNTT ~0.4 eV above E_V at room temperature but rising to ~ 0.5 eV at 90ºC. Close to the mobility edge, the DoS rises above that determined in [28] by SKPM but remains lower than determined for single crystal DNTT by Xie et al [25]. This may be an intrinsic property arising from the very different quality of the DNTT in the two cases - single crystal versus polycrystalline. That the SKPM spectrum also reveals a weak feature similar to that seen in our DoS suggests that it may be due to an intrinsic property of the polycrystalline grains in DNTT rather than associated with the substrate dielectric – polystyrene in our case.

As indicated earlier, because the Grünewald approach uses the Boltzmann approximation when describing the current flow, this will introduce errors in our DoS when the Fermi level approaches within a few kT (~50 meV) of the mobility/valence band edge. It should be noted, however, when finally deconvoluting the DoS from the extracted carrier concentration the step-function approximation of the Fermi-Dirac distribution is used [34] thus minimizing this source of error. A small systematic error in state energy could also arise from our method for estimating the mobility edge. Additional sources of error could include incorrect estimation of the voltage, V_{ON}, and/or current, I_{OFF}, corresponding to the flatband condition. We have undertaken a sensitivity analysis to test this possibility (section S.4 in Supplementary Information). Within reasonable limits, we find that such errors would be small.

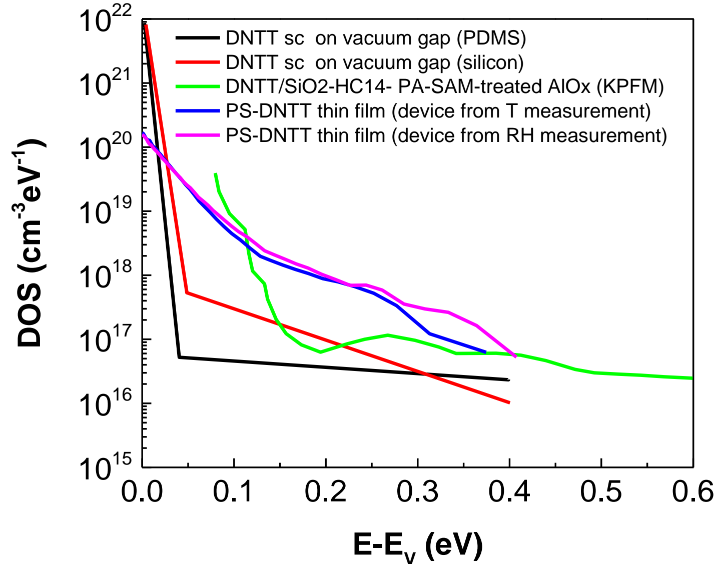


Figure 8 Comparison of DoS spectra obtained in the present work using the Grünewald et al model with those obtained by applying the Oberhoff et al model to single-crystal DNTT [25] and from evaporated films using Scanning Kelvin Probe Microscopy [28].

4. Conclusions

In conclusion, we have undertaken a detailed study of the effect of relative humidity and temperature on the density of states in thin film transistors based on DNTT as the active layer and polystyrene as the gate insulator. Using the approach reported by Grünewald et al [18], we extract density of states spectra from transfer characteristics obtained in the linear regime. By assuming

that the onset of constant mobility coincides with the valence band edge, we show that the DoS in DNTT is insensitive to relative humidity in the range 10 – 70%, and in the absence of parasitic currents perhaps to even higher RH. We further show that, as temperature increases, the only change observed in the DoS is a slight increase in the deeper states lying more than ~0.3 eV above the mobility edge. The device instability that is observed, i.e. shifts in V_{ON} and V_T, may be ascribed almost entirely to flatband voltage shifts arising from hole trapping in the polystyrene dielectric or its interface with DNTT. Such traps do not form part of the manifold of energy states contributing to the DoS in DNTT. Finally we have identified a weak trap feature located ~0.25 to 0.35 eV above the mobility edge, the origin of which requires further investigation.

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