13.5 A 17.5-to-20.94GHz and 35-to-41.88GHz PLL in 65nm CMOS for Wireless HD Applications

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This work shows a complete PLL that is integrated in standard industrial 65nm CMOS technology. This frequency synthesizer is fully compliant with *IEEE 802.15.3c* normalization [1-4]. This PLL delivers a quadrature LO signal around 20GHz and a differential LO signal around 40GHz and has 17.9% tuning range. The wide tuning range of 17.9% permits to cover the full *IEEE 802.15.3c* band with industrial margin. The phase noise is -100dBc/Hz at 1MHz offset and the total power dissipation is only 80mW including the output buffers and amplifiers. Short-range wireless multi-Gb/sec communication systems use the mm-wave band of 57GHz to 66GHz, according to the *IEEE 802.15.3c* normalization. The frequency synthesis is one of the key elements for these transceivers. Indeed, one must take into account the antagonist tradeoff between large band tuning range of the frequency synthesizer and phase noise performance. In transceivers using super-heterodyne architecture with double conversion, the frequency synthesizer signal f_{LO} can be equal to $2f_{RF}/3$ and $f_{RF}/3$. In this case, to cover the four channels of the *IEEE 802.15.3c* normalization, the frequency synthesizer has to deliver a first local oscillator (LO) signal between *19.44GHz* and *21.6GHz* and a second LO signal between *38.88GHz* and *43.2GHz*, respectively. This architecture offers a good trade off between the required large frequency tuning range (>15%) and low phase noise (<-95dBc/Hz).

The PLL architecture is depicted in Fig. 13.5.1. It is composed of a Push-Push Quadrature-Voltage-Controlled-Oscillator (QVCO) that delivers two 0°/90° LO signals around 20GHz and a harmonic signal around 40GHz. The QVCO is followed by a frequency divider chain with a division ratio varying from 640 to 1240. Next, the Phase/Frequency Detector (PFD) compares the VCO's divided signal to an external 36MHz reference signal which is divided by two. Finally, a Charge Pump (CP) followed by a 3rd order Loop Filter (LF) controls the QVCO's oscillation frequency.

Figure 13.5.2 shows the schematic of the QVCO. It is based on two cross coupled CMOS VCOs (MI_1 … MI_4 and MQ_1 … MQ_4). In order to generate the 0°/90° oscillation signals each basic VCO cell is coupled by two NMOS transistors (MI_5, MI_6 and MQ_5, MQ_6). The global QVCO oscillates around 20GHz. Each cell's resonator includes a single octagonal integrated inductance and a bank of varactors. The bank uses many varactors for oscillation frequency control. One of the varactors is connected to the loop filter (LF) voltage control (analog varactor) and the others are switched ON and OFF with the help of a 4 bits digital control (digital varactors). This technique helps to split the required oscillation band into sub-bands and to reduce the oscillator's gain for better PLL global stability. The oscillation sub-bands overlap between them thanks to a judicious choice of each of the varactors size. The required 40GHz signal is collected at the current source of the coupling transistors with the help of two short-ended quarter wave transmission line stubs. The 20GHz outputs of the VCO are followed by specific tree buffering in order to drive the PLL and the 100Ohm differential load impedance (Fig. 13.5.1). The 40GHz output is followed by a 40GHz cascode amplifier with differential 100Ohm output matching. All RF signals use micro-strip transmission lines. The first division of the VCO's 20GHz signal is done with the help of a grounded source frequency (GSF) divider. This architecture has been chosen for its benefits on current mode logic (CML) dividers in terms of operational frequency range, when process and temperature impacts are taken into account [5]. The GSF divider schematic is showed at the top part of Fig. 13.5.3. Conventional CML dividers are adopted for the frequency division after the GSF divider in order to reduce the power consumption. The choice of the communication channel is done by a programmable divider implemented, using 2/3 cells based on modular architecture prescaler, that has a Division Factor Range (DFR) of 16 to 31. In order to obtain the wanted DFR we need four 2/3 cells, and therefore, four bits are necessary to address the desired channels. The programmable divider is depicted at the bottom part of Fig. 13.5.3. Finally, the PFD, the CP and the 3rd order Loop Filter are implemented in order to detect the phase/frequency error and control the VCO with the analog control voltage. Note that for measurement convenience one part of the loop filter (R1, R2 and C2) are not integrated into this prototype version (Fig. 13.5.1). This 3rd order Loop Filter has been chosen to allow a better rejection of spurious out of the range ($\omega>\omega_c$).

The frequency synthesizer is fabricated in a 65nm CMOS process from STMicroelectronics. Figure 13.5.7 shows the die microphotograph which occupies 1.6x1.9mm² including pads. The dividers, the VCO and the buffers are supplied by 1.2V and the PFD-CP block is supplied by 1.8V using double-gate oxide. The total dissipated power of the PLL is 80mW including the 20GHz and the 40GHz buffers. In order to measure the characteristics of the frequency synthesizer, the chip has been mounted on a Rogers 4003 printed circuit board (PCB). All static and low frequency signals are wire bonded to the board for DC programming and digital control. The 20GHz and 40GHz signals are measured directly on chip using differential probes. Figure 13.5.4 shows the measured frequency of the 20GHz output signal of the VCO (opened loop) versus the control voltage. The measurement is performed by sweeping the analog control voltage from 0 to 1.8V, for each of the 16 digital channel selection combinations ("0000" to "1111"). The VCO provides continuously an oscillation frequency from 17.50GHz to 20.94GHz. According to Fig. 13.5.1 and Fig. 13.5.4 the PLL locks at frequencies that are given by:

$$f_{LOCK} = \frac{f_{REF}}{2} \cdot D_{DIV} \cdot D_{PROG} \quad (1)$$

Where f_{REF} is the 36MHz external reference, D_{DIV} is the fixed dividing ratio (=40) and D_{PROG} are the DFR values that give a locking frequency included into the oscillation range (D_{PROG}=25 to 29). Therefore, the PLL addresses 5 frequency channels from 18GHz to 20.88GHz with a step of 0.72GHz. The channels are depicted in Fig. 13.5.4 in square symbols. The last three channels correspond to the *IEEE 802.15.3c* normalization. Note that the PLL locks allover the oscillation frequency range of the QVCO if the reference frequency is swept.

Figure 13.5.5 shows the measured phase noise at the third channel (20.88GHz) of the standard. The phase noise is -100dBc/Hz at 1MHz offset and -126dBc/Hz at 10MHz offset. The inset of Fig. 13.5.5 shows the output spectrum at 20.88GHz. The spurious due to the reference frequency (36MHz) is lower than -50dBc. The table in Fig. 13.5.6 shows a comparison of this work with mmw-range frequency synthesizers in deep-submicron CMOS technologies. This PLL exhibits the best tradeoff in terms of frequency range to phase noise that can be found in literature.

Acknowledgements:
V. Lagareste and B. Martineau from ST are acknowledged for their support on frequency synthesizer and millimeter-wave simulations respectively.

References:
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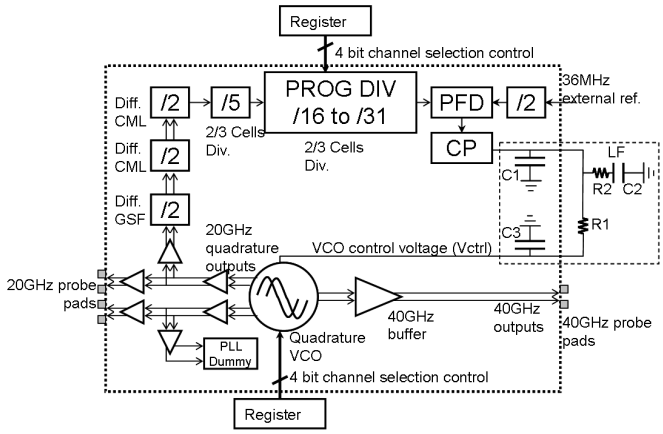

Figure 13.5.1: Frequency synthesizer architecture.

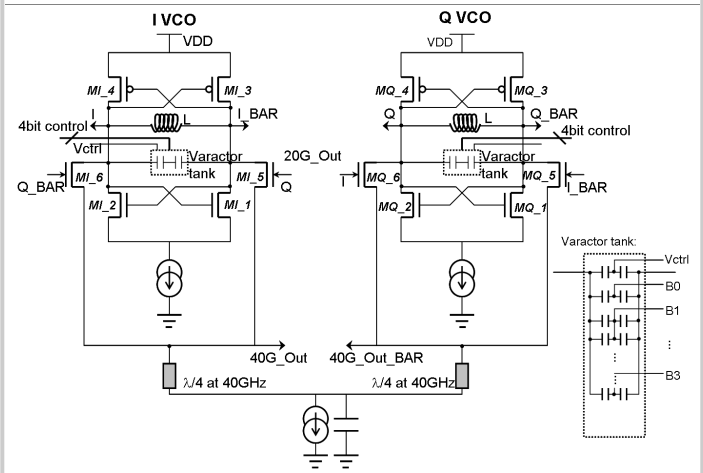

Figure 13.5.2: Electrical schematic of the quadrature VCO. Inset: varactor tank architecture.

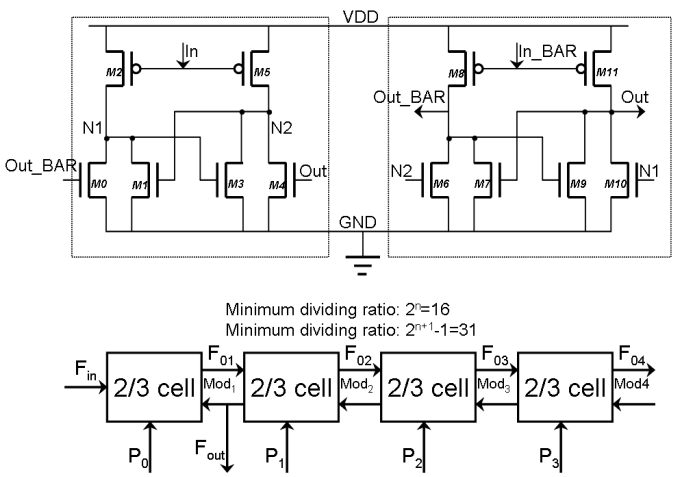

Figure 13.5.3: (top part) Schematic of the GSF divider. (bottom part) Block schematic of the modular programmable prescaler architecture.

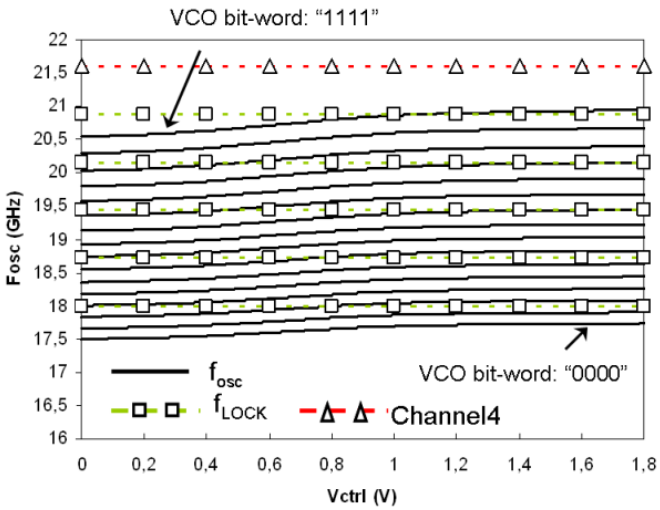

Figure 13.5.4: Locking frequencies of the Synthesizer.

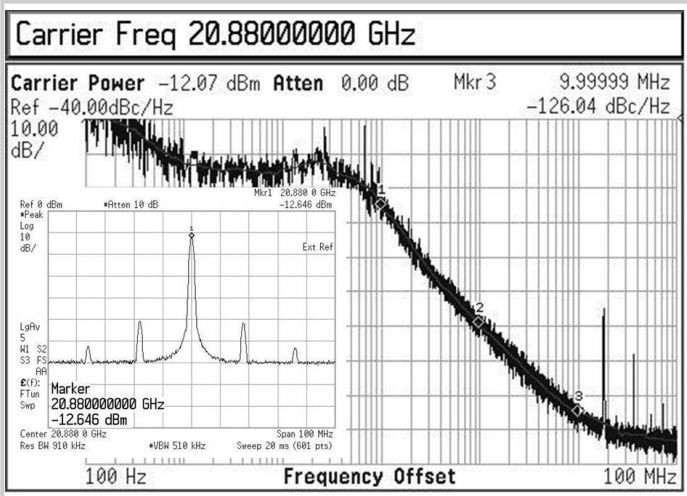

Figure 13.5.5: Measured phase noise of the frequency synthesizer at the 3rd channel (20.88GHz) of the IEEE 802.15.3c standard. Output spectrum at 20.88GHz.

	This work	[1]	[2]	[3]	[4]
Tech. [nm]	65 CMOS	90 CMOS	45 CMOS	90 CMOS	65 CMOS
Supply [V]	1.2**	1.2	1.1	1.2	1.2
Frequency range [GHz]	17.5 to 20.94 (17.9%) 35 to 41.88 (17.9%)	39.1 to 41.6 (6.2%)	57 to 66 (14.6%)	58 to 60.4 (4%)	96
Phase noise @1MHz [dBc/Hz]	-100 (20.88GHz) -97.5 (41.76GHz)	-90	-75	-85	-75.2
Calculated Phase noise @1MHz for 20GHz signal [dBc/Hz]	-100	-96	-84.6	-94.6	-88.9
F_{ref} [MHz]	36	50	100	234.1	375
Loop Type	Integer	Fractional	Integer	Integer	Integer
Division Ratio(s)	640 to 1240	512 to 2032	512 to 8184	256 to 258	256
Ref. Spur [dBc]	<-50	-54	-42	-50.4	-51.7
Power [mW]	80	64*	78	80	43.7*

*Without Output Buffer
**The supply voltage of PFD and CP is 1.8V

Figure 13.5.6: Measured performance summary and comparison.

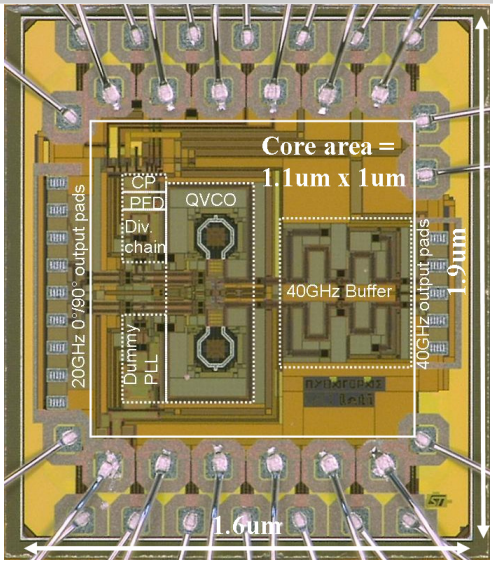

Figure 13.5.7: Chip micrograph of the PLL.

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