

Porting CMS Heterogeneous Pixel Reconstruction to Kokkos

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Abstract. Programming for a diverse set of compute accelerators in addition to the CPU is a challenge. Maintaining separate source code for each architecture would require lots of effort, and development of new algorithms would be daunting if it had to be repeated many times. Fortunately there are several portability technologies on the market such as Alpaka, Kokkos, and SYCL. These technologies aim to improve the developer productivity by making it possible to use the same source code for many different architectures. In this paper we use heterogeneous pixel reconstruction code from the CMS experiment at the CERN LHC as a realistic use case of a GPU-targeting HEP reconstruction software, and report experience from prototyping a portable version of it using Kokkos. The development was done in a standalone program that attempts to model many of the complexities of a HEP data processing framework such as CMSSW. We also compare the achieved event processing throughput to the original CUDA code and a CPU version of it.

1 Introduction

Graphics processing units (GPUs) are being used in scientific computing because of their cost and power efficiency in solving data-parallel problems. Currently each GPU vendor provides their own APIs and programming models, that also differ from the programming of the CPU. There are, however, similarities in these GPU programming models, and in many cases the code for very core pieces of algorithms can be shared between the CPU and the GPUs, but the surrounding code arranging the data and calling the algorithms has to differ. In multi-million line code bases that have many custom algorithms and have to be maintained for tens of years, such duplication of code would require significant development and maintenance effort, and be error prone to maintain.

Over several years, many technologies for fully portable code between CPUs and compute accelerators have emerged to ease the development and maintenance burden of heterogeneous applications. These technologies include C++ libraries, such as Alpaka [1–3], Kokkos [4], and RAJA [5, 6]; SYCL [7] that can be implemented as libraries such as triSYCL [8] and hipSYCL [9] or as specific compilers such as ComputeCpp [10] by Codeplay and DPC++ [11] by Intel; compiler pragma based solutions such as OpenMP [12] and

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17 OpenACC [13]; or as standard C++ itself via parallel STL where the compiler is solely re-
18 sponsible for generating necessary code for the offloading.

19 In this work we explore the applicability of Kokkos for portability across CPU and GPUs
20 using the Patatrack heterogeneous pixel reconstruction workflow [14] from the CMS exper-
21 iment [15] at the CERN LHC [16] as a use case for a set of realistic HEP reconstruction
22 algorithms that are able to effectively utilize a GPU. The work was done in the context of
23 the DOE HEP Center for Computational Excellent (HEP-CCE). We look into not only the
24 porting of the algorithms, but also the implications of integrating such an approach into a
25 HEP data processing software.

26 We mimic the setup of the CMS data processing software, CMSSW [17]. CMSSW is
27 multi-threaded [18–20] using the Intel Threading Building Blocks (TBB) [21], and the cur-
28 rent plan for direct same-node compute accelerators is to build code for all supported accel-
29 erators in the same release build, express all possibilities in the configuration, and decide at
30 runtime what code exactly to run based on hardware availability [22, 23]. We are looking for
31 a single-source solution that would provide portability at least across CPU and GPUs, would
32 be relatively easy to program with by HEP physicists, would provide adequate performance
33 on all relevant platforms, and would require the least amount of change in the CMSSW build-
34 ing and data processing model. It is unlikely that all these goals would be met by a single
35 technology, and therefore it is necessary to learn the details in all these aspects to find the
36 best compromise.

37 This paper is organized as follows. The technical aspects of the Patatrack pixel recon-
38 struction are described in Section 2. A brief introduction of Kokkos is given in Section 3.
39 The experience of porting the original CUDA application into Kokkos is reported in Sec-
40 tion 4. In Kokkos’ nomenclature a place that runs code is called an *execution space*. We
41 have tested Serial, Threads, CUDA, and HIP execution spaces of Kokkos, and we focus on
42 several aspects in how Kokkos would fit into a framework like CMSSW. We have measured
43 the event processing throughput of the Kokkos version’s CPU and CUDA execution spaces,
44 and compare those to direct CPU and CUDA implementations in Section 5. Conclusions are
45 given in Section 6.

46 2 Patatrack Heterogeneous Pixel Reconstruction

47 The Patatrack pixel reconstruction pioneered offloading algorithms to NVIDIA GPUs with di-
48 rect CUDA programming within CMSSW. The offloaded chain of reconstruction algorithms
49 takes the raw data of the CMS pixel detector as an input, along with the beamspot parameters
50 and necessary calibration data, and produces pixel tracks and vertices. CMSSW schedules
51 algorithms as units that are called *modules*. The pixel reconstruction algorithms are orga-
52 nized in five modules, depicted in Figure 1, that communicate the intermediate data in the
53 GPU memory through the CMSSW event data. The BeamSpot module only transfers the
54 beamspot data into the GPU. The Clusters module transfers the raw data to the GPU, un-
55 packs them, calibrates the individual pixels, and clusters the pixels on each detector module.
56 The RecHits module estimates the 3D position of each cluster forming hits. The Tracks mod-
57 ule forms n-tuplets from the hits, and fits the hit n-tuplets to obtain track parameters. The
58 Vertices module forms vertices from the pixel tracks. There are further modules to optionally
59 transfer the tracks and vertices to the CPU, and to convert the Structure-of-Array (SoA) data
60 structures to the data formats used by downstream algorithms in CMSSW, but those are not
61 considered in this work and therefore not shown in Figure 1.

62 In order to explore code portability technologies, the CUDA code of the Patatrack pixel
63 reconstruction was extracted from CMSSW into a standalone program [24]. The separation
64 from CMSSW gives us freedom to modify the compilers, build rules, external libraries, and

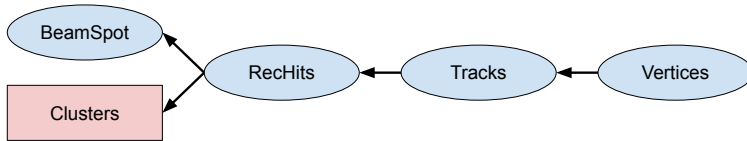


Figure 1. Directed acyclic graph of the framework modules in the Patatrack pixel reconstruction. The arrows denote the data dependencies of the modules, e.g. RecHits module depends on data produced by BeamSpot and Clusters modules. The Clusters module (red rectangle) is the only one that transfer data from the device to the host and uses External Worker synchronization mechanism, while the other modules (blue oval) do not.

code organization that would be more laborious to achieve in the full CMSSW software stack. The standalone program was crafted to mimic several aspects of CMSSW, including similar organization of code into shared libraries, plugin libraries that are loaded dynamically based on run-time information, and a simple framework that uses TBB for multi-threading. From the CMSSW framework concurrency features this simple framework includes only event loop based on TBB tasks, processing of multiple events concurrently, and processing of independent modules concurrently for the same event. There is only a single module type of each module having a separate instance for each concurrent event, and the *External Worker* concept [23] is included in order to use the CPU threads to do other work while the GPU is running the offloaded work. The CMSSW tools to use CUDA runtime directly in the modules [23] are also included.

The standalone setup includes a binary data file that contains raw pixel detector data from 1000 simulated top quark pair production events from CMS Open Data [25], with an average of 50 superimposed pileup collisions with a center-of-mass energy of 13 TeV, using design conditions corresponding to the 2018 CMS detector. All of the data, about 250 MB, are read into the memory at the job startup to exclude I/O from the throughput measurement. The necessary pixel detector conditions data are also stored in binary files, and read into the memory at the start of the job. The data processing throughput is calculated by measuring the time spent in the event processing, and dividing the number of processed events with that time. For each event, the object holding the raw data for that event is copied once from the aforementioned memory buffer to another object owned by the event data structure. The event processing time includes the time taken by this copy operation.

3 Kokkos

Kokkos is a programming model and a C++ library for writing performance portable applications. At the time of writing the latest version of Kokkos is 3.3.1, and it supports several execution spaces. An algorithm can be run serially on the host CPU via a *host serial* execution space, or it can be parallelized with one of two *host parallel* execution spaces that are OpenMP and (POSIX) Threads. An algorithm can also be offloaded to compute accelerators with *device parallel* execution spaces. NVIDIA GPUs can be used with CUDA or HPX execution spaces, and AMD GPUs can be used with HIP execution space. There are also OpenMP-Target and SYCL 2020 execution spaces that can support various platforms depending on the underlying toolchain. Currently all other device parallel execution spaces than CUDA are experimental. In this work we have tested Serial, Threads, CUDA, and HIP execution spaces.

```

// declarations of variables
constexpr uint32_t MaxNumModules;
constexpr uint32_t maxHitsInModule();
Kokkos::View<uint32_t const*, Kokkos::CudaSpace> cluStart;
Kokkos::View<uint32_t*, Kokkos::CudaSpace> moduleStart;

Kokkos::parallel_for(
    Kokkos::RangePolicy<Kokkos::Cuda>(0, MaxNumModules),
    KOKKOS_LAMBDA(const int index) {
        moduleStart(index + 1) = std::min(maxHitsInModule(), cluStart(index));
    });

```

Figure 2. A simplified example of using `RangePolicy` policy with `parallel_for`. The initialization of the declared variables is omitted for brevity. In this example the execution and memory space template argument are spelled out explicitly. If the compile-time defaults for those suffice, the explicit template arguments can be left out. Corresponding CUDA program is shown in Figure 3.

99 Kokkos makes use of a runtime library. The library can have the Serial, one host parallel,
100 and one device parallel execution space enabled at the same time, and this set is chosen at the
101 library build configuration time. In addition, at least for CUDA execution space, one library
102 can support only GPUs that have the same major compute capability number. For example,
103 one library can support Volta (compute capability 7.0) and Turing (7.5) GPUs, but not Volta
104 and Pascal (6.0) GPUs. In the code the execution space to be used can be chosen at compile
105 time with template arguments. If the execution space is not specified explicitly, the most
106 advanced execution space available in the library is used, i.e. device parallel execution space
107 is preferred over host parallel execution space, which is preferred over the Serial execution
108 space. Currently Kokkos supports only one device per process.

109 Kokkos provides high-level interface for parallel operations. These include
110 `parallel_for` for a for-loop of independent iterations, `parallel_scan` for a prefix scan,
111 and `parallel_reduce` for a reduction. Parallel operations can be nested with some restric-
112 tions. The details of the iteration are controlled with a policy. A `RangePolicy` can be used
113 for a 1-dimensional range where all elements of the range can be processed independently.
114 An example of `parallel_for` with `RangePolicy` is shown in Figure 2 and a corresponding
115 CUDA version in Figure 3. An `MDRangePolicy` extends the concept of the 1-dimensional
116 `RangePolicy` to many, up to 6, dimensions. A `TeamPolicy` introduces a *league of teams*
117 that consist of *threads*¹. Threads in a team can use a common scratch memory space, and can
118 synchronize within the team with a barrier. In addition, Kokkos has some support for tasks
119 and graphs, that are not explored in this work.

120 As well as parallel operations, Kokkos provides a datastructure for multi-dimensional ar-
121 ray, `Kokkos::View`. It is reference counted and behaves like `std::shared_ptr`, and can
122 be passed to device functions by value. A major feature of the `Kokkos::View` is that its
123 memory layout can be controlled with template arguments, and the default layout depends on
124 the memory space. In addition, intents for the memory can be expressed with additional tem-
125 plate arguments, for example specifying random-access constant data enables seamless use
126 of CUDA texture caches. Data transfers between the host and the device are done explicitly.

¹The *league* corresponds to *grid* in CUDA, and *team* corresponds to *block*.

```

// declarations of used variables
constexpr uint32_t MaxNumModules;
constexpr uint32_t maxHitsInModule();

__global__
void fillHitsModuleStart(uint32_t const* cluStart, uint32_t* moduleStart) {
    for(int i = threadIdx.x, iend = MaxNumModules; i < iend; i += blockDim.x) {
        moduleStart[i + 1] = std::min(maxHitsInModule(), cluStart[i]);
    }
}

uint32_t const* cluStart_;
uint32_t* moduleStart_;
fillHitsModuleStart<<<1, 1024>>>(cluStart_, moduleStart_);

```

Figure 3. CUDA version of the simplified example expressed in Kokkos in Figure 2. The initialization of the declared variables is omitted for brevity.

127 4 Porting experience

128 4.1 Impact on building

129 The current plan to support compute accelerators in CMSSW software stack is to build code
130 for all supported accelerators, and choose the exact version to be run at runtime [22]. The
131 various constraints of the Kokkos runtime library, described in Section 3, make it challenging
132 to deploy in this manner. A single runtime library supporting only one device parallel execution
133 space, and only one CUDA major architecture or CPU vector architecture, would, in
134 this plan, imply the need to build many versions of the runtime library. The correct version
135 would have to be loaded dynamically based on the available hardware. In this work we used
136 exactly one runtime library at a time.

137 Every source file that includes any Kokkos header must be built with a compiler that is
138 capable of compiling the code for all the enabled execution spaces, even if the source file
139 would not use any Kokkos functionality. For example, if the Kokkos runtime library was
140 built with CUDA execution space enabled, all source files including Kokkos headers must be
141 compiled with a CUDA capable compiler.

142 Kokkos provides an integration with the CMake build system. In this work, however, we
143 used CMake only to build the Kokkos runtime library itself, and we used a plain Makefile to
144 build the application code. We did this because CMSSW uses the SCRAM build system [26],
145 and therefore we'd have to understand the exact build rules in order to implement those for
146 SCRAM.

147 The inability of `nvcc` to link device code from shared objects imposed severe constraints
148 on how the Kokkos runtime library had to be built. We were able to use the runtime library
149 built as a dynamic library with `RangePolicy`, but with the first use of `TeamPolicy` that
150 approach lead to link errors from `nvcc`. The only build setup we managed to get to work was
151 to build the Kokkos runtime library as a static library without support for relocatable device
152 code, but with position-independent code for the host (`-fPIC`) to be able to link the static
153 library with dynamic libraries of the application. This setup implies that CUDA separate
154 compilation model can not be used, and therefore each source file must contain all device
155 code called from that file, either directly or via including other files. Also, CUDA dynamic
156 parallelism can not be used.

157 With the HIP execution space we were able to use a dynamic Kokkos runtime library, and
158 in fact were not able to get a static build to work with the HIP compiler.

159 4.2 Impact on code

160 As mentioned in Section 3, the Kokkos execution space is chosen at compile time. A choice
161 done at runtime would be a much better fit in the current plans of using compute accelerators
162 in CMSSW. We implemented the capability of choosing the execution space at runtime by
163 building each source file containing Kokkos code once for each execution space and using
164 namespaces to guarantee different symbols for each execution space.

165 Conversion of CUDA kernel calls to Kokkos parallel operations was mostly straightforward.
166 Kokkos provides a parallel scan and sort, and therefore we decided to use those instead
167 of trying to port the implementations of scan and radix sort device functions in the direct
168 CUDA version. The code uses team-wide scan, but before version 3.3, Kokkos provided only
169 league-wide scan. Before updating to Kokkos 3.3 we used the league-wide scan with two ad-
170 ditional kernels to post-process the league-wide result to be equivalent to a team-wide scan.
171 Kokkos' parallel sort function can be called only from the host code, which meant that we
172 had to split all the CUDA kernels that called the device-side sort function into two kernels,
173 and call the Kokkos' host-side sort function in between. Finding out the proper and efficient
174 way to transform the CUDA code to use the Kokkos' scan and sort APIs was the most time
175 consuming single effort.

176 For hierarchical parallelism, or thread teams, we found that the number of threads in a
177 team is not exactly portable. The Serial execution space requires it to be exactly one, Threads
178 execution space can use at most the number of CPU threads, and CUDA execution space has
179 the same limitations as CUDA itself. This disparity can be largely mitigated by specifying
180 the number of threads as `Kokkos::AUTO()`, that leaves the decision of the number of threads
181 to Kokkos.

182 We found `Kokkos::View` to be useful by providing a unified interface for memory allo-
183 cation, and smart pointer semantics for managing the ownership of the memory block. Also
184 the ability to avoid an additional memory allocation in code that transfers data from host to
185 device for CPU-only execution spaces is a plus. The more advanced features like multiple
186 dimensions and the layout control are not needed in this code, where nearly all arrays have
187 only one dimension. The only exception is the track covariance matrix, but we did not try
188 to transform the Eigen-based implementation in the original CUDA into multidimensional
189 `Kokkos::View`. In this code a SoA abstraction would be much more useful than multi-
190 dimensional array, and we do not see how `Kokkos::View` would help in crafting SoA data
191 structures.

192 In the first Kokkos version we found that about 80% overall kernel runtime was spent
193 in `Kokkos::View` initialization. In this code the first operation for all device memory is
194 a write either by a memory copy from the host memory, or by a computation done in a
195 kernel. Therefore all the initialization done by default is unnecessary, and avoiding that with
196 `Kokkos::ViewAllocateWithoutInitializing` argument to `Kokkos::View` constructor
197 improved the event processing throughput by almost a factor of 3.

198 At the time of writing, we have not been able to successfully run the full application with
199 the HIP execution space. A test application that uses the same build and dynamic library
200 infrastructure works well, but is not complex-enough to give meaningful insights into the
201 performance.

202 Furthermore, we have not yet managed to run the application with multiple concurrent
203 events with Serial or CUDA execution spaces. The Threads execution space explicitly pre-
204 vents calls from more than one thread, even if the calls would come at different times. Despite
205 of the Threads execution space being uninteresting to be used in the context of CMSSW, we
206 have included it as a comparison point in the performance measurements in Section 5 to show
207 how a parallelization strategy different from concurrent events would perform.

208 5 Performance comparison

209 The performance tests were done on GPU nodes of the Cori supercomputer at the National
210 Energy Research Scientific Computing Center (NERSC). A Cori GPU node has two sockets
211 with Intel Xeon Gold 6148 ("Skylake") processors, each with 20 cores and 2 threads per core,
212 and eight NVIDIA V100 GPUs. For this work we used only one CPU socket, to avoid the
213 impact of non-uniform memory access (NUMA), and one GPU. In all tests the threads were
214 pinned to a single socket. Each job was run for approximately 5 minutes, processing the set
215 of 1000 individual events for an integer number of times, and repeated 8 times on random
216 nodes of the GPU cluster. The code was compiled with GCC 8.3.0, and nvcc from CUDA
217 11.1.

218 In order to minimize the impact of the CPU frequency scaling the CPU programs were
219 tested by running another program on the background with as many threads as needed to fill
220 all the 40 hardware threads of the socket. Table 1 shows the throughput of the Kokkos ver-
221 sion with Serial and Threads execution spaces, and of the direct CPU version with 1 and 40
222 threads. The Kokkos version processes one event at a time, and with the Threads execution
223 space each Kokkos parallel operation is parallelized with the same number of threads. The
224 direct CPU version, on the other hand, is parallelized by processing multiple events concur-
225 rently, one event per thread. While comparing the multi-threaded throughput of these two
226 approaches is not exactly fair, it does show what can be achieved with a single process using
227 the different approaches.

228 The results in Table 1 show that the intra-event parallelization scales poorly, whereas par-
229 allelizing over events gives much better throughput and scales well. We have not concluded
230 yet why the direct CPU version gives 1.5 times better throughput than the Kokkos version
231 with Serial execution space.

232 The programs using CUDA were tested without any background activity on the CPU.
233 Table 2 shows the throughput of the Kokkos version with CUDA execution space, and of
234 the direct CUDA version. The direct CUDA version can process data from multiple events
235 concurrent with CUDA streams, and this approach helps to get 2.5 times higher throughput
236 from the V100 GPU than when processing one event at a time. With a single event in flight,
237 the memory pool, based on the `CachingDeviceAllocator` of the CUB [27] library, helps
238 to increase the throughput by 4.5 times compared to using raw CUDA memory allocations.

Table 1. Comparison of the event processing throughput between the Kokkos version of the program using Serial and Threads execution spaces and the CPU version implemented from the original CUDA version through a simple translation header. In all cases all the threads were pinned to a single CPU socket (Intel Xeon Gold 6148) that has 20 cores and 2 threads per core. Each test ran about 5 minutes, and CPU-heavy threads from a background process were used to fill all the 40 hardware threads of the socket. The work in the CPU version is parallelized by processing as many events concurrently as the number of threads the job uses without any intra-event parallelization, whereas in the Kokkos version there is only one event in flight, and all parallelization is within the data of that event. For the Kokkos version with Threads execution space the maximum throughput from a scan from 1 to 20 threads is reported. The reported uncertainty corresponds to sample standard deviation of 8 trials.

Test case	Throughput (events/s)
CPU version, 1 thread	13.5 ± 0.2
Kokkos version, Serial execution space	8.5 ± 0.2
CPU version, 40 threads	539 ± 9
Kokkos version, Threads execution space, peak (18 threads)	28 ± 1

Table 2. Comparison of the event processing throughput between the Kokkos version of the program using CUDA execution space and the original CUDA version. In all cases the CPU threads were pinned to a single CPU socket, and used one NVIDIA V100 GPU. Each test ran about 5 minutes, and the machine was free from other activity. The CUDA version can process data from multiple events concurrently using many CPU threads and CUDA streams, and uses a memory pool to amortize the cost of raw CUDA memory allocations. The maximum throughput from a scan from 1 to 20 concurrent events is reported for the CUDA version. In order to compare to the current state of the Kokkos version, the CUDA version was tested also with 1 concurrent event and disabling the use of the memory pool. The reported uncertainty corresponds to sample standard deviation of 8 trials.

Test case	Throughput (events/s)
CUDA version, peak (9 concurrent events and CPU threads)	1840 ± 20
CUDA version, 1 concurrent event	720 ± 20
CUDA version, 1 concurrent event, memory pool disabled	159 ± 1
Kokkos version, CUDA execution space	115.7 ± 0.3

239 The Kokkos version with the CUDA execution space reaches about 70 % of the through-
 240 put of the direct CUDA version when run on a single concurrent event and disabling the use
 241 of the memory pool. Profiling indicates that various overheads e.g. in the `Kokkos::View`
 242 are the main cause for the performance difference. From Table 2 it is also clear that the kind
 243 of data processing done in this application benefits greatly from a memory pool, and from
 244 processing multiple events concurrently.

245 6 Conclusions

246 We have ported the Patatrack heterogeneous pixel reconstruction code from CUDA to
 247 Kokkos. In our experience Kokkos provides an API that is at a higher level than CUDA,
 248 and would be easier to develop new algorithms by physicists that are not necessarily experts
 249 in programming. We have achieved almost full portability between CPU, CUDA, and HIP,
 250 even if work still continues to understand runtime failures of the HIP execution space version
 251 of the code. This analysis shows that Kokkos can give 70 % of native CUDA performance in
 252 a simplified setup without either a memory pool or concurrent events. If similar performance
 253 proportion can be achieved also in a more realistic setup, it may be worth using a portable
 254 framework to reduce person power in maintaining a code base despite the loss of compute
 255 performance.

256 Our impression is that Kokkos would work well for a project that compiles the code
 257 separately for each target architecture, does not rely much on shared libraries, uses CMake as
 258 the build system, and does not rely on concurrent work outside of Kokkos. CMSSW doing
 259 all these in the opposite way implies that integrating the current version of Kokkos into the
 260 current data processing model of CMSSW would be challenging to do without sacrificing
 261 application performance. It is not, however, clear to us at this time to what extent these
 262 challenges are caused by design choices in Kokkos, or by the nature of the portability problem
 263 itself.

264 More work is needed to complete the study with Kokkos. In addition, comparisons to
 265 other portability technologies are planned within the HEP-CCE.

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