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Charge-partitioning study of a wide-pitch silicon micro-strip detector with a 64-channel CMOS preamplifier array

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ABSTRACT

The wider pitch readout operation of a 50μm-pitch double-sided silicon micro-strip detector has been studied specifically concerning its ohmic side. Every second readout and ganged configuration was examined by employing a newly developed 64-channel preamplifier array. The observed charge responses for collimated IR light were compared with a numerical model.

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1. Introduction

In the KEK B-factory experiment, BELLE[1], we are going to employ a wider-pitch silicon micro-strip detector than has been so far used. As long as we employ a barrel structure with flat detector modules we must take into account the amount of signal's charge gathered per strip for a Z-measurement. A narrow-pitch detector can gather smaller signals for inclined tracks than for perpendicular tracks. In order to compromise the signal-to-noise ratio and the coordinate measurement resolution, we are studying the nature of a wide-pitch readout. A theoretical study[2] showed that a wider-pitch detector requires a wider-electrode width to maintain the analog interpolation capability, where we assumed that the electric filed is perpendicular to the detector plane over the entire silicon bulk. While we know that the concentration of the electric field towards an ohmic-side readout electrode is rather small, we expect that it still has a non-negligible effect on the charge-collection efficiency. In order to take into account the effect of the field concentration we introduced a "capture width" in the later analysis section. In order to obtain the actual response of the double-sided detector specifically for its ohmic-side we employed a newly developed small-size double-sided detector in order to emulate the wider-pitch detector, which was fabricated together with a practical-size double-sided detector[3] on the same high-resistivity silicon wafer.

The objectives of this study were three-fold: the first is to demonstrate that the 64-channel preamplifier, which is a medium-stage product for a complete 128 channel preamplifier[4] for BELLE, is beginning to actually work; the second is to examine a brand-new double-sided detector developed by SII and BELLE; the third is to obtain insight about the charge-partitioning property and the charge-collection efficiency in order to tune the numerical model for the wide-pitch design. In order to cover these major objectives, the descriptions are organized as follows: section 2 deals with the brand-new double-sided detector and the 64-channel preamplifier array together with an infra-red injection system and subsidiary instruments; section 3 provide the measured charge responses together with a numerical model

analysis; section 4 concludes the discussion.

2. Experimental procedure

2.1. Small double-sided detector

Key issues for fabrication Short-strip detectors were fabricated as part of development work of a double-sided detector. The size of the small detectors was 21.5 mm by 14.9 mm, which was fabricated together with a practical-size double-sided detector on a (100) oriented, high-resistivity silicon of 4 $k\Omega cm$ (typically). The wafer was 4 inch in diameter and 300 μm thick. Further geometrical details are listed in Table 1. In order to supply bias voltages we employed high-sheet-resistance poly-silicon for both the junction and ohmic sides. The W/L ratio of the polysilicon was determined in such a way as to eventually provide a resistance of 10 to 20 $M\Omega$. In order to integrate a coupling capacitor onto the detector, we employed an ONO-stacked insulator film[5] which has a higher break-down voltage, and a longer lifetime than that of a single-layered silicon-dioxide film. The ONO insulator film had a three-layered structure, consisting of silicon-dioxide, silicon-nitride, and again silicon-dioxide. The p^+ and n^+ strips were arranged so as to be orthogonal to each other for the junction-side and ohmic-side, respectively. The readout strips for the ohmic-side were located for each 50 μm, each of which was isolated from each other by the action of a field-plate. The field-plate was 12 μm wide and was located on a 5 μm -wide n^+ implantation. The number of readout strips was 209, each having a length of 12.9 mm. The strips were surrounded by an n^+ guard ring, which absorbed extra leakage current generated at the fringe of the detector. The bias ring was located at the end of the detector, from which the bias voltages for the n^+ strips were supplied through poly-silicon resistors. The junction-side had p^+ implantation for each 25 μm , while the readout strip was located for each 50 μm . The strips, which were not readout, took the role to provide an interpolation capability as well as to improve the uniformity of the electric field. The number of readout strips was 250 with a length of 19.5 mm. The

strips were surrounded by a p^+ guard ring as was provided for the ohmic-side. All of the p^+ strips were biased through a poly-silicon resistor connected to the bias ring. The bias ring was located at at the outer-most area, as was designed for the ohmic-side. The detectors were operated with +25 V on the ohmic-side and -25 V on the junction-side to prevent any possible insulator break-down.

Assembly for the experiment Figure 1 shows four configurations for the readout of the 50μm -pitch detector for its ohmic-side, which were:

a) Every channel readout with 50 μm ,

b) Every second readout with 100 μm ,

c) Ganing neighboring two strips for readout with an effective readout pitch of 100 μm , and

d) 200 μm readout with ganging as in *c*).

A photograph of the small detector mounted on a PCB frame is shown in Figure 2 together with the preamplifier chip.

2.2. IR illumination equipment

The detector assembly was located on an X-Y controllable table so as to be illuminated by a collimated IR light pulse. The X-Y table was part of a microscope from Olympus. We prepared two light sources: one had a wavelength of 850nm; the other was 1150nm. While 850 nm-IR penetrated into silicon bulk by 20 to 30 μm in depth, the 1150 nm-IR almost completely passed through the 300 μm silicon wafer. Before finding a side-effect of the 1150 nm-IR, we had believed that e 1150 nm-IR is more adequate than 850 nm-IR to emulate a charged-particle beam. The side effect came from a reflection of IR from an aluminum strip located at the far side. When moving the stage along the p^+ strip, we found a clear structure of the ohmic-side aluminum in the signal's response, which heavily distorted the charge-sharing characteristics between the adjacent strips. For this reason we chose to employ 850 nm-IR for this study.

The IR light was guided to a microscope via a single-mode fiber. A collimator lens located instead of the eye-adaptor lens squeezed the IR so as to be almost parallel to the optical axis of the microscope. The parallel beam was focussed again by a low-magnification object lens before making a spot on a detector surface. The size of the spot was determined by employing shadowing by a 10 μm-aluminum trace on the detector. Assuming that the IR spot was disk-shaped and the light power was equally distributed over the disk, we could determine the disk size by taking the minimum-to-maximum ratio of the detector response for the IR. The radius of the IR spot was eventually measure to be 11.5 ± 0.5 μm. We should keep it in mind that there might have existed some long-tail spread for the actual lateral profile of the IR spot. Table 2 summarizes the parameters for the IR exposure system.

2.3. 64-CHANNEL PREAMPLIFIER CHIP AND ITS OPERATION

We have recently successfully fabricated a 64-channel CMOS amplifier array as an intermediate step towards the complete design of a 128-channel preamplifier for the B-factory experiment. Taking the code name of the VLSI design project, we call the 64 channel preamplifier $SMA^2SH-64A$. A microphotograph of the $SMA^2SH-64A$ chip is shown in Figure 3. Table 3 summarizes its major parameters. Since the complete circuit was described for a single-channel prototype,[6] we skip many details of the circuit design. The fabrication technology was a 1.2 μm N-well CMOS with double-poly and double-metal capability. An exact circuit schematic for the preamplifier stage appears elsewhere.[7] Since the layout pitch of the 64-channel amplifier was 100 μm, it was quite adequate to accomodate the wide-pitch detector. $SMA^2SH-64A$'s were located on each side of the detector to be controlled in a cascaded fashion. The input pattern for digital signal, i.e. CK, CKB, RESET, REQ, and CSIN, were prepared with a HP16500B logic analyzer/pattern generator. CK and CKB were complementary clock signals to synchronously proceed an analog capture sequence. While the nominal clock frequency was 2 MHz, we employed a clock frequency of 1 MHz for the convenience

of the pattern generator. RESET was used to reset a built-in control circuit of $SMA^2SH-64A$ as well as to restore the base line of the analog circuit. RESET was also fed into an HP8082A pulse generator in order to provide a drive pulse for the LED driver. The timing and width of the drive pule were adjusted in such a way that the IR pulse was injected in the analog capture window. The detector needed to be shone in the -7 to -4 μs range before being triggered for readout. The readout sequence could be asynchronous. During the readout CK and CKB paused to toggle. CSIN moved the circuit from the analog capture mode to the readout mode. The preamplifier circuit responded to REQ with a low-asserting signal ACKB, which was associated with two analogs, OUT1 and OUT2. The readout sequence proceeded from the ohmic side to the junction side. Once the ohmic side was completely readout, CSOUT was cascaded to CSIN for the junction side. OUT1 and OUT2 were "after", and "before" base-lines of the amplifier, respectively. The voltage differences between the two provided a net amplitude for an in-coming charge. The signal's scale was typically 200 mV per 4 fC. The output analogs, i.e. OUT1, and OUT2, were observed with a Tek 11403A digitizing oscilloscope. In order to take a difference between OUT1 and OUT2 we employed a differential amplifier plug-in (11A33). As for a trigger source of the oscilloscope we employed a CSOUT from the ohmic-side or ACKB, as appropriate to observe the readout analogs. Schematic diagrams for the readout instruments are shown in Figure 4.

3. Response for a wide-pitch silicon-strip detector

3.1. CHARGE COLLECTION EFFICIENCY

Moving the X-Y stage along the p^+ strips and shining IR from the junction side, we observed the response for a specific readout channel on the ohmic side. The amount of IR power was monitored in terms of the sum for the clustered signals on the junction side. The charge-collection efficiency was defined as the ratio of the ohmic-side signal to the cluster-sum for the junction side. The integrated signals

over the cluster were 30000 to 50000 electrons. Figure 5 shows the measured data together with some implication from a numerical charge-sharing model. The charge-sharing model employed was just a minor modification of that in ref. 2. The parameters employed for the model analysis are listed in Table 4. As a convenience for discussion, we start from a description of the 100 μm detector (type b)). The origin of the coordinate of Figure 5 b) is taken at the center of the readout strip. The data shows a smooth curve, starting from 80% at 0 μm and arriving at 5% at 100 μm with a kink at 50 μm. In the original charge-sharing model, the kink (or flat region) appearing around 50 μm was larger than the measurement. During the analysis procedure, we noticed that the original charge-sharing model had an assumption that the electric field was perpendicular to the detector plane all over the area. In order to relax this assumption we have introduced a "capture width" (CW). The actual procedure was to enlarge the weighting field region assigned for the readout electrode width (W). We tried three values for CW (50, 60, and 70 μm). It appeared that the qualitative nature was well reproduced for $CW = 60\ \mu m$. An apparent discrepancy around 0 μm region was due to a finite impedance of the n^- surface, which provided a charge leakage path for the induced signal. Besides the deficit at 0 μm, there existed some excess beyond 50 μm, which indicated that the deficit signals were shared again over a larger number of readout strips. The response for the ganged structure (Figure 5 c))could be reproduced with a superposition for the 50 μm pitch readout (Figure 5 a)). The solid line appearing in Figure 5 c) is just a superposition of the solid line in Figure 5 a) with a 50 μm skew. Since the charge-capture width was restricted by the readout pitch, we employed a value of 50 μm for CW instead of 60 μm. The origin of the coordinate for Figure 5 c) was located at the mid-point between the ganged strips, while for Figure 5 a) the origin was taken as usual at the center of the readout strip. The agreement between the data points and the numerical model is again very reasonable when we taking into account the effect of the finite impedance of the n^- surface.

3.2. Towards wider-pitch readout

By employing the ganged structure in Figure 5 c) we examined a 200 μm readout. As shown in Figure 5 d), the coverage of the weighting field for the ganged electrode was still not sufficient to keep a good charge-collection efficiency over the entire inter-readout region. There might have been some practical solutions for keeping the efficiency, including a lateral drift field to supplement the action of the weighting field. The way to gang more electrodes is not adequate, because of an increase in the detector capacitance, and an increase in the defects of the integrated capacitor. We chose to find a solution in between the wide-p-stop detector and the complete field-plate device. In the wide-p-stop detector the drifting carrier never reaches the ohmic-side edge, except for the readout electrode, because of the repelling force of the p-stop implantation, and is attracted by a very weak lateral field until being captured by the readout electrode. The wide-p-stop detector has a reverse-field region over the p-stop implantation region, which extends to 20 to 25 μm in depth, which might respond to the inclined charged tracks in an improper way, thus distorting the coordinate measurement.

4. Summary

We have confirmed that two brand-new materials, a 64-channel preamplifier and a double-sided-detector with an ONO insulator film, worked together to provide information concerning the charge- partitioning nature of a wide-pitch readout. The global nature of the wide-pitch readout of the existing 50 μm pitch detector was well characterized by introducing a charge-capture width. The lateral spread of the measured charge-collection efficiency was wider than the expected value based on a numerical model; we can thus understand the reason why the peak charge efficiency was smaller than the expected value in a consistent manner. This was possibly due to an insufficient resistivity of the n^- inter-readout-strip region, which mediated the charge so as to spread over the entire detector surface. If this interpretation is plausible for the wide-pitch detector (wider than 100 μm),

we should provide some structures/mechanisms to keep the impedance of the n^- surface high, or to guide the drifting carriers in the lateral direction. Even if the weighting field at the intermediate region might be small, it does not matter if there exits some guiding field to attract the carries to the readout electrode. A wide p-stop design in between the readout electrode is nearest to the case with some penalty of the position-interpolation capability and possible induction of a reverse-polarity signal around the p-stop surface. A compromised design is being searched for to separate the p-stop implantation in a few parts.

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This work was part of a developmental effort to build a silicon vertex detector for the BELLE collaboration. The directors of the physics department of KEK (S. Iwata, F. Takasaki, and M. Kobayashi) and T. Takahata, president of Seiko EG&G, are acknowledged for their encouragement during the work.

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TABLE CAPTIONS

1: Parameters of the small double-sided detector

2: Parameters for the IR exposure system

3: Parameters for $SMA^2SH - 64A$

4: Parameters for the numerical charge-sharing model

Table 1. Parameters of the small double-sided detector

Size of the detector	21.5 mm by 14.9 mm
Number of strips	250 for junction side 209 for Ohmic side
Strip length	19.5 mm for junction side 12.9 mm for ohmic side
Strip pitch (diffusion)	25 μm for junction side 50 μm for ohmic side
Strip pitch (readout)	50 μm
Strip width (diffusion)	5 μm
Strip width (aluminum)	10 μm for junction side 24 μm for ohmic side
Field plate	16 μm for ohmic side
Integrated capacitor Top oxide Nitride Bottom oxide	ONO less than 1 nm 150±20 nm 42±2 nm
Bias resistor Sheet resistivity Resistivity	Poly-silicon 100 $k\Omega$ /square 20 $M\Omega$
Wafer Bulk resistivity Surface orientation Thickness Diameter	Double-sided mirror-finished silicon wafer 4-8 $k\Omega cm$ (100) $300 \pm 15 \mu m$ 4 inch

Table 2. Parameters of the IR exposure system

Wave length	850 nm (FED085K3WD, Fujitsu) 1150 nm (FED115K1WB, Fujitsu)
Output power	85 μW max. (850 nm) 26 μW max. (1150 nm)
t_r and t_f	10 ns (typ)
Optical Fiber	10/125 (Fujikura)
Microscope	STM5-311 (Olympus)
Magnification of the object lens	3
Spot size	11.5 $\pm$ 0.5 μm (radius)
Accuracy of the stage	0.5 μm (step for increment) $\pm$ 2.5 μm (back-rash)
Stroke of the stage	5 cm for x and y

Table 3. Parameters of the 64-channel preamplifier chip

Number of channels	64
Die size	8.7 mm by 3.2 mm
Amplifier pitch	100 μm
Preamplifier configuration	Cascode with drain output
Feed back capacitor	0.2 pF
W/L of the input FET	1260/2 in μm
Drain current for input FET	160 μA (Typical)
Transconductance for input FET	2.5 mS (Typical)
Noise level	1000 e's at 20pF (tentative)
Input protection	nMOS off-transistor
Output signal	200 mV per 4 fC with internal gain
Sampling	8-stage analog pipe-line (2 MHz)
Noise filtering	Quadruple-correlated noise filter
Output control	No sparsification No prompt hit output

Table 4. Parameters for the numerical charge sharing model

Cut-off parameter	l_c	200 μm
Gap	s	4 μm
Diffusion length	σ	10 μm
Electrode width	w	10 μm
IR spot radius	-	11.5 μm

FIGURE CAPTIONS

1) Configurations for readout
   a) Every channel readout with 50 μm
   b) Every second readout with 100 μm
   c) Ganing neighboring two strips for readout with an effective readout pitch of 100 μm , and
   d) 200 μm readout with ganging as in c)

2) Small detector assembly

3) Microphotograph of the $SMA^2SH - 64A$ chip

4) Schematic diagram for the readout instruments

5) Charge-collection efficiency for ohmic-side readout
   a) Every channel readout with 50 μm .
   b) Every second readout with 100 μm
   c) Ganging neighboring two strips with an effective readout pitch of 100 μm
   d) 200 μm readout with a ganging structure as in c)
   The open circles are data from the measurement. The error-bar shows the typical expected measurement error. The lines in the figure come from a numerical charge-sharing model.

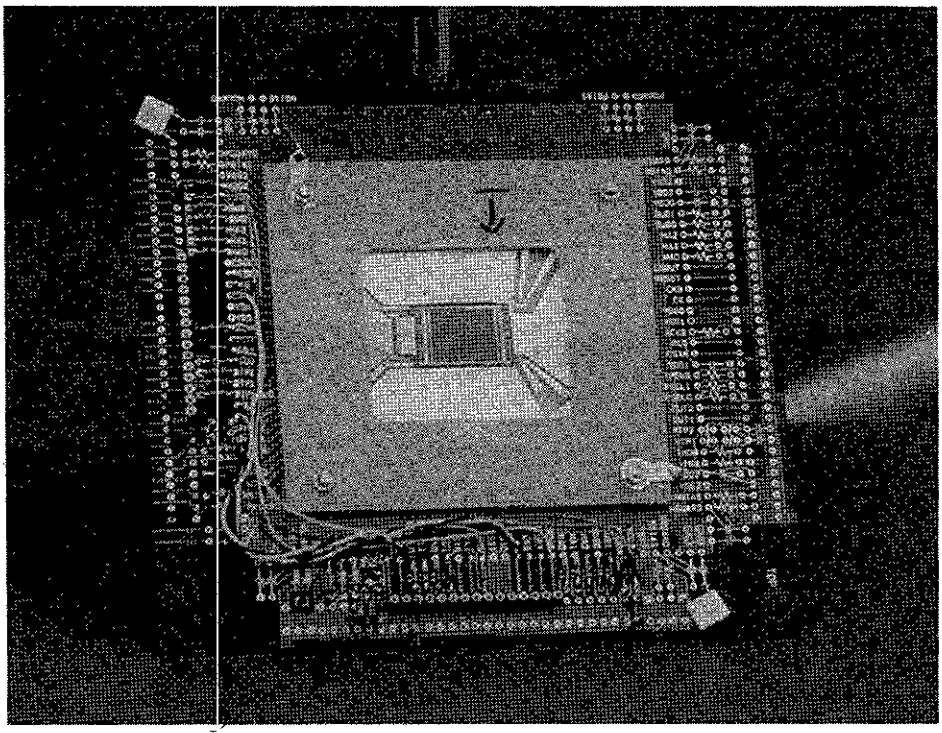

FIGURE 2 : Small detector assembly

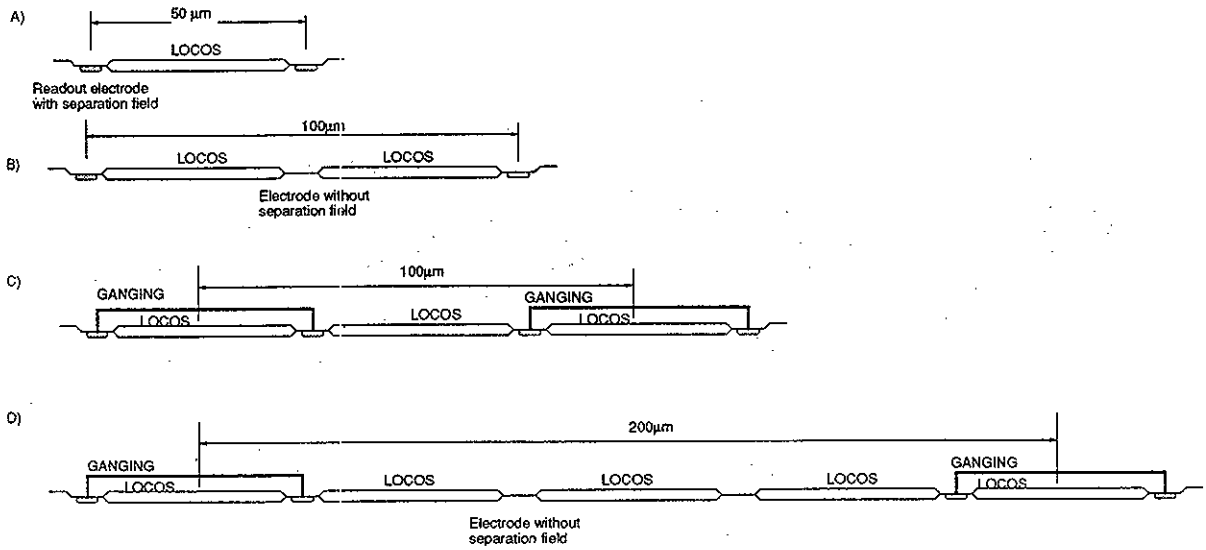

FIGURE 1

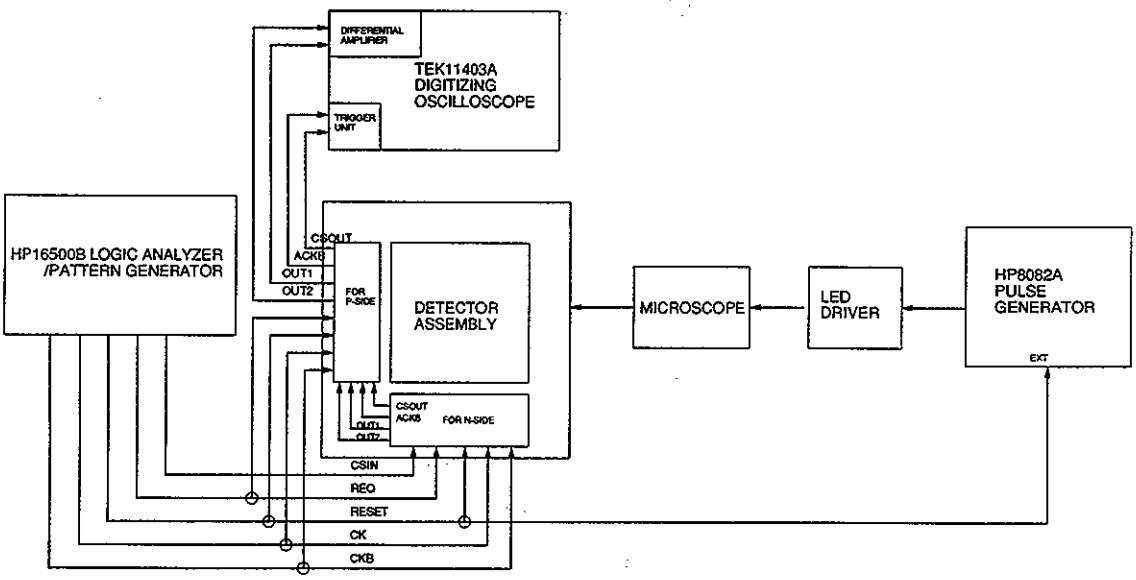

FIGURE 4

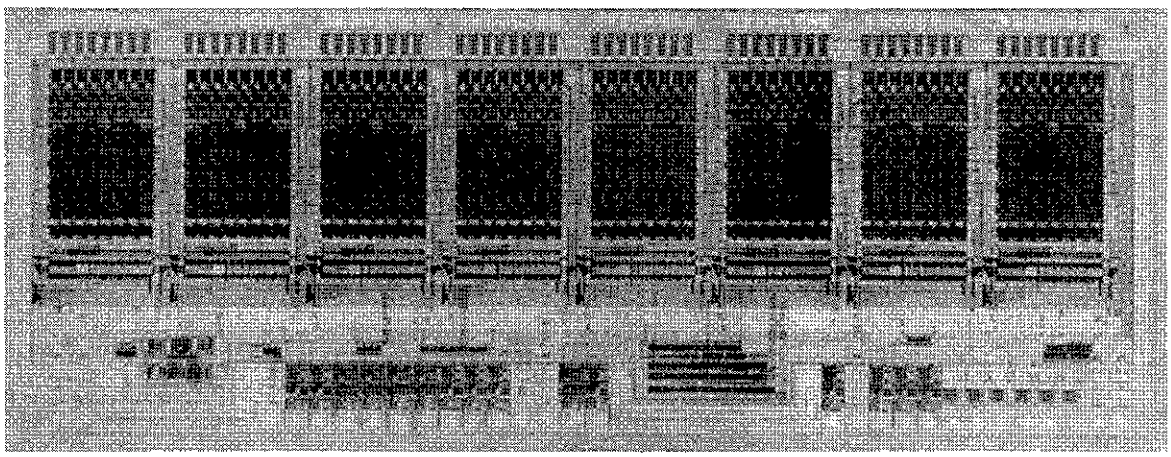

FIGURE 3: Microphotograph of the SMA^{2}SH-64A chip

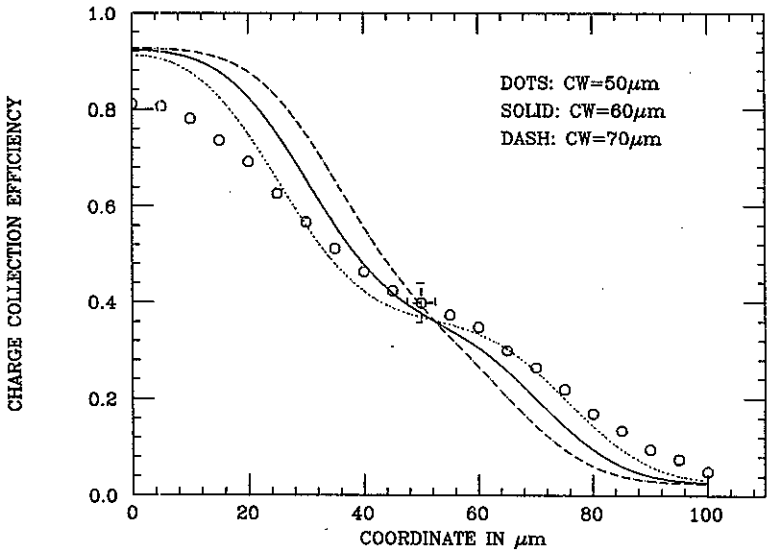

FIGURE 5 B)

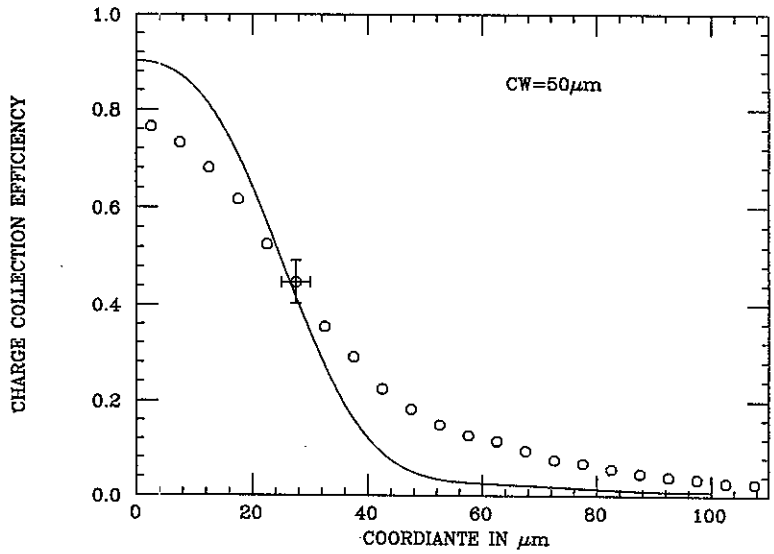

FIGURE 5 A)

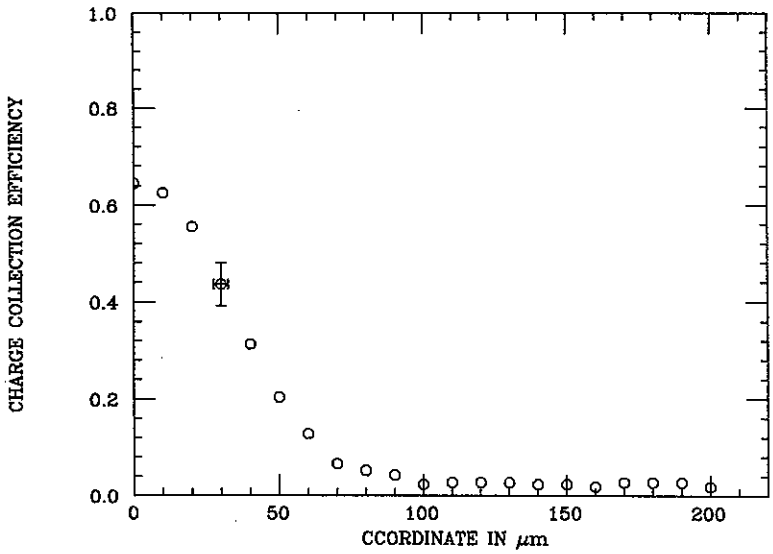

FIGURE 5 D)

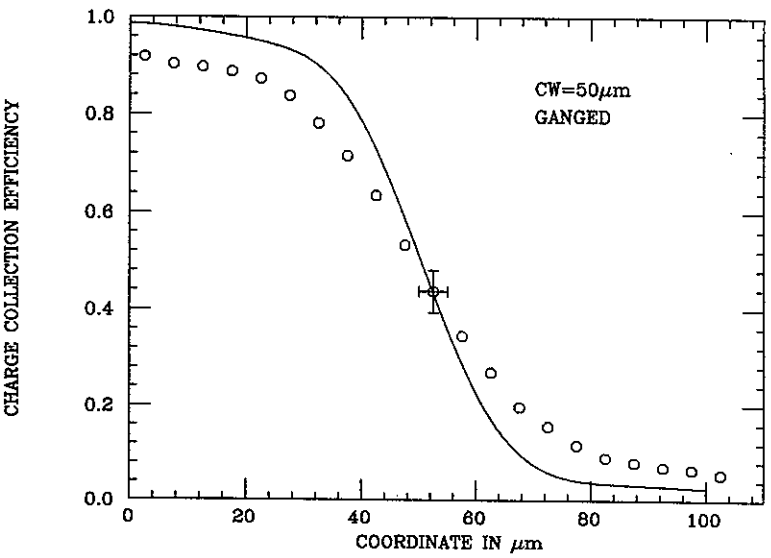

FIGURE 5 C)