Self Directed Channel Memristors

Rev. 3.2, October 6, 2019

Taxonomy

The Knowm Self Directed Channel (SDC) Memristor material stack is metal ion-conducting device often referred to as an electrochemical metallization cell (ECM) which relies on Ag+ movement into channels within the active layer to change the device resistance. A metal-catalyzed reaction within the device active layer generates permanent conductive channels that contain Ag agglomeration sites. The amount of Ag within the channel determines the resistance of the device. **SDC memristors are distinct from (and superior to) Conductive Bridge RAM (CBRAM) technology and represent their own class of memristor.** For more information on the distinction, please see the open-access paper "Self Directed channel memristor for high temperature operation" by Dr. Kristy A. Campbell.

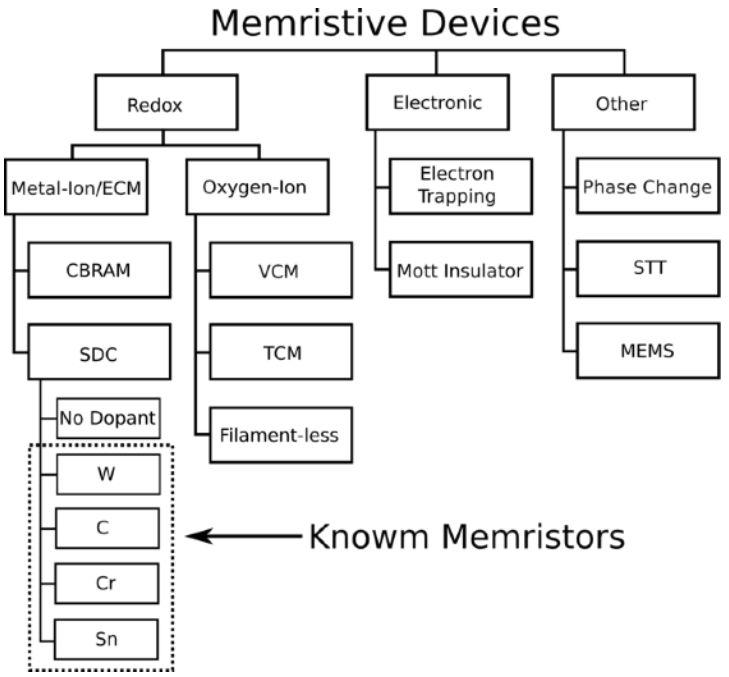
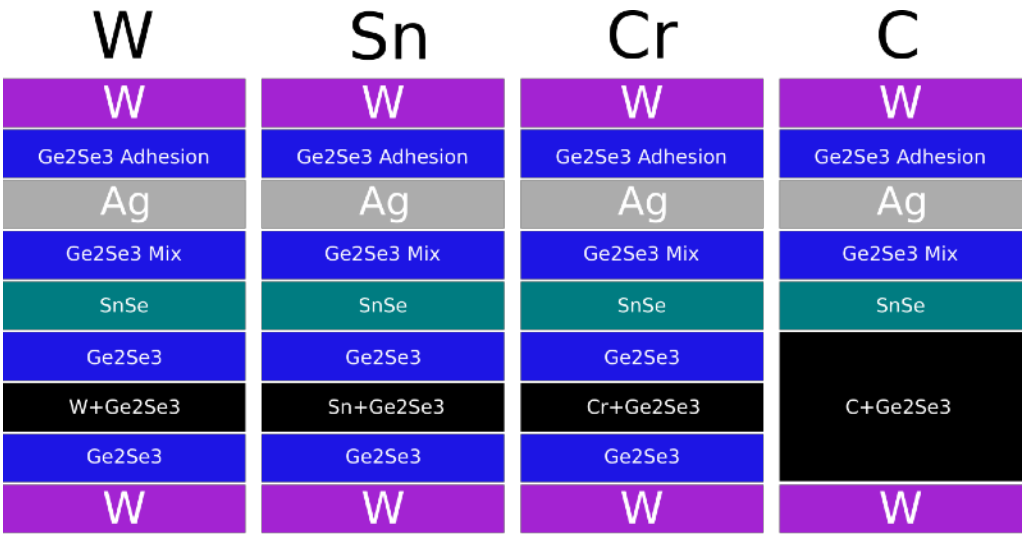


FIGURE 1: TAXONOMY OF MEMRISTORS

Physical Mechanisms

SDC devices are initially in a high resistance state (MΩ–GΩ range) following fabrication. The first time a device is operated after fabrication the device self-directed channel is formed during application of a positive potential to the top electrode. The potential required for this operation is the same as required during normal device operation. This first operation generates Sn ions from the SnSe layer and forces them into the active Ge_2Se_3 layer.

Theory predicts that these Sn ions facilitate the incorporation of Ag into the active layer at the



Ge-Ge bonding sites. This occurs through an energetically favorable process in which the

FIGURE 2: SDC MATERIAL STACK. DOPANTS (W,SN,CR,C) ARE ADDED TO ENHANCE AND OPTIMIZE DEVICE PROPERTIES.

electrons entering the active layer from the negative bottom electrode, concurrently with the formation of Sn ions from the SnSe layer, enable formation of a pair of self-trapped electrons in the Ge_2Se_3 active layer strongly localized around the Ge-Ge dimers present in this Ge-rich glass. The result of this is that Sn ions facilitate an energetically favorable reaction of Ag substitution for Ge on the Ge-Ge bond. During this reaction, the glass network is distorted, creating an ‘opening’ near the Ge-Ge sites. The open regions provide good access for Ag+ to the Ag-Ge site and become natural ‘conductive channels’ within the active layer for the movement of Ag+ during device operation. This self-directed channel is a result of the natural glass structure and follows the location of the initial Ge-Ge dimers within the glass. Since Ag has a tendency to agglomerate with other Ag atoms, these sites may encourage Ag agglomeration within the glass. Thus, device resistance changes by adding or removing Ag from the agglomeration sites within this in-situ generated pathway. It is expected that conduction could occur between clusters of Ag agglomeration sites. This pathway does not therefore have to consist of conductive metallic filaments spanning the two electrodes, as in the CBRAM device. It is simply a channel that has varying concentrations of Ag within it at these Ag agglomeration sites. The concentration of Ag at a given agglomeration site, and the distance between agglomeration sites dictates the device resistance. The resistance is tunable in the lower and higher directions by movement of Ag onto or away from these agglomeration sites through application of either a positive or negative potential, respectively, across the device.

Knowm Memristors currently come in four variants: W, C, Sn and Cr, which refers to the ‘dopant’ introduced in the active layer during fabrication. Each dopant results in modification to the memristors switching characteristics.

Critical Notes / Warnings

- **Static Sensitive**—Please use accepted methods for handling static-sensitive devices including anti-static packaging, work-surfaces, wrist straps, etc. Devices may be irreversibly damaged if ESD precautions are not observed.
- **Do not measure memristor resistance with a multi-meter.** Due to high open-circuit voltages, multi-meters can damage the devices.
- **Limit Device Current**—Set a compliance current or use series resistance. A forward applied voltage without current limiting will cause devices to enter a very low-resistance state and consequently burn out.
- **Limit Applied Voltage**—Formed devices typically change resistance between 0.1 and 0.75 Volts and are intended to be normally operated under 1V. High voltages may induce damage, especially if current is not limited.

Device Forming

The shipped raw die devices have not been formed. Packaged die may not have been completely formed when delivered, as only enough sinusoidal voltage was applied for quality control to make sure the internal wire bonding was successful. Forming entails applying a gradually increasing voltage, while limiting current, until the necessary conductive pathways have formed. Forming voltages do not need to exceed normal operating voltages.

Phase-Change Response

When exposed to high voltages and currents, the W memristors can be put into a state that consists of a combination of ion conduction and phase-change. The hysteresis and incremental response will vary depending on which mode the memristor is currently in. Phase-change operation can only occur after the device has previously been operated at least once in the ion conduction mode because there is a permanent material change in the active layers that occurs upon ion conduction. Typical phase-change device melt-quench operating procedures should be used to increase resistance when in this mode. Additionally, this mode allows single polarity operation, if desired. To get the device out of phase-change mode apply a short, higher voltage, melt and quench pulse. The device can switch polarity in the ion conducting mode when the operational mode goes from phase-change back to ion conduction. This means that the voltage polarities needed at the electrodes in order to increase the resistance are opposite from what they were initially. The ion conduction polarity switch occurs especially if the phase change operation applied a positive potential pulse to the device top electrode. In this case, the ion-conducting mode will operate as if the excess silver layer has moved towards the original bottom electrode. Application of pulses or a DC sweep to drive the silver back towards the top electrode will return the device to its original operating polarity.

Symbol and Polarity Conventions

This symbol is used internally at Knowm as it is easier to draw by hand and more accurately represents a defining characteristic of a memristor. As Leon Chua, the theoretical inventor of the memristor, has said: “If it's pinched its a memristor”.

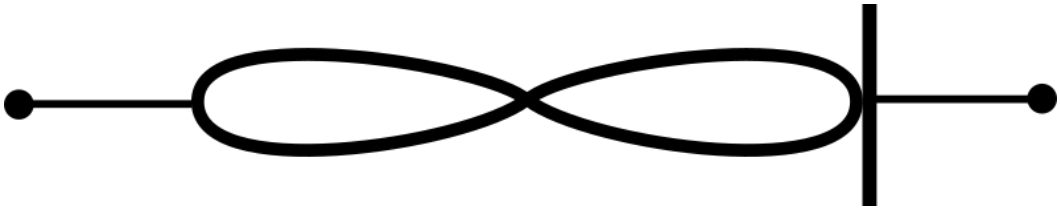


FIGURE 3: KNOWM MEMRISTOR SYMBOL

A voltage applied across the device (forward voltage) with the lower-potential end on the side of the bar, will drive the device into a high conductance state, while a reverse voltage will drive the device into a less conductive state. The bar signifies the electrode adjacent to the active chalcogenide layers. In the pristine device, this is the layer furthest away from the original Ag layer. We believe the natural direction for conductance change in a memristor should defined as increasing, as this is how most adaptive dissipative systems in Nature evolve over time. By convention, a bar signifies the lower potential end in other devices like diodes. Furthermore, from an electro-chemistry merged with a semiconductor devices perspective, we believe having the bar on the 'cathode' makes the most since this is where reduction occurs. Note that this is opposite to the typical memristor symbol polarity convention.

Knowm Memristor Symbol Download Files

PNG	http://knowm.org/wp-content/uploads/Memristor_Symbol_Knowm_400.png
PNG	http://knowm.org/wp-content/uploads/Memristor_Symbol_Knowm_200.png
PNG	http://knowm.org/wp-content/uploads/Memristor_Symbol_Knowm_100.png
PNG	http://knowm.org/wp-content/uploads/Memristor_Symbol_Knowm_64.png
SVG	http://knowm.org/downloads/Memristor_Symbol_Knowm.svg

Maximum Ratings

Characteristic (@T = 25°C)	Value
Max Forward Voltage	3 V
Max Reverse Voltage	-5 V
Max Current (W, Cr, Sn) , see note 1	1 mA
Max Current (C)	.05 mA

Note 1: High Resistant State (HRS) will be irreversible reduced from 1MΩ to 100kΩ or less if operated at these currents, see Figure 4. High voltages and currents can lead to a phase-change response, see "Phase-Change Response" in Critical Notes section.

NOMINAL ELECTRICAL CHARACTERISTICS

W, Sn, C Types

Characteristic	Condition	Min	Typ	Max
Forward Threshold	DC / Quasi-static	.15V	.26V	.35V
Reverse Threshold	DC / Quasi-static	-0.27V	-0.11V	-0.05V
Cycle Endurance	1.5Vpp, 500Hz sine wave, 50kΩ series resistor	50M	100M	5B

Cr Type

Characteristic	Condition	Min	Typ	Max
Forward Threshold	DC / Quasi-static	0.22V	0.33V	0.56V
Reverse Threshold	DC / Quasi-static	-0.66V	-0.19V	-0.04V
Cycle Endurance	1.5Vpp, 500Hz sine wave, 50kΩ series resistor	1M	50M	100M

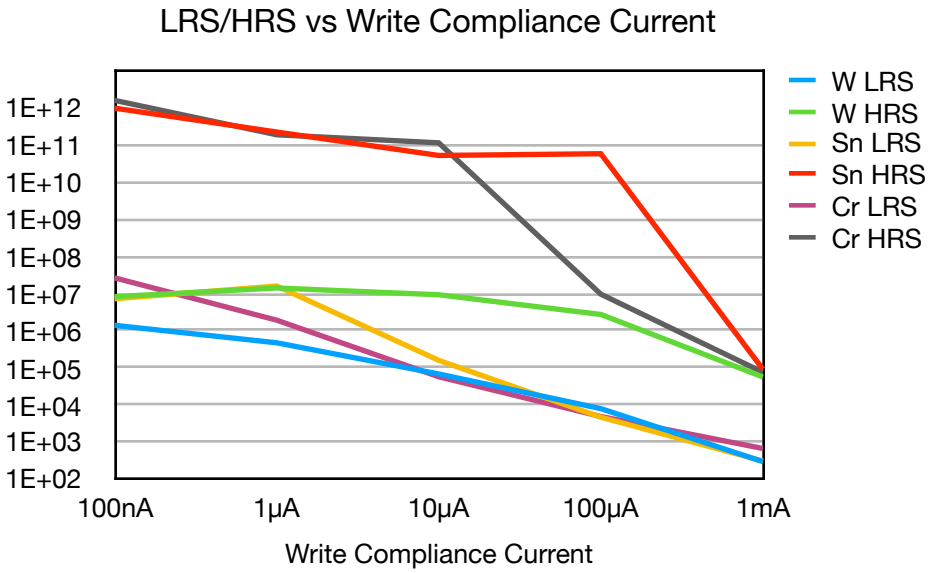


FIGURE 4: NOMINAL LOW RESISTANT STATE (LRS) AND HIGH RESISTANT STATE (HRS) VERSUS WRITE COMPLIANCE CURRENT.

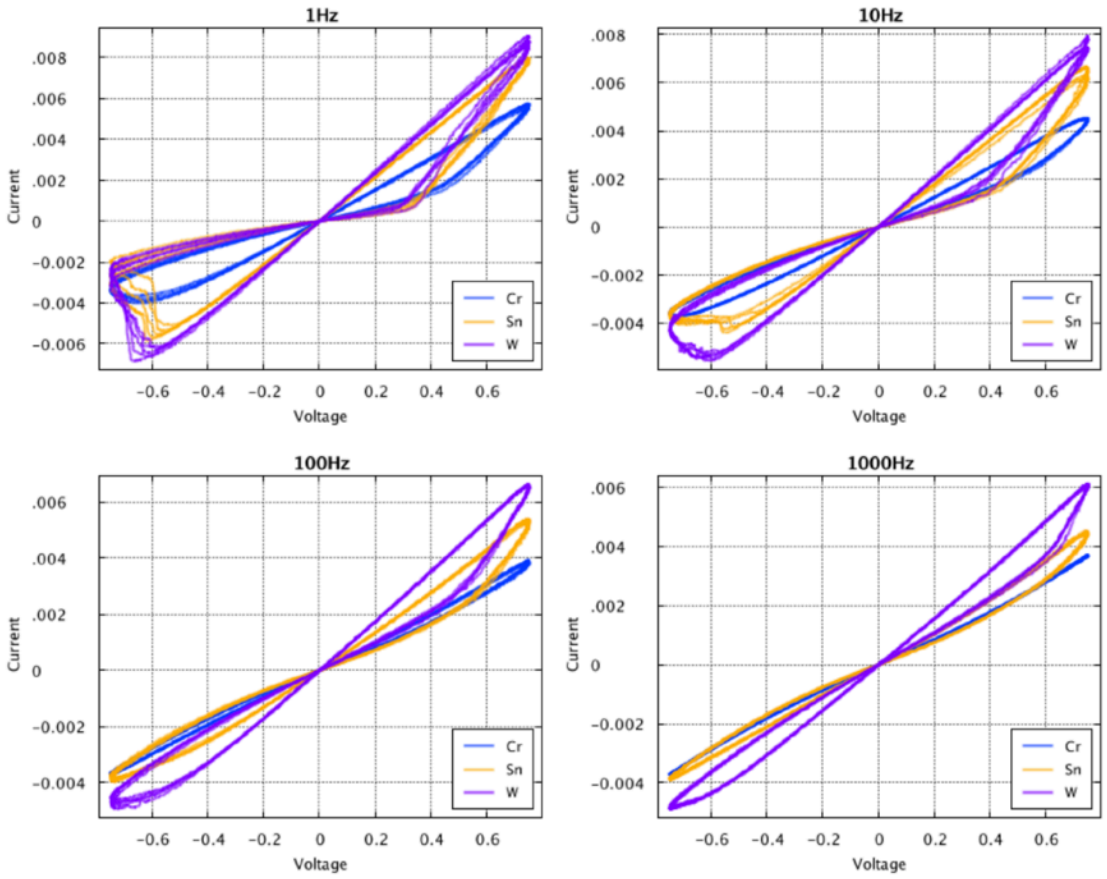


FIGURE 5: HYSTERESIS FREQUENCY RESPONSE FOR CR, W AND SN DEVICES.

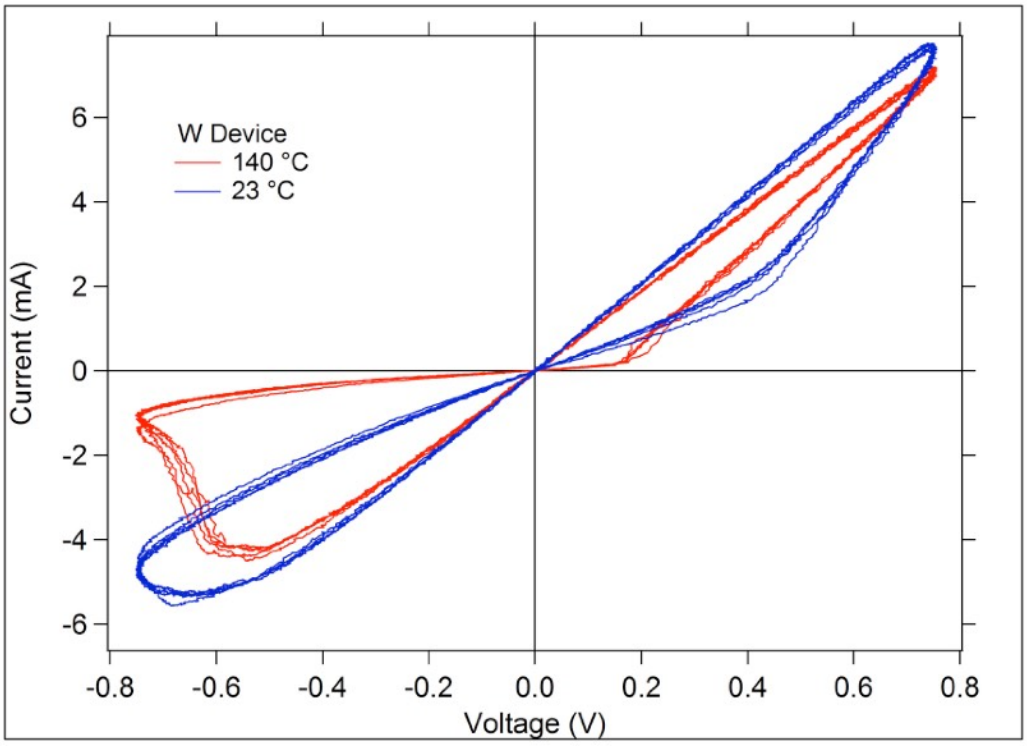


FIGURE 6: W DEVICE TEMPERATURE RESPONSE. NOTE THAT FORWARD THRESHOLDS REDUCE AS TEMPERATURE INCREASES.

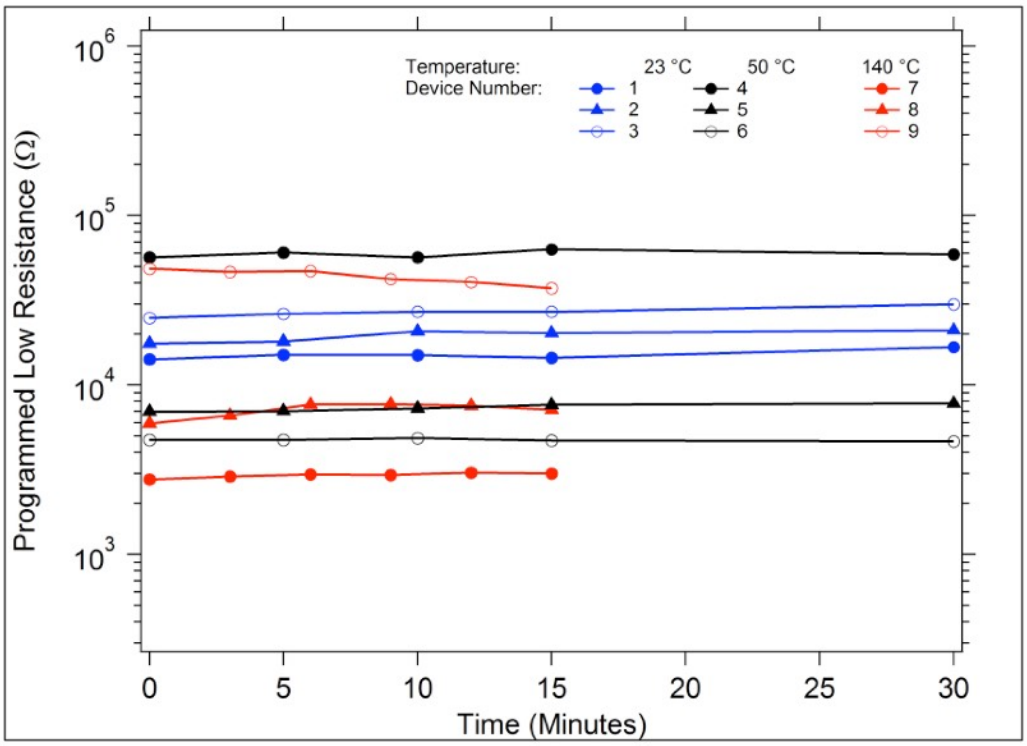
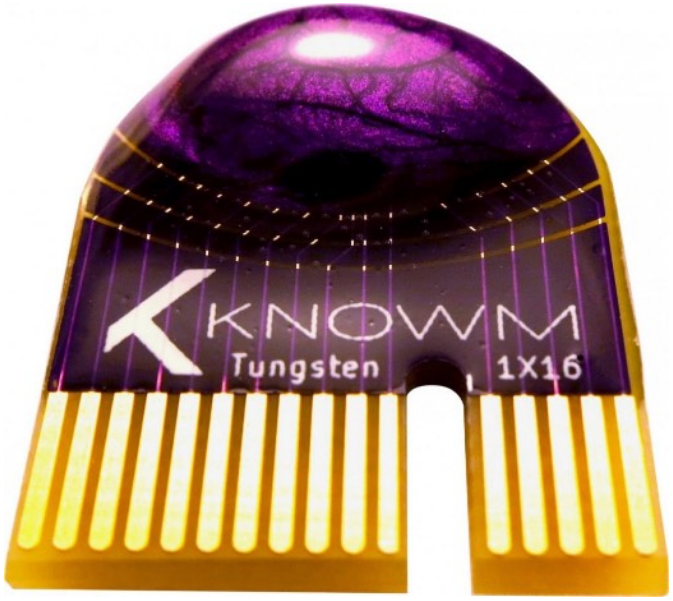
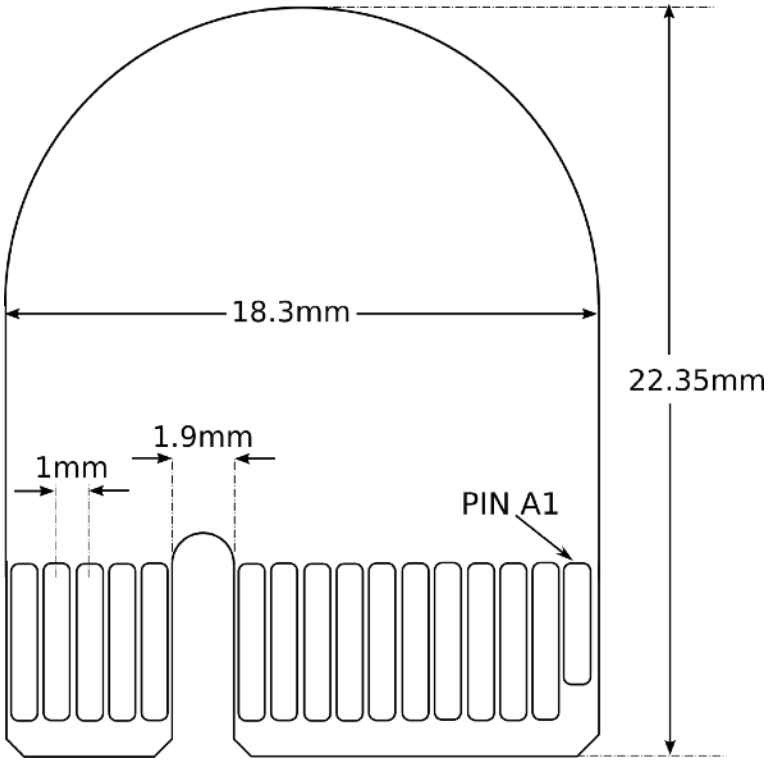


FIGURE 7: W DEVICE STATE RETENTION AND TEMPERATURE RESPONSE.

Packages

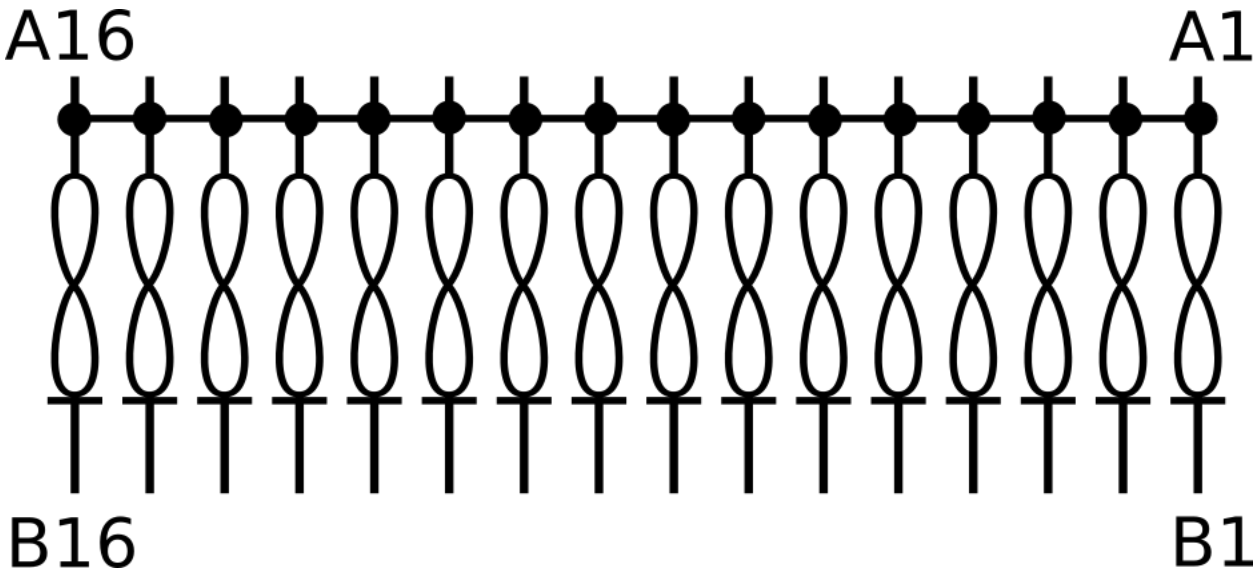
32 Pin Encapsulated Edge Board



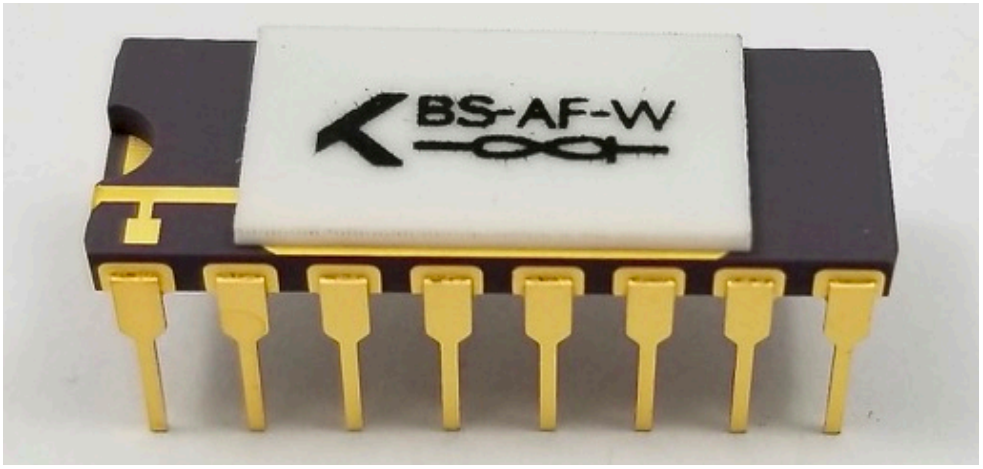


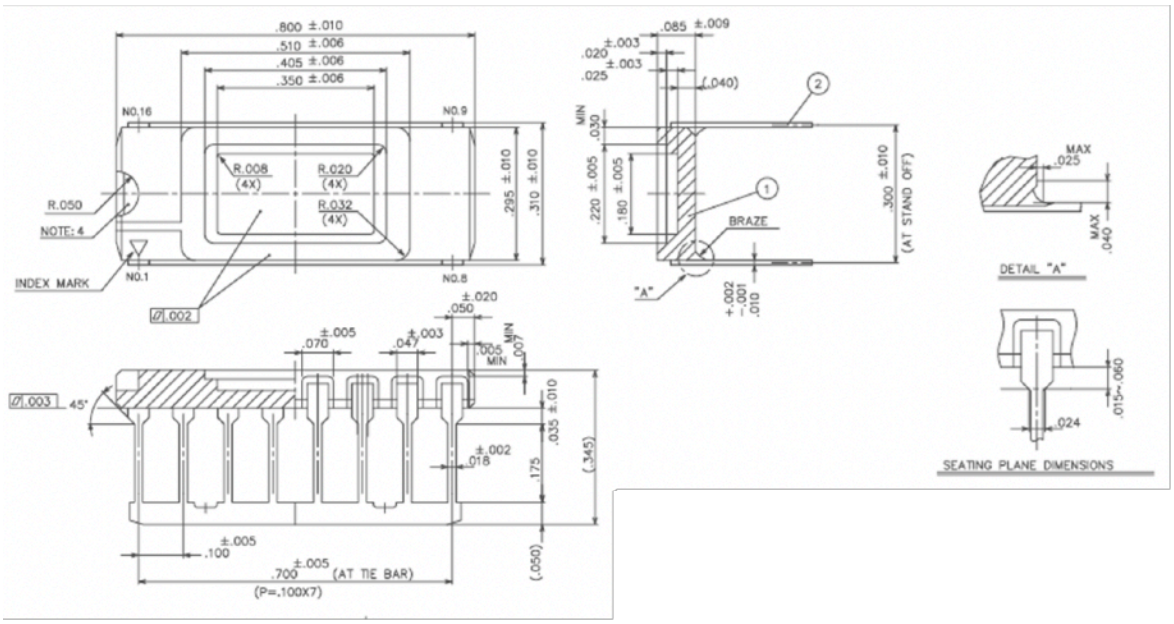
32 Pin Encapsulated Edge Board Pinouts

1X16 Linear Array Pinout

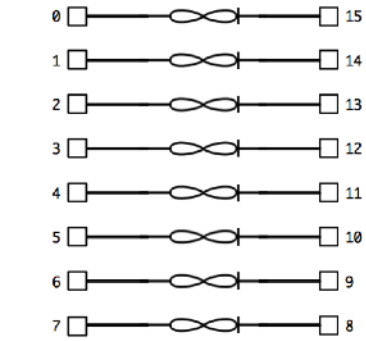
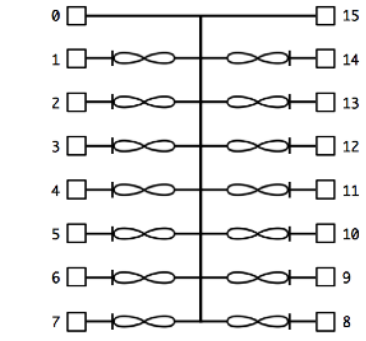


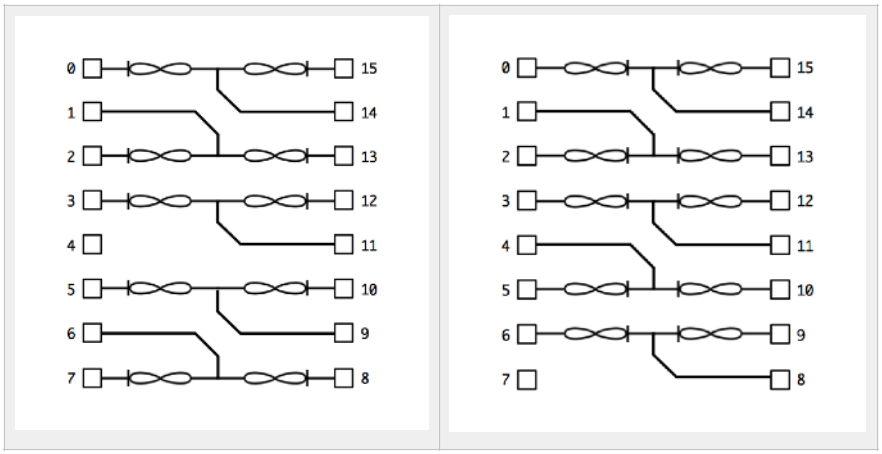
16 Pin Ceramic DIP



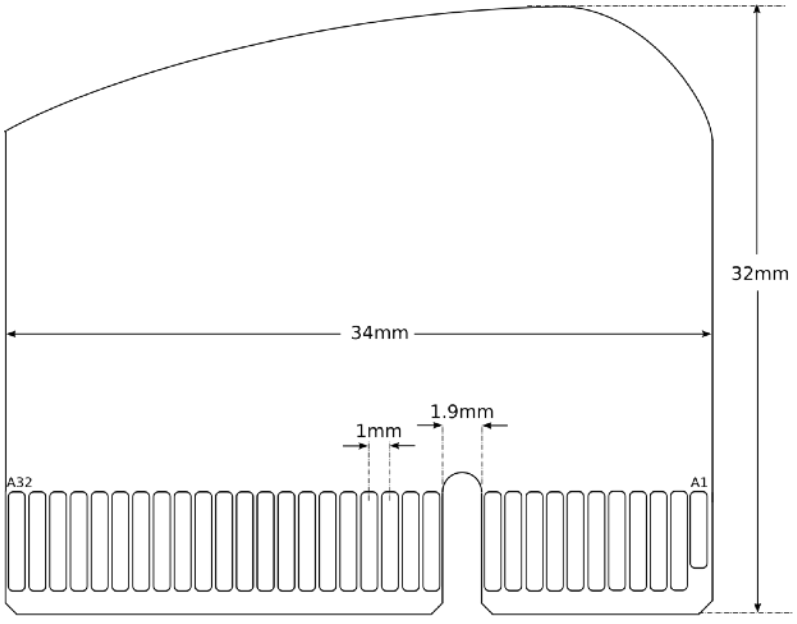


16 DIP Chip Pinouts

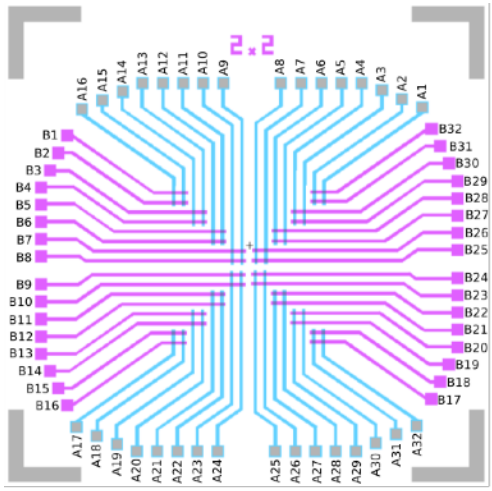
Discrete	1-2 AHaH Node
	
1-2 Synapse	**1-2i Synapse**

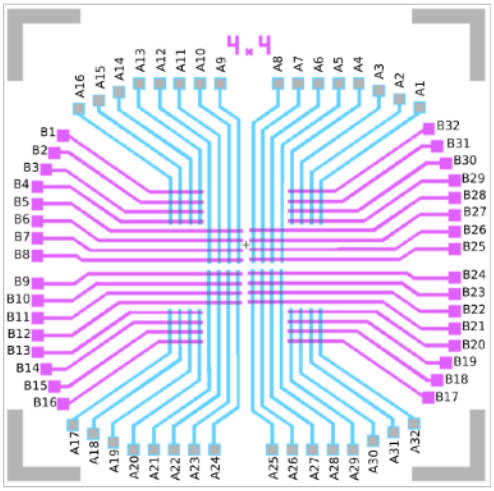

0
1
2
3
4
5
6
7
15
14
13
12
11
10
9
8
0
1
2
3
4
5
6
7
15
14
13
12
11
10
9
8

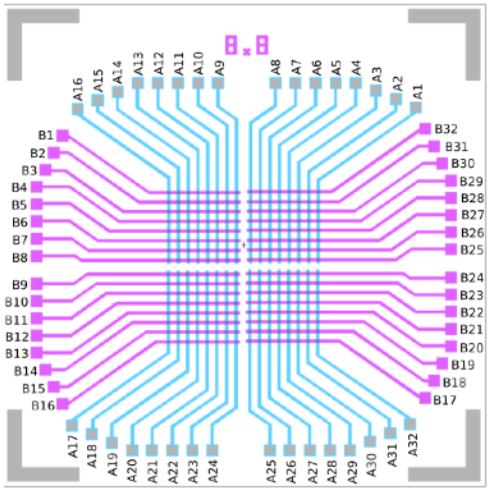
64 Pin Encapsulated Edge Board

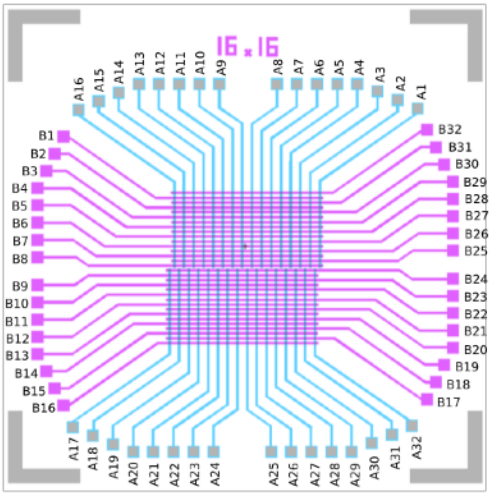


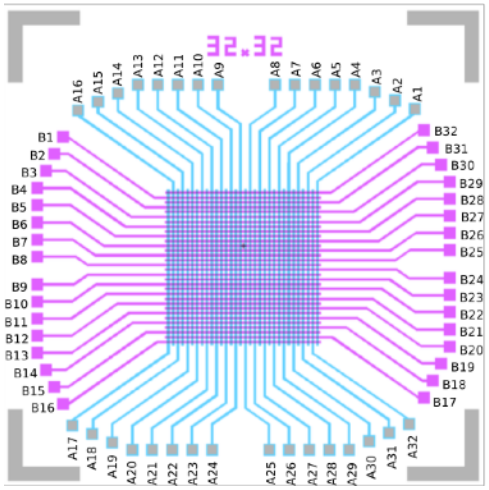
64 Pin Encapsulated Pinouts

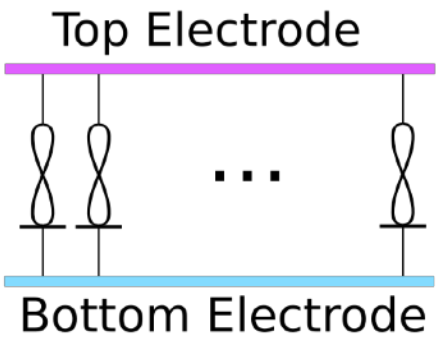












Research Probe Die

The die are 7860 µm by 5760 µm and consists of 9 columns of devices, each corresponding to a different device size. The size is listed at the bottom of each column. Each column contains 20 rows of each device size per column, for a total of 180 devices. The row number is listed at the left of each row. The top row, not numbered, is a metal continuity row that is used as a diagnostic tool for checking probe station functionality. There are no devices in this row. Instead the row consists of two shorted top electrode bond pads and two shorted bottom electrode bond pads above each column.

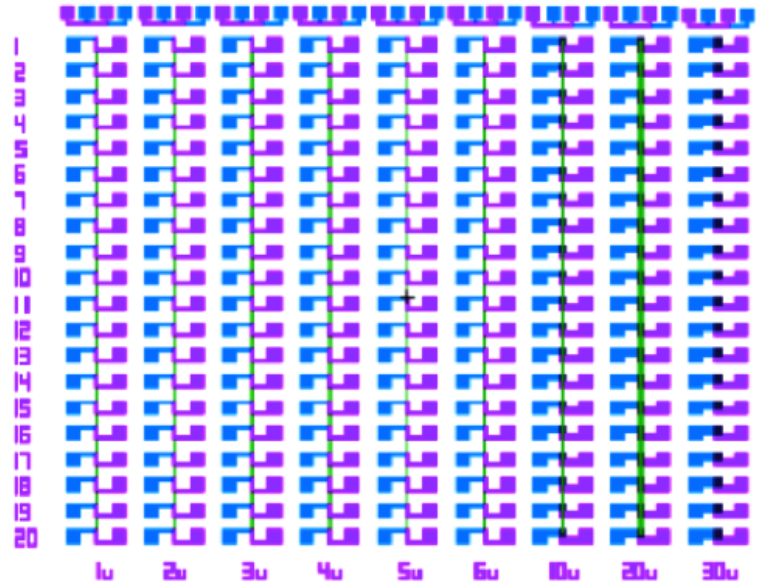


FIGURE 8: RESEARCH PROBE DIE MASK.

The top and bottom electrodes for each device are denoted by the purple and blue squares, respectively.

The device via confines the device material between the top and bottom electrodes and defines the size of the device. The device via is located at the intersection of the top and bottom electrodes. This is the region where the top electrode metal and bottom electrode metal intersect. The device sizes included in the research die are 1µm, 2µm, 3µm, 4µm, 5µm, 6µm, 10µm, 20µm, and 30µm and refer to the dimension of the device via. For devices of size 6 µm or less, the device via is round and the size refers to the nominal via diameter. For devices of sizes 10 µm, 20 µm, and 30 µm, the device via shape is square and the size corresponds to the nominal length of a side.

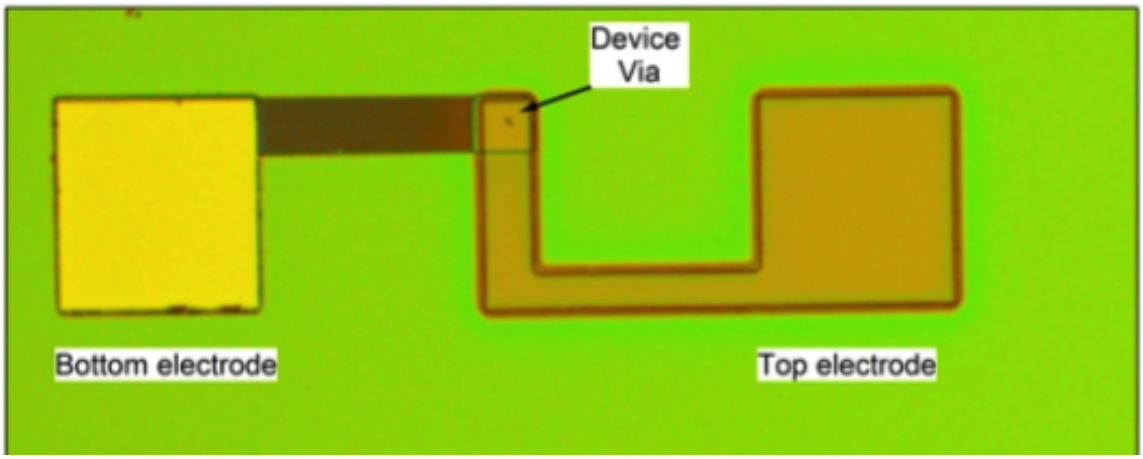


FIGURE 9: INDIVIDUAL MEMRISTOR DEVICE ON RESEARCH PROBE DIE.

SDC Memristor Device Inventor

Kris Campbell is a scientist and an engineer, with a passion for creating and building new device technologies. She loves everything about chemistry and believes that a solid foundation in chemistry is one of the best things a student in any science or engineering discipline can give to themselves. With it comes an appreciation for all things in nature and in the science surrounding technology. As both a chemist and an electrical engineer, she has had a range of professional experiences from electro-optic circuit design, and nonvolatile memory device technology development and fabrication, to teaching. She is currently an Associate Professor in the electrical and computer engineering department at Boise State University. Kris Campbell has over 10 years of electrical engineering industry experience in the areas of microfabrication and optoelectronic circuit design. Kris has published over 20 papers in peer reviewed journals, 2 book chapters, and several conference proceedings. Her current research interests are in the areas of reconfigurable electronics based on ion-conducting chalcogenide glasses, and new electronic memory technologies based on ion-conduction and electron spin zero-field splitting.

University of California, Davis Physical Chemistry Ph.D.
University of Nevada, Las Vegas Electrical Engineering B.S.E.E.