Irradiation testing of ASICs for the ATLAS HL-LHC Upgrade

Andie Wall

University of Pennsylvania

On behalf of ATLAS ITk

Topical Workshop on Electronics for Particle Physics

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Outline

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3. Proton irradiation program and results
    a. Experimental setup
    b. Cross-section calculations and HL-LHC projections

ATLAS and the Inner Tracker

- For HL upgrade to LHC, ATLAS's Inner Detector will be replaced with all silicon Inner Tracker (ITk)
  - More radiation hard & has faster readout
  - Consists of two systems: strips & pixels
- ITk strips contain 3 kinds of ASICs:
  ABCStar, **HCCStarv1**, **AMACStar**
  - ABCStar: ATLAS Binary Chip
    - Front end analog detector readout
    - Irradiation tests have already been performed
  - **HCCStar**: Hybrid Control Chip
    - Sends clock & control signals to ABCStar
  - **AMACStar**: Autonomous Monitoring and Control Chip
    - Monitors & controls voltage, current, temperature
  - ASICs will reside between 385-762 mm with worst case endcap maximum dose of 50.4 MRad
    - Need to make sure ASICs will operate successfully in high-radiation environment

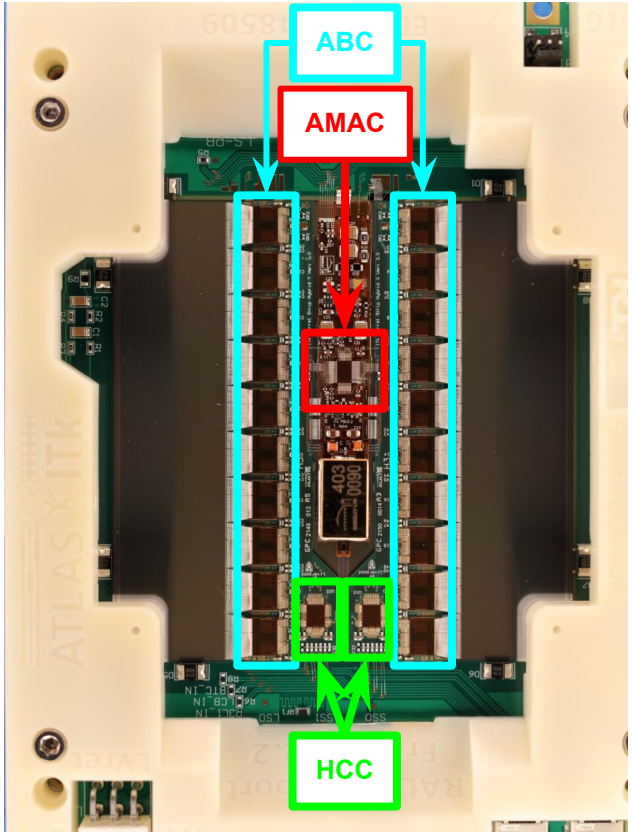


Image credit: Brookhaven National Laboratory

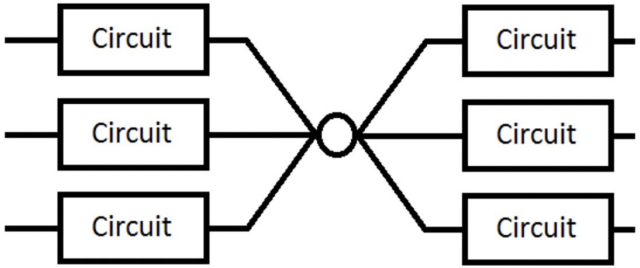
SEE background

- High energy particles can ionize materials they pass through
  - Our ASICs are sensitive to 2 kinds of Single Event Effects (SEEs)
    - Single event upset (SEU): change of state caused by ionizing particle
      - Affects flip flops
      - In our case, logic states flip in configuration registers or in data as it is being processed
    - Single event transient (SET): signal inversion caused by voltage pulse
      - Affects logic gates
- To make sure ASICs are protected from SEEs, we use test beams at national laboratories
  - ASICs are placed in beam & performance is monitored
    - Continuous loop counts how many times SEEs occur & are corrected
    - Expect to see SEEs occurring & being corrected during beam
  - Beam tests don't differentiate between SEU & SET but simulation shows ASIC designs protect against both

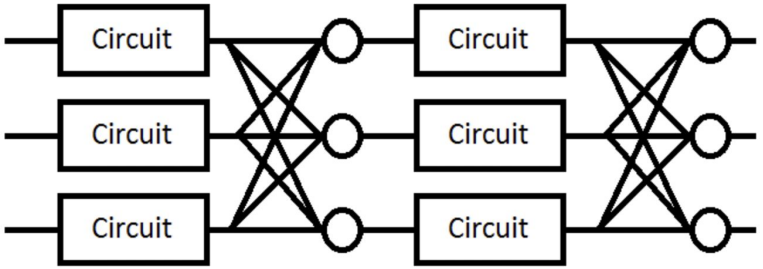
SEE background continued

Triplication & majority voting

- Nearly all logic in both chips is triplicated
  - Triplication of flip flops protects against SEUs
    - 3 data copies compare & save majority value
  - Triplication of logic protects against SETs
    - Accomplished by also triplicating voters
    - Deglitchers on wires offer additional protection
  - HCC has some memories related to the hit/cluster data that are not triplicated
- Highly unlikely to have 2 SEUs flip same bit
  - Would completely flip the triplicated logic states
  - Not expected to occur at HL-LHC with any frequency
- Use test beam results to confirm that ASICs have sufficient triplication



Triplicated data with single voter



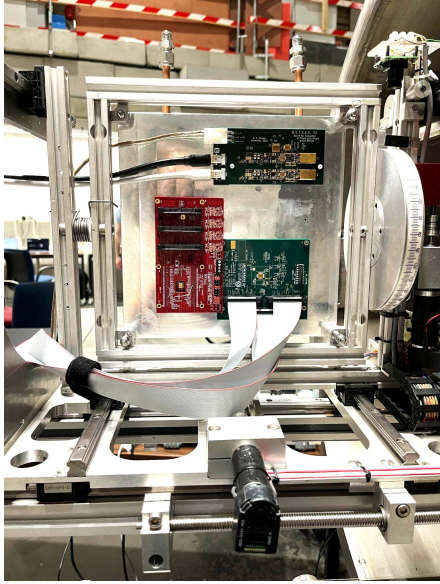
Triplicated data & triplicated voters

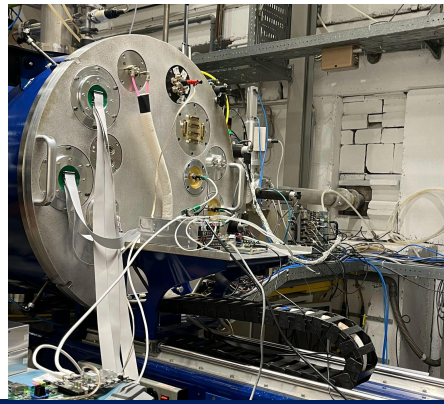
Images from Wikipedia

Experimental setup for heavy ion irradiation

- Heavy ion irradiation testing at UCLouvain
  - Average fluence of 5.5E7 ions/cm^2
- **HCC**, **AMAC**, **BETSEE** placed on cold plate in vacuum with flanges connecting to outside electronics
  - BETSEE is Board for Evaluating Triple Chip SEEs & results can be found here
- Continuous loop checks for flipped bits that have been corrected & records them
- Linear energy transfer (LET): energy per unit length lost by particle passing through material
  - Ions with higher LET cause higher rate of bit flips
  - Fitting data from ions of various LETs helps predict performance in other environments
- Used 8 ions for HCC & AMAC:

  ($^{13}C^{4+}$, $^{22}Ne^{7+}$, $^{27}Al^{8+}$, $^{36}Ar^{11+}$, $^{53}Cr^{16+}$, $^{84}Kr^{25+}$, $^{103}Rh^{31+}$, $^{124}Xe^{35+}$)
  - LETs ranging from 1.4 to 62.5 MeV•cm^2/mg
  - Can extrapolate from fit to environment's expected LET to get projected cross-section, multiply by total hadron flux to get expected SEE rate





Heavy ion irradiation results

- HCC & AMAC performed extremely well operationally
  - Saw evidence of single SEEs occurring in triplicated logic & being corrected
  - No double SEEs occurred
  - Disabling one clock (which disables triplication) showed uncorrected SEEs
    - Confirmed that triplication was working
  - SEEs increased with LET as expected
- HCC & AMAC needed resets for two highest LET ions
  - Rh @ 46.1 & Xe @ 62.5 MeV $\cdot$ cm^2/mg

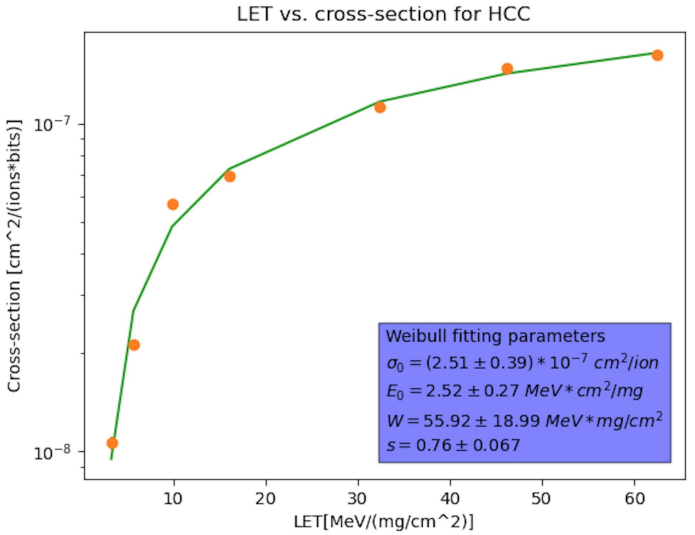
Heavy ion cross-section calculations and Weibull fit

- #SEEs counts corrected bitflips (CBFs) recorded across all configuration registers

$$\sigma = \frac{\#\text{SEEs}}{\text{fluence} \cdot \text{bits monitored}}$$

- Weibull fit is commonly used to model observed failures of components
- Can predict SEE rates at HL-LHC by determining 4 parameters:
  σ_0= saturated cross-section, E_0=threshold energy, W=width of rising portion, s=shape modification

$$\sigma(E) = \sigma_0 \left\{ 1 - \exp\left[\left(\frac{E - E_0}{W} \right)^S \right] \right\}$$



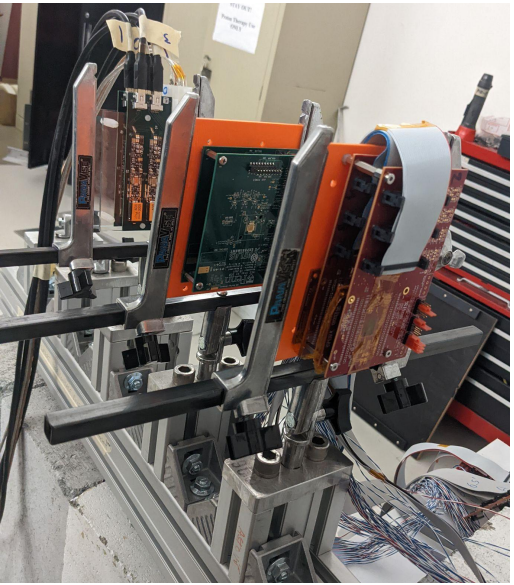
	$\sigma_0 \left[\frac{cm^2}{\text{ion}}\right]$	$E_0 \left[\frac{\text{MeV}\cdot\text{cm}^2}{\text{mg}}\right]$	$W \left[\frac{\text{MeV}\cdot\text{cm}^2}{\text{mg}}\right]$	S
AMAC	$(2.5 \pm 0.4) \cdot 10^{-7}$	2.5 ± 0.3	56 ± 19	0.8 ± 0.1
HCC	$(3.3 \pm 0.6) \cdot 10^{-7}$	2.3 ± 0.7	31 ± 13	0.7 ± 0.1

Table 1: Weibull parameters based on Louvain heavy ion data

Further analysis of heavy ion data

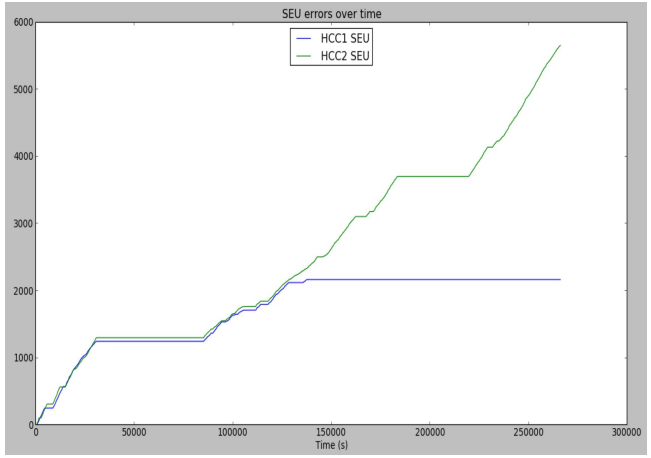
- Corrected bitflips (CBFs) were checked across registers & across time
  - No unexpected behavior observed
  - Corrected bitflips are not problematic thanks to ASIC designs
- Bit flip rate in non-triplicated HCC data expected to be 10 orders of magnitude lower than electronic noise
- Combining Weibull parameters with expectations for various LETs at HL-LHC gives expected XS of CBFs
  - Can then multiply projected cross-section by total hadron flux to get expected CBF rate
    - In HL-LHC lifetime, expect 50 CBFs per HCC bit & 120 CBFs per AMAC bit
- HCC needed register resets for 2 highest LET ions (Rh @ 46.1 & Xe @ 62.5)
  - High LET ions deposit more energy across chip surface & can cause more disruptive issues than single bit flip
  - High LET effects much rarer at HL-LHC, & none expected above Kr @ 32.4 MeV $\cdot$ cm^2/mg
- AMAC had communication issues during highest 2 LET ions
  - Solved by hard resets

Proton beam time summary

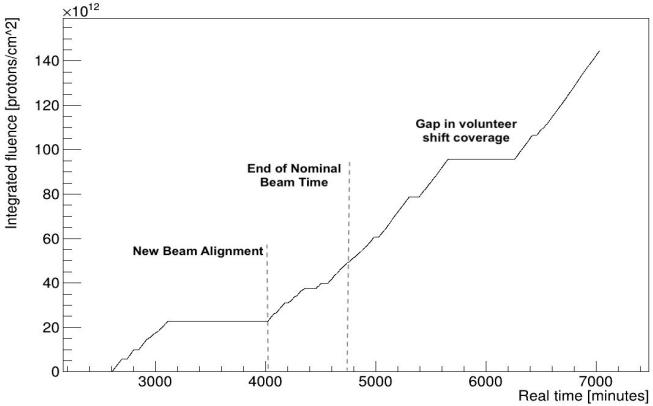


- TRIUMF Proton Irradiation Facility
  - Goal to confirm Louvain findings
  - Total fluence ≈8% of HL-LHC lifetime
- Ran 2 **HCC**, 2 **AMAC**, 2 **BETSEE** setups simultaneously
  - Attached boards to mounting apparatus & aligned chips with beam
  - Boards attached to electronics in bunker via long cables
- HCC & AMAC performed well overall
- HCC needed some register resets & AMAC setup needed to be power cycled
  - Similar to issue seen at Louvain & in testbench
  - Not issues with functionality

SEUs over time and cross-section calculations



Fluence over time



- Used similar method to Louvain but corrected for fluence as needed

$$\sigma = \frac{\#\text{SEEs}}{\text{fluence} \cdot \text{fluence correction factor} \cdot \text{bits monitored}}$$

	Cumulative CBF cross-section
HCC1	$1.5 \cdot 10^{-13}$
HCC2	$2.1 \cdot 10^{-13}$
AMAC1	$2.2 \cdot 10^{-13}$
AMAC2	$2.6 \cdot 10^{-13}$

Table 2: Cumulative CBF cross-sections from proton data

- Average CBF cross-section is $1.78 \cdot 10^{-13}$ for HCC & $2.39 \cdot 10^{-13}$ for AMAC
  - Gives lifetime projection of 180 CBFs per HCC bit & 240 CBFs per AMAC bit

Conclusion

Based on heavy ion data:

- **No resets of any kind required for LETs expected at the HL-LHC**
  - No hard resets/power cycles required for HCC
  - AMAC experienced communication errors which required hard resets for highest 2 LETs
  - Single SEEs occurred in triplicated logic & were corrected by ASIC designs
- Running without triplication showed uncorrected SEEs
- Data well described by Weibull fit model

Based on proton data:

- HCC required register resets very infrequently & AMAC required power cycles to fix communication
- **Louvain results were confirmed**
- Both ASICs passed Production Readiness Review

From Louvain & TRIUMF testbeam data, we expect HCCStarV1 and AMACStar to perform acceptably under irradiation at HL-LHC with O(10) correctable bit flips per bit per year

Related talks and posters

Pre-Production Testing of the AMACStar ASIC at Penn for the ATLAS ITk Detector

Thomas Gosart, Tuesday poster session

BETSEE: Testing for System-Wide Effects of Single Event Errors on ITk Strips Modules

Ryan Roberts, Tuesday poster session

Simulated verification of the ASIC functionality and radiation tolerance for the HL-LHC ATLAS ITk Strip Detector

Jeff Dandoy, ASIC track talk, Tuesday at 11:20

Radiation tolerance studies of the HV-Mux GaN FETs for the HL-LHC ATLAS ITk Strip Detector

Luis Felipe Gutierrez Zagazeta, Thursday poster session

Testing of the HCC and AMAC functionality and radiation tolerance for the HL-LHC ATLAS ITk Strip Detector

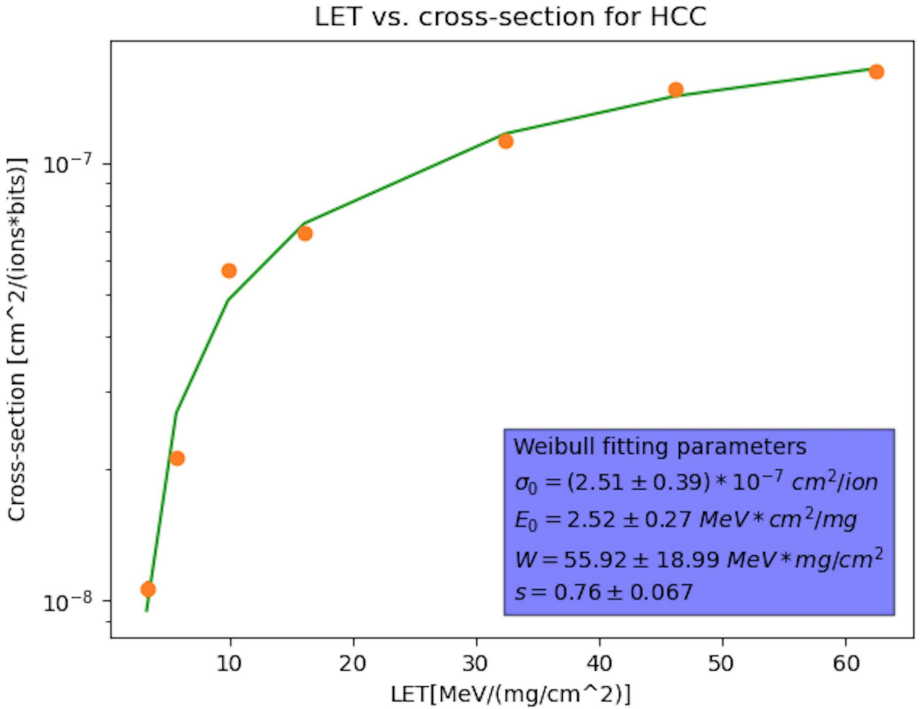
Luis Felipe Gutierrez Zagazeta, Thursday poster session

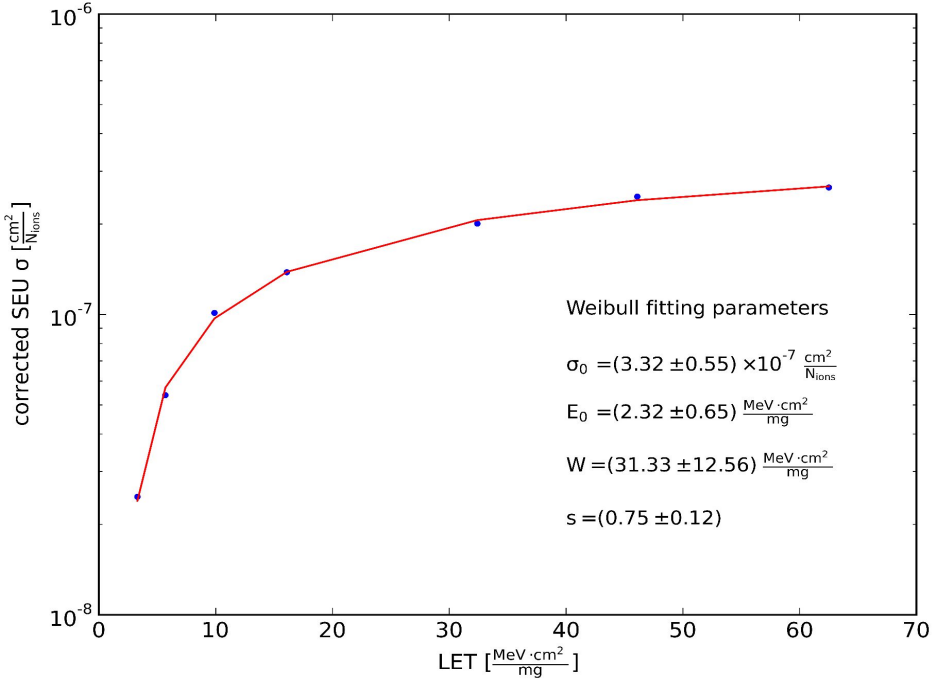
Pre-Production Testing of the HCCStar at Penn for the ATLAS ITk Detector

Bobby McGovern, Thursday poster session

Backup

Cross section plots with Weibull fit





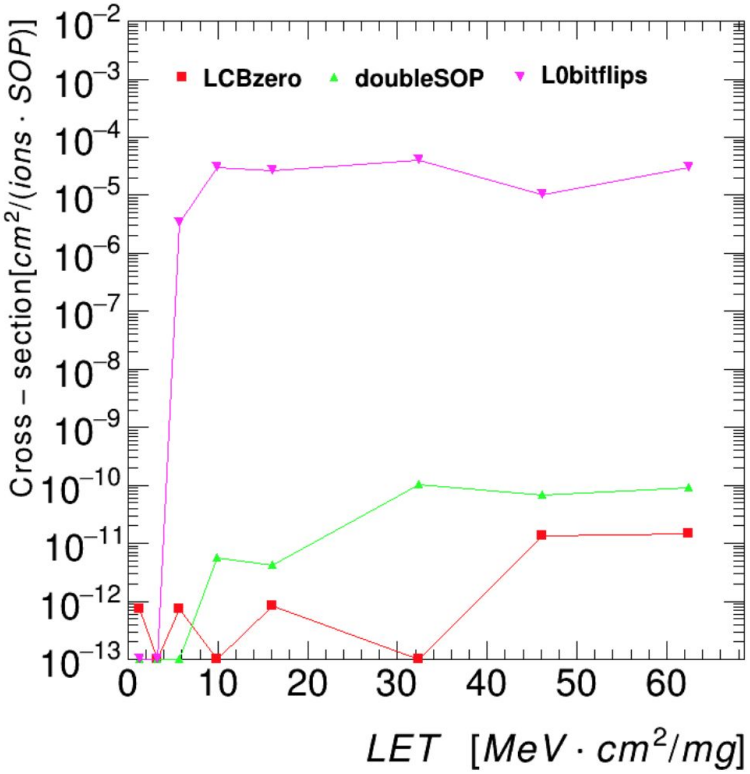
- Carbon's LET is below threshold energy E_0 for both ASICs
  - Did not have significant number of corrected bitflips (<10 in 1.5 hours), subsequently excluded from fit

Louvain cross-sections

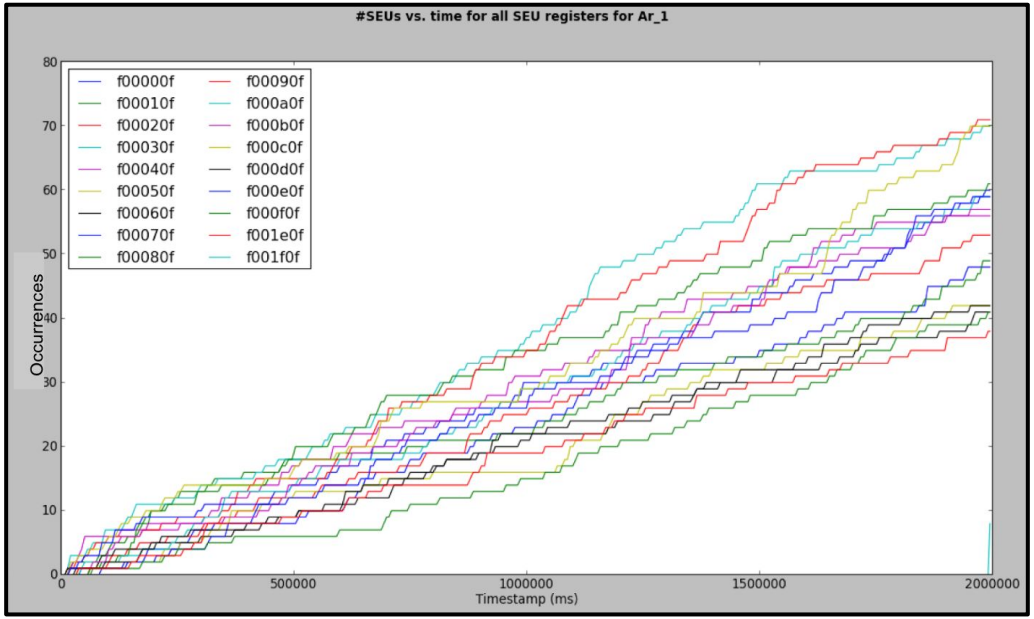
Ion	**LET** [MeV•cm^2/mg]	**AMAC cross-section** [cm^2/ions•bits]	**HCC cross-section** [cm^2/ions•bits]
$^{13}C^{4+}$	1.3	$(4.200 \pm 1.878) \cdot 10^{-11}$	$(6.510 \pm 3.759) \cdot 10^{-10}$
$^{22}Ne^{7+}$	3.3	$(2.472 \pm 0.037) \cdot 10^{-8}$	$(1.061 \pm 0.048) \cdot 10^{-8}$
$^{27}Al^{8+}$	5.7	$(5.387 \pm 0.006) \cdot 10^{-8}$	$(2.127 \pm 0.068) \cdot 10^{-8}$
$^{36}Ar^{11+}$	9.9	$(1.012 \pm 0.009) \cdot 10^{-7}$	$(5.684 \pm 0.136) \cdot 10^{-8}$
$^{53}Cr^{16+}$	16.1	$(1.383 \pm 0.008) \cdot 10^{-7}$	$(6.904 \pm 0.130) \cdot 10^{-8}$
$^{84}Kr^{25+}$	32.4	$(2.006 \pm 0.015) \cdot 10^{-7}$	$(1.128 \pm 0.022) \cdot 10^{-7}$
$^{103}Rh^{31+}$	46.1	$(2.467 \pm 0.021) \cdot 10^{-7}$	$(1.471 \pm 0.031) \cdot 10^{-7}$
$^{124}Xe^{35+}$	62.5	$(2.646 \pm 0.022) \cdot 10^{-7}$	$(1.62 \pm 0.033) \cdot 10^{-7}$

Error cross-sections for Louvain “strange” high LET events for HCC

- Highest two LETs (Rh & Xe) have these strange types of error
- The so-called “strange high LET events” can be seen here (based on HCC data) to occur at a frequency of ~5-6 orders of magnitude lower than the correctable bit flips
  - For comparison, expect 18 CBFs/year/bit for HCC and 24 CBFs/year/bit for AMAC



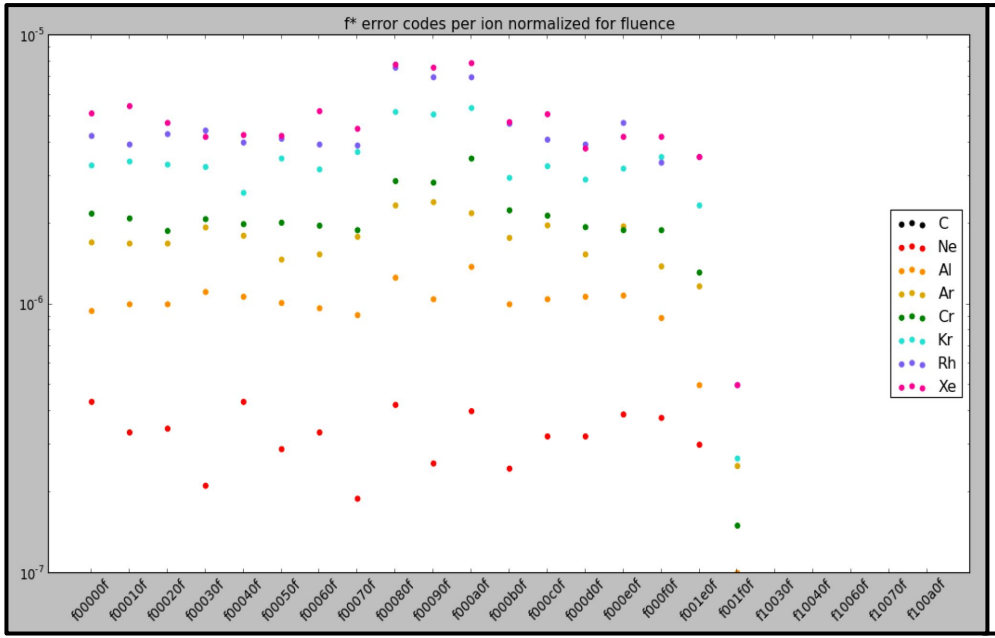
Louvain SEU accumulation by time for HCC



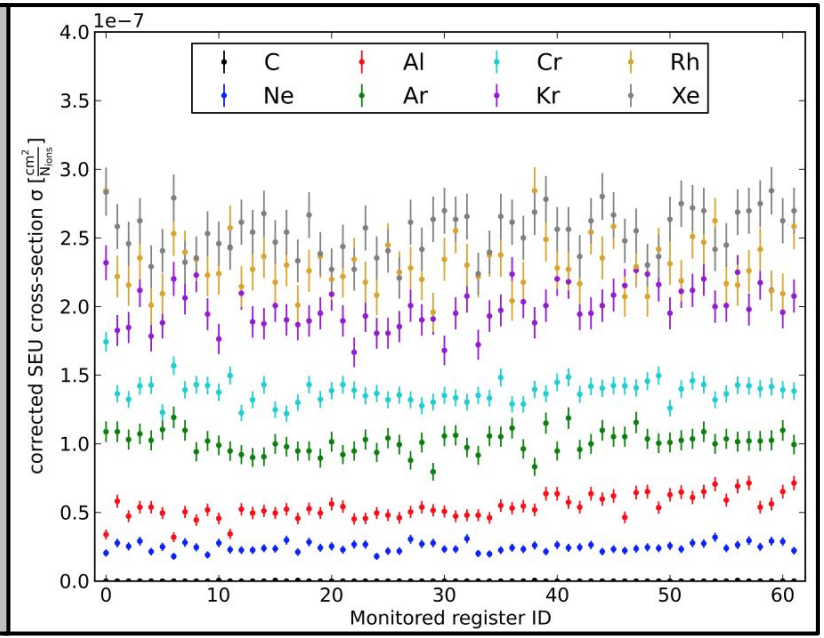
- Status codes beginning with f are bitflips seen in the SEU registers
- Looked at SEUs vs. time for all ions
  - Linearly increasing in all cases, nothing unexpected observed

Louvain SEU accumulation by register

HCC



AMAC



- 3 registers (OPMode, OPModeC, Cfg1) had ~2x bitflips of all others
  - Noticeable in Al & above
  - Could be related to register position on the chip
- Some outliers noticeable at high LETs
  - Register 38 for Rh, 11 for Kr

Alternate (comparable) calculation of expected rate of corrected bit flips (CBFs) based on Louvain data

- Follow the ABCStar paper calculation

$$\phi_{\text{hadrons}} = \mathcal{O}(10^{-3}) \frac{\text{hadrons}}{\text{cm}^2 \cdot \text{pp collisions}} \langle \mu \rangle \cdot \text{rate of BCs}$$

$$\text{Taking } \langle \mu \rangle = 200 \text{ and rate of BCs} = 40 \text{ MHz}$$

$$\phi_{\text{hadrons}} = \mathcal{O}(10^{-3}) \frac{\text{hadrons}}{\text{cm}^2 \cdot \text{pp collisions}} \cdot 200 \cdot \frac{4 \cdot 10^7 \text{ pp collisions}}{\text{second}}$$

$$\phi_{\text{hadrons}} = \mathcal{O}(10^{7}) \frac{\text{hadrons}}{\text{cm}^2\text{s}}$$

$$\text{Assuming 4 months/year of continuous running } (\sim 10^7 \text{seconds/year}) :$$

$$\text{Rate}_{\text{CBF}} = \mathcal{O}(10^{7}) \frac{\text{hadrons}}{\text{cm}^2\text{s}} \frac{\sigma_{\text{SEU}}}{\text{chip}} \frac{10^7 \text{seconds}}{\text{year}}$$

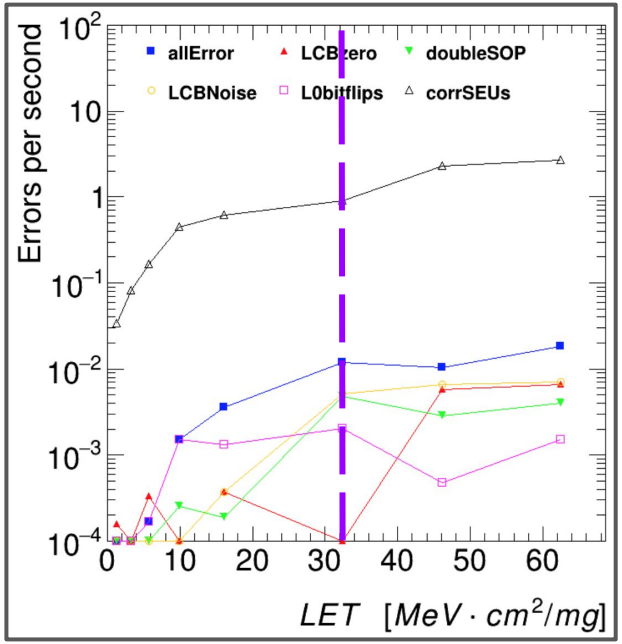
$$\text{Rate}_{\text{CBF, AMAC}} = 10^7 \frac{\text{hadrons}}{\text{cm}^2\text{s}} \cdot 1.2 \cdot 10^{-13} \frac{\text{cm}^2}{\text{ion}} \frac{10^7 \text{seconds}}{\text{year}} = 12 \frac{\text{CBFs}}{\text{year} \cdot \text{AMAC}}$$

$$\text{Rate}_{\text{CBF, HCC}} = 10^7 \frac{\text{hadrons}}{\text{cm}^2\text{s}} \cdot 5.2 \cdot 10^{-14} \frac{\text{cm}^2}{\text{ion}} \frac{10^7 \text{seconds}}{\text{year}} = 5 \frac{\text{CBFs}}{\text{year} \cdot \text{HCC}}$$

Analysis of “strange” high LET events seen by HCC

- High LET ions deposit more energy across chip surface, can cause more disruptive issues than single bit flip
  - However high LET effects **much rarer** at HL-LHC, & none expected above **Kr @ 32.4***
- A few instances of **register resets** needed, mainly for highest 2 LET ions (Rh @ 46.1 & Xe @ 62.5)
  - Error is reproducible in testbench without radiation, likely source for lower LET instances
  - Error is evident from HCC’s automatic HPR’s (malformed but still at 1 ms rate)
  - Register resets & reconfigurations quick to perform [O(ms)]
- 2 transient issues rarely seen & no action required (**DoubleSOP** & **LCBNoise**)
  - May be related to testbench & firmware, not HCC itself
  - Errors would not affect operation or data taking
- **No hard resets required at all**
- **L0bitflips** discussed in next slide

LCB Hybrid Line noise



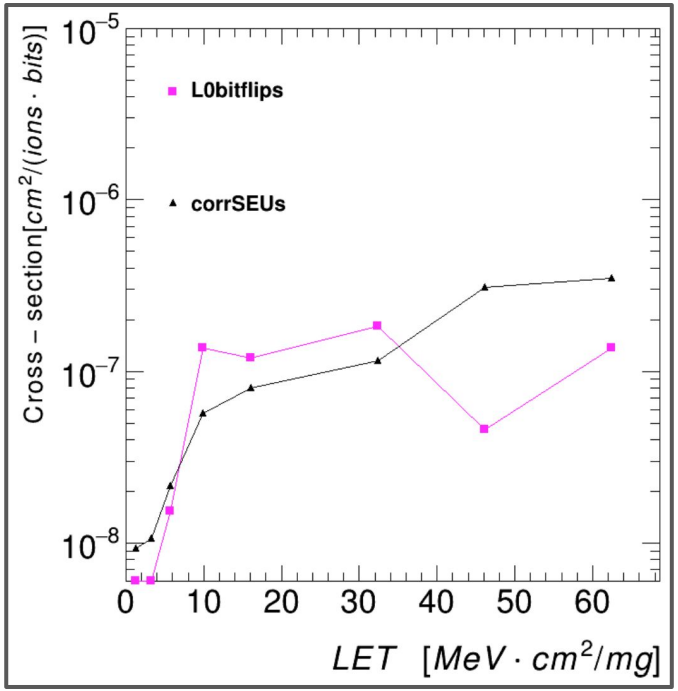
*Paulo Moreira’s AUW lpGBT presentation

**Jeff Dandoy’s in-depth analysis slides

Analysis of “strange” high LET events seen by HCC (cont.)

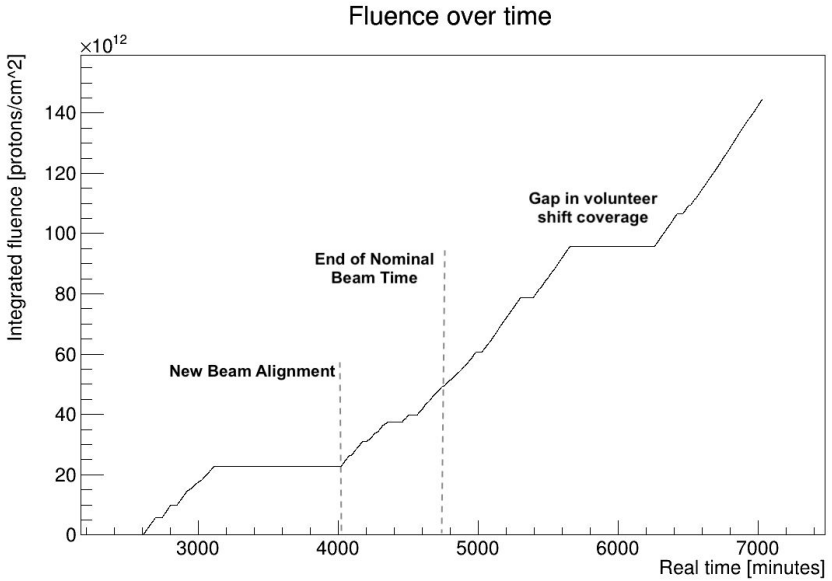
- Size constraints - could not triplicate full data path of HCC
  - Hard to see in irradiations because data is stored very briefly within HCC’s logic - hard to flip bits
- Saw small number of single bit flips in nontriplicated data path
  - Calculated **bitflip XS of L0 data** based on rough estimation of time data is in memory
    - L0 bitflips are data only (no metadata)
  - Good agreement with corrected bit flip cross-section in registers
- Very rough extrapolation for each HCC: 1 bitflip in data (a bad hit) per 10 billion triggers
  - Compare with expected sensor noise of ~2 spurious hits per trigger per HCC

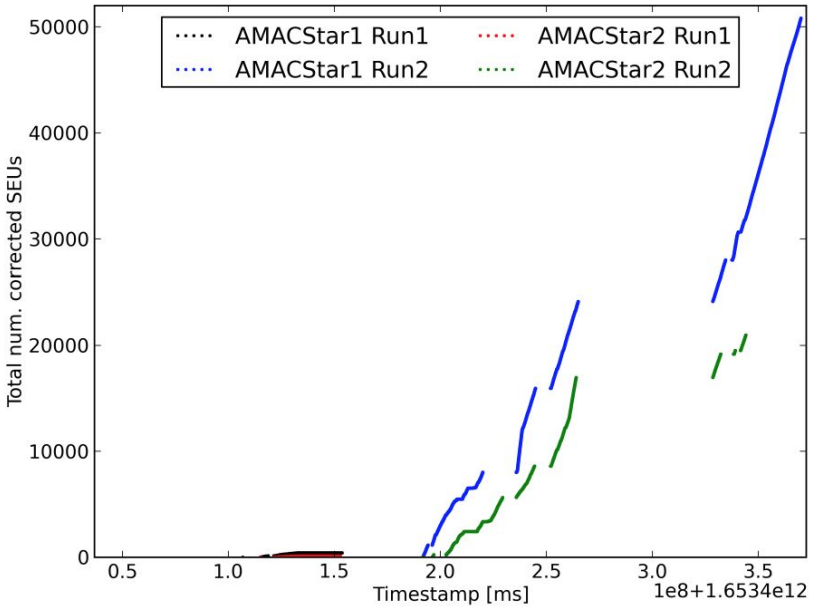
Bitflip cross-section per bit



**Jeff Dandoy’s in-depth analysis slides

SEU accumulation over time for AMAC at TRIUMF





- Plot is not continuous for AMAC because of test board failures and interruption in beam delivery
- Error with file timestamps, approximations applied to correct the issue

Adjustments necessary

- Needed to realign after fixes were made on TRIUMF side
  - Beam position shifted from what we originally aligned with, so we realigned the chips to maximize fluence
- Priority was realignment of AMAC
  - HCC was slightly off-center due to height constraint & being too active to correct for
- Because beam shape is unknown, we need to correct fluence for x-y displacement
  - Using AMAC's second alignment as "truth", we can determine a fluence correction factor using the relative bitflip rate between HCC & AMAC
  - Correction factors are ½ for 1st alignment & ⅓ for 2nd alignment

Calculation of expected SEU rate at the HL-LHC

- Combining Weibull parameters with expectations for various LETs at HL-LHC gives expected XS of corrected bit flips **(CBFs)**
  - Automatically corrected bitflips cause no operational issues but can be used as guide for comparison with much rarer operational issues
- Can multiply projected SEU cross-section (provided by Federico Faccio) by total hadron flux to get expected rate of SEUs
  - Based on ITk Strips TDR lifetime 1 MeV equivalent neutron fluence for worst case endcap of $8.1 \cdot 10^{14}$ cm^{-2}
  - For heavy ions, use safety factor of 5 (recommendation from ATLAS Radiation Effects Task Force)
- For the non-triplicated hit/cluster data path of the HCCStarV1, we predict around 10^{-10} bit flips in actual data per trigger
  - Can compare with 19 good hits per trigger & 2 noise hits per trigger
- Ran for ≈2.7 MRad at TRIUMF
  - Assuming 10 year HL-LHC lifetime: 7.7% of ASIC lifetime (9 months running)
- From Louvain, extrapolation # of register resets needed per HCC as 5 per year
  - Assumes all instances of register resets were irradiation-induced HCC issues (have seen occurrences in testbench) & HL-LHC rate extrapolation is identical for effects turning on at LET > 46.1 (register resets) as for LET > 3.3 (CBFs)
  - If this occurs at HL-LHC, would be quick to identify & perform corrective action
  - Based on TRIUMF extrapolation, expect to need 9 register resets/HCC/year

	Projected HL-LHC lifetime CBFs per HCC bit	**Projected HL-LHC lifetime CBFs per AMAC bit**
Louvain data	50	120
TRIUMF data	180	240

Table 3: Projected HL-LHC CBF rates

Extrapolating number of errors from TRIUMF to HL-LHC

- ≈2.7 MRad delivered combined for both HCCs during triplicated data taking
  - Equivalent to roughly 7.7% of HCC lifetime (9 months running)
- Need to correct certain error types based on effective time sensitive
- LCBzero issue: 100% effective time sensitivity
  - Happened 7 times (requiring register resets) ⇒ 9 expected/year
  - Also saw this with beam off, so could still be testbench related
  - Error is evident from HPR's (malformed but still at 1 ms rate)
    - Takes <1 ms to identify, quick to perform register resets/reconfigurations [O(ms)]
- Readout time: code reads out HCC 30% of total time
  - Brief LCB unlocking: saw 2 times on LCB_HYB ⇒ 9 expected/year
    - None seen on LCB_IN
- Triggering rate: operated HCC triggering @ 4.5 kHz overall with ITSDAQ
  - Roughly 0.45% of expected triggering rate
  - Bit flips in returned LP data
    - 1 instance @ 4.5 kHz ⇒ 295 expected/year @ 1MHz
  - Bit flips in outgoing LP on HYB_LP
    - 11 instances @ 4.5 kHz ⇒ 3150 expected/year @ 1MHz