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Thermoelectric Coolers for On-chip Thermal Management: Materials, Design, and Optimization

Wen-Yi Chen[1,a], *Xiao-Lei Shi*[2,a], *Jin Zou*[1,3], *Zhi-Gang Chen*[2*]

[1] School of Mechanical and Ming Engineering, The University of Queensland, Brisbane, Queensland, 4072, Australia

[2] School of Chemistry and Physics, Queensland University of Technology, Brisbane, Queensland 4001, Australia

[3] Centre for Microscopy and Microanalysis, The University of Queensland, Brisbane, Queensland 4072, Australia

[a] These authors contribute equally to this work.

Corresponding authors

E-mail addresses: Chen, ZG. (zhigang.chen@qut.edu.au)

Abstract

Compared with traditional active cooling methods, thermoelectric coolers are more accessible to be integrated with electronics as an effective thermal management solution due to their reliability, silence, compatibility, and controllability. Considering the rapid development of processors and chips in electronics, this work comprehensively reviews the progress of state-of-the-art on-chip thermoelectric coolers and summarizes the related fundamentals, materials, designs, and system logic. Particularly, we highlight on-chip thermoelectric coolers with self-cooling design and on-demand requirement. In the end, we point out current challenges and opportunities for future improvement of designs, performance, and applications of on-chip thermoelectric coolers.

Keywords: thermoelectric; cooler; chip; thermal management; materials.

Graphical Abstract

1. Introduction

In the past five decades, the development of the semiconductor industry, especially microchips, keeps following the Moore's Law, which predicted the number of transistors on a microchip being double every two years [1-3]. Transistors are the critical components on the integrated circuit (also called microchips) to assist computer calculations and tasks [3, 4]. Till now, one 14 nm microchip is comprised of millions or even billions of transistors to satisfy the demand of human daily life [5]. However, the heat dissipation of microchips with high-density transistors gradually becomes an increasingly critical issue, owing to the high heat dissipation, which has limited the maximum operating frequency of chips and reduced the lifetime under the poor thermal management [1, 6]. Therefore, a well-designed and efficient thermal solution is required to handle the high heat generated by the chips and in turn promise the miniature of chips [7]. Traditional active cooling methods, such as fans and liquid, have a high cooling performance in the thermal management of chips. However, with the development of chips in recent years, the larger size of heatsinks, higher frequency of fans, and higher heat capacity of liquid are required [8]. Therefore, they increasingly become incompatible with the demand for portable, silent, and light electronics, especially for laptops and mobiles [9]. Most mainstream companies try to improve the design, materials, and software control to improve the thermal management of chips as well as promise the portable and light of the laptops and mobiles [10], but these passive cooling methods need to limit the actual maximum heat flux density to avoid overheating of chips, so passive cooling limits the performance to promise the cooling situation of chips compared to active cooling [11, 12]. Although some novel cooling methods, such as liquid cooling, are developed [13], their volume, reliability, complexity, weight, and cost cause these applications are not the prior choice for portable electronics [13-18].

Based on the Peltier effect, thermoelectric coolers (TECs) can directly transfer electricity to the temperature difference (ΔT). As well, with the advantages of no moving parts, fast

thermal response, silence, reliability, and scalability, TECs are suitable for long-term operation and less maintenance [19-22]. Especially, the on-chip thin-film-based [10, 23-33] and microstructured [19, 34-39]. TECs are emerging in recent years, making TECs one of the most potential candidates in high-performance thermal management of electronics. **Figures 1(a-c)** illustrate the process of fabricating thin-film-based TECs used for chip cooling, in which the TECs are composed of the p- and n-type Bi_2Te_3-based thin-film thermoelectric legs [23], as shown in **Figure 1(a)**. A typical package of TECs and chips includes the heat sink, integrated heat spreader (IHS), thermal interface material (TIM), chip die, TECs, and chip substrate, as displayed in **Figures 1(b-c)**. **Figure 1(d)** illustrates the schematic of the side view of the chip package, including the heat sink, IHS, TIM, chip die, TECs, and chip substrate [40]. The increasing demand for high-performance personal computers (PCs) and light-weight notebooks is driving more powerful miniature chips with amounts of heat dissipation, and the heat generated by chips is increasing with the years. In the thermal management in chips, the theory of thermal design power (TDP) expresses the maximum amount of heat generated by the computer chips that need to be dissipated by the designed cooling system in the computer. **Figure 1(e)** summarizes the TDP of released chips by Intel in the past five years, and the TDP of the latest chips has reached 120 W which is three times the chips in 2017. **Figure 1(f)** summarizes some reported maximum temperature difference ΔT_{max} of the film based and micro-bulk TECs, and it shows that the best ΔT_{max} of TECs can achieve 75 K, which is sufficient to satisfy the thermal management of chips [28, 41-45], and the opposite Seebeck coefficient (S) can also be used as thermoelectric generators (TEGs) to harvest the waste heating and generate the extra electricity for supporting TECs [7, 19, 46-49]. Hence, the well-designed TEC-TEG system is the most potential candidature for cooling the hotspot of chips.

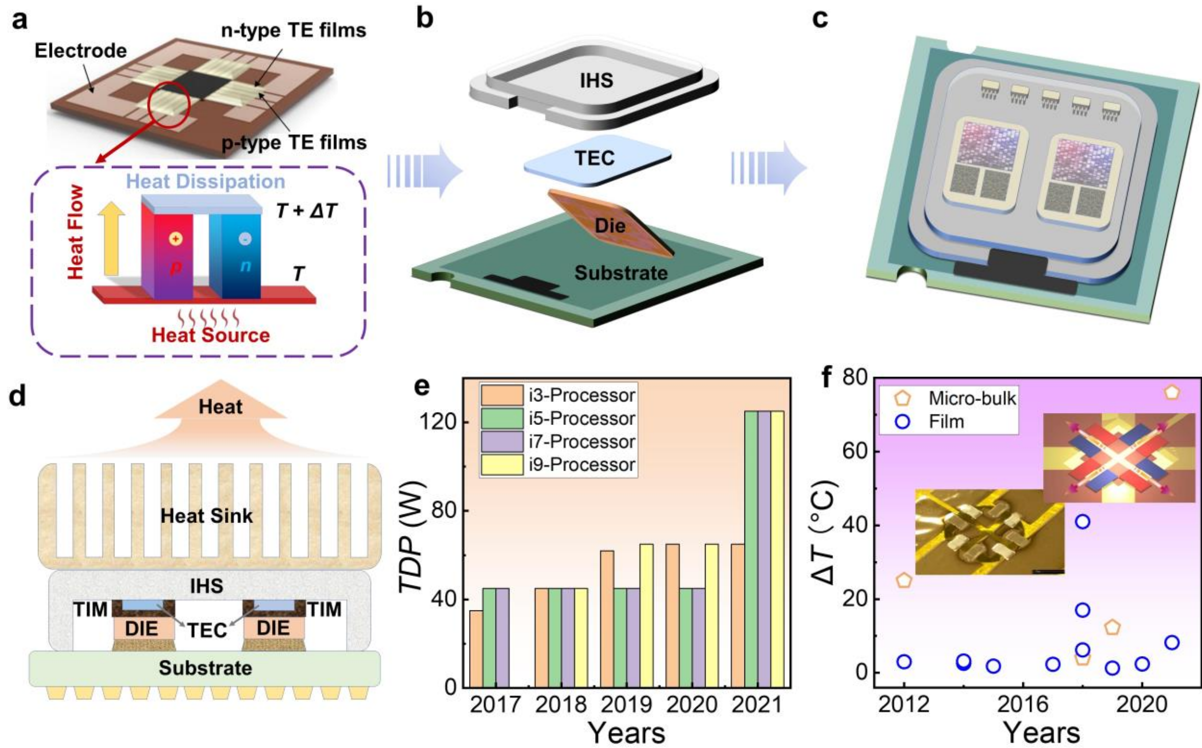

Figure 1 **(a)** A classic thermoelectric thin film fabricated by the p-type and n-type thin-film TE legs. Reproduced with permission [23]. Copyright 2015, Elsevier. **(b)** illustrates the process of the package of the TE coolers and the chips. **(c)** illustration of the assembled chip package with TE coolers. **(d)** illustration of the schematic of the side view of the chip package, including the heat sink, integrated heat spreader (IHS), thermal interface material (TIM), chip die, TECs, and chip substrate [40]. **(e)** The TDP of released chips by Intel in the past five years [50]. **(f)** Reported maximum cooling temperature deference ΔT_{max} of the film-based TECs in recent years. Reproduced with permission [28, 41-45]. Copyright 2015, IEEE.

With the development of thermoelectric science and technology, TEC gradually becomes a promising active cooling technique with the rise of performance and unique advantages [9, 10]. With the continuous development of high-performance chips and the need for portability, the demand for active cooling especially TECs has massive potential to be the mainstream in the future, therefore, a timely review that summarizes the most recent progress of TEC-based on-chip thermal management is urgently required. To achieve this goal, in this work, we focus

on reviewing fundamentals, materials, designs, structures, and systems of TECs for chips and provide the challenges and outlooks toward future development. We hope this review can attract and benefit more researchers who have interests in this field and promote the development of the TECs in electronics.

2. Fundamental of TECs on Chips

2.1 Basic Concept of TEC

Conventional thermoelectric devices (TEDs) are sandwich-structured and assembled by two ceramic electrical insulators, a series of parallel thermocouples, and interconnection metal strips [20, 51]. The thermocouples consist of connected p- and n-type thermoelectric legs by the metal strip, in which the p-type carriers are mainly holes and the n-type carriers are mostly electrons [19, 20]. Therefore, the p-type presents the negative potential while the n-type presents the positive potential. As a result, when applying a current through the thermocouple, the ΔT is achieved [19, 20, 51]. The phenomenon of heat released or absorbed per unit time is called the Peltier effect, which can be described as [52]:

$$\frac{dQ}{dt} = \Pi_{np} I \tag{1}$$

where Π_{np} is the Peltier coefficient of the module ($\Pi_{\mathrm{np}} = \Pi_{\mathrm{p}} - \Pi_{\mathrm{n}}$), and I is the electric current. In addition to the Peltier effect, the Joule effect ($Q_{\mathrm{J}} = I^2 R$) and heat conduction ($K(T_h - T_c)$) also need to be considered when calculating the energy balance of the cooling side [51]. Therefore, the heat conducted from the cold side to the hot side can be expressed as [51, 52]:

$$Q_c = \Pi_{np} I - 0.5 I^2 R - K(T_h - T_c) \tag{2}$$

where R is the electrical resistance, K is the thermal resistance, T_h is the temperature of the hot side of TECs, and T_c is the temperature of the cold side of TECs.

The cooling efficiency of TECs is a critical parameter to evaluate the performance, which is also called the coefficient of performance (COP) that is related to the Q_c, the input power

(P), and the optimum current (I_{opt}) [52]. P is the power that applied to overcome the Seebeck voltage to generate the ΔT of the two sides, expressed as [52]:

$$P = S_{np}(T_h - T_c)I + I^2R \tag{3}$$

The applied current also needs to be optimized to minimize the extra joule heat when flowing through TECs. Therefore, the optimum electric current (I_{opt}) can be calculated [52], expressed as:

$$I_{opt} = \frac{(S_p - S_n)(T_h - T_c)}{R\sqrt{ZT_{avg} + 1} - 1} \tag{4}$$

According to the analysis of **Equation (1)**, **(2)**, **(3),** and **(4)**, the COP can be expressed as [52]:

$$COP = \frac{T_c}{T_h - T_c} \times \frac{\sqrt{1+ZT} - T_h/T_c}{\sqrt{1+ZT} + 1} \tag{5}$$

where the dimensionless figure-of-merit ZT of thermoelectric materials is defined as $ZT = S^2\sigma T/\kappa$, in which σ is the electrical conductivity; κ is the thermal conductivity; and T is the absolute temperature [52-54]. A high ZT value indicates high thermoelectric performance of the material. Therefore, the desirable COP of TECs requires superior thermoelectric materials with high ZT [52]. Generally, high ZT requires the thermoelectric materials to have high S and σ as well as low κ.

2.2 Design TECs by using Finite Element Analysis

TECs with an accurate model is crucial to present the best cooling performance on chips. The existing model is normally classified into simplified 1D energy equilibrium model and 3D coupled Multiphysics model [55-66]. Simplified 1D energy equilibrium model was used for evaluating the cooling flux on the cold side of TEC devices [55], which can be shown in **Figure 2(a)**. The Kirchhoff's current law is the critical parameter to characterize the cooling capacity of TEC [31, 67]:

$$q_c = q_P - q_{Jh} - q_{Fourier} \tag{6}$$

where q_P is the heat flux caused by Peltier effect, q_{Jh} is the Joule heating, and $q_{Fourier}$ is the Fourier transfer effect. The heat flux moved from cold side to hot side can be expressed as [55]:

$$q_P = STJ \tag{7}$$

where J is the current density along the positive direction of *x*-axis. The heat flux caused by Fourier transfer effect can be expressed as [55]:

$$q_{Fourier} = -\kappa \frac{\Delta T}{\Delta x} = \kappa \frac{T_h - T_c}{L} \tag{8}$$

Besides, the cold side can cause extra heat flux from Joule heating, which can be calculated by [55]:

$$q_{Jh} = \frac{1}{2}\frac{Q_{Jh}}{A} = \frac{1}{2}\frac{J^2 L}{\sigma} \tag{9}$$

where Q_{Jh} is the heat produced by Joule heating, L is the thickness of the TEC leg, and J is current density along the positive direction of *x*-axis. Therefore, the cooling heat flux can be presented according to the **Equation (6)**, **(7)**, **(8)**, and **(9)** [55]:

$$q_c = ST_c J - \frac{1}{2}\frac{J^2 L}{\sigma} - \kappa \frac{T_h - T_c}{L} \tag{10}$$

When assuming that the cold side is adiabatic ($q_c = 0$), the temperature on the cold side can be obtained by [55]:

$$T_c = \frac{T_h + 0.5\frac{J^2 L^2}{\kappa\sigma}}{1 + \frac{SJL}{\kappa}} \tag{11}$$

Hot side is normally integrated with a heat sink to dissipate the heat from the heat source, so the temperature on the hot side can assumed to be constant (T_0). Therefore, the temperature difference can be calculated by [55]:

$$\Delta T = T_h - T_c = \frac{T_0 + 0.5\frac{J^2 L^2}{\kappa\sigma}}{1 + \frac{SJL}{\kappa}} \tag{12}$$

When applying the derivative of Equation is set to zero, the ΔT_{max} can be obtained. Similarly, the maximum cooling heat flux q_c can be obtained when defining the $\Delta T = 0$ ($T_h = T_c = T_0$), which can be expressed as [55]:

$$q_{max} = 0.5\frac{S^2 {T_0}^2 \sigma}{L} \tag{13}$$

q_{max} also presents the maximum cooling heat flux that the TEC can pump from the cold side to the heat sink. However, when the thermal gradient is large, 1D energy equilibrium model cannot provide the accurate results since the model simplified the Peltier, Joule heating, and Fourier heat transfer effect. Therefore, 3D coupled Multiphysics model can describe thermal and electric fields for accurately analyzing the TEC devices, as shown in **Figure 2(b)**.

The electric field can be defined as [67, 68]:

$$E = -\nabla \emptyset \tag{14}$$

where $\emptyset$ is the potential in the TEC and ∇ is the vector gradient operator. Therefore, the current continuity equation can be formulated as [55]:

$$\nabla \cdot J = \nabla \cdot (-\sigma \nabla \emptyset) = 0 \tag{15}$$

For the boundary condition, one side is set to ground boundary condition $\emptyset$ ($x = 0$, y, z) = 0, and the other side is excited by an idea voltage source $\emptyset$ (x = L, y, z) = V.

The thermal field can be defined as [55]:

$$q = q_{Fourier} + q_P = -\kappa \nabla \mathrm{T} + \mathrm{PJ} \tag{16}$$

When considering the Joule heating, the heat conduction equation can be rewritten as [55]:

$$\nabla \cdot q = \nabla \cdot (-\kappa \nabla \mathrm{T} + \mathrm{STJ}) = \frac{\|J\|^2}{\sigma} \tag{17}$$

For the boundary conditions, hot side is integrated a heat sink to dissipate the heat, so hot side is normally set to be a constant temperature in the boundary condition [55]:

$$T(x = 0, y, z) = T_0 \tag{18}$$

The other side (cold side) is used for remove the heat from the heat source (chip), which can be set as the heat flux boundary condition [55]:

$$-n \cdot q(x = L, y, z) = -n \cdot (\kappa \nabla \mathrm{T} + \mathrm{STJ}) = q_c \quad (19)$$

where n is the unit outward normal vector of the boundary surface. After that, the maximum temperature and cooling heat flux can be calculated and evaluated using a similar method, called as the 1D energy equilibrium model [55]. The partial differential equations (PDEs) can be solved by using finite element calculation in ANSYS, COMSOL, and finite volume method (FLUENT) to mitigate the problem and time to find the solution. **Figure 2(c)** presents 3D coupled Multiphysics model for the typical micro-TECs with symmetrical π-structure, which was fabricated by chemically depositing the $(Bi_{1-x}Sb_x)_2Te_3$ as p-type and $Bi_2(Te_{1-x}Se_x)_3$ as n-type [69]. The various geometrical dimensions include the thickness of top and bottom contact, and three dimensions (width, length, and height) of the thermoelectric legs, as well as the electrical and thermal fields of devices that are optimized through finite element calculation in COMSOL [69]. For example, **Figure 2(d)** illustrates the resistance R and ΔT as a function of the thickness of top contact (TCT) [69]. The increase of TCT can cause the reduction of R and in turn reduce the contribution to the heat balance, leading to the corresponding increase of ΔT [69]. Similarly, the other geometric parameters can be optimized and in turn achieve the best cooling performance of the TECs.

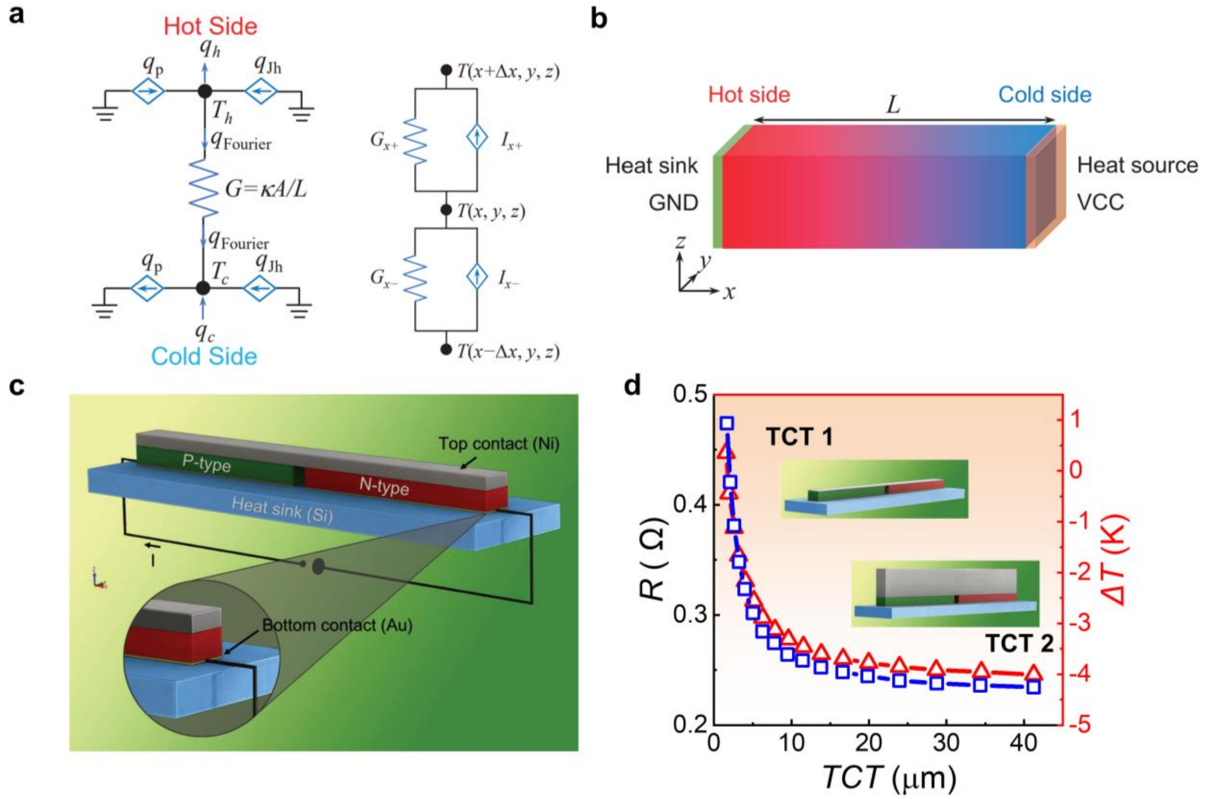

Figure 2 (a) Simulated thermal circuits of a TEC leg based on simplified 1D energy equilibrium model. **(b)** Schematic of the p-type TEC leg based on 3D coupled Multiphysics model. Reproduced with permission [55]. Copyright 2021, IEEE. **(c)** Schematics of two-leg TEC with the initial geometry before optimization containing silicon substrate (blue), bottom gold contact (yellow), p-type semiconductor (green), n-type semiconductor (red), and top nickel contact (gray). **(d)** Dependence of R (blue) and ΔT (red) as a function of the TCT at constant geometry of the thermoelectric legs. Reproduced with permission [69]. Copyright 2019, Wiley.

2.3 System Level Optimization of Thermoelectric Cooling on the Chip

Some additional design factors should be considered during the integration of TECs on the chip, including device configuration, parasitic effects, and operating conditions [70]. Besides, an appropriate integration design of TECs and microchips can maximize the cooling efficiency of TECs on the chips [71]. However, each design parameter can bring different effects on the

cooling performance of TECs [72]. The trade-off of each design parameter is time-consuming since many complicated experiments need to be carried out [72]. Therefore, the Taguchi method with the Grey Relational Analysis (GRA) was developed to identify important design parameters and determine optimal design parameter combinations under different conditions [72-75]. **Figure 3** exhibits the design flow of the 3D electronic package with integrated TECs [72]. Generally, 3D coupled Multiphysics model can be performed in ANSYS or COMSOL to calculate the appropriate device geometry factor and integrated factor. The signal-to-noise (S/N) ratio can be employed to evaluate the sensitivity of the design factors on the cooling performance of the TEC [72]. The analysis of variance (ANOVA) can be used to analyze the mean S/N ratio under each factor level, which aimed to determine the contribution ratio of each factor to the performance of the TEC [72]. The Taguchi analysis with Grey relational analysis can be simultaneously conducted to identify the complicated relationships among the multiple factors, and in turn build an optimum combination for best cooling performance [72]. **Figure 4(a) and (b)** illustrate a schematic of a 3D electronic package with an integrated thin-film TEC. The 2×2 mm^2 thin film TEC was fabricated by Bi_2Te_3/Sb_2Te_3 superlattice materials and then were integrated on a silicon carbide chip with the dimensions of $10 \times 10 \times 0.4$ mm^2 [72]. **Figure 4(c)** shows the simulated and experimented maximum temperature change on the ceramic heater under fixed heating power, which shows simulations were highly matched with the experimental results [72]. **Figure 4(d)** presents the contribution ratios of design factors to the passive cooling and active cooling effect, which can show that the electrode height is the most important design factor that affects the passive cooling and active cooling [72]. Therefore, the system level optimization of TECs can comprehensively present the influence mechanism of the design factors for the TECs, and thereby providing researchers with the optimum design factor combinations.

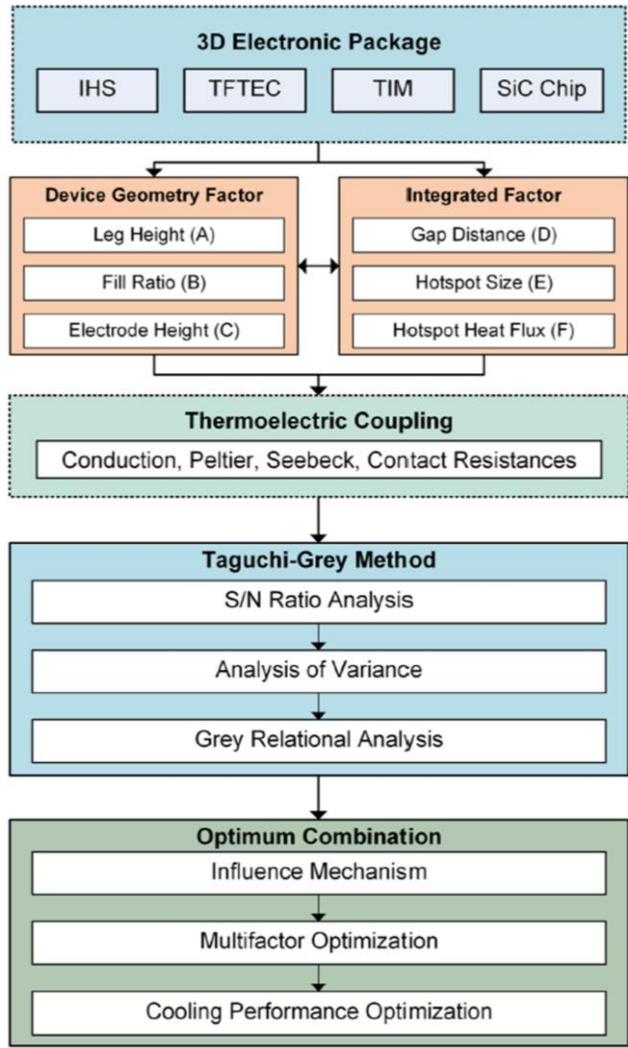

Figure 3 System level optimization design of TECs on the chips. Reproduced with permission [72]. Copyright 2022, Elsevier.

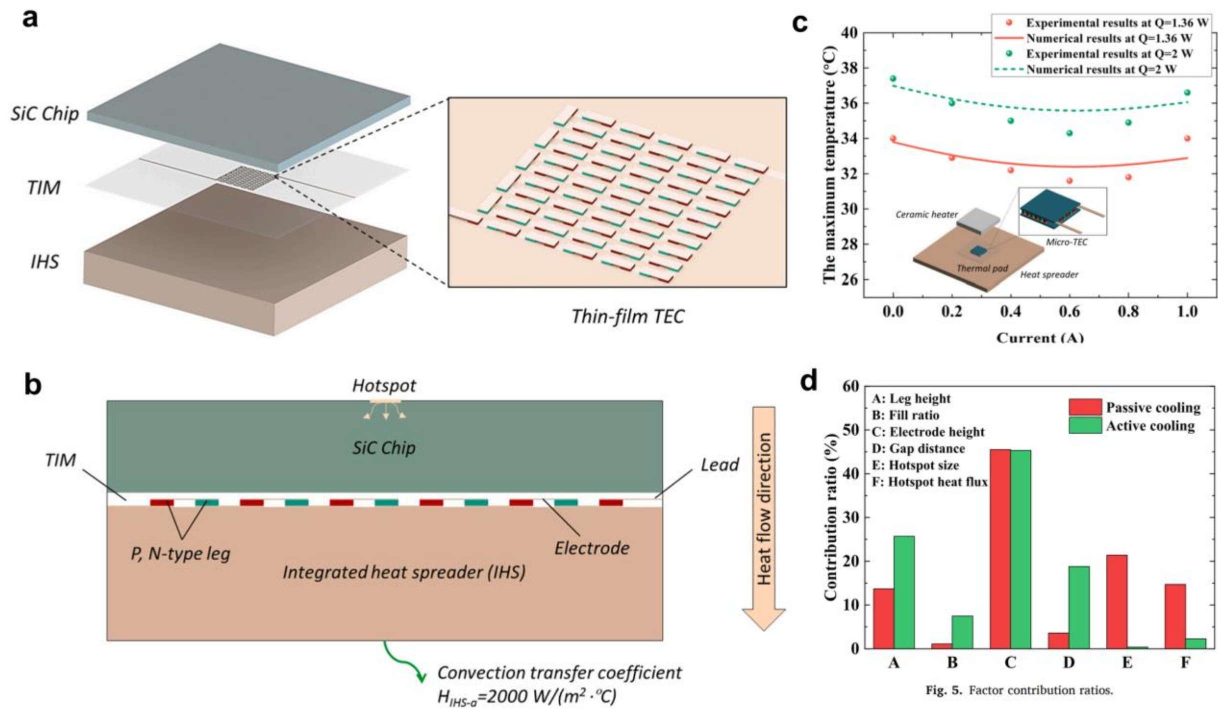

Figure 4 Schematic illustration of the **(a)** main view and **(b)** side view of the 3D electronic package with integrated TECs. **(c)** Comparisons of the simulated and experimented maximum temperature change on the ceramic heater under fixed heating power as a function of input current. **(d)** Contribution ratios of each design factors to the passive and active cooling effect. Reproduced with permission [72]. Copyright 2022, Elsevier.

2.4 Basic Thermal Management of TECs on the Chip

The main consideration of thermal management of chips focuses on the thermal resistance for the whole die package as well as the heat flux density dissipated by the chips [26, 76, 77]. The main die packages can be divided into two type, which are two-dimensional (2D) architecture and three-dimensional (3D) architecture [76]. 2D architecture die package is defined as interconnecting the silicon chips side-by-side on a package [76]. In addition to traditional 2D architecture, in order to achieve higher interconnect density, by applying different mediums, the enhancement of the interconnection between the silicon chips can be called 2D enhanced architecture [76]. The mediums can be further categorized as organic and inorganic medium,

and can generate sub-categories of 2D enhanced architectures, which is 2DO (2D Organic) and 2DS (2D Si-based) [76]. In terms of 3D architecture, two or more chips are always vertically stacked, which can effectively increase efficiency due to higher bandwidth and low-latency communications [76]. Besides, the method of chip stacking can also provide more available space on the substrate. However, the 3D stack has higher thermal resistance than the 2D package since the 3D stack has extra interconnect/underfill layers and the back-end-of-the-line (BEOL) layers [76]. Therefore, the vertical model of the 3D stack may cause a higher temperature within the package. To solve this issue, an ideal thermal management method should be developed to cool the stack through both the bottom and top to generate the double cooling capacity, but the corresponding design is very complex [76].

In recent years, TECs are receiving increasing attention due to their high reliability, high cooling heat flux, and ability to locally cool the hotspot and be integrated with chips [8, 26, 35, 77]. **Figures 5(a)** and **(b)** present the schematic diagrams of ultra-thin TECs integrated with the 2D and 3D chip packages, which show that the TECs can be easily attached to the two main chip packages and provide the cooling capacity [40, 76]. The temperature distribution within the chip package can be explained by the Fourier' conduction equation, expressed as [8, 40]:

$$\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} + \frac{\partial^2 T}{\partial z^2} + \dot{Q} = \frac{\partial T}{\alpha \partial t} \tag{20}$$

and within the TEC, expressed as [40]:

$$\dot{Q} = \frac{I^2}{A^2 \sigma \kappa} \tag{21}$$

where α is the thermal diffusivity, I is current, and A is the area of an element. The cooling heat flux at the cold side of TEC can be obtained when applying the boundary conditions, expressed as [8, 40]:

$$q''_{TE.c} = \frac{-SIT_c + I^2 R_{ec}}{A} \tag{22}$$

Similarly, the heating heat flux can be obtained when applying the appropriate boundary conditions, expressed as [8, 40]:

$$q''_{TE.h} = \frac{SIT_h + I^2 R_{ec}}{A} \tag{23}$$

where R_{ec} is the electric contact resistance. The *SIT* refers to the thermoelectric cooling power, and I^2R_{ec} is the Joule heating from the electric contact resistance at the interfaces between the thermoelectric element the metallization layer, and the interfaces between the thermoelectric module and heat spreader layer [8, 40].

So far, Fourier's conduction simulation models have been developed to analyze the vertical cross-section temperature contours of the chip bottom surface, and the hot side and cold side of TECs [40, 78, 79]. For example, the simulation model was developed to analyze the operation of TECs with dimensions of 3.5 mm × 0.008 mm × 3.5 mm on the hotspot of chips [40]. **Figure 5(c)** illustrates the temperature contours in a vertical cross-section of a 2D electronic package [40]. Besides, the computational results also indicate that the response time of the Peltier cooling is lower than the Joule heating, leading to that TECs reach the steady-state operation in a short time when applying the high amplitude transient current [40]. This effect enables TECs being effective on-demand cooling devices on the hotspot, which can reduce the temperature below the steady-state of running TECs [40]. **Figure 5(d)** illustrates the ΔT of hotspot of chips in 2D electronic packages when applying the different currents on TECs [40]. The ΔT of hotspot can reach the steady-state 10 °C cooling within 0.06 s when applying a current of 6 A, and higher amplitude currents can promote the Joule heating to become more significant than the Peltier cooling, and lead to the cooling temperature firstly reaching the lower value and then gradually increase to the steady-state [40]. This effect can effectively provide the extra cooling capacity in the transient operation of TECs [40]. After that, the stacking 3D package with 3 mm × 0.008 mm × 3 mm TECs was also analyzed through the same simulation model, and found that the nonuniform power density from the 3D stacking

technology can cause time and space-varying hotspot, but these challenges can be solved by TECs since their characteristics of high response time and transient cooling are suitable for the on-demand and localized cooling on chips [78, 80]. **Figure 5(e)** illustrates the temperature contours in a horizontal plane through the bottom chip, which shows the hotspot temperature [78]. **Figure 5(f)** shows the variation of hotspot temperature with the applied current in TECs [78]. When applying the current of 1.75 A and 0.75 A through the TECs, the maximum cooling on the bottom hotspot and top hotspot can reach 5.6 °C and 0.9 °C [78]. However, the contact resistance is significant in the stacking package model, and strong vertical coupling between the top and bottom chips can lead to the bottom chips heating the top hotspot during the operation [78]. Hence, the rational design, the control of contact resistance, and appropriate current are critical for applying TECs in the 3D stacking package.

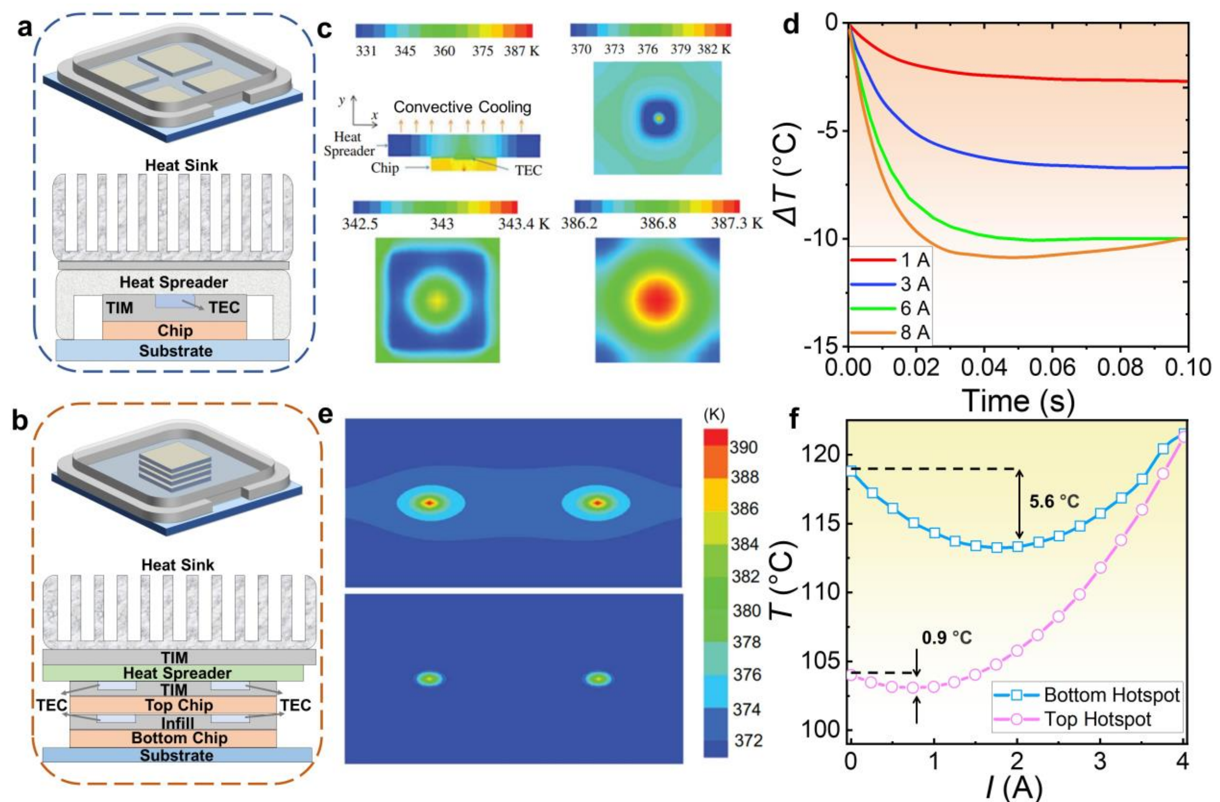

Figure 5 (a) Schematic of a 2D electronic package containing heat spreader, heat sink, thermal interface material (TIM), thermoelectric cooler (TEC), chip, and substrate. **(b)** Schematic of a 3D stacking electronic package containing heat spreader, heat sink, TIM, effective resistance

layer (ERL), TEC, chip, and substrate. **(c)** Temperature contours of a vertical cross-section of an electronic package [top-left], bottom surface of the chip [top-right], and cold and hot side of the TEC [bottom-left and right]. **(d)** The temperature difference of hotspot with time when applying the different current amplitudes through the TEC. Reproduce with permission. Reproduced with permission [40]. Copyright 2011, IEEE. **(e)** Temperature contour plot in a horizontal plane through bottom chip showing hotspot temperatures with 0 A [top] and 1.75 A [bottom] through the TEC. **(f)** Variation of hotspot temperature with the applied current in the TEC. Reproduce with permission [78]. Copyright 2013, IEEE.

3. Fabrication and Performance of on-chip TEC

On-chip TECs are normally composed of near-room-temperature thermoelectric materials with high *ZT*s of >0.5 from room temperature to 100 °C. Historically, Bi_2Te_3-based semiconductors, including n-type $Bi_2Te_{3-x}Se_x$ and p-type $Bi_{2-x}Sb_xTe_3$ [27, 37, 38, 81-87], are the prior choices in the commercial TECs because of their outstanding *ZT*s of >0.7 at <350 K, contributing to ΔT_{max} of 60-70 °C in their TECs [88]. Generally, the micro-bulk-based and ultra-thin-film-based TECs are the main TECs used in thermal management of on-chip applications since the smaller cross-section and shorter length of thermoelectric legs are easier to be integrated with various portable devices [89, 90]. So far, in addition to Bi_2Te_3-based semiconductors, there have been several new materials investigated in micro-bulk and ultra-thin-film TECs, including Si-based material such as holey Si and Si nanowires [36, 91-94], SiGe [25], carbon-based materials such as graphene sponges [95-97], oxides such as $Al_{0.02}Zn_{0.98}O/Ca_3Co_4O_9$ [24], zintls such as $Mg_3Bi_xSb_{2-x}$ [98], $Cu_{0.9}Ni_{0.1}AgSe$ [99], $CsBi_4Te_6$ [100], and superlattice materials [10, 26, 31, 101]. Besides, several materials have considerable potential to be the materials of TEC due to their high thermoelectric performance around the ambient temperature but still lack studies on their cooling performance, including semimetals (CoSi [102], Cd_3As_2 [103]), n-type

Ag_2Se [102], p- and n-type SnSe [104-107], and GeTe with improved near-room-temperature performance after tuning the phase transition temperature [108-113].

3.1 Micro-Bulk

Micro-bulk-based TECs possess conventional vertical sandwich structures but only have micro-meter or nano-meter dimensions [114]. Compared to the planar thin-film structures, vertical bulk structures have lower electrical resistance and no extra energy loss through a substrate, but the bonding of thermoelectric legs and the upper electrode is difficult in the micro dimensions, which is the main challenge for the fabrication of the micro-bulk TECs. However, several technologies, including flip-chip technology [115], electroplating [116], photolithography [116], complementary metal-oxide-semiconductor (CMOS) [36], and electrochemical deposition (ECD) [117], have been developed to solve this issue. Flip-chip technology is normally used to deposit the semiconductor chip to the solder bumps of the external circuitry on the chip pad. This method was found to have the potential to effectively deposit the electrode onto the micro-sized thermoelectric legs, and have been successfully bonded the electrode to the Bi-Te and Sb-Te micro-thermoelectric legs, fabricated by the electrodeposition [115]. The fabricated TEDs consist of 242 pairs of legs with a thickness of 2.5-20.2 μm [115]. Besides, the process of pulsed electroplating with photolithography was also used to fabricate the micro-bulk TEDs, and the fabricated legs only have a diameter of 200 μm and a thickness of 10 μm [116]. Electrochemical deposition is regarded as a method that has the advantages of cost-effectiveness, impressive thermoelectric performance, and potential fabrication of thick film [117]. A TED was fabricated through ECD to integrate the materials inside the self-supporting flexible substrate, and the diameter and thickness of thermocouples were 600 and 200 μm [117].

There are several novel on-chip micro-bulk TECs developed in recent years. As illustrated in **Figure 6(a)**, a micro bulk TEC with four vertical layers contain the substrates, the bottom

contact, the thermoelectric elements, and the top bridge contact, fabricated by the modified ECD and standard photolithography [37]. Compared with the conventional method, the main modification of ECD is that thermoelectric materials (n-type $Bi_2(Se_{0.1}Te_{0.9})_3$ and p-type $(Bi_{0.25}Sb_{0.7})_2Te_3$) were transferred to the bath of Au electrolyte after each deposition during the fabrication [37]. It can electroplate 1 μm Au layer on the top of the leg, and effectively avoid oxidation in the following process while further reducing the contact resistivity between the Au and legs [37]. **Figure 6(b)** presents the top-view of the TECs through scanning electron microscopy (SEM) [37]. The fabricated p- and n-type legs only have a width of 30 μm and length of 40 μm, and 220 leg pairs can be integrated within a 2 × 2 mm^2 substrate area [37]. **Figure 6(c)** shows the experimental and simulated net cooling temperature of two leg pairs in the electric current range 5-140 mA at room temperature [37]. When applying 100 mA current through the TECs, the net cooling temperature can reach 6 °C [37]. Besides, the stable net cooling temperature can last 30 days with a constant direct current of 70 mA [37]. **Figure 6(d)** illustrates the Si nanowires (SiNWs) fabricated by the top-down CMOS process on an 8-inch silicon wafer, and electrically connected in series via TaN/Al on the top and silicon substrate at the bottom [36]. **Figure 6(e)** shows the SEM images of SiNWs with lengths of 1.1μm and 0.6 μm [36]. **Figure 6(f)** illustrates the ΔT varying with the voltage and different length (1 μm, 2 μm, 3 μm) of SiNWs. As can be seen, the optimum voltage and ΔT_{max} are 0.07 V and 27 °C [36]. These results indicate that the SiNWs possess great potential for the thermal management of microchips.

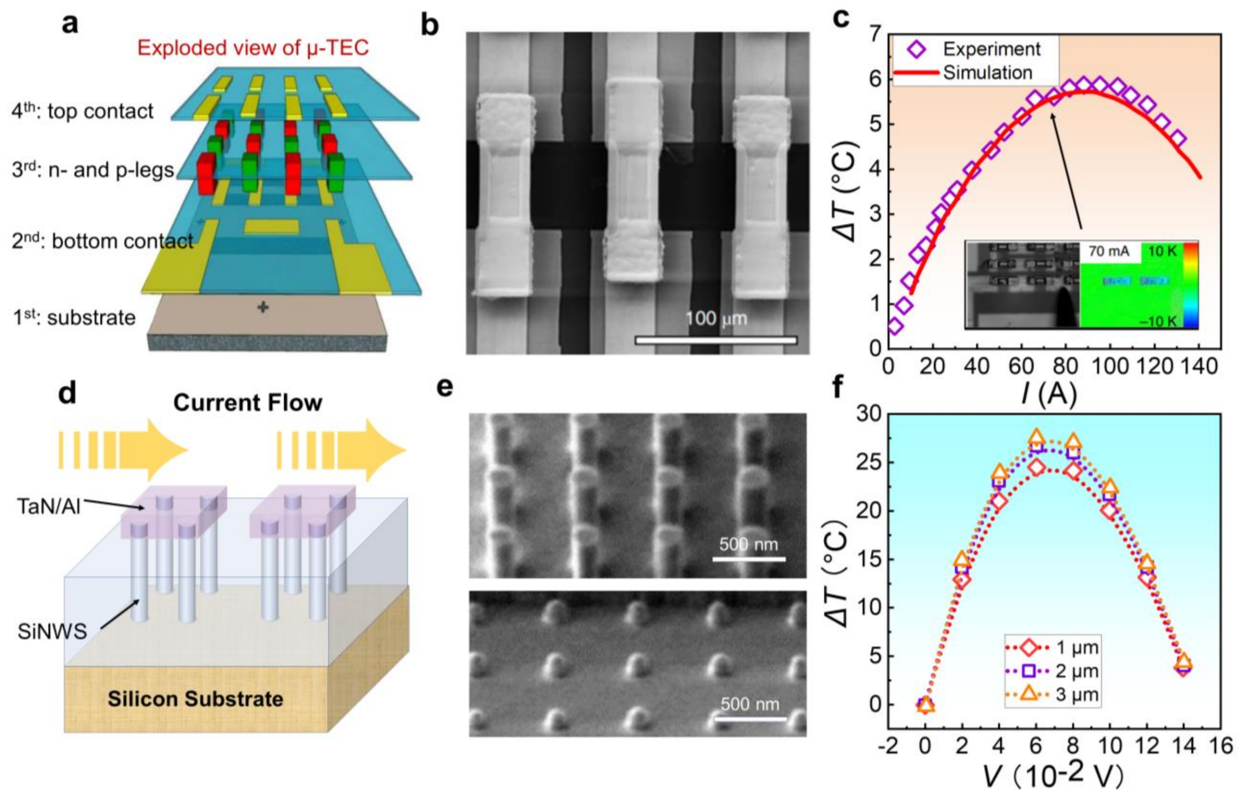

Figure 6 **(a)** Schematic fabrication process for integrating the four layers of micro-bulk TECs. **(b)** Corresponding SEM views of the top-side of the TEC device. **(c)** Experimental and simulated net cooling temperature of two leg pairs in the electric current range 5 - 140 mA at room temperature ~ 20 °C. Inset: optical and thermo-reflectance images with an applied electric current of 70 mA. Reproduce with permission [37]. Copyright 2018, Springer Nature. **(d)** Schematic illustration of the fabrication process of SiNWs. **(e)** Corresponding SEM images of SiNW with length 1.1 μm and its exposed tips after SiO_2 etch back. **(f)** Comparison of ΔTs in different lengths of SiNWs as a function of operating voltages. Reproduce with permission [36]. Copyright 2012, Springer Nature.

In addition to the TECs used for the computer chips, the micro-bulk TECs for light-emitting diodes (LEDs) were also developed. LEDs are widely used for display backlighting, communications, medical services, signage, and general illumination [118, 119]. Similarly, LEDs are normally designed as a micro-chip, and heat flux production and operating temperature increases with the miniaturization of LEDs, so the TECs are also regarded as the

effective thermal management solution of LEDs [38, 74, 120]. **Figure 7(a)** illustrates the fabrication process of the TEC on LEDs. The elements (p-type $Bi_{0.5}Sb_{1.5}Te_3$ and n-type $Bi_2Te_{2.7}Se_{0.3}$) were placed into the rubber mold for alignment and then were welded on the copper layer of the substrates, which was fabricated by the direct plated copper technology [38]. The fabricated TECs have the size of $11.5 \times 11.5 \times 3.15$ mm^3 and consist of 17 pairs of elements [38]. **Figure 7(b)** shows the thermal infrared images of the cold-side surface of the TEC at the input current of 0.5, 1.0, 1.5, and 2.0 A, respectively [38]. **Figure 7(c)** illustrates the temperature and voltage of the TEC when applying different input currents [38]. The maximum voltage and lowest temperature can reach 3 V and -23 °C [38]. **Figure 7(d)** presents the maximum temperature of the LED chip with TEC on and off as the function of the input current. The results indicate that the TEC can reduce the chip temperature from 232 °C to 114 °C when the input current of 1 A. Besides, the light density with TEC on is higher than the light density with TEC off [38]. These results indicate the micro-bulk TEC has massive potential for portable electronics, especially on-chip cooling.

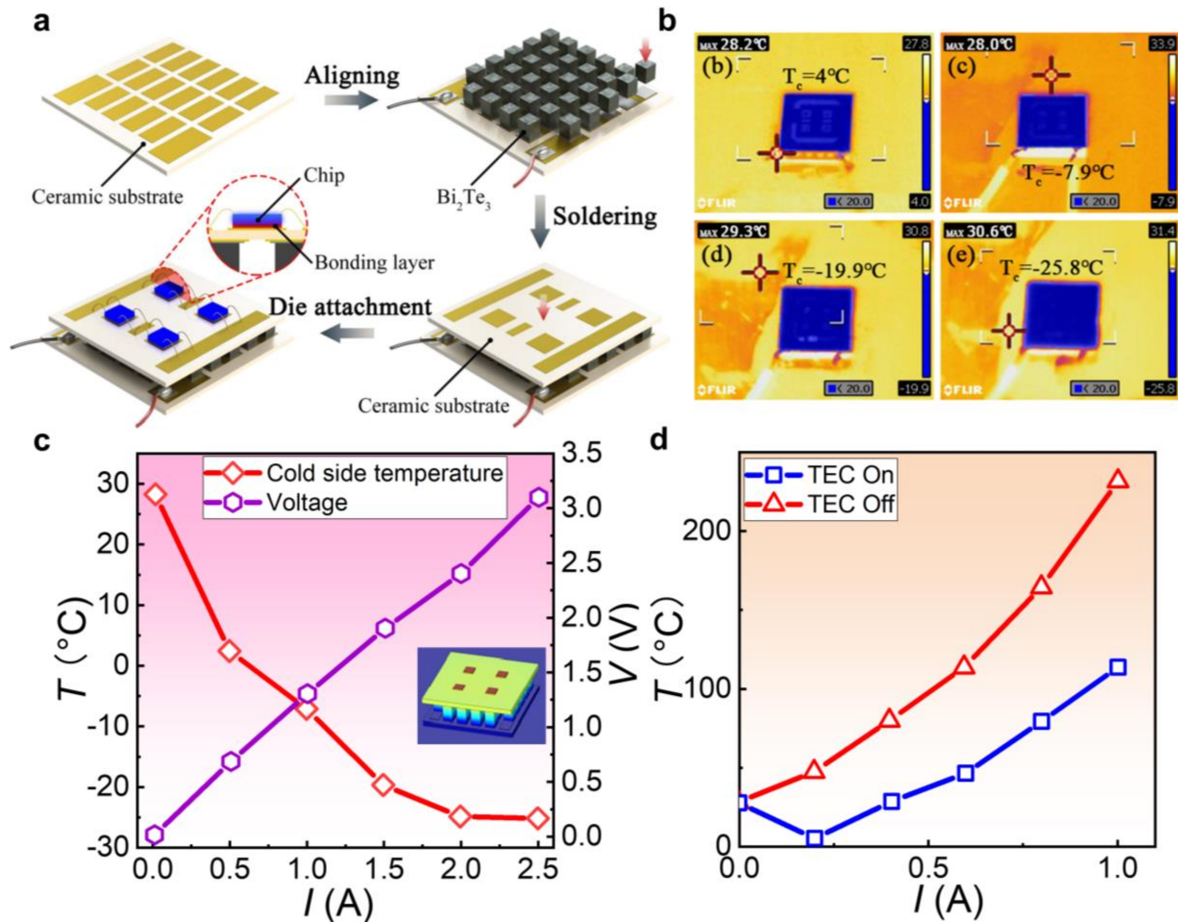

Figure 7 (a) Schematic illustration of fabrication and packaging process of LED with TECs. **(b)** Corresponding thermal infrared images of the cold surface of TEC at the input current of 1.0 and 2.0 A. **(c)** The cold-side temperature and voltage of TEC as a function of input currents. **(d)** Comparison of the chip temperature with TEC on and off as the function of input current. Reproduce with permission [38]. Copyright 2021, IEEE.

3.2 Film-Based

Film-based TECs are defined as the TECs with a planar-radial structure. Compared with micro-bulk TECs, film-based TECs have lower thickness and are easier to be integrated with portable electronics [121-127]. However, film-based TECs normally face issues about the parasitic heat loss on substrates. Hence, several methods have been investigated to solve this issue, which contains eliminating the support substrate or membrane to avoid the parasitic heat loss [25],

developing the unique design of TECs to maximize the effective cooling area ratio [32], and optimizing the thickness and materials of the TECs to maximize the cooling performance [27, 128, 129]. **Figure 8(a)** illustrates the design of the free-standing planar structure [25]. Compared to the conventional design, there are no supporting substrates and membranes in design, which address the issues about parasitic heat loss [25]. The thermoelectric legs are fabricated by the high-performance nano-grained SiGe thin films via standard low-pressure chemical vapor deposition [25]. The thermoelectric legs connect the external substrates and heat-sink (hot-side) to the central SiN_x square island (cold-side) [25]. **Figure 8(b)** presents the SEM image of the single-stage film-based TECs [25]. The dimension of the devices is 420 × 420 μm^2, in which the thickness of the n- and p-type thermoelectric legs is only 1 μm, and the area of the central square (cold-side) is 100 × 100 μm^2 [25]. Besides, the contact resistance at the end contact was also investigated, and was improved by applying the Ti/Al metal connections instead of the conventional Cr/Pt metal connections [25]. **Figure 8(c)** compares the ΔTs as the function of input current under different contacts [25]. The ΔT of improved contact is significantly higher than the conventional design, in which the $\Delta T_{\max}$ can reach 10.37 K [25]. In addition to eliminating the supporting substrate, optimizing the thickness of planar thermoelectric legs can effectively reduce the Joule heating effect on the cooling performance. **Figure 8(d)** illustrates the fabricated film-based TECs [27]. The fabrication process was applying the co-evaporator to deposit the n-type Bi_2Te_3 and p-type Sb_2Te_3 on the polyimide (PI) substrates [27]. The size of the fabricated legs was only 2.5 cm × 3.75 cm [27]. **Figure 8(e)** presents the temperature profile and total heat flux of TECs from the ANSYS simulation, which shows the average heat flux flow through the thermoelectric legs is above 36 mW/mm^2 [27]. **Figure 8(f)** illustrates the temperature changes of the cold and hot junction of n- and p-type legs as a function of the ratio of the thickness (n/n + p) at input current ~ 10 mA [27]. It can be seen that the optimum n- and p-type thicknesses are 5.05 μm and 5.45 μm [27]. Besides,

the ΔT_{max} between the cold and hot junction of 1-pair optimized TEC can reach 1.3 °C [27]. These results indicate the planar thin-film TECs pose massive potentials on active cooler systems, especially control hotspot in portable electronics.

In addition to eliminate the support substrates and adjust the thickness of TECs, novel planar-radial design improves the cooling performance and effective cooling area. **Figure 8(g)** illustrates a design of planar-radial structured TEC [32]. The TEC was fabricated by depositing the n-type Bi_2Te_3 and p-type Sb_2Te_3 thin film on the PI substrates via a co-evaporator [32]. The total area of the thermoelectric legs was 68.89 mm^2 with an optimized thickness of 5.05 μm for n-type legs and 5.45 μm for p-type legs [32]. Five pairs of n-type and p-type legs were constructed with a radial leg structure, and connected in series by Cu electrodes [32]. **Figure 8(h)** presents the thermal image of a chip with 5-pair TEC at input current of ~ 10 mA, and shows that the ΔT_{max} between hot and cold junctions are 1.7 °C and 2.4 °C, respectively [32]. **Figure 8(i)** illustrates the temperature changes of the hotspot on the chip according to the operation of TECs (10 mA) [32]. When 2 W input power was applied to the chip, the temperature of the chip can reach 90 °C, and can be continuously cooling approximately 2.42 – 3.87 °C while operating the TECs [32]. These results indicate that the effective design of TECs is one of the most potential candidates for the thermal management of chips, especially in the mobile environment.

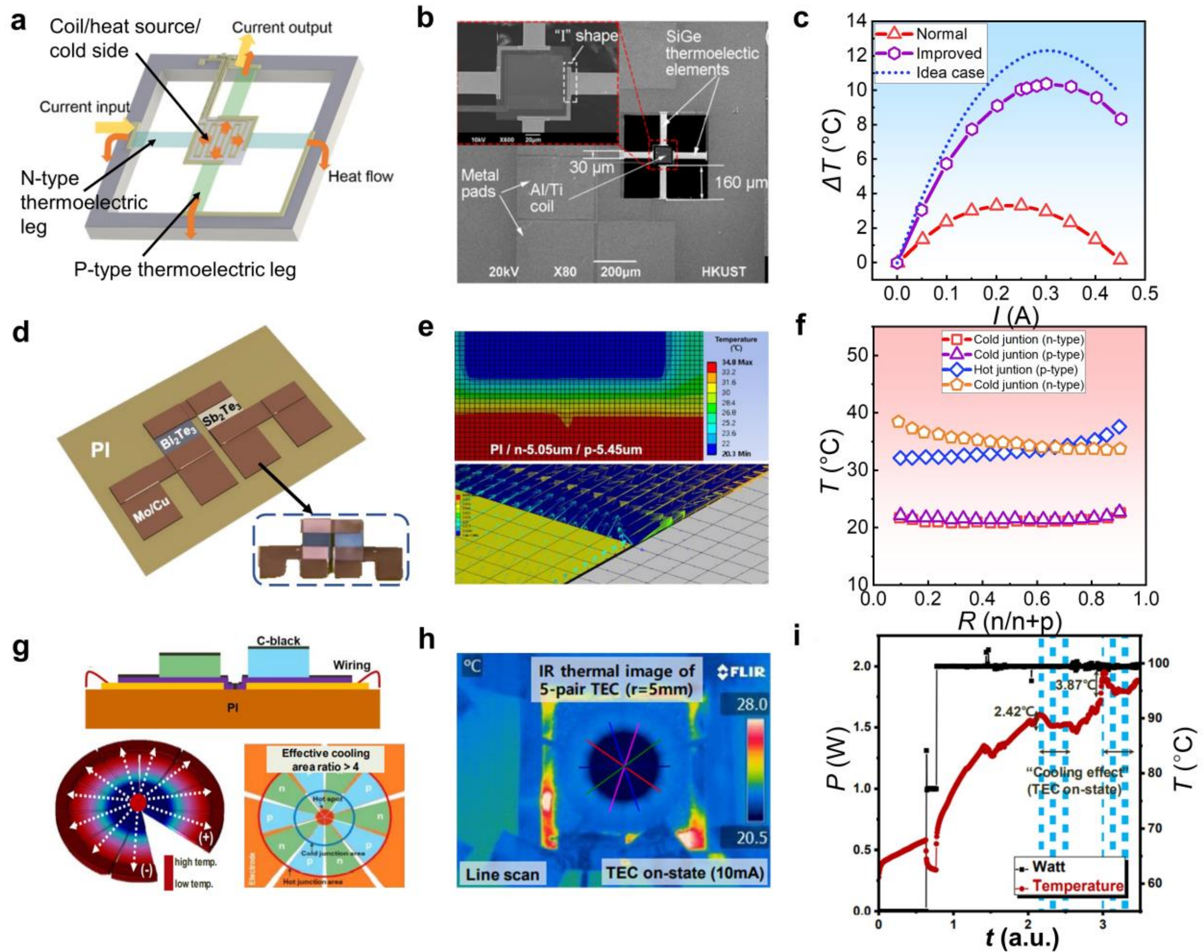

Figure 8 (a) Schematic illustration of the free-standing planar design of TECs. **(b)** SEM image of single-stage film-based TEC. Inset: the central coil and the contacts of I-shaped thermoelectric legs at the cold side. **(c)** Comparison of the steady-state cooling performance of TECs with different contact designs as a function of input current. Reproduce with permission [25]. Copyright 2018, Elsevier. **(d)** Schematic image of a 1- pair TEC on the PI substrate with a thickness of 5.05 μm n-type and 5.45 μm p-type TE leg. **(e)** Corresponding specific images about the heat flux analysis and temperature profile of TEC. **(f)** Comparison of temperature change of hot and cold junction in different ratios of TE film thickness. Reproduce with permission [27]. Copyright 2019, Springer Nature. **(g)** Schematic illustration of the novel planar-radial structured TEC. **(h)** Corresponding thermal infrared images of the chips with the TEC at the input current ~ 10 mA. **(i)** Temperature change of hotspot on chips according to the TEC operation (10 mA). Reproduce with permission [32]. Copyright 2020, IEEE.

3.3 Advanced Structure

In addition to microbulk and film-based TECs, there are many novel structures and designs developed with the rise of TECs on hot spot management, which exhibits extra properties such as stretchability and compatibility. For example, holey silicon-based lateral TECs were fabricated by depositing the Peltier cooler (cold side) and ground electrode (hot-side) on top of the Si substrate to form Peltier junctions [91], as shown in **Figure 9(a)**. Silicon-based TECs offer advantageous attributes that facilitate the integration with electronics. In addition to the high compatibility with electronics, holey silicon-based TECs also have shown the advantages of the low in-plane κ caused by the substantial phonon boundary scattering in small necks, which can keep a large temperature gradient junction [91]. Besides, the neck size and trench depth of holey silicon are the critical factors that affect the phonon boundary scattering, so appropriate adjustment of design of neck size and trench depth can optimize the cooling performance under specific conditions [91]. **Figure 9(b)** presents the ΔT of TECs as the function of applied current with 1.9, 3.0, 3.4, and 4.4 μm-wide necks under 100 °C background temperature, which indicates the optimized neck size (3.4 μm) can promote the higher cooling performance of TECs [91]. **Figure 9(c)** presents the ΔT of TECs as the function of applied current with 0, 21, and 25 μm-deep trenches under 100 °C background temperature [91]. As the result, when the background temperature was 100 °C, the holey silicon with 1.9 μm-wide necks and 21 μm-deep trenches can reduce 1.2 °C of hotspot temperature [91].

With the development of stretchable electronic devices and displays, stretchable TECs as stretchable heat-dissipation strategies are necessary. **Figure 9(d)** and **(e)** illustrate the design of the stretchable TECs. The stretchable TECs are fabricated by placing the Bi-Te TE legs on the stretchable elastomers and then connected with the liquid metal electrode (Galinstan) [130]. **Figure 9(f)** presents the temperature drop of the top surface of the device (ΔT_{top}) at the different

strains (0 %, 10 %, 20 %, 30 %) under a constant conduction heat load of 0.8 W [130]. The results show the maximum ΔT_{top} can reach 1.31 K at 30 % strain, which indicates the stretchable TECs pose massive potential on active cooler systems, especially control hotspots in stretchable electronics [130].

In addition to optimizing the structures of TECs, an appropriate design base on the thermoelectric interface materials (TEiMs) is also the key to optimizing the electrical contact and stability of the interface between thermoelectric materials and metal electrodes [81, 131]. The conventional CMOS process typically deposits TE materials and electrodes in stacks, resulting in the connection being mainly based on van der Waals rather than solder [81]. It can cause the element interdiffusion between TE materials and electrode, thereby resulting in additional electrical resistance. Therefore, rational choice and design of TEiMs can optimize the electrical contact and also can exhibit as the diffusion barriers for the thermoelectric materials [81]. **Figure 9(g)** presents the fabrication process for thin-film TECs through the magnetron sputtering system to deposit Bi-Te thermoelectric materials, TEiMs, and Cu films on the Si/SiO2 substrate, which can avoid the stack of the TE materials and electrodes and thereby optimizing the cooling performance of TECs [81]. **Figure 9(h)** shows the maximum temperature difference (ΔT_{max}) without or with different TEiMs (Cr and Ag) on the original devices. The ΔT_{max} can achieve 72.14 K when Ag is the TEiM on both p-type and n-type TE materials [81]. **Figure 7(i)** presents the maximum cooling flux ($Q_{c,\ max}$) without or with different TEiMs (Cr and Ag) on the original devices [81]. The $Q_{c,\ max}$ can achieve 300.04 W/cm^2 when Ag is the TEiM on both p-type and n-type TE materials [81]. These results indicate that the effective design of TEiMs for TECs possess great potential for the thermal management of microchips.

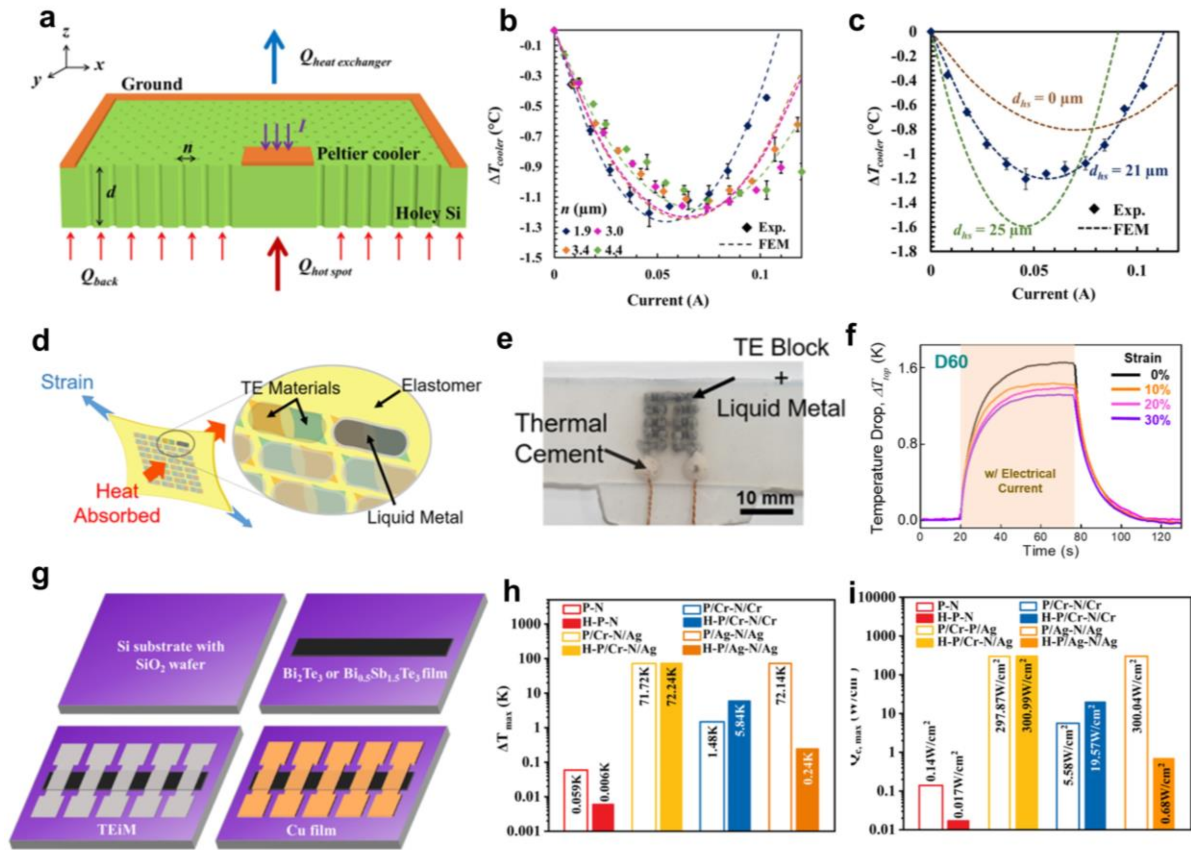

Figure 9 **(a)** Schematic illustration of the holey silicon-based TEC for hotspot cooling. Metal electrodes are used as the Peltier cooler and ground electrode, respectively. (*n* and *d* are holey silicon neck size and trench depth, respectively.) **(b)** Comparison of experimented and simulated ΔT as the function of applied current with 1.9, 3.0, 3.4, 4.4 μm wide necks under 100 °C background temperature. **(c)** Comparison of experimented and simulated ΔT of TECs as the function of applied current with 0, 21, and 25 μm-deep trenches under 100 °C background temperature. Reproduce with permission [91]. Copyright 2022, IEEE. **(d)** Schematic illustration of the stretchable thermoelectric device. **(e)** Corresponding photograph of the fabricated device. **(f)** Comparison of ΔT_{top} at the different strains (0 %, 10 %, 20 %, 30 %) under a constant conduction heat load of 0.8 W. Reproduce with permission [130]. Copyright 2021, American Chemical Society. **(g)** Schematic illustration of fabrication process for thin-film TECs through the magnetron sputtering system. **(h)** Comparison of ΔT_{max} with and without different TEiMs (Cr and Ag). **(i)** Comparison of $Q_{c,\ max}$ with and without different TEiMs (Cr

and Ag). (The “P−N” refers to model without TEiM. The “P/X−N/Y” refers to model with X, Y as TEiM for p-type and n-type TE leg respectively. The “H” in “H-P/X−N/Y” and “H-P-N” means heat treatment.) Reproduce with permission [81]. Copyright 2022, American Chemical Society.

4. Application of On-chip TECs

With the rapid development of the on-chip TECs, the applications of TECs gradually is integrated into the electronics including smart phones, laptops, and even the intelligent furniture and medical application. [132-134]. **Figure 10(a)** presents the schematics of an array TEC covering the surface of the CPU to produce the TE electricity and dissipate the heat to cool the CPU simultaneously [95]. **Figure 10(b)** shows the corresponding photograph of a 4 × 4 array TEC cover on the CPU [95]. **Figure 10(c)** shows the temperature of CPU and TEC voltage as the function of the time [95]. As the result, compared with the condition without the TEC, the temperature of the CPU can be cooled from 84.6 °C to 76.6 °C with a constant TE voltage ~of 21 mV [95]. These results present that the array TEC poses the practical application potential for the thermal management of the computer chips.

In addition to the conventional computer CPU, the other processors or dies also require the thermal management of TECs. For example, more powerful computing units are required with the rise of machine learning, so the tensor processing units (TPU) gradually become popular due to the efficiency of power usage and throughput compared to GPUs [135]. **Figure 10(d)** presents the finite-element simulation model of the TPU [135]. **Figure 10(e)** presents the superlattice TEC is mounted directly on top of the TPU die without any thermal interface material inside [135]. **Figure 10(f)** illustrates the floorplan of TPU die based on Google’s TPU [135]. The TPU chips are divided into three main areas: Matrix-Multiply Unit (MMU), Unified Memory Buffer (UMB), Auxiliary Management Interface (AMI) [135]. **Figure 10(g)** shows

the thermal map of the baseline TPU die without any active cooling besides convection-based cooling under high load [135]. **Figure 10(h)** presents the thermal maps of the TPU die with the mounted superlattice TEC with an applied current of 5 A [135]. As the result, the hotspot temperature on the TPU can be reduced from 116 °C to 82 °C when the superlattice TEC is mounted on the TPU [135]. These results indicate that the TEC can be indispensable when conventional convection air-based cooling is insufficient.

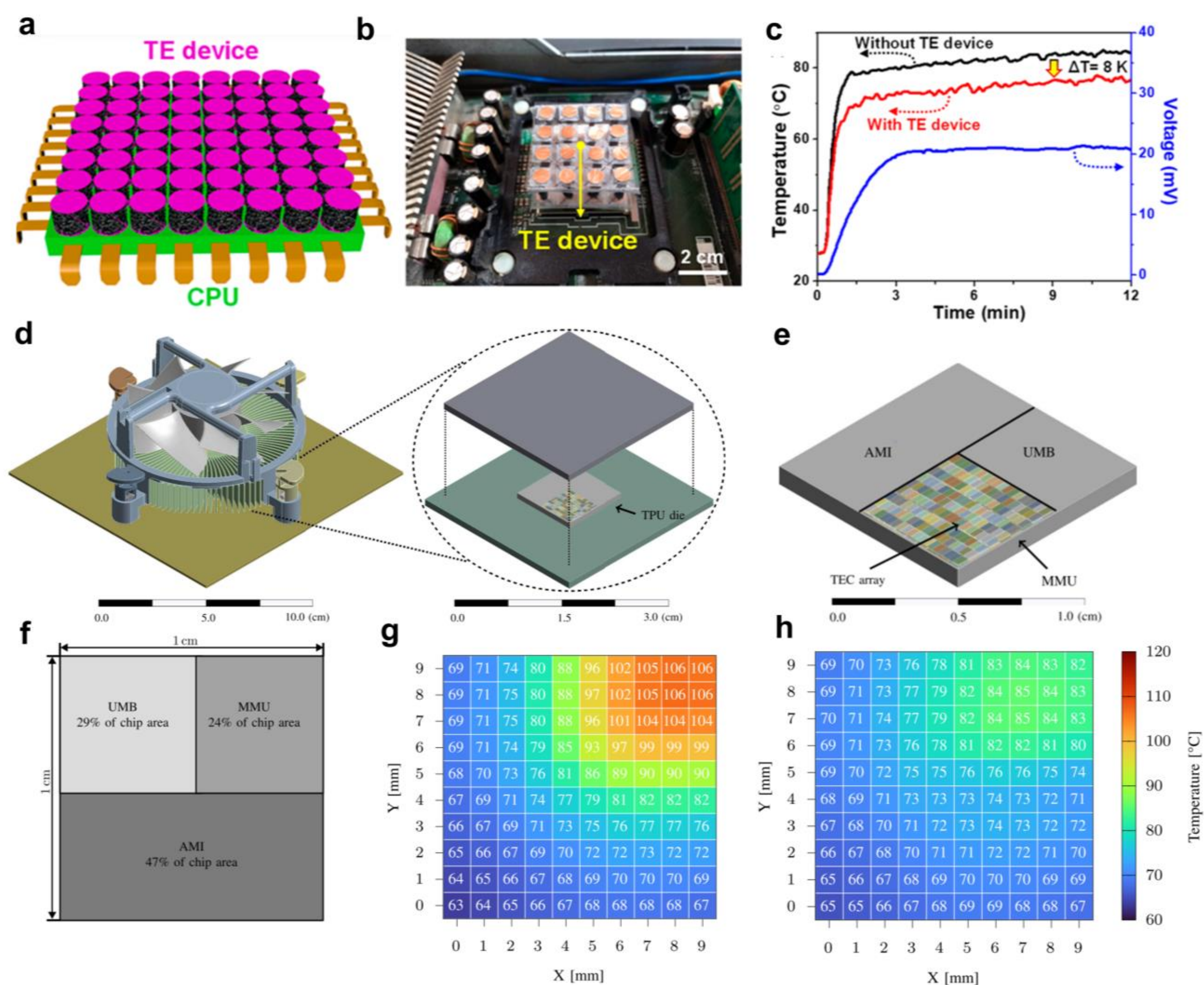

Figure 10 **(a)** Schematic illustration of an array TEC cover on the surface of the CPU. **(b)** The corresponding optic image of a 4 × 4 array TEC is placed on the surface of a normal working CPU. **(c)** Comparison of temperature curves and corresponding TE voltage as the function of time with and without TEC. Reproduce with permission [95]. Copyright 2022, American Chemical Society. **(d)** Schematic illustration of finite-element simulation model of the TPU **(e)**

Schematic illustration of a close-up view of the superlattice TEC mounted on top of the TPU. **(f)** illustrates the floorplan of TPU die based on Google's TPU, including the three main segmentations: Matrix-Multiply Unit (MMU), Unified Memory Buffer (UMB), Auxiliary Management Interface (AMI). **(g)** Thermal map of the baseline TPU die. **(h)** Thermal map of the TPU dies with the mounted superlattice TEC with 5 A of current. Reproduce with permission [135]. Copyright 2022, IEEE.

In addition to the processors or processing units, dynamic random-access memory (DRAM) is also a critical hardware in the electronics, especially in autonomous driving through Deep Neural Networks (DNNs) [136]. DRAM is working as memory, which are built upon bit cells that store charges in capacitors [136]. The advanced driver assistance systems inevitably demand DRAMs to exhibit low latency, high bandwidth, and extreme-low bit error rate to ensure the tight reliability and performance constraints [136]. However, the data retention time and correctness can be seriously affected by the high temperature of DRAMs, so TECs are also regarded as the effective thermal management solution of DRAMs [136]. **Figure 11(a)** presents a photograph of the DRAMs integrated with the TEC [136]. **Figure 11(b)** and **(c)** shows the simulated thermal profile of the DRAM chips integrated with and without the TEC under the ambient temperature of 120 °C [136]. When using the TEC on the DRAMS, the temperature of the four DRAM dies can reduce to 77.5 °C [136]. **Figure 11(d)** presents the impact of the TEC cooling on improving the available bandwidth of DRAM, which the average bandwidth of all benchmarks is improved 31 % [136]. **Figure 11(e)** the average response latency of DRAM is also improved due to the impact of TEC cooling, the average response latency reduction for all benchmarks is up to 30 % [136]. These results indicate that the TEC can be the most potential candidate to improve the reliability and efficiency of DRAM in DNNs.

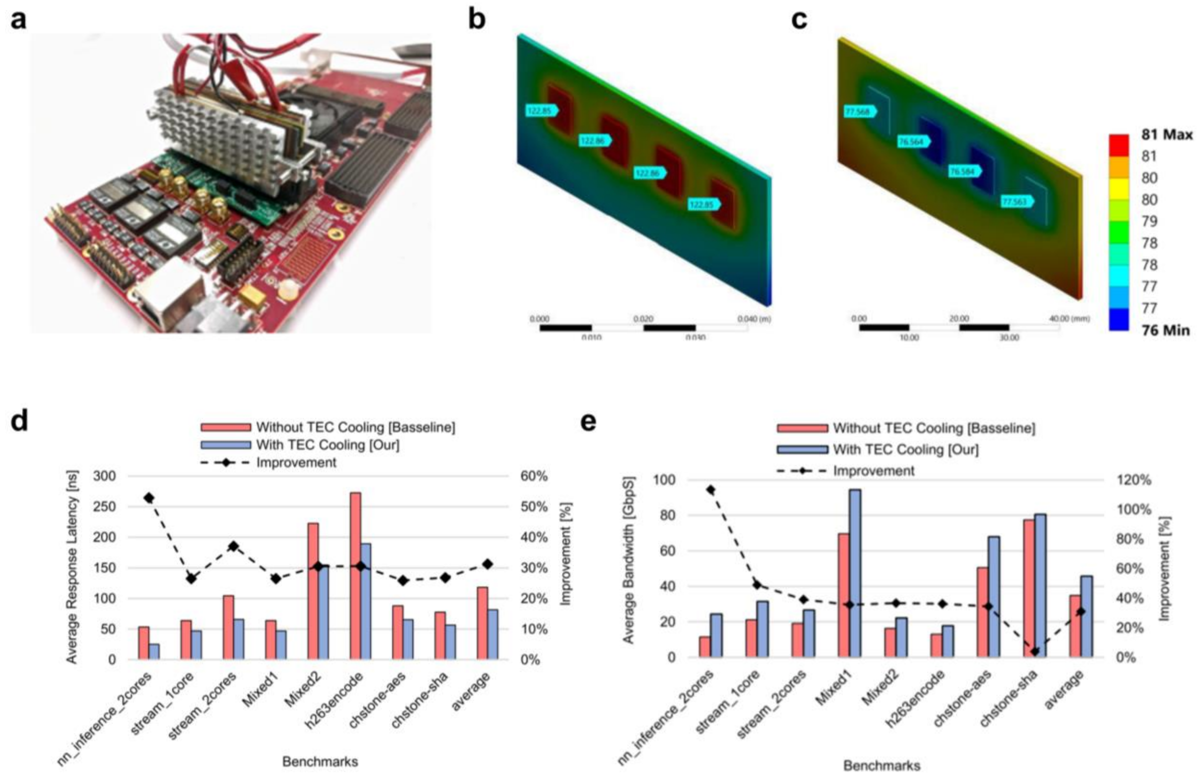

Figure 11 (a) Optic image of DRAM integrated with a TEC. **(b)** Simulated thermal profile of the DRAM integrated without TEC and **(c)** with TEC. **(d)** Impact of TEC cooling in improving the available bandwidth. **(e)** Impact of TEC cooling in reducing the average response latency of DRAM. Reproduce with permission [136]. Copyright 2021, IEEE.

5. System and Design of Thermal Management

With increasing the power density generated by the chips, complex designs of physical heat dissipation solutions have become expensive [137-139]. Hence, on-demand thermal management system have been developed to further optimize the cooling performance by system monitor and control [47, 140]. The on-demand system can apply TECs to alleviate the hotspots, and effectively reduce the Dynamic Thermal Management (DTM) invocations that influence the operating frequency of chips to maximize the on-chip cooling performance [4, 9, 137]. DTM has been widely used in the thermal management of microprocessors to avoid over-temperature during the operation of chips [9, 137]. DTM is a mechanism to monitor the

temperature distribution of chips by using on-chip thermal sensors and regulate and adjust the operation frequency and power accordingly [4, 9]. However, the adjustment of the operation frequency and power by DTM can reduce the performance of chips [47, 137]. Therefore, the TEC with an on-demand system has become the most potential candidate for optimizing the control strategies of DTM and improving the efficiency of thermal management [19, 47, 137, 140]. In most recent, several systems have been developed to optimize the cooling performance of the computer [19, 138, 140] and mobile chips [47, 137], and there are also some systems and designs that allow the self-cooling to supply the TECs [19, 47, 137, 140, 141].

5.1 Fundamental of On-demand and Self-Cooling

On-demand cooling. On-demand cooling can dynamically control TECs to cool the hotspot on the chips according to the operating frequency and temperature of the processors. The main operation logic of the on-demand cooling is maximizing the operating frequency of the chip, while the promised temperature and power are meet the constraints [139, 142]. The power consumption of the chips is related to the operating frequency and the workloads. The processor power consumption is normally expressed as [142]:

$$P_{chip} = P_{chip} + P_{chip} = CV^2 f\alpha + V(\beta_1 T_{chip} + \beta_0) \tag{24}$$

Besides, the thermal model to dynamically control the TEC according to the chip temperature can be expressed as [142]:

$$T_{chip} = T_{amb} + R_{amb}P_h + (R_{TEC} + R_{amb})(P_{chip} - P_c) \tag{25}$$

The system logics of thermal management with the TEC can be expressed as [142]:

Given $\alpha \ and \ T_{amb}$ (26)

Find $\max_{I_{TEC}} f$ (27)

$\boldsymbol{s.t} \ T_{chip} \leq T_{max}$ (28)

$P_{chip} \leq P_{max}$ (29)

where α is the processor activity factor caused by the workloads, f is the operating frequency of the chips, T_{chip} is the temperature of chips, T_{amb} is the ambient temperature, P_{chip} is the power consumption of the chips [142]. T_{max} and P_{max} are the constraints of the maximum temperature and power consumption of the chips, respectively [142]. **Equation (26)** expresses the input parameters to the system [142]. **Equation (27)** expresses the objective of the logic system, which is maximizing the operating frequency of the chips [142]. **Equation (28-29)** express the constraints imposed into the system, in which the temperature and power of the chips are required to be lower than the temperature threshold and power constraint [142].

During the operation of a CPU, the workload and temperature vary dynamically with time [142]. Hence, there are normally two sensors installed in the most portable electronics, in which one sensor is responsible for learning the T_{chip}, and the other is used for monitoring the T_{amb} [142]. The measured T_{chip} and T_{amb} are inserted into **Equation (25)** to calculate the P_{chip}, and then it can be used in the processor power model (**Equation (24)**) to study the α, which is related to the application workloads. Finally, input the α and T_{amb} into the system, the maximum operating frequency of chips with the optimized TEC cooling current can be obtained to achieve the thermal management [142].

Self-cooling. Self-cooling can directly supply the demand power to TECs by applying TEGs to harvest the waste heat from chips [47, 140]. TEGs are installed on the units with the lower temperature to harvest the heat, and then convert to electricity via the Seebeck effect to supply TECs on the hotspots. The design guideline can be summarized as [140]:

$$P_{TEG,generation} \geq P_{TEC,requirement} \quad (30)$$

$$\boldsymbol{s.t}\ T_{cool}^{'} \leq T_{hotspot} \quad (31)$$

$$T_{hotspot}^{'} \leq T_{hotspot} \quad (32)$$

where $T_{cool}^{'}$ is the temperature of the cool area after TEG application, $T_{hotspot}^{'}$ is the temperature of the hotspots after the TEC application, and $T_{hotspot}$ is the temperature of the

hotspots without TECs [140]. **Equation (30)** expresses the objective of the system, which the power generation of TEGs can satisfy the required power from TECs. **Equations (31-32)** are the constraints, that is, the temperature of areas with TEGs and the hotspots with TECs should be both lower than the hotspot temperature without TECs [140]. According to the design guidelines, the proper placement of TEGs and TECs can be identified via repeated experiments [140].

5.2 Computer

TECs with self-cooling designs can reduce the power usage on thermal management as well as sustain the high performance of computer chips. **Figure 12(a)** illustrates an architecture of TECs with the self-cooling (SCOOL) on a computer chip and the heat map of each functional unit when the computer runs the cactusADM [140]. Here, the TEGs are installed on the functional area with lower temperature, and the TECs are installed on the functional areas that generate the hotspot, where the TEGs can harvest the waste heat from the chips and supply the operation of the TECs [140]. **Figure 12(b)** compares the temperature distribution of the chips with and without the SCOOL designs when running the cactusADM. As can be seen, SCOOL can effectively alleviate the hotspots according to the temperature differences between the functional units [140]. **Figure 12(c)** compares the temperature of each functional unit of chips with and without the SCOOL design. As can be seen, the temperature of three hotspots can be reduced by as much as 15.45 °C [140]. **Figure 13(a)** illustrates a 5×5 arrays of miniature commercial TEDs for cooling the computer chips [19]. **Figure 13(b)** displays the TECs and TEGs placed on 15 mm×15 mm chips. **Figure 13(c)** and **(d)** presents the corresponding temperature contours for the chip surface when the TEC-TEGs system is "on" or "off" [19]. These results present that the average hotspot temperature can be reduced from 142.9 °C with "TEC-TEGS OFF" to 70.6 °C with "TEC-TEGs ON" without extra electrical power, indicating

that self-cooling design has the massive potential to become the sustainable thermal management of processors [19].

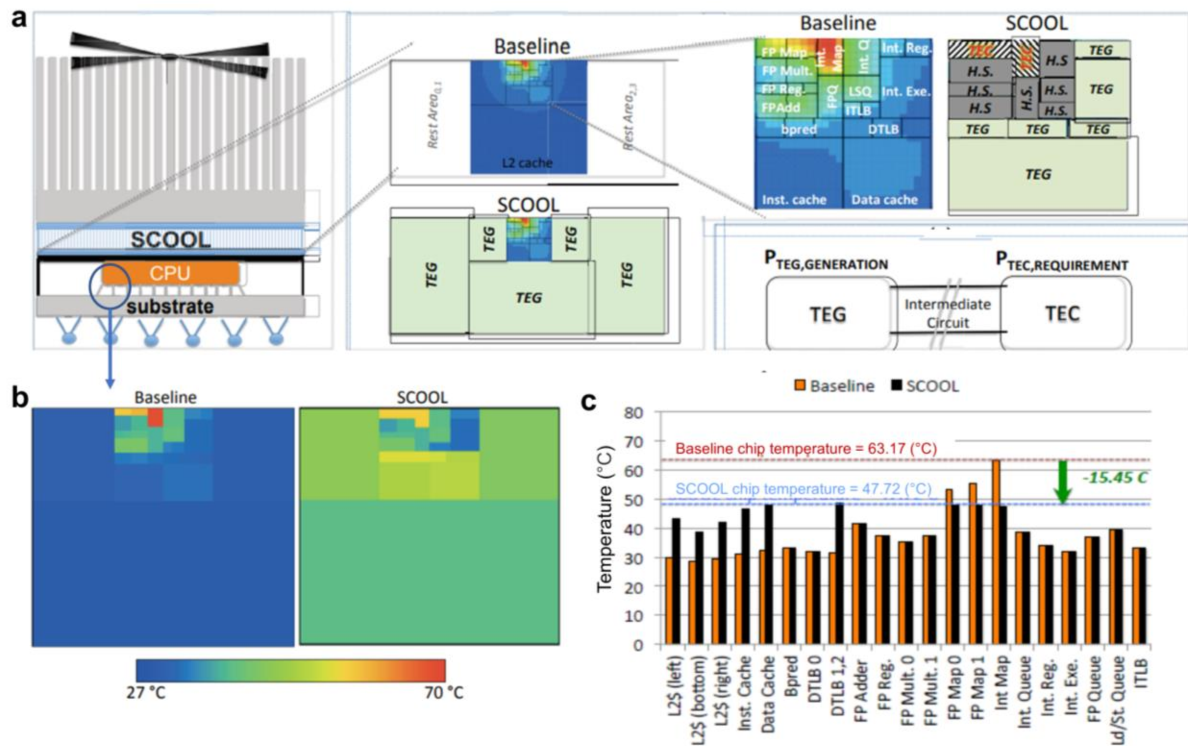

Figure 12 (a) Illustration of the architecture of SCOOL design. Left: the design is placed between the CPU heat spreader and the heat sink in the baseline system. Central: Top-down view of the heat spreader layer with and without SCOOL layer on top of CPU die. Right: Heat map of the temperature of each functional unit on the chips when running the cactusADM, and the intermediate circuit block connects the TEGs with the TEC. **(b)** Comparison of the temperature distribution of the chips with and without the SCOOL design. **(c)** Comparison of the temperature of the various functional units with and without the SCOOL design. Reproduce with permission [140]. Copyright 2016, IEEE.

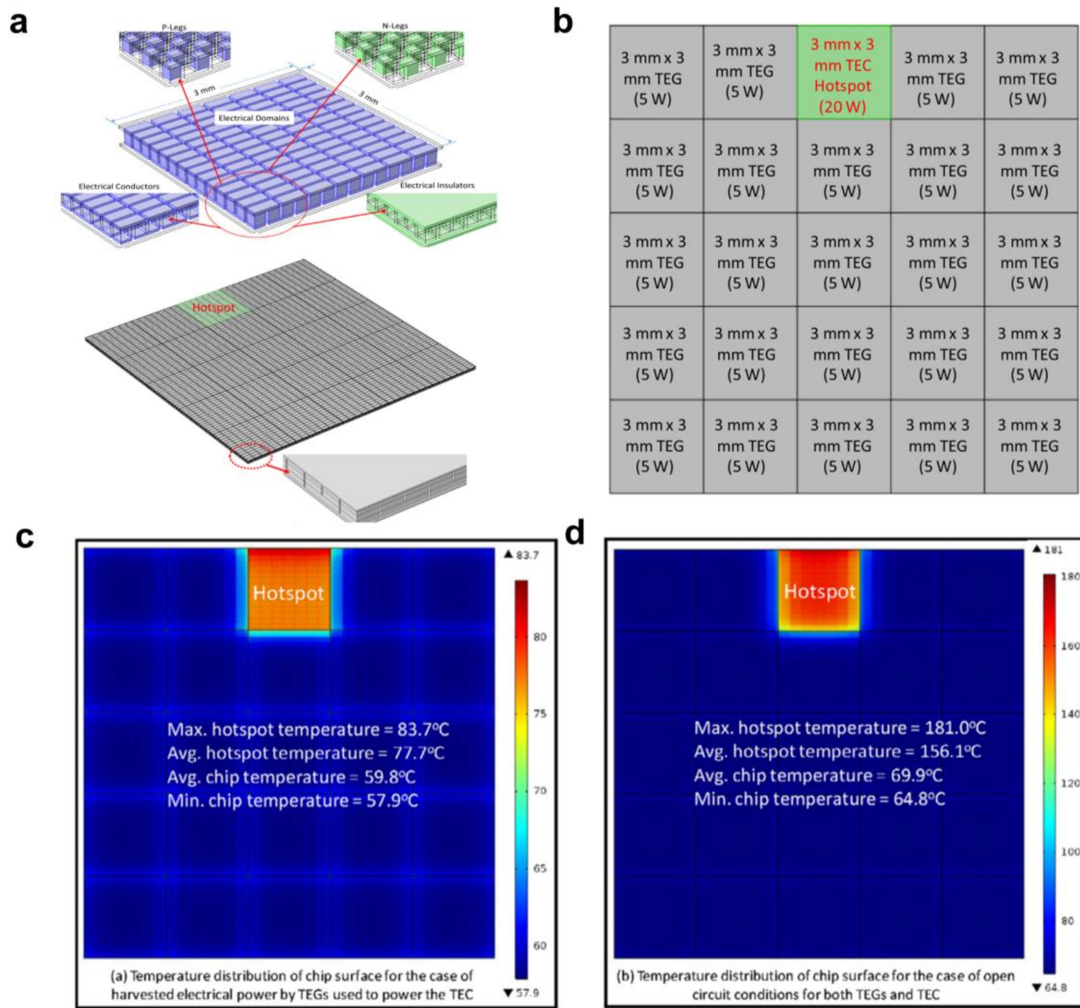

Figure 13 (a) Illustration of a 5×5 thermoelectric array on the computer to for thermal management. **(b)** Thermoelectric modules act as thermoelectric generators (TEGs) and thermoelectric coolers (TECs) that cover on a 15×15 mm^2 chip surface. Temperature contours of the chip surface in the cases of **(c)** "on" and **(d)** "off" of the TEC-TEGs system. Reproduce with permission [19]. Copyright 2020, Elsevier.

5.3 Mobile

The performance and speed of smartphones are significantly improved with the development of semiconductors. Similar to the computer, the advanced function of smartphones requires stronger chips with higher power density, which results in a higher temperature. However, the thermal management of smartphones is more challenging than the computer since the smaller

dimensions, higher power density, and limited energy drain (battery) [47, 137]. Hence, the integration of the on-demand cooling system and self-cooling design is regarded as the most potential sustainable thermal management in the mobile environment. **Figure 14(a)** illustrates the process of the additional layer with dynamic thermal energy harvesting reusing (DTEHR) that install on the mobile [137]. The additional layer was added between the printed circuit board (PCB) board and battery instead of the original air block, and then test the temperature map through running the Layer at the ambient temperature of 25 °C [137]. According to the temperature distribution, the corresponding placements and structure of TECs, TEGs, and micro-supercapacitors (MSCs) are identified, as shown in **Figure 14(b)** [137]. The TEGs and TECs are dynamically controlled by a similar on-demand cooling system according to the operating frequency and temperature of the processors [137]. The system can dynamically switch power generating mode and spot cooling mode. When the processor is under common usages, the power generating mode controls the TEGs to harvest waste energy from the chips [137]. When the hotspot temperature exceeds 65 °C, the spot cooling mode starts to dynamically control the TEC to decrease the temperature of hotspots according to the input power and temperature of processors (on-demand cooling logics shown in **4.1**) [137]. **Figures 14(c)** and **(d)** illustrate the ΔT between the hotspots and cold areas with and without DTEHR on the back cover and internal components, respectively [137]. The results indicate that DTEHR can reduce the temperature difference of internal components by an average of 9.6 °C, and also sustain the surface ΔT of mobile below 6 °C [137]. Similarly, the thin-film thermoelectric array can use the same method to integrate into the commercial multicore mobile chips [47]. **Figure 15(a)** illustrates the floorplan of the mobile chip used for the measurement [47], which indicates the specific location and names of each functional element of the chip. **Figure 15(b)** presents the corresponding hotspot temperature at various points of time on the different cores [47]. The TED on the chips is composed of an array, and each unit

on the array can be either TEC or TEGs according to the chip temperature [47]. **Figure 15(d)** presents the comparison of the temperature captured by the IR camera and temperature from the transient thermal Multiphysics simulation model. The actual and simulated temperature is highly matched, which indicate the accuracy of the simulated model [47]. **Figure 15(d)** shows the temperature reduction of core0 with and without TECs [47]. This result indicates that the average temperature reduction of core0 can reach approximately 10 °C [47]. Besides, the harvested energy when the array is TEGs can compensate for about 89 % of demand energy [47]. These results indicate that the self-cooling design and the on-demand system can be the most potential candidate to solve the hotspot issues and achieve sustainable thermal management.

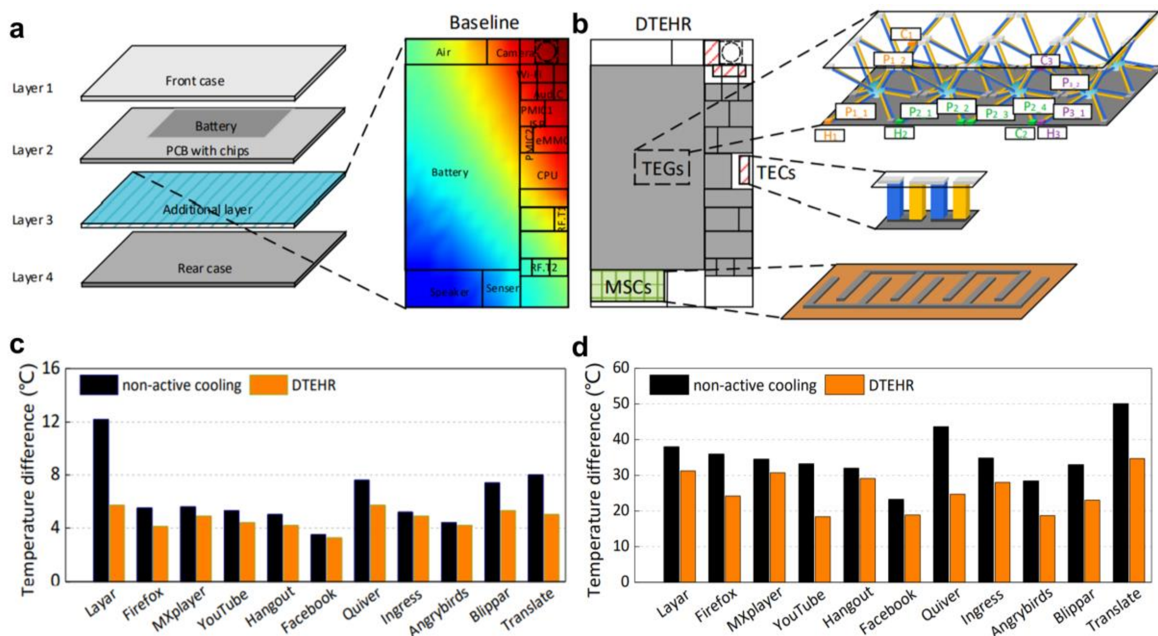

Figure 14 (a) Illustration of the process of the additional layer with DTHER is installed between the rear case and PCB of the mobile, and the corresponding temperature map. **(b)** Illustration of the placement of TECs, TEGs, and MSCs on the additional layer, and their corresponding structures. The temperature difference between hotspots and cold areas with and without DTHER: **(c)** the back cover, **(d)** the internal components. Reproduce with permission [137]. Copyright 2018, ACM.

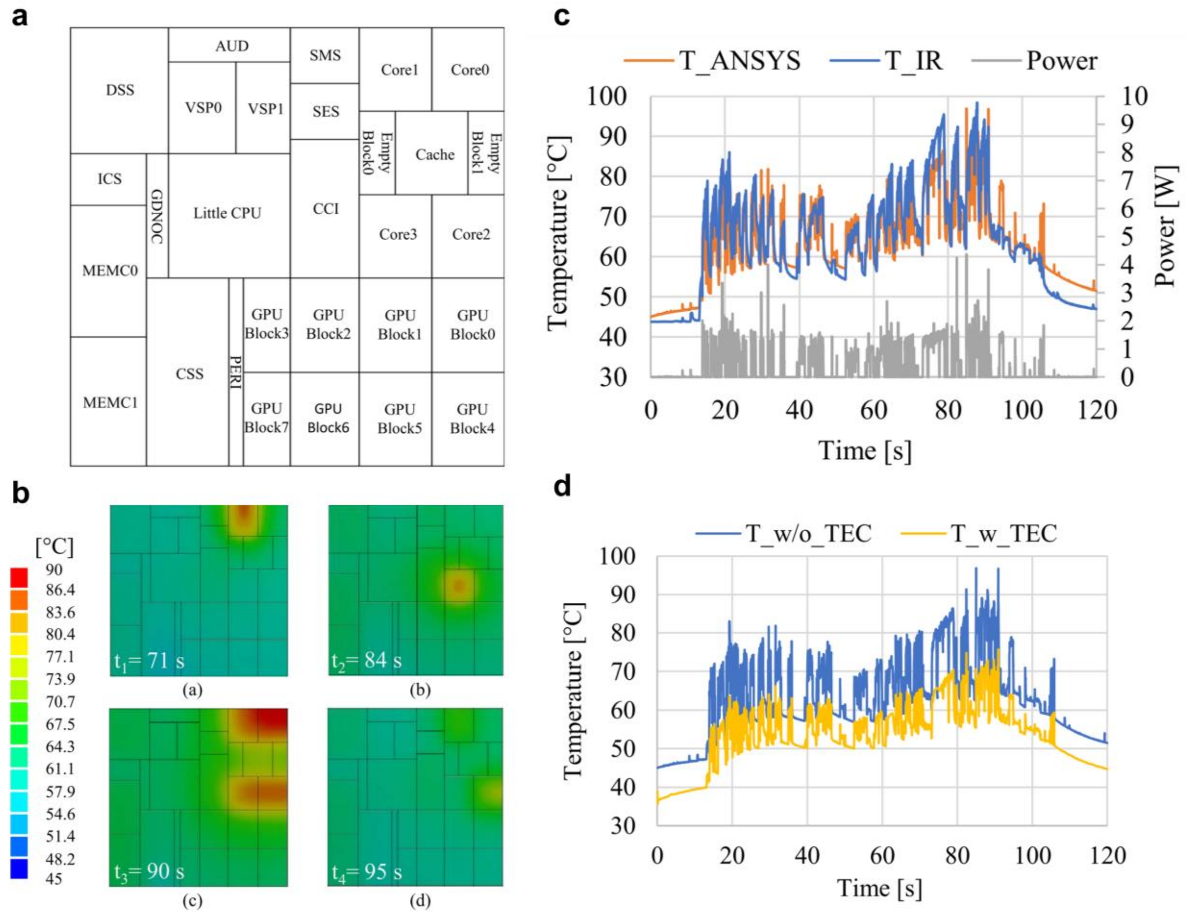

Figure 15 (a) Illustration of the floorplan of the mobile chip that is used for measurement. **(b)** Illustration of the chip temperature during the thermal analysis at various points of time. **(c)** Comparison of the temperature from the IR camera and transient thermal Multiphysics simulation model. **(d)** Comparison of the temperature of core0 with and without TEC. Reproduce with permission [47]. Copyright 2021, IEEE.

6. Conclusion and Outlook

Owing to their reliability, silence, compatibility, and controllability, TECs have become a critical active cooling option in most electronics. The micro-bulk and film-based TECs can be accessible to be integrated into the various electronics and provide sustain and transient cooling according to the requirements on chips with the package of 2D and 3D architectures. The TEC with self-cooling design and the on-demand system has become a hot research topic due to the

continuous development of chips that bring higher performance and speed but also higher heat flux and power density. Current self-cooling design can flexibly switch the Seebeck and Peltier effects of TEDs to achieve the energy harvest and thermal management, and can further improve the cooling efficiency via an on-demand system to dynamically control and optimize TECs. Therefore, the continuous research on new materials, design, and systems of TECs is of significance on the thermal management of electronics and is regarded as the main goal of current and future research of TECs.

It should be noted that there is still a considerable challenge in developing TECs. The materials, structure, design, and heat dissipation are the main factors that affect the performance of TECs. However, these factors are complementary to each other, so the optimized design of TECs is still the main direction. Firstly, the performance of TECs is highly related to the *ZT* vlaue of materials, but high *ZT* vlaue is difficult to achieve since simultaneously optimizing $S^2\sigma$ and suppressing κ have always been challenges in thermoelectric materials, especially for near-room-temperature thermoelectric materials since their high *ZT*s are mainly within low temperatures. Meanwhile, micro-bulk and film-based TECs have difficulties in fabrication and optimization. The process of the electrodes that bond with the legs of micro-bulk structure TECs is difficult due to complex fabrication routes under micro-dimensions. Meanwhile, the thickness of the substrate and length of legs of the film-based TECs are hard to be optimized to reduce the influence on the thermal resistance and the Joule heating effect due to a lack of regular design guidelines. Besides, the on-demand system and self-cooling design are unique for the specific TECs, so the on-demand system is required to design separately for different TECs, which means the system logic and TEC optimization is hard to be unified for research and commercial application.

In terms of the outlooks for the future development of TECs on chips, we summarize the following points, which are schematically illustrated in **Figure 16** [130, 142-150]:

1. **Investigating advanced materials**. *ZT* values of materials needs to be further improved by optimizing and investigating the current doping level, composition, and structure designs. In addition to the optimization of materials, the designs of TEDs are also important to develop for reducing the thermal resistance and the Joule heating effect, which include the length of legs, the thickness of the substrate, choice of the electrode, *etc*. Besides, the novel fibers, superlattices, NWs, and organic/inorganic hybrid materials also pose massive potentials on miro-bulk and film-based TECs for the thermal management of portable electronics.

2. **Enhancement of fabrication process**. Till now, TECs are the most potential candidate to integrate into various portable electronics as the active cooling option due to their reliability, silence, compatibility, and controllability. However, the research of fabrication and synthesis of micro TECs is rare and the progress is still at the early stage. There are several advanced technologies that contain flip-chip technology, electroplating, photolithography, complementary metal-oxide-semiconductor (CMOS), and electrochemical deposition (ECD) exhibit the massive potential to synthesize and fabricate TECs under micro-dimension, but most technologies required complex fabrication routes and high costs, so it is necessary to in-depth optimize or investigate the fabrication process for achieving integrate TECs into commercial applications.

3. **Optimization of related systems and designs**. The novel design of TECs with a self-cooling and on-demand system can address the satisfy requirement of the most portable electronics manufactures, which solves the issues of hotspot and is free of extra power for thermal management solutions. With the rapid development of processors and chips, the self-cooling TECs with on-demand cooling systems can also be the most candidate for thermal management on artificial intelligence, LED, server, *etc*. Till now, there are few studies on the self-cooling designs and on-demand cooling systems for TECs, and these designs and systems

are still at the stage of simulation. Hence, continuously in-depth research on these areas of TECs is the key development direction in the future.

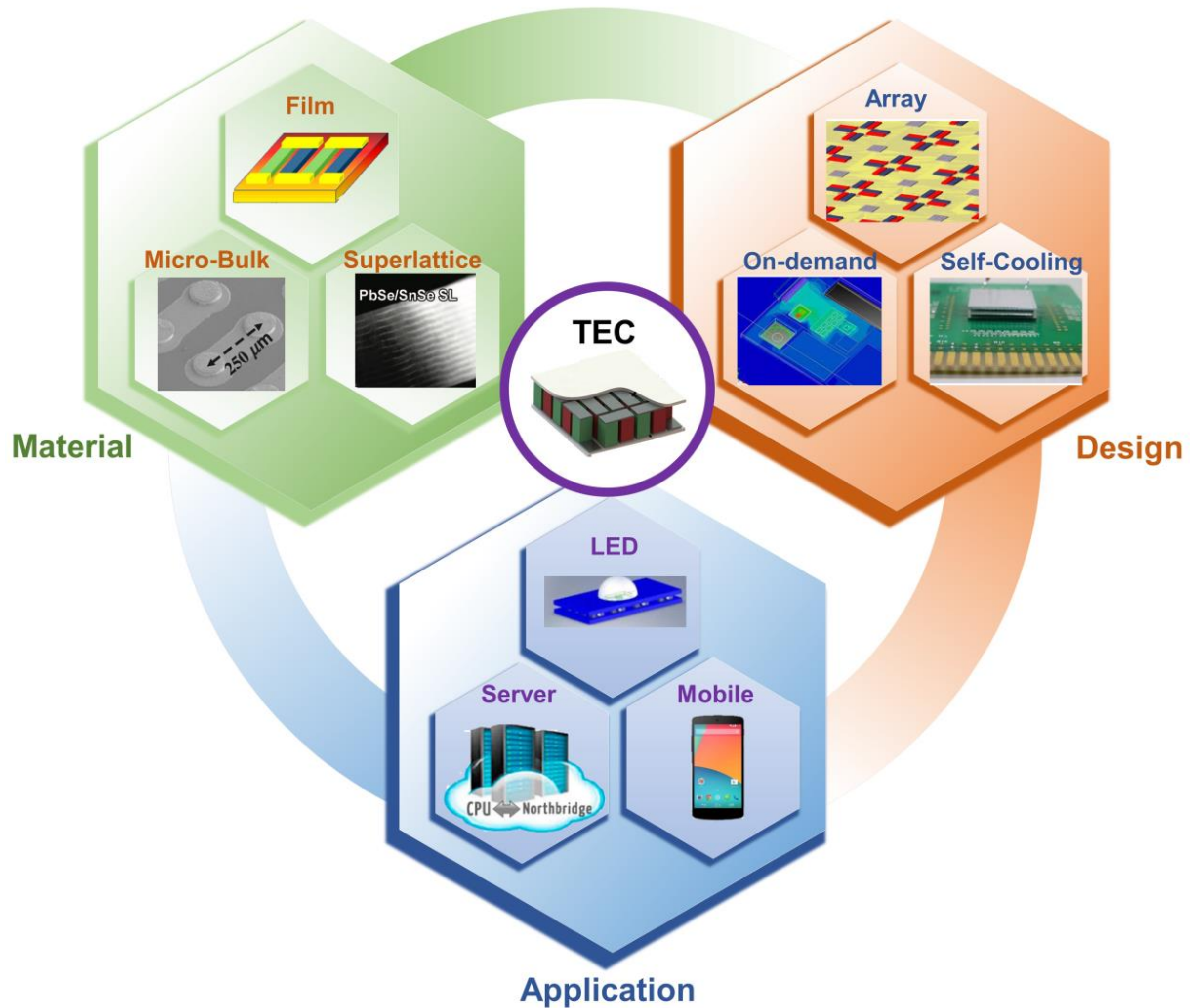

Figure 16 Outlooks of on-chip TECs based on three aspects, namely material, design, and applications. For Material: Film, reproduced with permission [143]. Copyright 2020, MDPI. Micro-bulk, reproduced with permission [144]. Copyright 2013, Springer Nature. Superlattice, reproduced with permission [145]. Copyright 2020, Wiley. For Design: Array, reproduced with permission [146]. Copyright 2008, Elsevier. On-demand, reproduced with permission [147]. Copyright 2014, AIP Publishing. Self-cooling, reproduced with permission [148]. Copyright 2007, IEEE. For Application: LED, reproduced with permission [149]. Copyright 2007, IEEE. Server, reproduced with permission [150]. Copyright 2015, Elsevier. Mobile, reproduced with

permission [142]. Copyright 2017, IEEE. TEC: reproduced with permission [130]. Copyright 2021, American Chemical Society.

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