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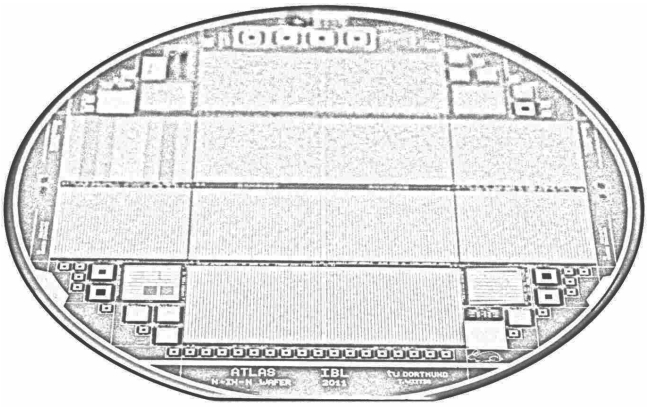
zur Erlangung des akademischen Grades eines Doktors der Naturwissenschaften in der Fakultät Physik der Technischen Universität Dortmund

Slim Edge Studies, Design and Quality Control of Planar ATLAS IBL Pixel Sensors



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1. Introduction

In the 20th century the massive progresses of the particle physics have led to a deep understanding of the microscopic structure of the universe. The investigations and characterizations of the elementary particles and the fundamental forces have resulted in the standard model. It consists of three generations of quarks and leptons and four gauge bosons. Latter are the exchange particles of the three forces: The electromagnetism, the strong nuclear and the weak nuclear interaction. The gravitation is not included. The deeper understanding of matter and interactions was enabled by the advance to smaller scales which became possible because of particle accelerators running at ever increasing energies. The collisions at the interaction points generate new particles which are detected by detector systems which have become increasingly complex featuring more precise measurement techniques, higher resolution and a faster read-out. An increasing processing speed and computing power additionally enable to cope with high luminosities and thus to collect high statistics.

The LHC is currently the largest ring collider. With energies up to $7 + 7\,\mathrm{TeV}$ and a design luminosity of $10^{34}\mathrm{cm}^{-2}\mathrm{s}^{-1}$, it enables the exploration of rare and high-energetic processes. The discovery of a new particle with a mass around $126\,\mathrm{GeV}$, published in July 2012, represents one outstanding success of the operation of the LHC. At the time being, the assumption that the particle is a Higgs boson is more and more likely. This could represent the last missing component of the standard model. However, the standard model is limited and does not describe various matters which will have to be investigated in the future. Further fields of investigations are for example the description of the Higgs mechanism, a Grand Unified Theory, the super symmetry and the CP violation which could explain the asymmetry of matter and antimatter in the universe. Improvements of accelerators and detectors are hence mandatory in the future to explore beyond the standard model.

One of the four large experiments at the LHC is the ATLAS detector, a multi purpose detector. Its pixel detector, composed of three layers, is the innermost part of the tracker. As it is closest to the interaction point, it represents a basic part of the track reconstruction. Besides the requested high resolution one main requirement is the radiation hardness. In the coming years the radiation damage will cause deteriorations of the detector performance. With the planned increase of the luminosity, especially after the upgrade to the High Luminosity LHC, this radiation damage will be even intensified. This circumstance necessitates a new pixel detector featuring improved radiation hard sensors and read-out chips.

The present shutdown of the LHC is already utilized to insert an additional b-layer (IBL) into the existing ATLAS pixel detector. The current n^{+}-in-n pixel sensor design had to be adapted to the new read-out chip and the module specifications. The new stave geometry requests a reduction of the inactive sensor edge. In a prototype wafer production (Chapter 5) all modifications have been implemented. The sensor quality control was supervised which led to the decision of the final sensor thickness. In order

to evaluate the performance of the sensor chip assemblies with an innovative slim edge design, they have been operated in test beam setups before and after irradiation.

The second main topic of this thesis is the quality control of the planar IBL sensor wafer production (Chapter 6). The production was supervised from the stage of wafer delivery to that before the flip chip process. During the quality control, the most important measurements have been coordinated, analysed and documented to ensure that a sufficient amount of functional sensors are available for the module production.

In Chapter 7 improvements of the design and the dicing step are illustrated which are either already investigated or will be in the course of coming productions. They should help to cope with requirements and specifications of future ATLAS pixel detector upgrades concerning radiation hardness and slim edges.

2. The LHC and the Present ATLAS Detector

2.1. LHC

The Large Hadron Collider (LHC) at CERN, Geneva, is currently the world's largest particle accelerator. It is a ring collider with a circumference of 27 km where protons are accelerated to a maximum energy of $7 + 7$ TeV. The high magnetic fields of up to 8.4 T which are required to deflect the beam, are generated by superconducting dipole magnets. The LHC is the last part of a chain of several pre-accelerators which form the CERN accelerator complex seen in Figure 2.1. At four interaction points, the

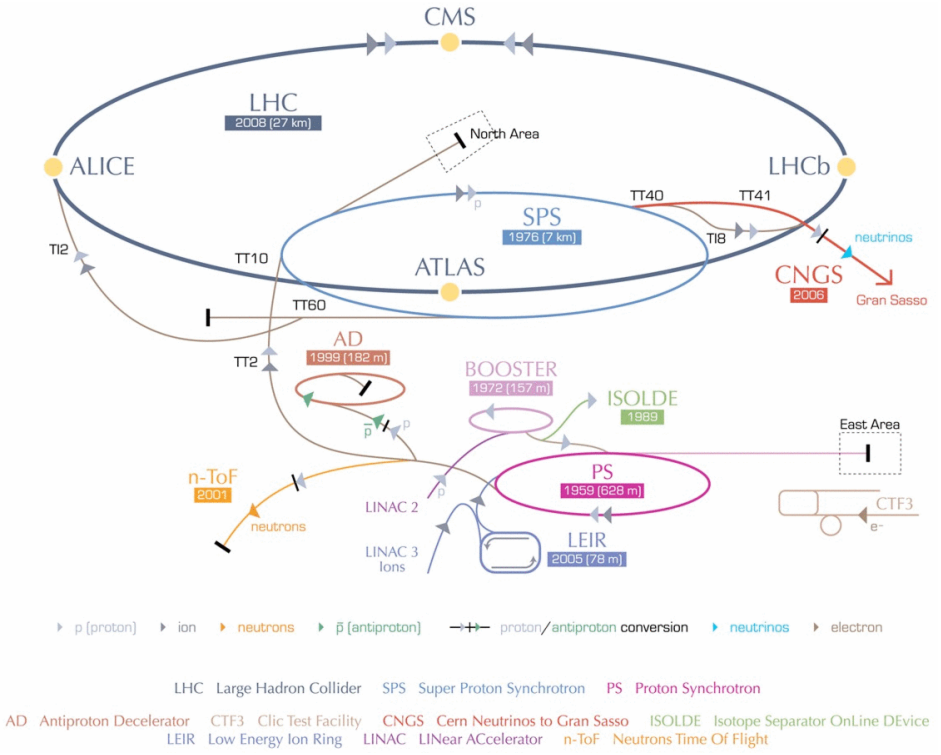


Figure 2.1.: Illustration of the CERN accelerator complex. [Lef06]

beams are crossed in order to provoke collisions and produce new particles. At each interaction point one of the four large experiments is located. These particle detectors are ALICE[1], ATLAS[2], CMS[3] and LHCb[4]. ALICE is a detector system specialized

[1] A Large Ion Collider Experiment
[2] A Toroidal LHC Apparatus
[3] Compact Muon Solenoid
[4] Large Hadron Collider beauty

in heavy ion collisions, LHCb one specialized in tests on CP violation in $b\bar{b}$-systems. ATLAS and CMS are multi purpose detectors. With a bunch crossing rate of 40 MHz, a design luminosity of $10^{34}\text{cm}^{-2}\text{s}^{-1}$ can be reached [LHC95].

In the first years of its operation starting in 2009, the LHC was operated at 3.5+3.5 TeV and 4+4 TeV. At the beginning of 2013, the first large machine shutdown started which will presumably last until spring of 2015. It is used to initiate first upgrades of the collider and the detectors. The total integrated luminosity which is collected so far is some tens of fb^{-1} [LHCSt].

2.2. ATLAS Detector

The ATLAS experiment [Aad08a] is a 4π multi purpose detector. One of its main goals is to prove or disprove the existence of the standard model Higgs boson as its mass has to be in the energy range of LHC. Due to the high luminosity and the associated high production rates, high statistic measurements up to the TeV scale can be done. Furthermore, the detector enables for example to do precision measurements of the top quark, to investigate the CP violation or new physics in terms of super symmetry.

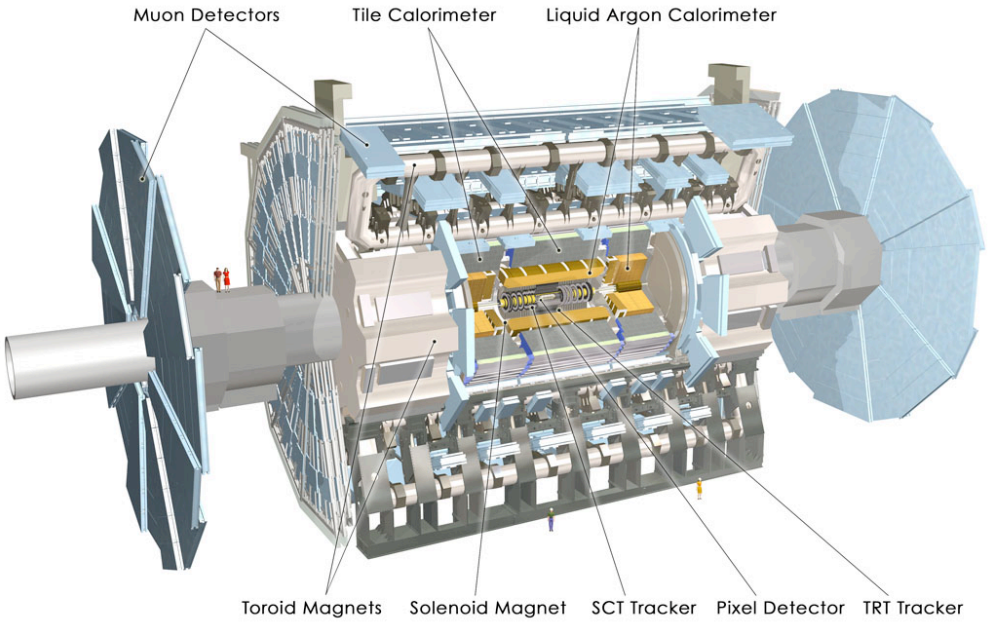


Figure 2.2.: Illustration of the ATLAS detector. [Apic]

The ATLAS detector has an overall diameter of 25 m, a length of 46 m and a weight of about 7000 t. It can be divided into subdetectors which are arranged cylinder symmetrically around the interaction point, see Figure 2.2. These are from the inside outwards the inner detector or tracker, the calorimeters and the muon detectors.

The tracker is enclosed by a solenoidal magnetic system which produces a nearly homogeneous field of 2 T causing track deflection for charged particles. The calorimeter is surrounded by superconducting toroidal air coils producing a magnetic field of more than 4 T for the muon spectrometer. The muon tracks are deflected and detected in high-precision tracking chambers.

The calorimeter is divided into an electromagnetic (EM) calorimeter and a hadronic calorimeter. Both are using the sampling technique to determine space resolved the energy of electrons respectively of hadron jets. They consist of alternating layers of passive absorber materials and scintillators with liquid Argon as an active medium.

The inner detector is consisting of the transition radiation tracker (TRT), the silicon strip detector (SCT) and the pixel detector. Its purpose is a high-precision measurement of the particle tracks. The number of layers is a compromise of higher track resolution and the increased probability of scattering due to a larger radiation length (see Section 3.1.2). Furthermore, it implicates high costs especially for the pixel detector.

The TRT consists of 4 mm thick straw tubes containing a xenon-based gas surrounding a sense wire. The particles crossing the tubes create transition radiation and are thus detected.

The SCT consists of silicon microstrip sensors in p^+-in-n (see Section 3.1) technology. Each module has an area of $6.36 \times 6.4\,cm^2$ with 768 read-out strips in a $80\,\mu m$ pitch. The cylindric barrel region of the detector has 8 layers where always two are mounted back-to-back at a 40 mrad angle in order to obtain a better tracking resolution which is in the order of $16\,\mu m$ in the radial direction ($r\phi$) and $580\,\mu m$ along the beam pipe (z-direction).

The pixel detector [ATL98, Aad08b] is the unit which is closest to the interaction point and thus the most important part of the tracking system especially for the b-tagging. A sketch is shown in Figure 2.3.

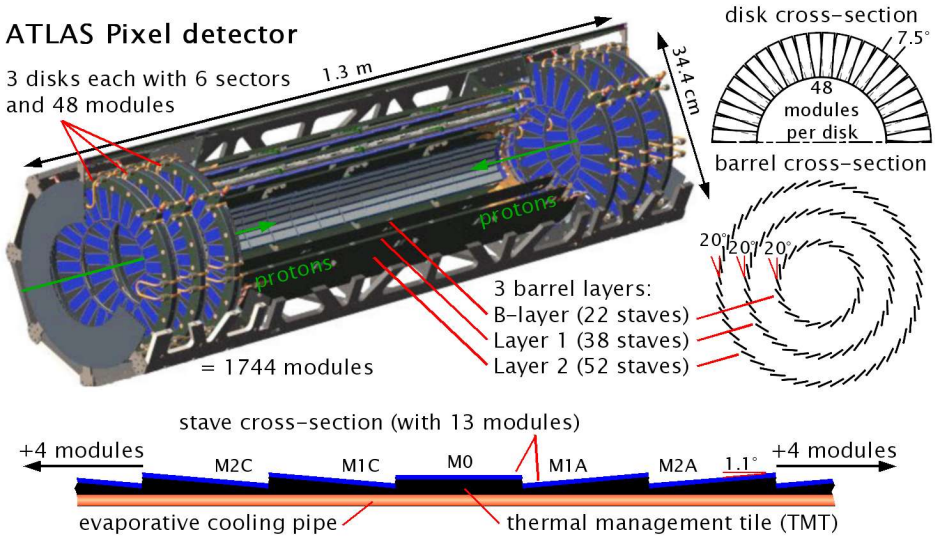


Figure 2.3.: Illustration of the ATLAS pixel detector [Bar02]. For further details see text.

The pixel detector consists of 1744 pixel modules (see Section 3.4.3). Around the interaction point, the modules are mounted consecutively on so called staves. The staves are forming three cylindrical barrel layers. The innermost one is called b-layer which illustrates its importance for the b-tagging efficiency.

Further modules are mounted on six end cap disks which complete the detector on

both sides for larger η values[5]. On each disk, the modules are placed back-to-back and staggered to maximize the detection efficiency.

The resolution of the pixel detector is $12\,\mu$m in $r\phi$- and $66\,\mu$m in z-direction for the barrel section. Including the disks it spans a pseudorapidity range $|\eta| < 2.5$.

The stave assembly is discussed in detail in Section 3.5.

[5]pseudorapidity $\eta = \ln(\tan\theta/2)$ with the polar angle θ with respect to the beam axis

3. ATLAS Pixel Sensors

This chapter should help to understand the basic concepts which are necessary to understand the design, functionality and operation of the ATLAS pixel sensors. The first two sections give a brief introduction to silicon sensor technology. A detailed description of the band theory and the functionality of silicon sensors in general can be found in [Lut99].

It is followed by a description of the layout of the current ATLAS pixel sensors and modules. Much more detailed descriptions can be found in various works, for example [Hue01, Kla05, Kra04, Mo99].

3.1. Functionality of Planar Silicon Sensors

A planar silicon sensor is basically a semiconductor diode, i.e. a junction of n-doped and p-doped silicon. It is produced on silicon wafers which consist of a slightly n- or p-doped bulk material in the first place. Additionally, one surface is highly doped with an n^+, the other one with a p^+-implantation. At the junction between the n- and p-doping a slim depletion zone is naturally formed due to the charge carrier recombination.

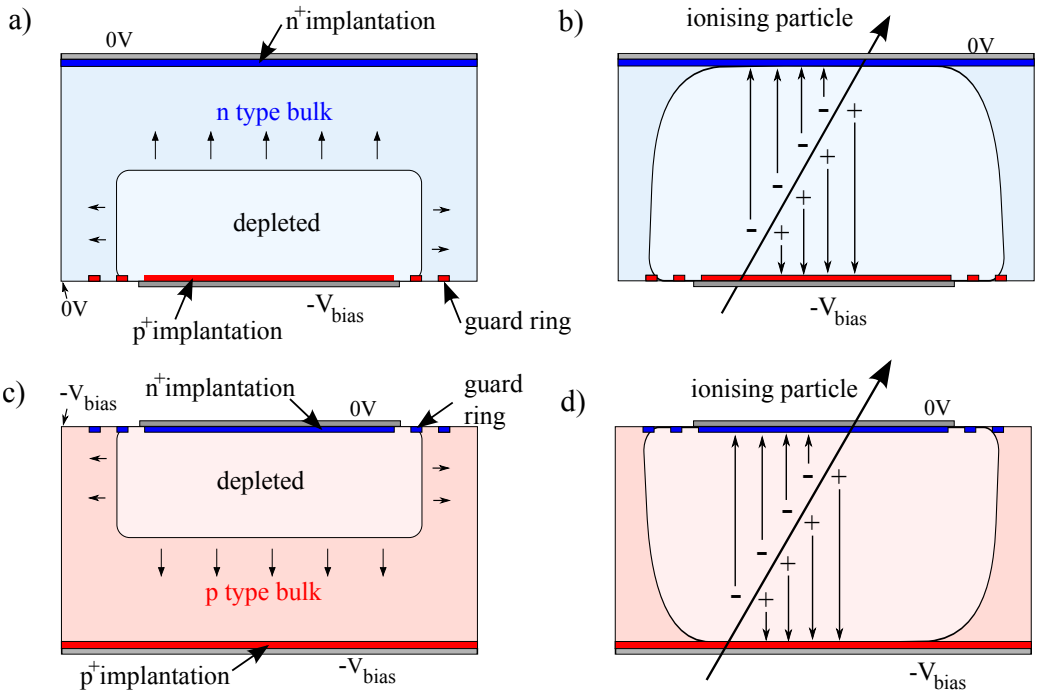


Figure 3.1.: Cross section through a silicon sensor for n-type bulk (a) and b)) and p-type (c) and d)). Adapted from [Kla05].

If a negative bias voltage V_{bias} is applied to the p-side whereas the n-side is kept on ground, the depletion zone grows through the bulk towards the other side (see Figure 3.1 a) for n-type bulk and c) for p-type bulk). The voltage at which the bulk is completely depleted is called depletion voltage V_{depl}. It is mainly dependent on the bulk thickness d and the bulk resistivity ρ:

$$V_{\text{depl}} = \frac{d^2}{2\,\rho \cdot \mu_e \cdot \varepsilon_{\text{Si}} \cdot \varepsilon_0} \tag{3.1}$$

with the electron mobility $\mu_e = 1427\,\frac{\text{cm}^2}{\text{Vs}}$, the dielectric constant of silicon $\varepsilon_{\text{Si}} = 11.75$ and the permittivity constant $\varepsilon_0 = 8.85 \cdot 10^{-6}\,\frac{\text{pF}}{\mu\text{m}}$ [Lut99, Kla05].

3.1.1. Leakage Current

If a silicon sensor is biased reversely, a leakage current arises which can be caused by several effects. The volume or bulk generation current and the avalanche breakdown are intrinsic even for an ideal sensor. Because it is impossible to produce silicon sensors without any impurities and defects, the interface generation current as well as ohmic currents can also contribute. The latter ones can stem from the bulk due to its non-negligible ohmic conductivity or also from the surface. For further details see [Kla05] and [Wue01].

An important feature of the dominant bulk generation current is the temperature dependency. In order to compare leakage current measurements which have been taken at different temperatures, Equation (3.2) can be used.

$$I_{\text{R}} = I \cdot \left(\frac{T_{\text{R}}}{T}\right)^2 \cdot \exp\left[-\frac{E_{\text{g}}}{2\,k_{\text{B}}}\left(\frac{1}{T_{\text{R}}} - \frac{1}{T}\right)\right] \tag{3.2}$$

I is the current measured at any temperature T (in K), I_{R} is the current corresponding to a reference temperature T_{R} (in K) to which it is normalized. $k_{\text{B}} = 8,167 \cdot 10^{-5}\,\text{eV/K}$ is the Boltzmann constant and $E_{\text{g}} = 1.21\,\text{eV}$ the silicon band gap energy [Chi11, ATL03, Lut99]. An increase of the temperature by 7 °C approximately doubles the leakage current. This is the reason why a temperature monitoring is important in order to be able to compensate any fluctuations.

Both the n- and p-type bulk designs exhibit the problem that during the operation there is a potential difference between the p-n-junction and the cutting edge. In order to prevent the sensor from possible electric discharges due to high fields, this region is provided with so called guard rings. These are floating highly doped implantations surrounding the p-n-junction electrode. On the basis of the so called punch-through effect, the bias voltage is decreased gradually from ring to ring. For further details see [Bis93, Hue01].

3.1.2. Particle Detection

Particles traversing matter are interacting in various ways depending on their characteristics. Photons can cause three different effects. The probability of which effect is preferred is highly energy dependent. The photoelectric effect is dominant at lower

energies, followed by the Compton effect at energies between 30 keV and 5 MeV. For higher energies the pair production is dominating.

A charged particle can interact with matter in several ways besides ionization. Bremsstrahlung is an electromagnetic radiation caused by the deceleration of the particle. It is inversely proportional to the radiation length which is an inverse measure of the energy loss dependent on the material. For heavier particles the Bethe-Bloch equation describes various kinds of interactions such as the mean elastic and inelastic energy loss as well as Čerenkov radiation. The characteristic of this differential energy loss features a minimum which is at 3.8 MeV/cm for silicon. A particle in the region of this minimum is called a minimum ionizing particle (MIP).

A MIP which crosses the depleted sensor bulk generates a tube of electron-hole pairs uniformly along its track. To generate one electron-hole pair in silicon, 3.6 eV are necessary. In a thin bulk material the energy loss of a particle can be described by a Landau distribution. In comparison to a Gauss distribution which is expected for sufficiently thick materials, it takes into account the possibility that a particle can loose a large fraction of its energy at once. This effects a distortion of the Gauss distribution at higher energies. The mean energy loss is not equal to the most probable energy loss but shifted to higher energies. With thicknesses of 250 μm and below, the present silicon sensors fall into this category of thin materials. The most probable energy loss for example in a 250 μm thick silicon bulk results to 70 keV. Divided by 3.6 eV, this is equal to 19400 electron-hole pairs [Rum09]. For further details see [Leo94].

Because of the applied voltage, the holes are drifting to the p-side which is on negative bias voltage whereas the electrons are drifting to the n-side which is grounded (see Figure 3.1 b) and d)). The electrons can be measured as a signal with an appropriate read-out chain. In order to obtain a spatial resolution which is required for a high energy collider tracking detector, one implantation can be segmented into strips or pixels which then have to be read-out separately. A planar pixel sensor with a p-type bulk where the n-side is segmented is called n^+-in-p, i.e. n-pixels on p-bulk. This means the lowly n-doped substrate contains highly n^+-doped implantation on the front side and highly p^+-doped implantation on the back side. An n-bulk with n-pixels is analogously called n^+-in-n.

3.2. Radiation Damage in Silicon Semiconductors

3.2.1. General Radiation Effects

The discussed ionizing charge generation is reversible and does not damage the silicon crystal lattice. In contrast a non-ionizing interaction can damage the lattice permanently. Besides the interaction of a particle with a nucleus which can be converted, these damages can manifest in so called point defects like interstitials or vacancies caused by the removal of an atom. If enough energy is transferred to this atom, it can in turn cause further damage which leads to defect clusters. It is called Primary Knock-on Atom (PKA).

Because different particles like hadrons, electrons or pions are causing different effects, the extent of the defect is scaled to a so called standard irradiation. It is important for

the comparison of different types of irradiation. The radiation damage caused by this Non-Ionizing Energy Loss (NIEL) is therefore converted to the energy loss which would be caused by neutrons with the energy of 1 MeV. The measurement unit is n_{eq}/cm^2. The fluence Φ_{irr} which is applied at an irradiation facility can be normalized into an equivalent fluence $\Phi_{eq} = \kappa \cdot \Phi_{irr}$. The hardness factor κ is unique for each irradiation facility [Mo99, Rum09].

With an increasing irradiation there are several effects which have influence on the effective doping concentration. Besides donor removal due to defects in the crystal lattice, one important effect is that displacement damages act as acceptor-like states. The donor concentration N_D is thus decreasing while the acceptor concentration N_A is increasing. An n-type doped bulk is starting with a positive effective doping concentration $N_{eff} = N_D - N_A$. After a certain irradiation dose it will get negative which means a type conversion of the bulk, it is getting p-type like. In other words the absolute value of the effective doping concentration $|N_{eff}|$ has a minimum. The fluence where the type conversion sets in, is dependent on the initial doping concentration. For bulk material comparable to that of the ATLAS pixel sensors the minimum of the effective doping concentration is in the region of $1 - 10 \cdot 10^{13} n_{eq}/cm^2$ [Wun92, Hue01].

The depletion voltage can also be described in dependence on the absolute value of the effective doping concentration (for comparison see Equation (3.1)):

$$V_{depl} = \frac{e_0 |N_{eff}|}{\varepsilon_{Si}\,\varepsilon_0} \frac{d^2}{2} \quad . \tag{3.3}$$

This relation leads to an increasing depletion voltage with higher irradiation fluences. Especially for higher fluences it is not worthwhile anymore to attempt to fully deplete thick sensor bulks as V_{depl} increases disproportional.

In the course of the ROSE Collaboration (RD48) it was investigated how to improve the radiation hardness of silicon sensor material [RD48, ROS96]. It was discovered that the radiation induced lattice defects can be significantly reduced if the standard float zone (FZ) silicon is oxygen enriched during the process. It is called diffusion oxygenated float zone (DOFZ) material. Besides improvements related to the annealing, the effective doping concentration is significantly less increasing with the fluence for DOFZ material. For further details see [Wun92, Web04].

3.2.2. Annealing

The effective doping concentration N_{eff} can change in the course of time due to an effect called annealing. It can be classified into three differently acting parts according to the *Hamburg model* [RD48, Mo99, Kra04]:

$$\Delta N_{eff}(\Phi_{eq}, t(T_a)) = N_a(\Phi_{eq}, t(T_a)) + N_c(\Phi_{eq}) + N_y(\Phi_{eq}, t(T_a)) \tag{3.4}$$

N_a is called the *short term annealing* or *beneficial annealing* part. It increases N_{eff} which leads to a lower depletion voltage for a type converted n^+-in-n sensor. N_a decreases with time and is surpassed on a long time scale by the *anti-annealing* or *reverse annealing* part described by N_y. Latter counteracts the beneficial annealing by decreasing N_{eff} and thus increasing the depletion voltage. N_c is a damage constant in time which only depends on the fluence.

As indicated in Equation (3.4) the annealing speed is dependent on the annealing temperature T_a because the mobility of defects grows with temperature. For the operation it means that the detector should always be kept as cold as possible. Interim deliberate warm-ups of the pixel detector can be used to benefit from the beneficial annealing. On the contrary, to minimize further sensor deteriorations, the warm-up periods should not last beyond the minimum in the annealing curve. For further details see [Kra04].

The leakage current of an irradiated sensor is proportional to the acquired equivalent fluence Φ_{eq} and the depleted volume W:

$$I = \alpha \cdot \Phi_{\text{eq}} \cdot \text{W} \tag{3.5}$$

The proportionality factor α is called *current related damage rate*. It can be parameterised in the following way [Mo99]:

$$\alpha(t) = \alpha_I \cdot \exp\left(-\frac{t}{\tau_I}\right) + \alpha_0 - \beta \cdot \ln\left(\frac{t}{t_0}\right) \tag{3.6}$$

t_0 is set to 1 min. The temperature dependent variables are

$$\alpha_0 = -(8.9 \pm 1.3) \cdot 10^{-17}\text{A/cm} + (4.6 \pm 0.4) \cdot 10^{-14}\text{A K/cm} \cdot \frac{1}{T_a} \quad \text{and} \tag{3.7}$$

$$\frac{1}{\tau_1} = k_{0I} \cdot \exp\left(-\frac{E_I}{k_{\text{B}} T_a}\right) \tag{3.8}$$

with the parameter values

$$k_{0I} = 1.2^{+5.3}_{-1.0} \cdot 10^{13}\text{s}^{-1} \tag{3.9}$$

$$E_I = (1.11 \pm 0.05)\,\text{eV} \quad . \tag{3.10}$$

The temperature independent parameters are

$$\alpha_I = (1.23 \pm 0.06) \cdot 10^{-17}\text{A/cm} \qquad \text{and} \tag{3.11}$$

$$\beta = (3.07 \pm 0.18) \cdot 10^{-18}\text{A/cm} \quad . \tag{3.12}$$

3.3. Design of ATLAS Pixel Sensors

For the ATLAS pixel production the wafers have been produced by the two vendors CiS[1] and TESLA/ON[2]. The so called sensor tile of the current ATLAS pixel detector is a planar n^+-in-n silicon sensor. It is processed on n-type doped, 250 μm thick DOFZ substrate material. The n^+-implantation is segmented into a matrix of 400 μm long (in z-direction) and 50 μm wide (in $r\phi$-direction) pixels. Respectively one array of 18 columns and 160 rows are read out by one Front End I3 (FE-I3) chip [Per06].

The sketch in Figure 3.2 shows a cross section of the sensor bulk and the differently processed layers on its surface. The n^+-in-n design requires a double-sided wafer process

[1] CiS Forschungsinstitut für Mikrosensorik und Photovoltaik GmbH, Erfurt, Germany, http://www.cismst.org/

[2] ON Semiconductor Czech Republic a.s., Roznov, Czech Republic, http://www.onsemi.cz

because both sides have to be structured. Each surface consists of five layers which are from bottom to top:

1. n^+/p^+-implantation
2. oxide passivation
3. inner nitride passivation
4. metal (AlSi alloy)
5. outer nitride passivation

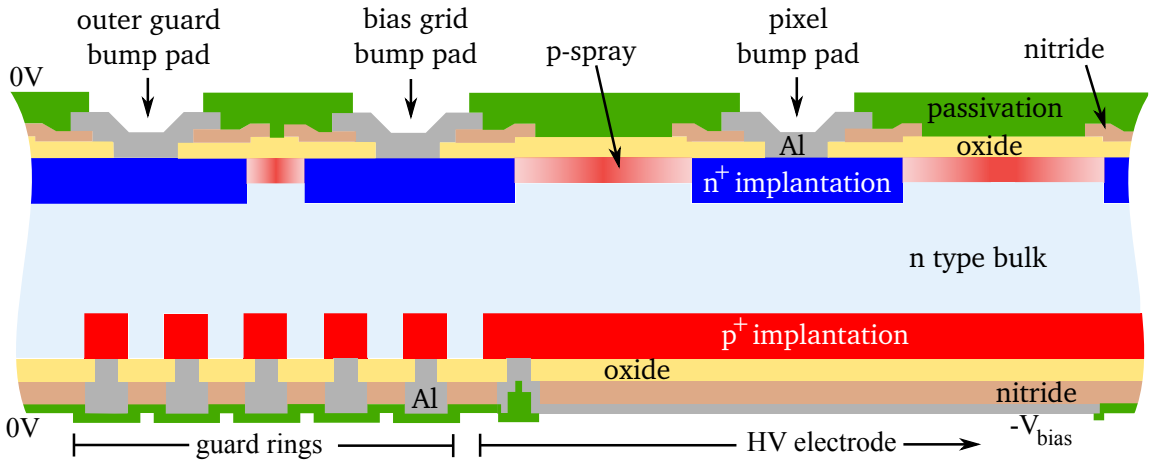


Figure 3.2.: Cross section of the ATLAS pixel sensor. Dimensions are not to scale. For detailed description see text. Original taken from [Dob04] and modified.

On the n-side it is possible that the oxide charges can cause a conducting n-channel between the pixel implantations. In order to insulate the n^+-implantations, a so called p-spray doping is applied to the pixel side between the steps 3 and 4. Its concentration is higher than the low doping of the bulk substrate but significantly lower than the n^+-implantations. For the present ATLAS pixel sensor design it is used a so called moderated p-spray. The p-doping is spread homogeneously over the complete wafer surface, i.e. there is no need of an additional mask. The strength of the doping is moderated by the nitride layer which is already existent. The full dose is placed in those regions without nitride, a reduced dose in those regions with nitride as indicated in Figure 3.2. The effective doping profile results in a smooth distribution without high field intensities next to the pixel implantations. Within the n^+-implantations the p-spray doping is completely compensated due to the large differences of the concentrations. For a more detailed description of the process steps see [Hue01, Web04, Roh99].

The p^+-implantation is implemented as one large high voltage pad opposite of the pixel matrix which is surrounded by 16 guard rings. The purpose of the guard rings is a controlled potential drop from the high voltage pad to the grounded cutting edge. A more detailed description of the sensors edge design can be found in Section 5.3.2. Besides the pixelated n^+-implantation which represents the active area there are two surrounding guard rings which represent the inactive edge: the bias grid ring and the outer guard.

The bias grid is implemented in order to have the possibility to test the sensor before the interconnection with the read-out chip, the bump bonding (see Section 3.4.2). Because

it is not practicable to contact the thousands of pixel cells one has to rely on the punch through effect. Two implantations on the n-side are insulated due to the intermediate p-spray. The intrinsic depletion zones which are generated at the p-n-junctions are separated. If the potential differences between the two implantations is exceeding a so called punch through voltage, the depletion zones connect and generate a conducting path between the implantations. The latter are drawn to the same potential minus the respective punch through voltage. This voltage difference is dependent on the distance between the two implantations. For further details see [Bis93, Hue01].

If the ground potential is applied to the sensors edge, the punch through takes place between the implantations from the edge inwards. The effect is not sufficient to guarantee an active area having a homogeneously potential above V_{depl} because the potential difference between edge and pixel increases with each row [Roh99]. In order to obtain the same potential on each pixel, they are connected via the bias grid (see Figure 3.3). A metal bias rail runs between each double column and is connected to the bias dot. The latter is a circular implantation inside the pixel implantation. The punch through takes place in between these implantations so that each pixel is on the same potential. The bias rails are connected to the bias grid ring. If a sensor is tested, the dicing street

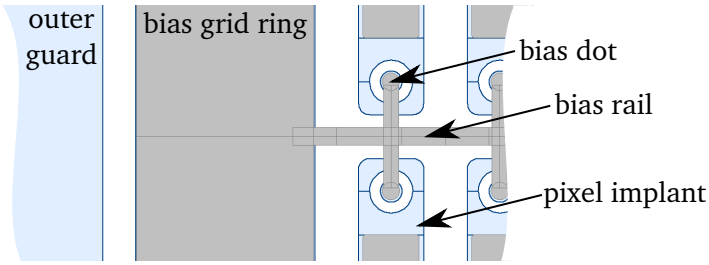


Figure 3.3.: Top view of the bias grid of the ATLAS pixel sensor. The n^+-implantation is blue, the metal grey. The bias grid rails connect the bias dot implantations which are surrounded by the pixel implants.

which is connected to the outer guard is on ground potential. In order to guarantee that each pixel is also on ground potential, the punch through effect has to take place only twice: One larger distance of 15 μm from the outer guard to the bias grid ring and one small distance of 5 μm between the bias dot and the pixel implantation.

During the assembly the sensor is connected to the FE-I3 read-out chip via bump bonds (see Section 3.4.2). The bump bond pads are located at the end of the pixel implants, opposite to the bias dots. Each pixel as well as the n^+-edge-implantations are hence put on ground potential. Even if some bumps are not connected, those pixels are not floating and thus affecting the sensor performance due to the bias grid which keeps them close to ground potential.

One sensor tile is read out by 2×8 FE-I3 chips (see also Figure 5.8). The chips need a safety margin between each other in the order of 400 μm. Because there is no direct read-out possible in this region and the sensor should not have any inactive part within the active area, the pixel layout is modified in the edge region of the chips as seen in Figure 3.4. The pixels of the edge columns are elongated to 600 μm, called long pixels. The four pixel rows which cannot be covered by the chip are connected via metal conductors to every second of the last seven pixels which do have bump connections. These are called ganged pixels. Due to the larger capacitance these pixels feature the disadvantage of an increased noise.

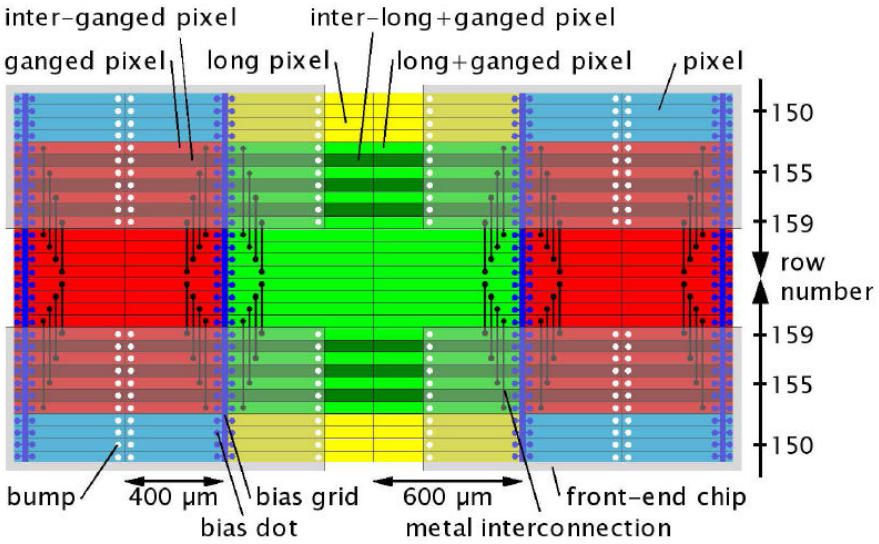


Figure 3.4.: Top view sketch of the ATLAS sensor-chip assembly in the corner region between four FE-I3. For detailed description see text. [Dob04].

3.4. Modules and Read-Out Cards

3.4.1. Front End Chip

The Front-End chip represents the first part of the processing electronics. Each pixel cell of the sensor is connected to one pixel cell of the front end via bump bonds (see Section 3.4.2). Each Front End pixel cell features an analogue and a digital part. A schematic of the analogue part of a FE-I3 can be seen in Figure 3.5. The charge which

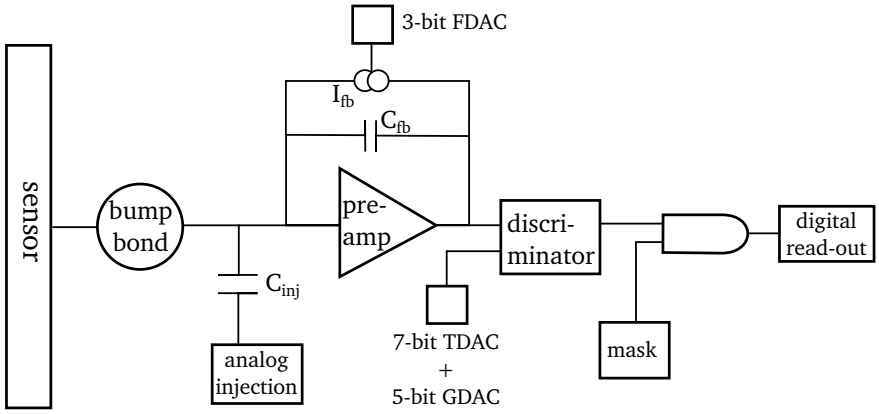


Figure 3.5.: Schematic of the analogue part of a FE-I3 read-out cell. Original taken from [Rei06] and modified.

is coming from the sensor is amplified by a preamplifier. The feedback capacity C_{fb} is charged by the signal and discharged by the feedback current I_{fb}. The resulting output of the preamplifier has a rising and a trailing edge of the signal as seen in Figure 3.6. The discriminator digitizes this signal by converting it to a time-over-threshold (ToT) value. The ToT is thus a measure of the amount of charge. The same input signal can cause differing outputs of the discriminators of different Front End pixel cells as their properties are varying. Each chip thus has to be tuned before its operation. It can be done by optimizing the discriminator threshold and the feedback current using several DACs[3]. The injected charge, threshold and feedback current dependencies of the ToT are illustrated in Figure 3.6. It can be seen that the ToT is increased with a higher amount of charge, a lower threshold or a lower feedback current. Further details can be found in [Dob04], for FE-I4 also [Jen11].

[3]Digital Analog Converter

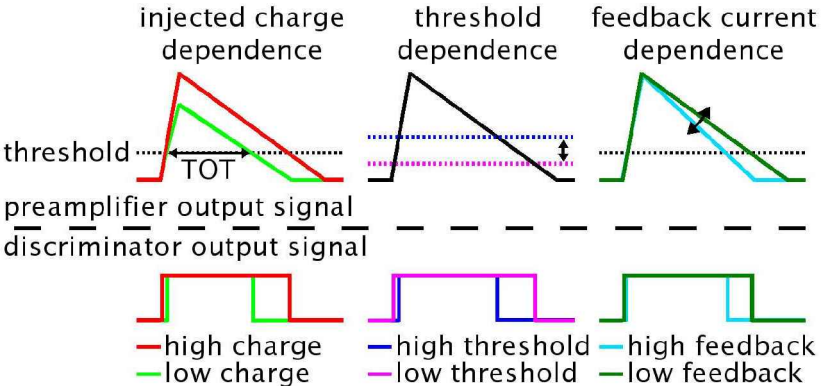


Figure 3.6.: Injected charge, threshold and feedback current dependencies of the ToT in the Front-End preamplifier and discriminator. [Dob04]

3.4.2. Bump Bonding

The interconnection between the sensor and the read-out chip is done via so called bump bonds. This is an industrially used technique which is needed as each sensor pixel cell has to be read out by one pixel cell of the Front-End chip. For the ATLAS pixel production there have been two bump bond vendors who used different techniques. The IZM[4] uses tin-silver bumps (formerly lead-tin) while AMS[5] uses indium bumps. For all sensor productions which are investigated during this thesis, the only bump vendor is IZM. It is thus confined to the tin-silver bump process. A sketch is seen in Figure 3.7. Before the actual bump bond process, the pads of the sensor and the

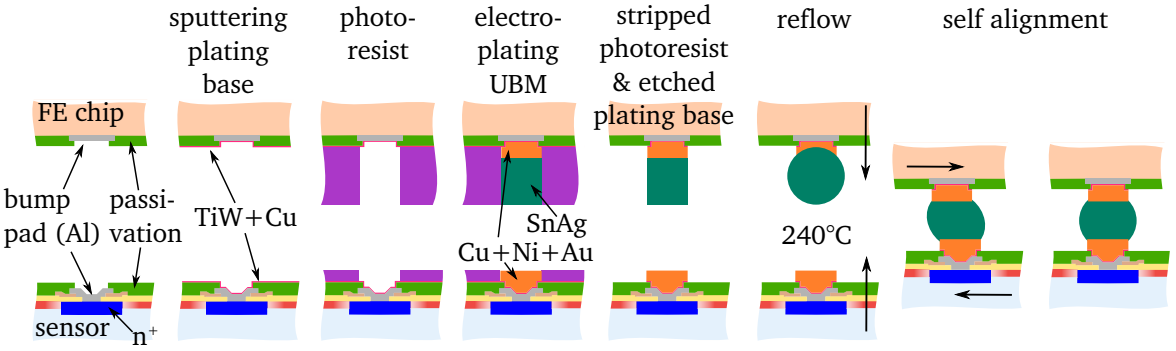


Figure 3.7.: Tin-silver bump bonding process which is performed at IZM. For further description see text. Taken from [Dob04] and modified.

chip have to be prepared with additional metal layers, the so called under bump metal (UBM). They are applied onto the passivation openings to achieve a good mechanical and electrical contact for the bumps. The UBM pads which consist of three layers of copper, nickel and gold are electro-plated. They are in total approximately 7 μm high. As the electro-plating is a wafer-level process, it has to be executed before the dicing step. The bump bond is applied on the pads of the chip. It is a 20 μm high cylinder which consists of an eutectic alloy of 96.5% tin and 3.5% silver. After a reflow step at 240 °C, the bump takes the form of a sphere. The interconnection step between sensor and chip is called the flip chip process. Due to the surface tension of the melted bumps, a self alignment occurs which balances a possible misalignment. A detailed description of the bump bonding process can be found in [Web04].

[4]Fraunhofer Institut für Zuverlässigkeit und Mikrointegration, Berlin, Germany, http://www.izm.fraunhofer.de/

[5]Alenia Marconi Systems, Rome, Italy, now SELEX, http://www.selex-es.com/

3.4.3. Modules

The ATLAS pixel module is the smallest unit of the present ATLAS pixel detector (see Figure 3.8 and also Figure 5.8). The assembly of sensor tile and 16 FE-I3 chips is called

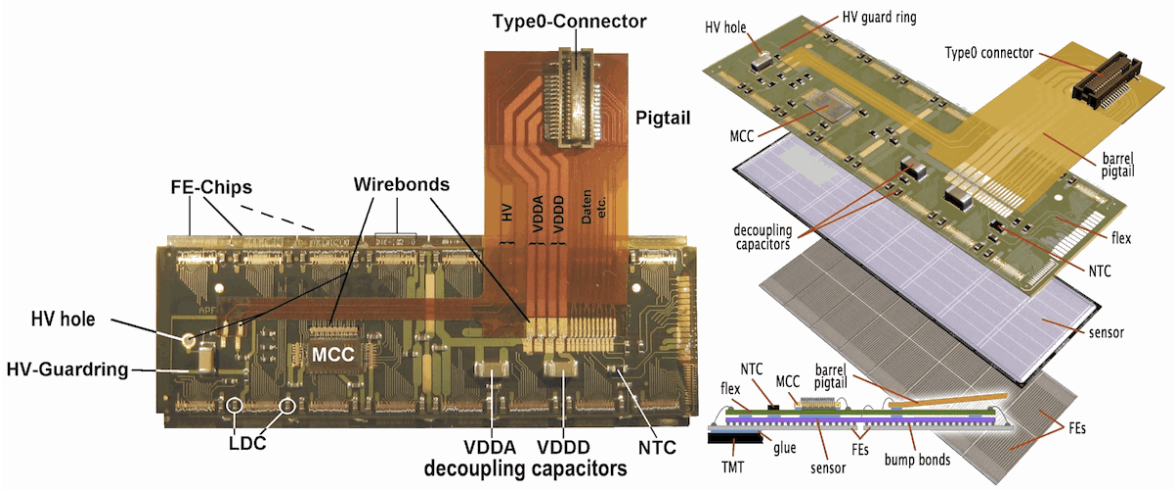


Figure 3.8.: Sketch of the ATLAS pixel module. For detailed description see text. [Tro12]

bare module. It is glued to a flex which contains passive SMD components, a 10 kΩ ceramic NTC thermistor and an active module control chip (MCC). The high and the low voltage supplies as well as the signal processing is routed via an attached so called pigtail to a type 0 connector. The FE-I3 chips are wire bonded to the flex. The high voltage is wire bonded from the flex via a HV-hole directly to the sensors p-side. A detailed description of the ATLAS pixel modules can be found in [Dob04, Boy03].

3.4.4. Read-Out Cards

In order to test the performance and efficiency of sensor chip assemblies in lab or at test beam setups (see Section 5.5), they have to be wire bonded to special read-out cards. Figure 3.9 shows a FE-I3 single chip card (SCC). It was originally designed at the university of Bonn. Besides being responsible for LVDS and HV supply, this

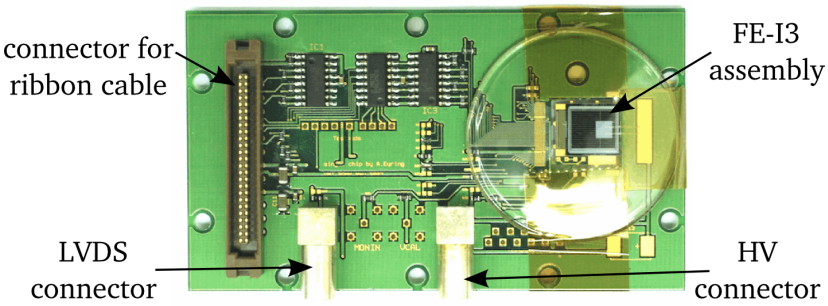


Figure 3.9.: FE-I3 single chip card to operate a sensor chip assembly in lab or test beam. For detailed description see text. Original taken from [Tro12] and modified.

circuit board is read out by a ribbon cable which is connected to the USB-Pix system [USBPix]. The latter is operated by the STControl software [STCon]. This system is able to perform tunings and scans of the assembly. This is necessary in order to guarantee that all pixels are tuned for example to the same threshold and the assembly

is thus configured homogeneously. Further details of the USB-Pix system and the STControl software can be found in [Jen11] and [Lap12].

3.5. Stave Assembly

In the barrel section of the ATLAS pixel detector, 13 modules are mounted on one stave. The stave is made of a carbon-fibre composite material and serves as a mechanical support for the modules, cables and the cooling pipe. (see also Figure 2.3) [Aad08b]. In Figure 3.10, a bi-stave can be seen, i.e. two staves which share one cooling loop. The staves are mounted cylindrically around the beam pipe and form the barrel layers.

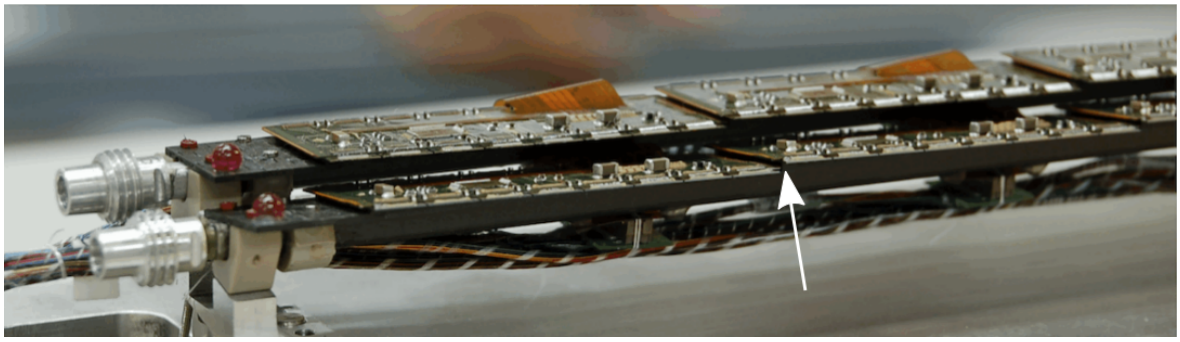


Figure 3.10.: Bi-stave of the ATLAS pixel detector before mounting. The arrow marks the point where two modules are shingled on top of each other's edges. The roofing of the two staves can be seen as well. At the left end of the staves, the connectors for the cooling pipes are visible. [Tro12]

In order to compensate the dead space of 1.1 mm due to the sensors inactive edge area, the module edges overlap each other (called 'shingling') at their short side on the stave, see arrow in Figure 3.10. This arrangement implicates a significantly increase of required space in rϕ-direction for each layer. The compensation of the dead space at the long side of the modules is done by an overlap of the staves, called 'roofing'. With this kind of arrangement the detector gets hermetic enclosed in the barrel region.

4. Plans for ATLAS Upgrades

4.1. LHC Schedule

In the current LHC shutdown, the collider will be prepared to run at its design energy of $7 + 7\,\text{TeV}$ (see Figure 4.1). The instantaneous luminosity which has reached up to now values up to $7.7 \cdot 10^{33}\text{cm}^{-2}\text{s}^{-1}$ [ATLPub] will be increased to the designated value of $1 \cdot 10^{34}\text{cm}^{-2}\text{s}^{-1}$. Until a shutdown in 2018, the integrated luminosity will have

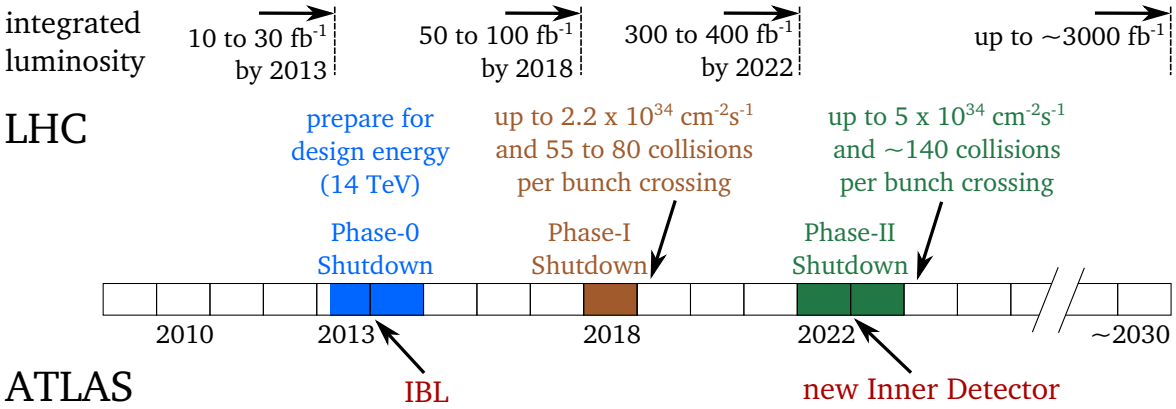


Figure 4.1.: Time schedule for the upgrades of LHC and ATLAS. Informations taken from [ATL12].

reached up to $100\,\text{fb}^{-1}$. After this Phase-I upgrade of the LHC, the peak instantaneous luminosity will increase to $2.2 \cdot 10^{34}\text{cm}^{-2}\text{s}^{-1}$ and deliver around 300 to $400\,\text{fb}^{-1}$ by 2022. At this time, the potential increase in statistics will not justify the effort of running such a huge and expensive machine. However, further improvements in the generation and collimation of high-intensity beams indicate that a luminosity of up to $5 \cdot 10^{35}\text{cm}^{-2}\text{s}^{-1}$ might be achievable with some upgrades to the accelerator. In this Phase-II, the so called High Luminosity LHC (HL-LHC) will begin collisions around 2024. It is planned to operate the machine until a total integrated luminosity of up to $3000\,\text{fb}^{-1}$ is reached [ATL12].

The costs for this improvement are a significantly increased number of pile-up events per bunch-crossing. This will lead to larger occupancies and radiation damage especially for the inner tracking detectors. The current LHC detectors will thus as well have to be upgraded to cope with these challenges.

4.2. ATLAS Pixel Upgrades

The upgrades of the ATLAS pixel detector are planned for the Phase-0 and the Phase-II shutdowns.

4.2.1. IBL

The design luminosity of the present ATLAS pixel detector is $10^{34}\mathrm{cm}^{-2}\mathrm{s}^{-1}$. As a first step to ensure a satisfactory operation of ATLAS also with higher luminosities, the current Phase-0 shutdown is used to install an additional pixel b-layer, the so-called insertable b-layer (IBL). The principle motivation is to provide an increased tracking performance like improving the track pattern recognition capability, the reconstructed track accuracy and the primary and displaced vertex identification performance (b-tagging) in high-luminosity conditions [IBL12]. This is particularly necessary as the tracking performance of the present pixel detector will decrease due to the emerging radiation damages.

Figure 4.2 shows a cross section of one quarter of the IBL, looking into beam direction. This new layer contains 14 staves and will be mounted on a new, smaller beam pipe at an average radius of 33 mm. With an outer envelope of 40 mm it fits within the existing b-layer.

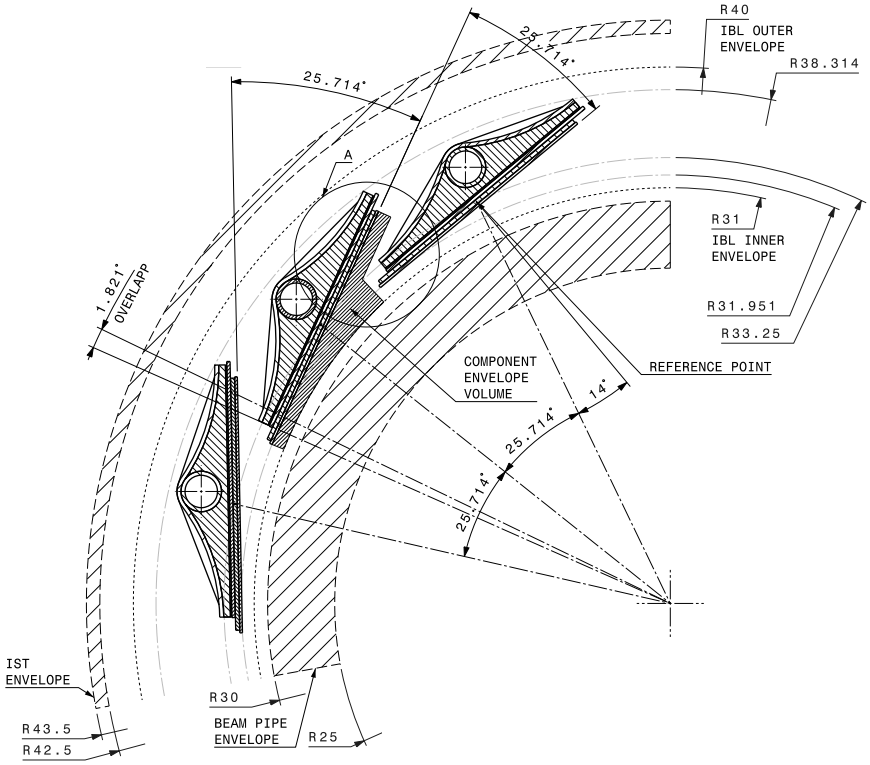


Figure 4.2.: Cross section of the $r\phi$-plane of one quarter of the IBL. [IBL10]

Due to the close proximity to the interaction point, a radiation tolerance up to a fluence of $5 \cdot 10^{15}\mathrm{n_{eq}}/\mathrm{cm}^2$ is required for sensors and read-out chips. This fact, as well as an expected high occupancy per pixel cell, leads to the necessity of a new read-out chip, the FE-I4 (see [IBL12]). Its pixel cells are shortened to $50\,\mu\mathrm{m} \times 250\,\mu\mathrm{m}$ so that the z-resolution is significantly improved. The pixels are arranged in a matrix of 336 rows times 80 columns, leading to dimensions of 20.2 mm × 18.8 mm; about five times larger than those of the present FE-I3.

The requirements for the sensors are furthermore the ability to operate at −15 °C after irradiation with a maximum bias voltage of 1 kV. The maximum power dissipation

at this temperature must not exceed 200 mW/cm^2 due to the limited cooling power capabilities. Because of the extreme spatial constraints of the IBL, its modules cannot be shingled anymore on the staves. They have to be arranged in a flat way so that the small module edges abut. The geometric inefficiency of the sensor caused by its inactive edge has to stay below 2.2% (see Section 4.3.1).

The current planning for the IBL foresees two scenarios. One option is to equip the central 75% of the staves with planar n$^+$-in-n sensors and in the high-η region 25% with 3D silicon sensors [Via09]. The second option foresees a 100% planar sensor solution. In both cases the planar modules are Double Chip Modules (DCM), i.e. one planar n$^+$-in-n sensor (Double Chip Sensor, DCS) is read-out by two FE-I4 chips. At the time of the submission of this thesis, the decision of which scenario will be carried out is not yet made. Further details of the IBL can be found in [IBL10].

4.2.2. New Inner Detector

To cope with the increased occupancy at HL-LHC, a complete replacement of the inner tracker will be necessary. Currently, only two detector technologies are foreseen: The strip detector outside the radius of $\sim$ 30 cm and the pixel detector inside of the $\sim$ 30 cm radius from the beam. The TRT is omitted completely. Outside the $\sim$ 30 cm radius the costs for pixel sensors would become unaffordable whilst inside, both occupancy and radiation damage become too large for strip sensors. For further details see [ATL12].

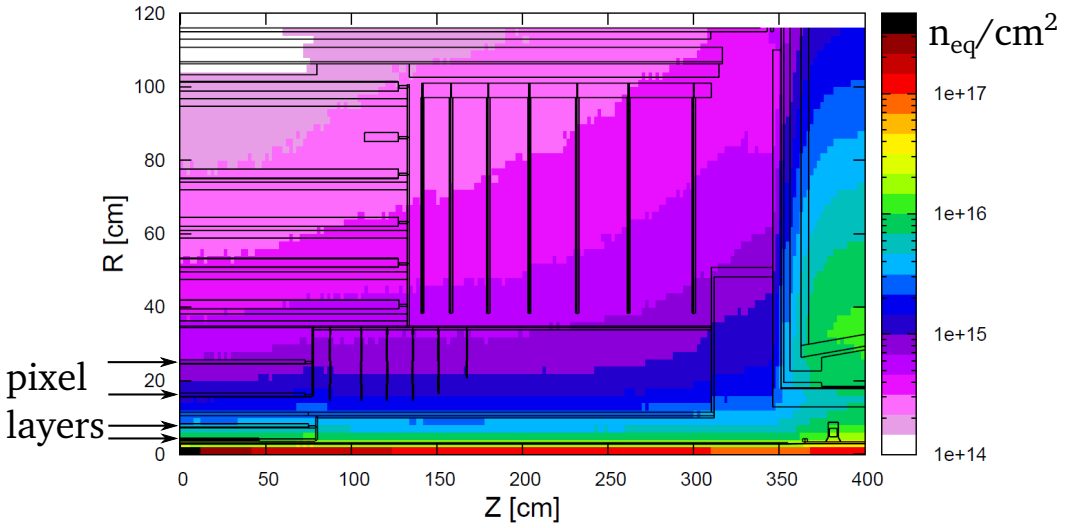


Figure 4.3.: Simulation of an rz-map of the neutron equivalent fluence, expected for the ATLAS Inner Tracker region, normalised to 3000 fb^{-1} of 14 TeV minimum bias events. Taken from [ATL12] and modified.

As ATLAS is using planar pixel sensors now and will continue to gain considerable experience during its operation, it is a natural choice to explore whether their radiation hardness is sufficient for HL-LHC usage. Simulations as seen in Figure 4.3 predict a NIEL dose of about $2 \cdot 10^{16}$n$_{eq}$/cm^2 for the innermost layer and around 10^{15}n$_{eq}$/cm^2 for the outermost pixel layer. Investigations of the radiation hardness of n$^+$-in-n sensors at HL-LHC fluences can be found in [Rum13] and [Alt14]. Improvements of the design and technologies which are relevant and of use for the ATLAS pixel Phase-II upgrades are presented in Chapter 7.

4.3. Sensor Improvements

4.3.1. Slim Edges

The spatial constraints for the IBL necessitate a flat edge-to-edge mounting of the modules on the stave. If the edge design of the current ATLAS pixel sensor is inherited for the IBL DCS, this would cause a geometric inefficiency in the order of 5%. This is incompatible with the 2.2% which is mandatory. This fact necessitates a drastic reduction of the sensors inactive edge region. An inefficiency of 2.2% relating to the IBL DCS would require a decrease of the inactive edge down to 450 μm per side.

Besides the spatial constraints in the IBL, the shingling of the modules on the staves implicates generally several disadvantages. The mounting is complicated as the alignment on the inclined stave is more challenging as on a flat one. More material is needed in the detector which implicates an undesired larger radiation length of the tracker. Furthermore, the cooling performance of the modules is limited due to the irregular basis.

For the outermost layers of a future detector, the option of a double-sided stave is feasible which enables a module overlap. In contrast the inner layers will likely rely on flat staves requiring again slim edges to achieve sufficient geometric efficiency. It is conceivable that the specifications to the inactive sensor fraction are even more demanding than for the IBL. It is planned to use the IBL read-out chip FE-I4 for the outer layers and the end cap discs of the HL-LHC upgrade. A successor model which is based on the FE-I4 will be used for the inner layers [ATL12]. Hence all results obtained with IBL-type sensors are also relevant and of note for the Phase-II ATLAS pixel upgrade.

Because the inactive area of the present ATLAS pixel sensor is necessary to decrease the high voltage to the cutting edge it has to be investigated in how far a reduction is compatible with a reliable sensor operation. These slim edge studies represent one main topic of this thesis.

After reaching the pixel side, the depletion zone propagates laterally into the edge region with increasing bias voltage. If it reaches the cutting edge, many charge carriers can be induced by surface impurities and cause a massive increase of the leakage current. Thus, a dependency of the breakdown voltage from the safety margin distance is expected. Furthermore, it has to be investigated in how far the situation changes after irradiation of the sensor. Due to the irradiation induced bulk type conversion, the planar n-type sensor behaves like a p-type sensor. Results are presented in Chapter 5.

An innovative method to decrease the inactive sensor edge without risking to reduce the sensor yield is a shifting of the active area opposite to the guard rings. This subject is illustrated in Section 5.3.2. Because this design approach was not used before, it has to investigate in how far the efficiency of these pixels behaves. Analyses of data taken in test beam setups are discussed in Section 5.5.

4.3.2. IBL Sensor Production

The usage of a new read-out chip for the IBL necessitates the fabrication of new compatible n^+-in-n sensors. Therefore, the existing planar pixel sensor design has to

be adapted to the FE-I4 geometry as well as to the IBL module specifications. The slim edge results have to be incorporated in order to guarantee a sufficient geometric efficiency.

A prototype production preceding to the main IBL production is required in order to do pretests with the new designed sensors, evaluate their functionality and, if applicable, change the design moderately. The design and the quality control of both productions until the flip chip step represent another topic of this thesis. The respective results of the prototype production are presented in Sections 5.3 and 5.4, those of the main IBL production in Sections 6.1 and 6.3.

5. Prototype Sensor Studies

5.1. Slim Edge Dicing Trials on Sensors

A first step in order to investigate in how far the sensors inactive edge can be reduced is done with FE-I3 single chip sensors (SCS) of the ATLAS production. Results of initial dicing tests can be found in [Wit09]. Section 5.1.1 represents a summary of these measurements.

All results of this Section 5.1 have been published in [Mue10].

5.1.1. Dicing Trials

Procedure

In order to characterize the functionality of a silicon sensor, an IV measurement is the most meaningful test. An increasing negative high voltage is applied to the high voltage electrode on the p-side whilst the leakage current is measured on the grounded n-side. As long as the depletion zone expands in the bulk, the leakage current increases square root like, mainly caused by the volume generation current. After V_{depl} is reached, the current should saturate in a flat plateau for an ideal sensor. Because the bulk has a not completely negligible conductivity, the ohmic part of the current causes a more or less flat slope. A breakdown indicates an avalanche like increase of the leakage current. In order to guarantee a stable operation, the sensor should not be biased in the range of a breakdown.

A schematic of a setup for IV measurements can be seen in Figure 5.1. In this case the diced sensor is lying on a grounded metal chuck, n-side down. The high voltage pad is contacted via a probe needle. The measurement is done by a *Keithley 487* device which serves as a pico-amperemeter as well as the high voltage source. An additional temperature logging is done via a *Keithley 196* multimeter (not in the sketch) which measures the resistivity of a PT100 temperature probe. Both devices are read out via GPIB and controlled by a *Lab-View* software.

A total number of 76 diced FE-I3 SC sensors of the ATLAS production are IV measured initially up to 500 V to guarantee that all of them withstand voltages of more than 350 V. Concerning the ATLAS quality assurance criteria (see [ATL03]) the sensor should have a leakage current below 100 nA at the operation voltage of 150 V. These sensors with a much higher breakdown voltage have been selected in order to be able to see deteriorations in the IV characteristic afterwards.

The sensors are then cut with a conventional diamond wafer dicing saw outside the active area. They are divided into seven groups where each group is assigned to one

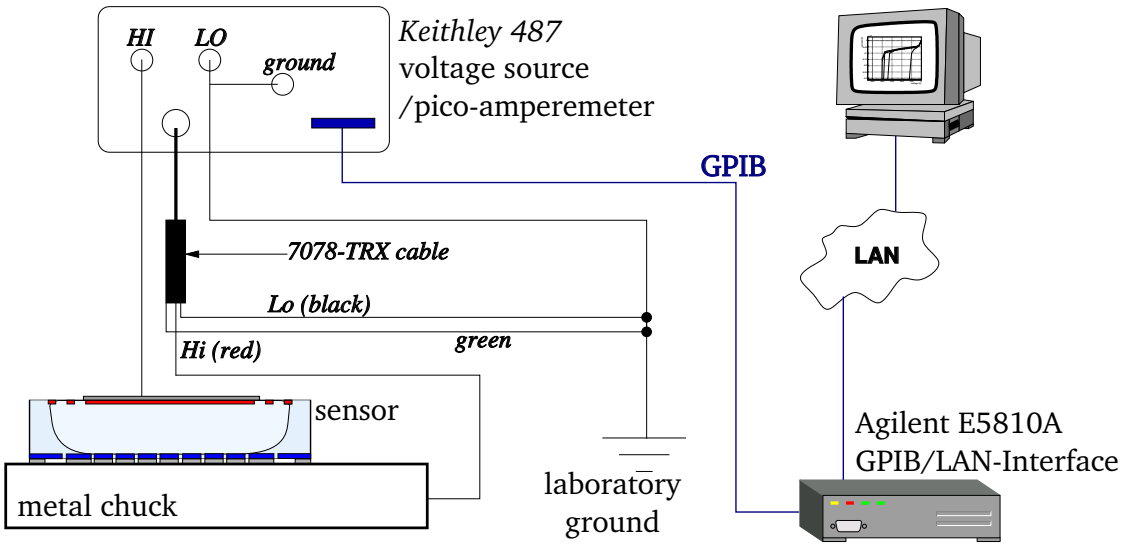


Figure 5.1.: Schematic of the setup for IV measurements. The high voltage is applied via a probe needle. In this sketch the sensor is already diced and the ground contact is given by a metal chuck. If the sensor is still not separated, the wafer is fixed at its edge and the ground is applied via a second probe needle to the dicing street. Original taken from [Rum09] and modified.

cutting position. An overview can be seen in Table 5.1. Figure 5.2 shows a sketch of the sensors inactive edge between the dicing street and the active area. The guard rings can be seen in red. The seven cutting positions are marked in green.

Table 5.1.: Overview of the seven cutting positions and distances from the high voltage pad.

	cutting position	distance from high voltage pad
1	half of safety margin cut away	810 μm
2	three quarter of safety margin cut away	670 μm
3	16 guard rings remaining	590 μm
4	15 guard rings remaining	530 μm
5	13 guard rings remaining	420 μm
6	11 guard rings remaining	315 μm
7	cut into inner guard rings	170 μm

Because of the imprecise alignment of the wafer saw, an error tolerance for the distance in the order of 30 μm has to take into account. The seventh position is, depending on the accuracy of the alignment, equal to six or seven remaining guard rings.

After cutting one or two sides (for some sensors even three or four sides) at the described positions, the sensors are characterised again after each step. It is observed that if a significant reduction of the breakdown voltage occurred, this happened already after the first cut. Subsequent cutting steps do not lead to significant further reduction.

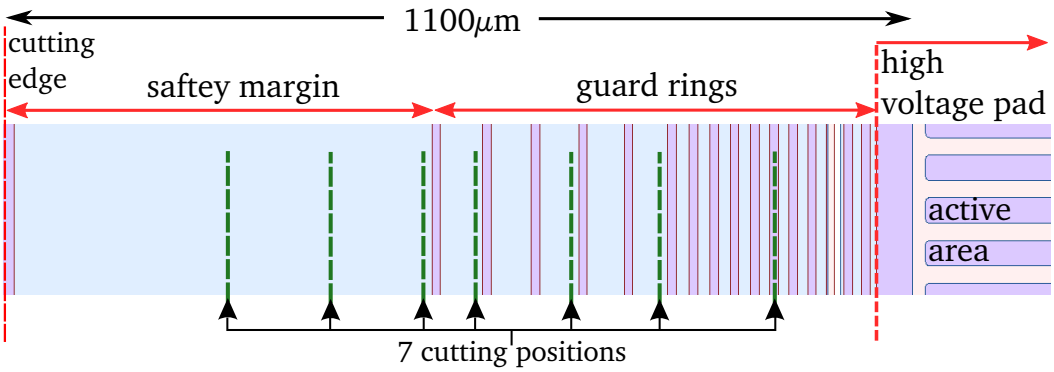


Figure 5.2.: Sketch of the different cutting positions that were chosen: The three outer ones only reduced the safety margin while the four inner ones removed some of the guard rings. n^+-implantation on the pixel side in blue, p^+-implantation on the back side in red.

Results

A summary of the described dicing trials can be seen in Figure 5.3. The mean breakdown voltage is plotted against the remaining inactive edge after cutting (see Table 5.1). The vertical error bars indicate the standard deviation, the horizontal ones the uncertainty due to the dicing position. In this case the breakdown voltage is defined as the last voltage value which was measured before reaching the current compliance of 1000 nA. If the compliance is not exceeded, the maximum voltage of 500 V is taken.

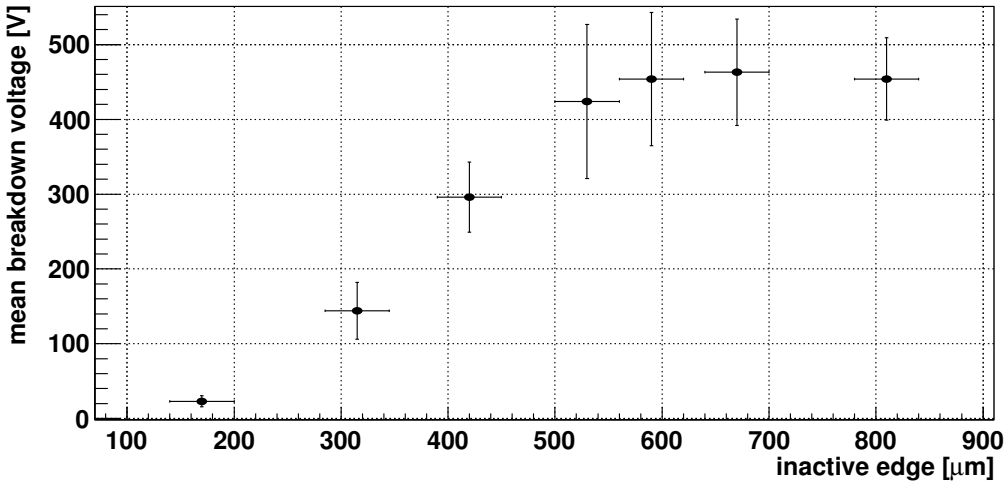


Figure 5.3.: Mean breakdown voltage of the unirradiated sensors, plotted against the remaining inactive edge after the slim edge cutting. The error bars indicate the standard deviations. As long as the guard rings are not affected (three rightmost positions), the breakdown voltage stays constant. By cutting off the guard rings the breakdown voltage decreases with the reduced safety margin.

In the plot two linear trends can be identified. As long as the cut is done in the safety margin outside the guard rings (positions 1, 2 and 3) the breakdown voltage appears to stay constant within the error bars. This effect can be attributed to the maximum bias voltage of the voltage supply so that higher breakdown voltages than 500 V cannot

be determined. If they were taken into account, it is supposable that the breakdown voltages would rise further with increasing safety margin.

The second linear trend is visible in the decrease of the breakdown voltage if the number of guard rings is reduced (positions 4 to 7). Nevertheless, only the most aggressively cut sensors definitely fail to fulfil the ATLAS quality assurance criteria. In particular, the position 5 with 13 remaining guard rings and approximately 420 μm of inactive edge width appears acceptable with sufficient safety margin for full depletion of a 250 μm thick sensor before irradiation. Eleven guard rings on average seem enough to grant full depletion. However, individual samples breakdown at around 100 V which is less than demanded by ATLAS quality assurance criteria. A further reduction to 7 guard rings or less prevents the operational capability of unirradiated sensors.

One explanation for this behaviour could be the fact that the cutting was done using a tool which might have inflicted crystal damage at the cutting edge. This damage can extend some tens of μm into the sensor area and disabling the function of more guard rings than have been cut. Besides, the fact that no dicing streets are used results in a blurred edge containing partially n^+-implants and/or metal which can modify the electric field at the edge.

5.1.2. Results after Irradiation

Procedure

In order to investigate in how far the IV characteristic changes after irradiation induced bulk conversion, 56 of the sensors are neutron irradiated at the TRIGA reactor of the Jožef Stefan institute in Ljubljana [Lju]. They are distributed again into four groups of different fluences:

- $0,5 \cdot 10^{15}\,\mathrm{n_{eq}/cm^2}$
- $2 \cdot 10^{15}\,\mathrm{n_{eq}/cm^2}$
- $7 \cdot 10^{15}\,\mathrm{n_{eq}/cm^2}$
- $15 \cdot 10^{15}\,\mathrm{n_{eq}/cm^2}$

The fluences cover different stages of irradiation during the operation of ATLAS. The lowest fluence corresponds to the situation shortly after type conversion whereas the highest one represents the magnitude of HL-LHC conditions. After irradiation, they were stored in a freezer to avoid uncontrolled annealing until the activation had sufficiently worn off after approximately 2 months. For reference purpose several sensors diced at the conventional cutting edge were included in the irradiation procedure.

The IV measurements of the irradiated sensors works in principle as described previously for unirradiated ones. A challenge is the leakage current which is highly increased for irradiated sensors in comparison to unirradiated ones (compare Section 3.2, Equation (3.5)). To compensate this and avoid a sensor self-heating, it has to be cooled during the measurement as it is done in later detector operation. Therefore, the sensor is lying on a brass plate which is cooled down to $\sim -15\,^{\circ}\mathrm{C}$ by a Peltier cooler. A PID (proportional-integral-derivative) control is used to stabilise the temperature at a constant level.

For planar sensors the depletion voltage is strongly correlated with the irradiation fluence (see Equation (3.3)). To guarantee a sufficient charge collection, the bias voltage has to be increased respectively. In this case the sensors are measured up to voltages of 1500 V applied by a *Keithley 248* HV source. The bias voltage is fed to the single chip sensors via a spring. The pixel side is contacted via the cutting edges of the sensors using the brass plate.

Results

Figure 5.4 shows one example of the IV measurements of the irradiated sensors with the fluence of $7 \cdot 10^{15}\,\mathrm{n_{eq}/cm^2}$. The leakage currents are normalized to the intended temperature of $-15\,°\mathrm{C}$ by using Equation (3.2).

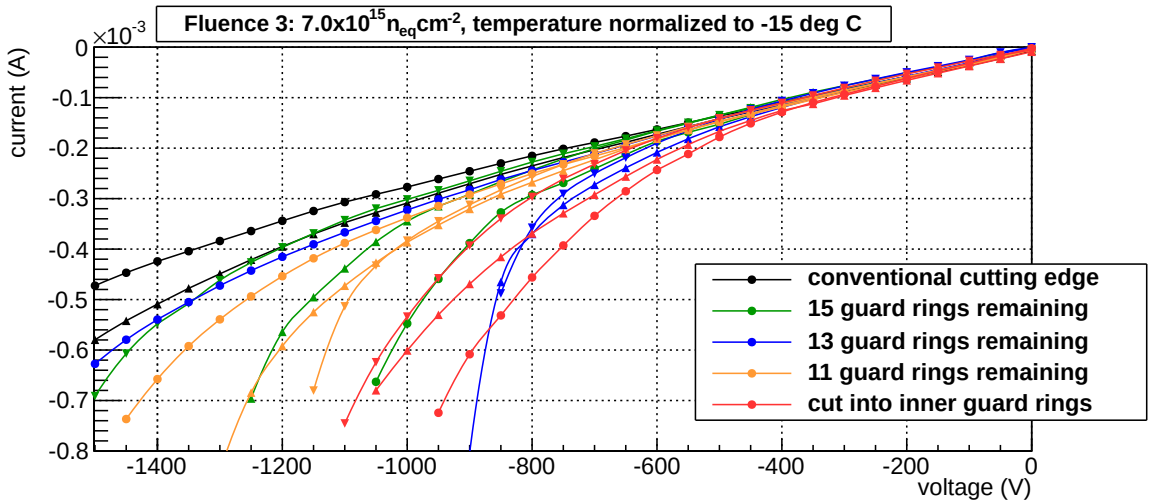


Figure 5.4.: Example of the IV measurements of the irradiated sensors with the fluence of $7 \cdot 10^{15}\,\mathrm{n_{eq}/cm^2}$. The leakage currents are normalized to $-15\,°\mathrm{C}$. The different cutting positions are encoded by different colours.

It can be seen that after irradiation, no sudden breakdowns occur any more. This indicates that the guard rings are mainly necessary before irradiation. After the irradiation induced bulk conversion it appears that their functionality is considerably changed. However some kind of escalations of the currents beyond a bias voltage of about 700 V are obvious. One explanation is a significant sensor self-heating due to an insufficient cooling. The measured temperatures on the brass plate showed an increase of more than 4 °C with increasing voltages. Although the leakage currents are normalized to $-15\,°\mathrm{C}$ it cannot be excluded that the actual sensor temperature was even higher than the temperature of the brass plate.

A trend that the escalation effect is more pronounced in samples with slimmer edges is visible. This could indicate that the number of guard rings is still important for the control of leakage currents after irradiation. On the other hand it is also conceivable that it is just an effect of a declined heat transfer from the sensor to the chuck due to the reduced contact surface at the sensors edges.

Because of the shape of the IV curves of the irradiated sensors it does not make any sense to identify a kind of breakdown voltage as it is done for the results of the

unirradiated sensors. To achieve a consistent picture, the mean leakage current at one defined voltage and the related standard deviation were derived for samples cut at different edge positions and irradiated to the different fluences. The values are plotted in Figure 5.5 against the remaining inactive edge after cutting. A voltage of 600 V is chosen as in that range the escalation is still not existent. The vertical error bars indicate the standard deviation, the horizontal ones the uncertainty due to the dicing position.

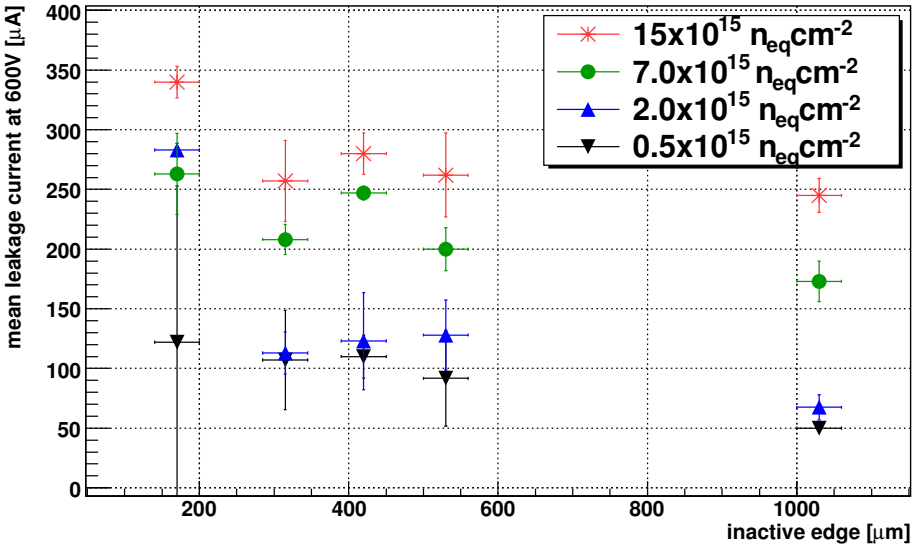


Figure 5.5.: Results of the slim edge cut sensors after irradiation. The mean leakage current at 600 V is plotted against the remaining inactive edge. The vertical error bars indicate the standard deviation, the horizontal ones the uncertainty due to the dicing position. The different fluences are encoded by different colours. It can be seen that the leakage currents are by trend increasing with the fluence and slightly for reduced edge widths. For the most aggressive cut a significant rise is seen especially for the two lower fluences.

As it can be seen the leakage currents of the irradiated sensors are increasing with the fluence as expected. Furthermore, they increase slightly for reduced edge widths. Only for the most aggressive cut, a significant rise is seen especially for the two lower fluences. This effect was already discussed before. The current changes down to 300 μm edge width are almost negligible if the uncertainty of the actual sensor temperature is taken into account. Nevertheless even the current increase of the most aggressively cut sensors is tolerable.

5.1.3. Discussion

The presented results show that a significant reduction of the distance between cutting edge and high voltage pad of ATLAS pixel sensors is feasible. Before irradiation the sensors with 13 remaining guard rings and $\sim$ 420 μm inactive edge clearly fulfil the ATLAS quality criteria. This is an important result as the IBL design specification of 450 μm inactive edge can already be fulfilled. Even a reduction to 11 guard rings seems realistic taking into account the option of adapting the quality criteria to future

sensor layouts. For example a reduced bulk thickness can implicate the possibility to decrease the operation voltage. This subject is further discussed in Section 5.4.

After irradiation the situation is getting less critical. The reduction of the safety margin including the guard rings has no considerable influence on the leakage current. The influence of the temperature on the leakage current is in contrast much more important.

5.2. Leakage Current Dependencies of Irradiated Sensors

It was shown that for irradiated sensors the reduced inactive edge distance only influences the leakage current insignificantly. It is expected that the sensor temperature as well as an annealing step will cause a larger impact on the leakage current and thus to the sensor power dissipation.

5.2.1. Temperature Dependencies

Three FE-I3 single chip sensors are regarded which are neutron irradiated to a fluence of $7 \cdot 10^{15}\,\mathrm{n_{eq}/cm^2}$. In order not to overlay different effects, those have been selected which have been diced at the conventional cutting edge. Figure 5.6 a) shows the result of the IV measurements at $-15\,℃$ in green and at $-25\,℃$ in blue.

The leakage current decrease with the lower temperature is obvious. For example at 1000 V and also below it is decreased by a factor of ~ 3.9. This is even a bit more than the theoretical value of 3.4 which is expected for these temperatures (compare Equation (3.2)). One explanation is that the sensor self-heating effect is much more dominant at higher temperatures. If the sensor is cooled to lower temperatures, this effect is supposably suppressed from the outset and an escalation is much more unlikely. It again has to be taken into account that the temperature is not measured on the sensor so that a possible light and lingering temperature increase could not be noticed.

In Figure 5.6 b) the values are translated to the electrical power $P = V \cdot I$ nominated per square centimetre. It can be seen that the approximative linear voltage dependency of the current translates into a quadratic dependency of the power. The yellow dashed line in both plots marks $200\,\mathrm{mW/cm^2}$. As already mentioned, this value is the normalized power dissipation benchmark for the IBL sensors. For the IBL condition at $-15\,℃$ and a maximum bias voltage of 1000 V the power consumption exceeds this limit as seen in the plot. One has to keep in mind that the fluence is actually a bit higher than the IBL benchmark of $5 \cdot 10^{15}\,\mathrm{n_{eq}/cm^2}$. It can be assumed that for the IBL end-of-life scenario the power dissipation would be slightly lower.

For possible HL-LHC scenarios higher voltages than 1000 V may be necessary for planar $\mathrm{n^+}$-in-n sensors to guarantee a sufficient collected charge. In this case a cooling down to $-15\,℃$ will not be sufficient at all as the thermal runaway gets uncontrollable as seen in Figure 5.6. However by cooling down to $-25\,℃$ the power dissipation reaches the $200\,\mathrm{mW/cm^2}$ limit at $\sim 1200\,\mathrm{V}$. To be operable up to 2000 V, the temperature would have to be reduced further, e.g. in this case down to $-35\,℃$. Furthermore, the investigated fluence of $7 \cdot 10^{15}\,\mathrm{n_{eq}/cm^2}$ is of course not representative for an expected

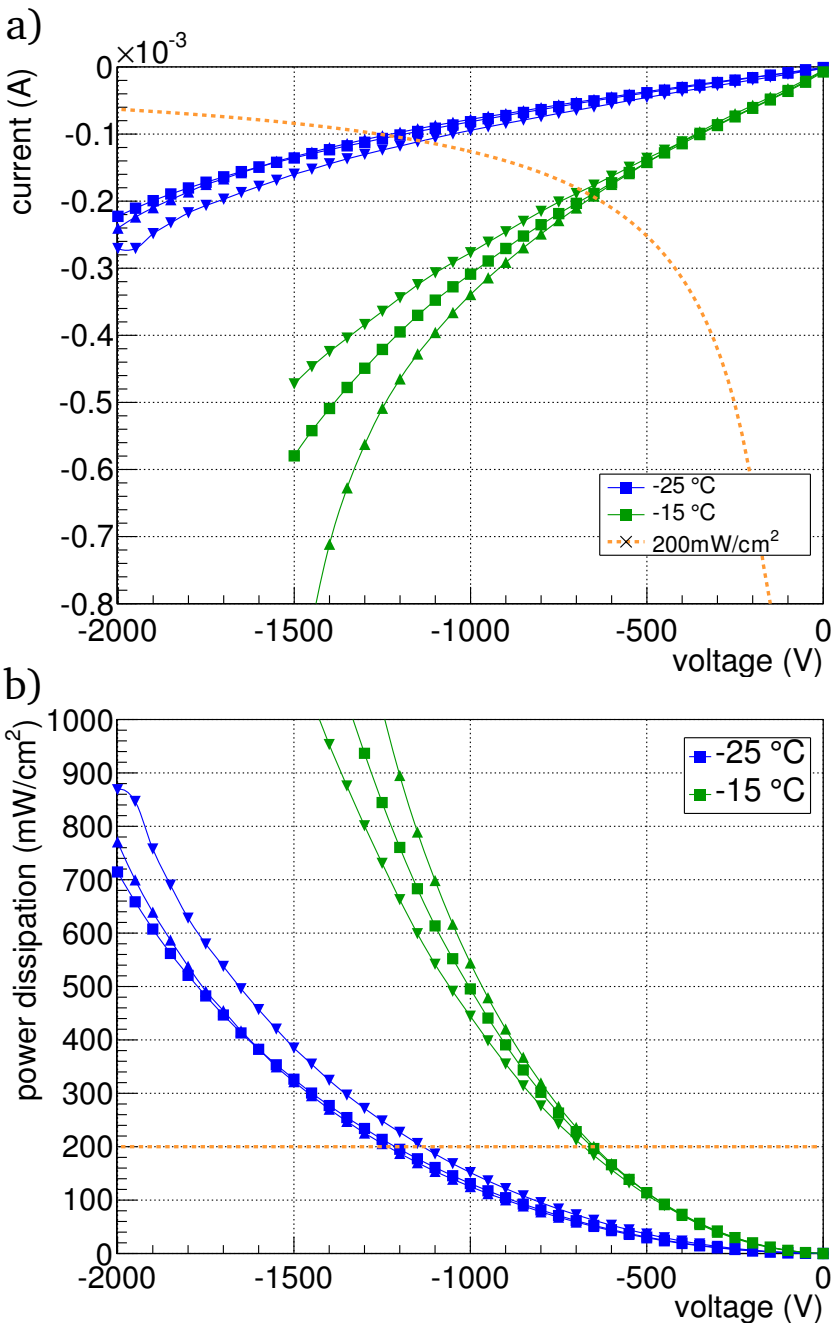


Figure 5.6.: a): IV measurements of three neutron irradiated sensors with a fluence of $7 \cdot 10^{15}\,\mathrm{n_{eq}/cm^2}$. The measurements are performed at $-15\,°\mathrm{C}$ (green) and at $-25\,°\mathrm{C}$ (blue). The current reduction at $-25\,°\mathrm{C}$ is obvious. In b) the currents are translated to the electrical power nominated per square centimetre. It can be seen that the approximative linear voltage dependency of the current translates into a quadratic dependency of the power. The yellow dashed line in both plots marks the IBL benchmark of $200\,\mathrm{mW/cm^2}$.

HL-LHC scenario. Higher power consumptions due to higher irradiation damages will have to be compensated with even lower operation temperatures or controlled annealing steps.

5.2.2. Annealing Studies

As pointed out in Section 3.2.2 there will be designated machine shutdowns where the ATLAS pixel detector will be warm-up for a longer time period. These monitored annealing phases are beneficial for the operation as the sensors leakage current and thus their power dissipation can be reduced.

An investigation is done with two sensors irradiated to $4 \cdot 10^{15}\,\mathrm{n_{eq}/cm^2}$. It is tried to simulate a warm-up period of 100 days at 20 °C which could be a realistic scenario. To

accelerate the annealing process significantly, the sensors can be heated in an oven. Therefore, it is calculated for which t-T_a-pairs the current related damage rate α (see Equation (3.6)) takes the same value as for 100 days at 20 °C which is

$$\alpha_{100\,\mathrm{d},20\,^{\circ}\mathrm{C}} = 3.145 \cdot 10^{-17}\,\mathrm{A/cm} \quad . \tag{5.1}$$

The result is ~ 5.75 hours at 60 °C. The measured power dissipation at −15 °C before (in green) and after (in red) annealing is seen in Figure 5.7.

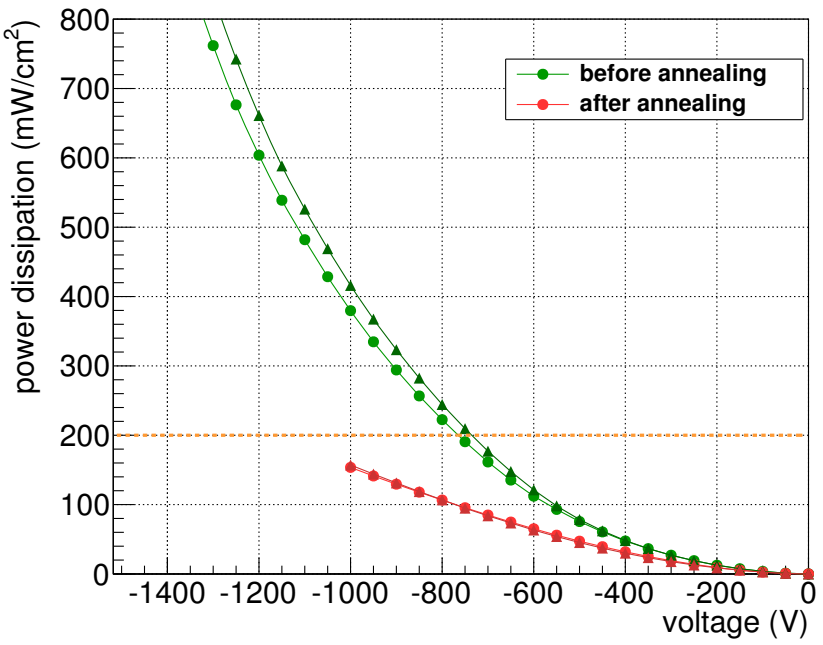


Figure 5.7.: Power dissipation at −15 °C of two sensors irradiated to $4 \cdot 10^{15}\,\mathrm{n_{eq}/cm^2}$ plotted against the operation voltage. It can be seen the results before (green) and after (red) the annealing step of $\sim$ 5.75 hours at 60 °C. A clear reduction can be observed afterwards. Even at 1000 V the power dissipation stays significantly below the IBL benchmark of 200 mW/cm².

The reduction of the power dissipation after the annealing step is obvious. Whereas the 200 mW/cm² limit is reached at 750 V before annealing it afterwards stays well below up to 1000 V. At 1000 V the power consumption is reduced by a factor of ~ 2.6. It has to be taken into account that the fluence applied to the sensors are slightly reduced compared to the IBL benchmark. The leakage current is linear dependent with the fluence if the same depleted volume is by approximation assumed to be constant (see Equation (3.5)). With this assumption an extrapolation of the expected power dissipation for $5 \cdot 10^{15}\,\mathrm{n_{eq}/cm^2}$ can be made by multiply the factor 1.25. Even for the maximum bias voltage of 1000 V it hence should not exceed the 200 mW/cm² limit. This extrapolation is actually conservative as the depleted volume is rather decreased for higher fluences and the resulting leakage current should be rather lower.

The previous results show that planar $\mathrm{n^+}$-in-n sensors are capable to deal with one of the basic IBL criteria. The power consumption benchmark of 200 mW/cm² can be maintained up to the maximum operation voltage of 1000 V at −15 °C taking into account a designated annealing phase. Thus, an operation under IBL conditions is in principle feasible. This result does not yet give information about the performance of irradiated sensors. Detailed radiation hardness studies including for example the hit efficiency and collected charge can be found in [Rum13] and [Alt14].

5.3. Design of the Prototype Sensors

Parts of this section have been published in [Wit12].

5.3.1. Modifications to the Present ATLAS Pixel Sensor

Based on the sensor design developed for the ATLAS pixel detector, modifications were made for the upgrade sensors. In order to be compatible to the newly developed FE-I4 read-out chip, the sensor geometry had to be adapted. The pixel size has been shrunk to 250 μm $\times$ 50 μm which results in better z-resolution of the detector along the beam pipe and in a lower hit occupancy per pixel. The pixel matrix is enlarged to 80 columns $\times$ 336 rows so that the area of an FE-I4 covers nearly six times the area of an FE-I3. The IBL will consist of n$^+$-in-n 2$\times$1 Double Chip Sensors (DCS), i.e. one sensor is read out by two FE-I4 chips as seen in Figure 5.8b).

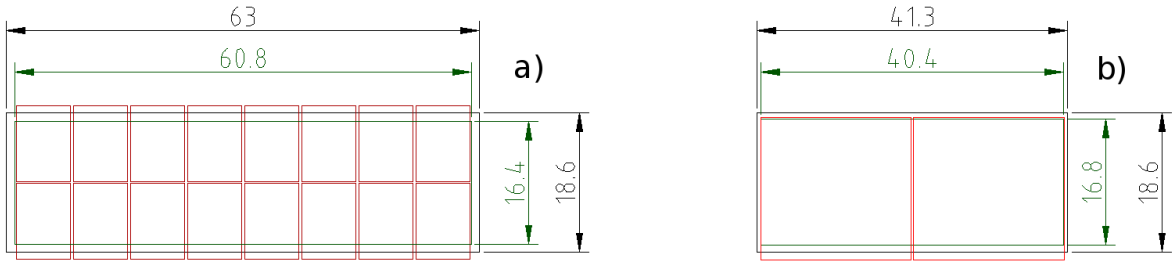


Figure 5.8.: Comparison of the dimensions of the present ATLAS pixel module (a)) and the planar IBL module (b)). The sensor cutting edges are in black, the sensor active area in green and the Front-End read-out chips in red. Dimensions in mm.

To accommodate the edge region of the read-out chip and a necessary gap between them, the sensor pixels of the inner edge columns (the last of the left and the first of the right chip) are extended to 450 μm. In comparison to the ATLAS pixel module there are no gaps between the Front End chips in the vertical direction which have to be covered with ganged pixels (compare Figure 3.4). For this reason the IBL DCS have no ganged pixels.

The additional bump pads which ground the bias grid ring and the surrounding outer guard can be seen in Figure 5.9. In the ATLAS pixel design these bump pads are placed within the first and last column, in the IBL design they are placed within the second and last but one (bias grid ring) and within the third and last but two (outer guard) column. These bumps are routed to ground via the read-out chip. Within the FE-I4A, the two bumps are shorted together while for the FE-I4B, they are accessible separately.

5.3.2. Sensor Edge Design

A comparison of the IBL and the ATLAS pixel sensor edge design can be seen in Figure 5.10. In the ATLAS pixel sensor design (Figure 5.10 a)) the 16 guard rings

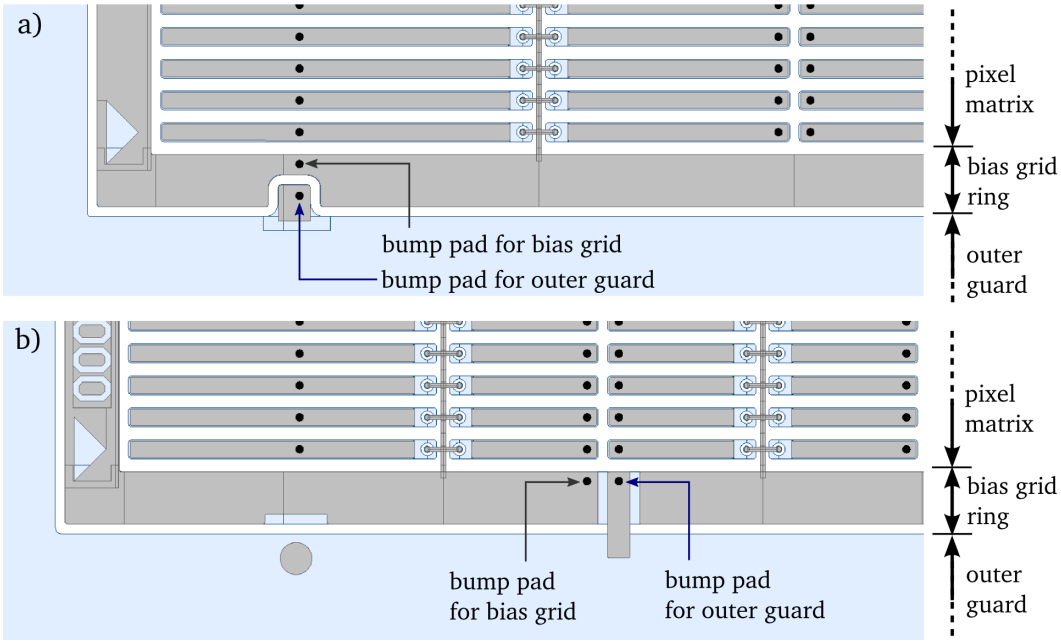


Figure 5.9.: Top view of the n-side corner of the active area of the ATLAS pixel (a)) and the IBL design (b)). The n^+-implantation is blue, the metal grey. The additional bump pads (black circles) which ground the bias grid ring and the outer guard are marked.

covering a width of about 600 μm and the 500 μm safety margin are adding up to an overall inactive edge of 1100 μm between the edge pixels and the cutting edge.

For the IBL design the inactive edge distance between the pixel matrix and the cutting edge has to shrink to below 450 μm. Figure 5.10 b) shows a conservative design which stays as close as possible to the proven and established ATLAS pixel design. The number of guard rings is decreased to 13 and the safety margin is reduced to $\sim$ 90 μm. The 450 μm distance from the high-voltage pad to the cutting edge is still above the 300 - 400 μm distance which appeared to be necessary for high yield and stable operation (see Section 5.1.1).

In order to minimize the sensors dead edge area, a second slim edge IBL design was produced which is shown in Figure 5.10 c). The only difference to the conservative design is that the edge pixels are extended to 500 μm length so that one half of them is placed opposite to the guard rings. This is possible for n^+-in-n sensors as guard rings and pixels are on opposite sides of the wafer. Concerning the breakdown behaviour there is no difference expected to the conservative design because the p-side on which the high voltage drop takes place is completely the same in both cases.

Because of the offset between the high voltage pad and the pixels in the slim edge design, an inhomogeneous electric field is expected in the region of the pixel overlap. Hence the depletion zone will not be developed uniformly and a decrease in the hit efficiency is supposable. This effect is in particular significant before irradiation induced type inversion as then the depletion zone grows from the high-voltage implantation side. After irradiation, the zone of maximum field strength is directly underneath the pixel implantation so large efficiencies are expected almost until the end of the implantation.

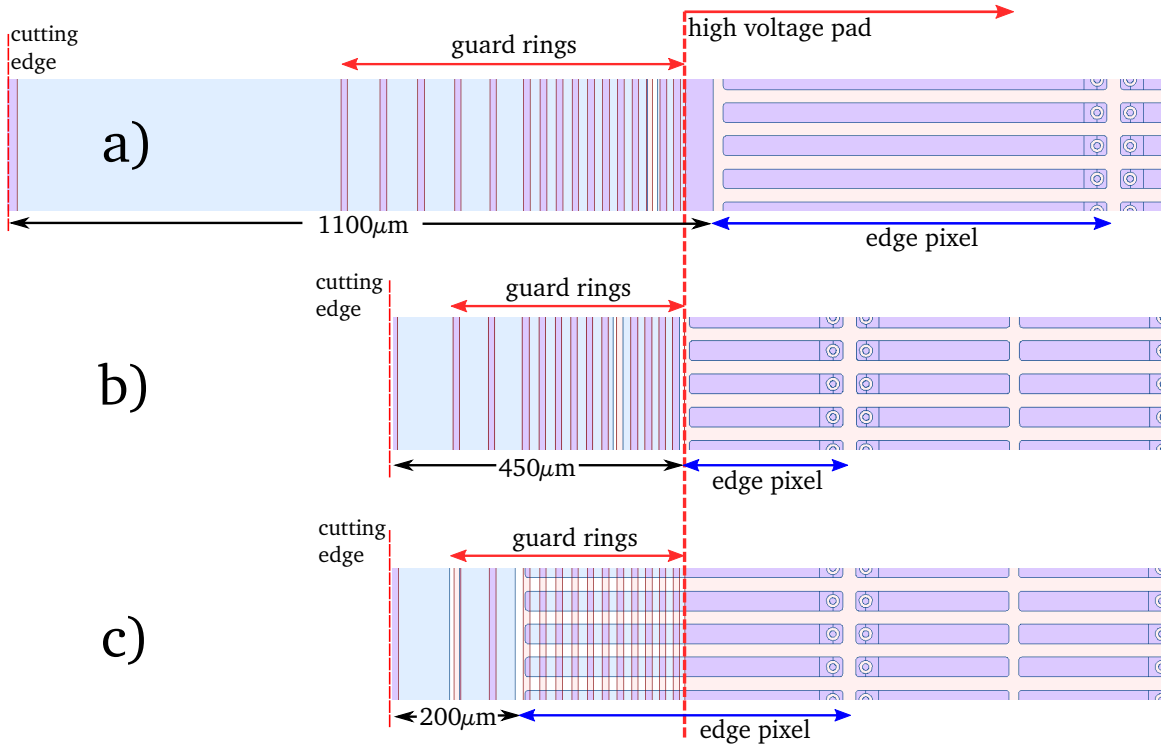


Figure 5.10.: Top view of the sensor edge region of the ATLAS pixel (a)), the conservative (b)) and the slim edge (c)) IBL design. The n^+-implantation is seen in blue, the p^+-implantation in red. By reducing the number of guard rings, narrowing of the safety margin and by extending the edge pixels beyond the high voltage pad, the inactive edge could be reduced from 1100 μm for the ATLAS pixel design to $\sim$ 200 μm for the slim edge IBL design.

5.3.3. Wafer Overview

The prototype wafer with four inch diameter in n^+-in-n technology was produced in 2010 at the sensor vendor CiS in the course of the ATLAS PPS community [PPS08]. One main goal was the production of FE-I4 compatible n^+-in-n sensors in which the IBL related constraints as described in the previous subsections were implemented. Furthermore, it was used to test several kinds of FE-I3 based sensors and diodes with different guard ring variations.

The process parameters were taken from the ATLAS pixel production [Hue01, ATL03] as these current sensors showed a well investigated and proven performance. The substrate material is DOFZ with a $\langle 111 \rangle$ bulk crystal orientation and a resistivity of 2 to 5 kΩcm.

One parameter to be changed was the bulk thickness which has been 250 μm in the ATLAS pixel production. As shown for other planar sensors, a higher charge collection especially after high irradiation was measured for thinner sensor bulks [Cas10, Cas11]. A possible explanation is that a certain bias voltage applied to a thinner sensor causes a higher electric field than for a thicker one. Further advantages are a reduction of the depletion voltage for the irradiated sensor and a reduced radiation length which is generally desired for the pixel detector. On the other hand the reduced bulk thickness necessitates a more careful handling. A lower yield not only in the initial step of

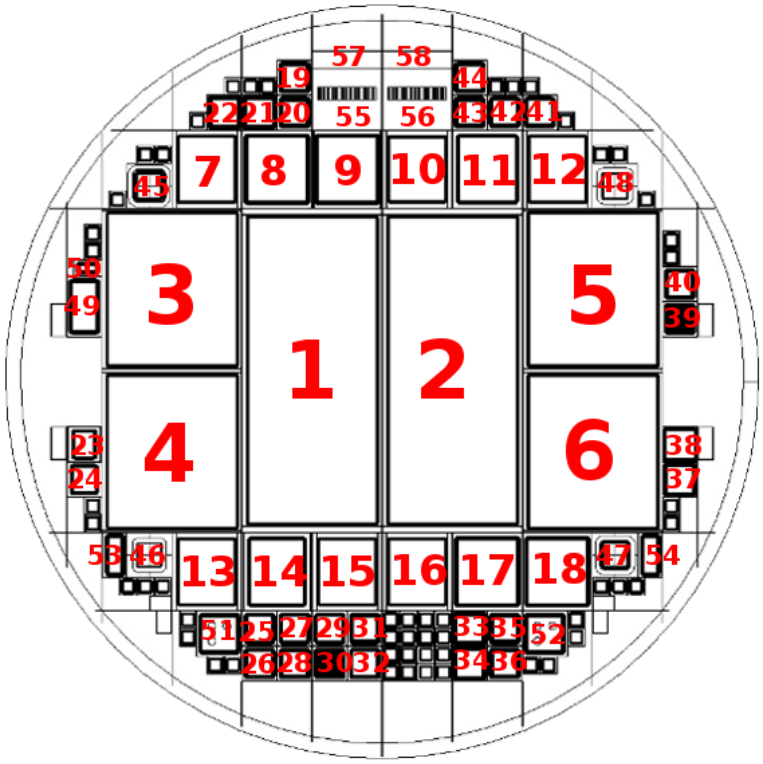


Figure 5.11.: Overview of the prototype production wafer of 2010. View to the n-side. The structures are listed in Table 5.2.

the wafer processing but also during the sensor measurements and the UBM post-processing and dicing are supposable. Furthermore, the charge generated by a MIP is dependent of the size of the depleted bulk (see Section 3.1.2). The reduced thickness will initially lead to less charge for the unirradiated sensor. This implication does though not represent any problem. As long as the sensor is unirradiated the total amount of generated charge is large enough. After irradiation this effect is supposably compensated by the higher electric field. For highly irradiated sensors it is anyhow not reasonable anymore to deplete the bulk completely as the depletion voltage is increasing disproportional (see Equation (3.3)).

The wafer production was divided into five batches with different bulk thicknesses. It have been ordered 10 wafers in 250 μm and respectively 5 wafers in 225, 200, 175 and 150 μm. The small steps of 25 μm were chosen in order to be able to compare the advantages and disadvantages of each thickness as no experience with thinner bulks were gained before. The wafer vendors have been Rockwood[1] and Okmetic[2]. The wafer thinning process was done at Wafer World[3].

The wafer layout is the same for all thicknesses. Figure 5.11 shows an overview of the wafer design and Table 5.2 gives a short description of the most important structures on the wafer. It contains two FE-I4 DCS and four SCS, respectively one half with the conservative and the other half with the slim edge IBL design.

The structures are placed and dimensioned in that way that most of the dicing streets can be sawed without the necessity of re-taping the wafer. Anyhow for the FE-I4

[1]Rockwood Wafer Reclaim, Greasque, France, http://www.rockwoodwaferreclaim.com/
[2]Okmetic Headquarters, Vantaa, Finland, http://www.okmetic.com/
[3]Wafer World Inc., Palm Beach County, FL, USA http://www.waferworld.com/

Table 5.2.: Reduced overview of the structures on the prototype production wafer of 2010.

	structure	properties
1	FE-I4 DCS	no long pixel v4, 13 GR, pixel overlap 0 μm
2	FE-I4 DCS	Slim Edge v2, 13 GR, pixel overlap 250 μm
3	FE-I4 SCS	Slim Edge v2, 13 GR, pixel overlap 250 μm
4	FE-I4 SCS	no long pixel v4, 13 GR, pixel overlap 0 μm
5	FE-I4 SCS	no long pixel v4, 13 GR, pixel overlap 0 μm
6	FE-I4 SCS	Slim Edge v2, 13 GR, pixel overlap 250 μm
7	FE-I3 SCS	Slim Edge v1, 13 GR, pixel overlap 250 μm
8	FE-I3 SCS	pixel shifted stepwise, 16 GR
9	FE-I3 SCS	conventional design v3, 16 GR, with p^+edge
10	FE-I3 SCS	Liverpool design, rd50, 6 GR on n-and p-side
11	FE-I3 SCS	LAL design v2, 6 GR pixel overlap 100 μm,
12	FE-I3 SCS	no long pixel v4, 13 GR, pixel overlap 0 μm
13	FE-I3 SCS	Slim Edge v2, 13 GR, pixel overlap 150 μm
14	FE-I3 SCS	LAL design v3, 6 GR pixel overlap 300 μm,
15	FE-I3 SCS	no long pixel v4, 13 GR, pixel overlap 0 μm
16	FE-I3 SCS	Slim Edge v1, 13 GR, pixel overlap 250 μm
17	FE-I3 SCS	pixel shifted stepwise, 16 GR
18	FE-I3 SCS	conventional design v2, 16 GR, without p^+edge
19 - 48	GR diodes	different design of GRs or active area
49 - 58	test structures	different purposes

sensors a second dicing step has to be made at the short pixel side, i.e. the so called slim edge side where the sensors have to stay within the 450 μm distance between edge and pixel matrix due to the IBL constraints. A sketch can be found in Figure 5.12.

The conventional dicing street in green is too far away from the active pixel matrix. Additional dicing steps have to be made at the slim edge dicing streets. These are implemented as simple p^+-implantation strips which are approximately twice the width of the cutting line. They are placed close to the outermost guard rings in order to guarantee a defined ground potential.

5.4. Quality Inspection of the Prototype Production

The quality inspection of the prototype wafer production comprises basically IV measurements of the FE-I4 based sensors to guarantee their operating ability. These sensors are the first of its kind which are investigated. Especially as no experience with thinner bulks were gained before it is reasonable to supervise the sensor performance during the complete post process chain.

The first quality inspection is done at the sensor vendor who performs IV measurements of the six FE-I4 sensors and a CV measurement on one diode after the processing. Upon receipt from the sensor vendor the IV measurements of the FE-I4 sensors of a few wafers are repeated to test the reliability of the sensor vendors data. The following

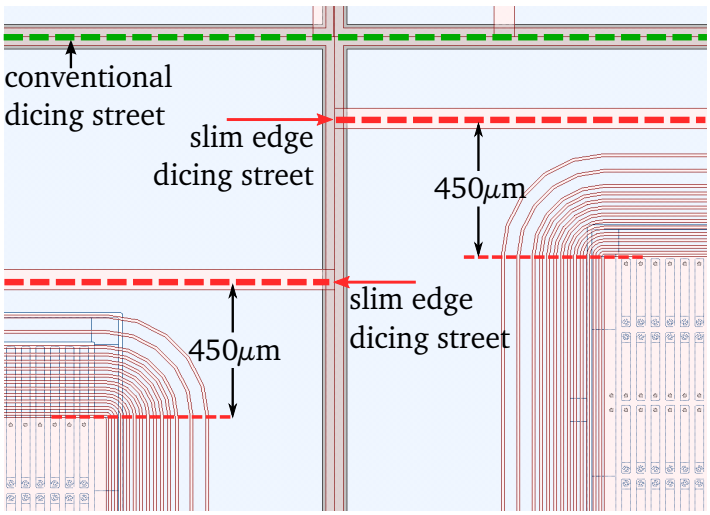


Figure 5.12.: Corner region between the FE-I4 sensors 02 and 05 on the wafer. The conventional dicing street in green which runs across the whole wafer is too far away from the active pixel matrix. Additional dicing steps have to be made at the slim edge dicing streets (red dashed lines) to stay within the required 450 μm distance. The p^+-implantation in red, n^+-implantation in blue.

IV measurements are done directly at the bump bond vendor IZM between the several steps of post-processing, i.e. after the UBM-process on wafer level, after the dicing at the dicing street and after the slim edge dicing step.

5.4.1. CV Measurements

The voltage dependent measurement of the sensor bulk capacity (CV) is a standard method to obtain the depletion voltage. Therefore, the setup for the IV measurement (see Figure 5.1) has to be slightly changed as seen in Figure 5.13.

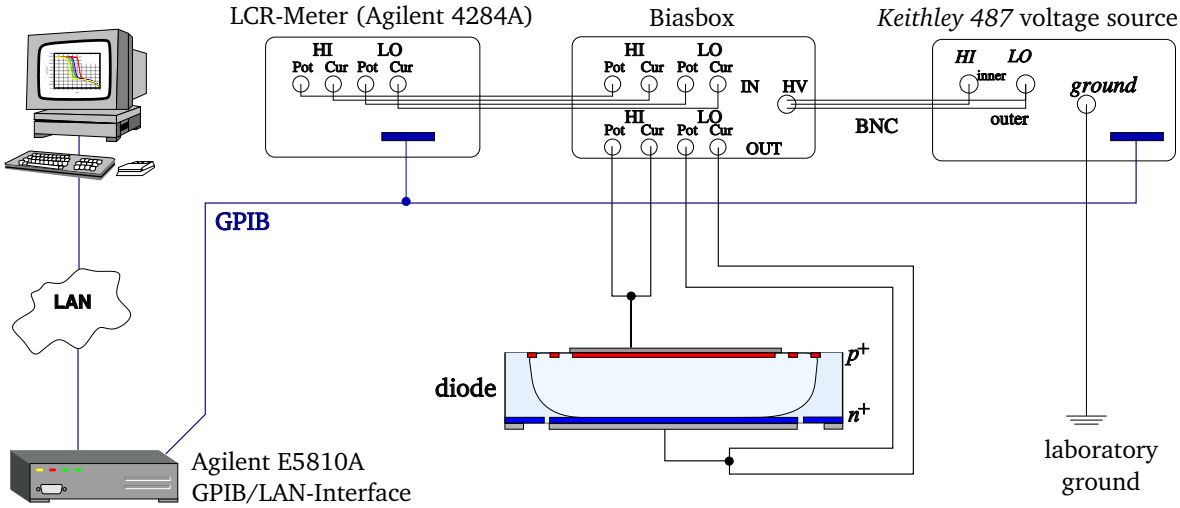


Figure 5.13.: Schematic of the setup for CV measurements. The high voltage is overlayed in a so called bias box with a high-frequency low voltage from an LCR-meter. A frequency of 10 kHz and an oscillation voltage of 50 mV are used. The LCR-meter measures the capacity between the n- and p-side of the diode which are contacted by probe needles. Original taken from [Raj03] and modified.

The high voltage supplied by a *Keithley 487* device is overlayed in a so called bias box with a high-frequency low voltage from an *HP Agilent 4284A* LCR-meter [Raj03].

Latter measures the capacity in the cpd-mode, i.e. the complex impedance is modelled as parallel circuit of capacity and conductance (see [Kli13]). A frequency of 10 kHz and an oscillation voltage of 50 mV are used. In this setup the diode should be contacted with probe needles from both sides, i.e. the oscillating high voltage on the p-side and the ground on the n-side.

If the inverse squared capacitance is plotted against the voltage, the depletion voltage can be easily read at the intersection of two fitted straight lines. One exemplary plot can be seen in Figure 5.14.

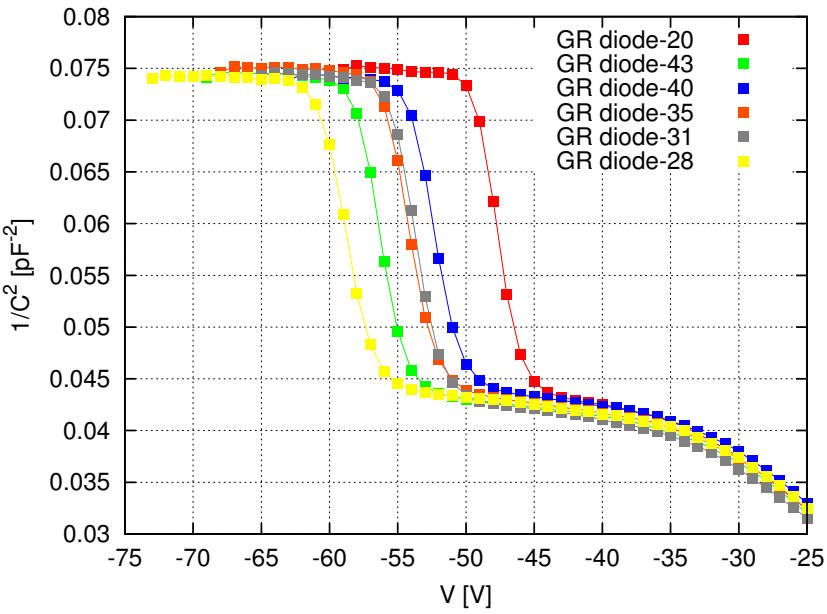


Figure 5.14.: Exemplary CV measurements of six diodes of one 250 μm thick wafer of the prototype production. The diodes are spread over the whole wafers edge, i.e. one should be able to comprise all deviations of the depletion voltage. In this case the depletion voltages range from -50 to -62 V.

One line is fitted to the steep slope, the other one to the subsequent plateau. The Figure 5.14 shows measurements of six diodes of one 250 μm thick wafer. Their numbers correspond to those seen in Figure 5.11. They are spread over the whole wafer edge, i.e. one should be able to comprise all deviations of the depletion voltage. In this case the depletion voltages range from -50 to -62 V. These differences could be explained by small inhomogeneities in the bulk resistivity. It is not possible to find a correlation between the value of the depletion voltage and the position on the wafer.

Figure 5.15 shows examplarily the results of respectively several diodes of two 250 μm and one 175 μm thick wafers. One colour always represents one wafer, one symbol stands for one diode number. It can be seen that the deviations of the depletion voltages do not only occur between diodes of one wafer but also between different wafers of the same thickness. This result is also understandable as wafer resistivities are not necessarily constant. The lower depletion voltages for sensors with thinner bulks like for 175 μm in Figure 5.15 are expected according to Equation (3.1).

The deviations of the depletion voltage have to be taken into account when defining a reasonable operation voltage. In order to guarantee a fully depleted sensor, it has to add a safety margin to the depletion voltage. For the former ATLAS pixel production the operation voltage was chosen to $V_{\text{depl}} + 50$ V but at least 150 V [ATL03]. This value has to be adapted as the current edge design has changed significantly. Because the distance from the high voltage pad to the dicing street was reduced from 1100 to 450 μm and three guard rings were omitted, a reduction of the breakdown voltage is supposable as shown in Section 5.1.1. Keeping the former quality criteria could

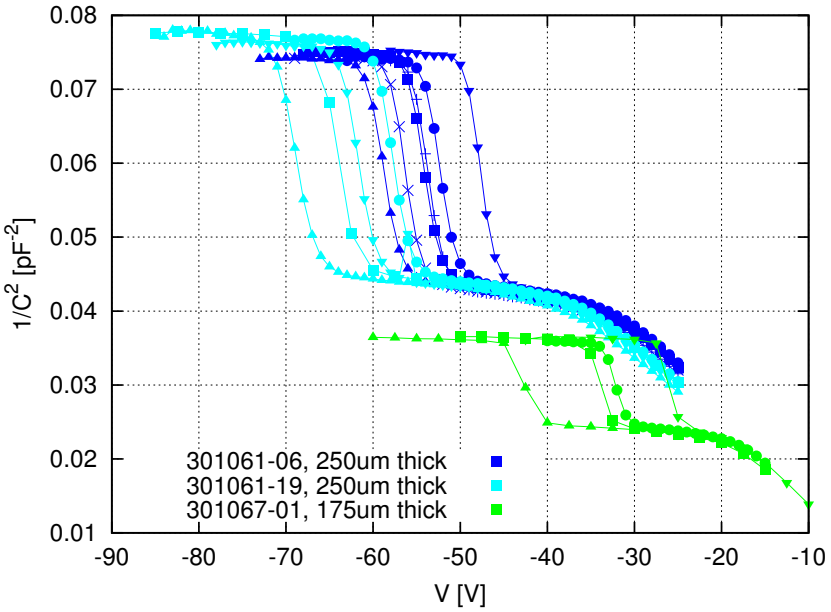


Figure 5.15.: Exemplary CV measurements of several diodes of two 250 μm and one 175 μm thick wafers. One colour always represents one wafer, one symbol stands for one diode number. The deviations of the depletion voltages do not only occur between diodes of one wafer but also between different wafers of the same thickness.

unnecessarily deteriorate the sensor yield by excluding too much sensors which could be operated fully depleted. As the largest fluctuations of the depletion voltages of diodes of the same bulk thickness did not extend 20 V the operation voltage was decided to be $V_{\text{depl}} + 30\,\text{V}$. This results in operation voltages of 100 V for 250 μm, 75 V for 200 μm and 50 V for 150 μm bulk thickness.

Unfortunately, the data of the CV measurements done at the sensor vendor to obtain the V_{depl}-values are not available for the analysis. The mentioned assumed depletion voltages are based on a few measurements of randomly chosen wafers.

5.4.2. IV Measurements

With a determined depletion and a defined operation voltage it is possible to give a statement if the sensor is operable after conducting an IV measurement. The maximum allowed leakage current at operation voltage, the so called operation current I_{op}, is set to 2 μA. This is the same value as for the ATLAS pixel production [ATL03] as the size of the active area of the former tiles are in the same order as for the IBL sensors.

To give a clear overview of the development of IV measurements, migration plots are used in the following. In these plots the operation current at one certain step is plotted against the operation current at a different step. Currents which do not change are represented by points on the marked diagonal line, increasing currents by those in the lower right area, decreasing currents by those in the upper left area. Larger values than 2 μA are projected to 2 μA. Double chip sensors are represented by squared symbols, single chip sensors by triangular ones; sensors with the conservative design by blue symbols, sensors with the slim edge design by red ones.

During the IV measurements at IZM no dedicated temperature logging was done. However IZM delivered temperature recordings of the clean room environment which show that the temperature fluctuates about 1 to 2 °C around 20 °C. According to Equation (3.2) a deviation of 2 °C from the reference temperature of 20 °C can already result in a current change of 20%. To give an impression of the error tolerance which has to take into account, there are two additional dashed lines which mark these 20% deviation.

250 µm bulk thickness

The post process quality inspection is firstly done for the 250 μm thick wafers as it is the thickness already used for the sensors of the past ATLAS pixel production, i.e. these are the most comparable sensors. In order to exclude any cause of defect, a total number of 36 sensors have been IV measured after the UBM process on wafer. This step should not cause any deterioration as no severe mechanical stress is induced to the wafers. Figure 5.16 shows the operation current migration plot of the stage after UBM compared to that before UBM.

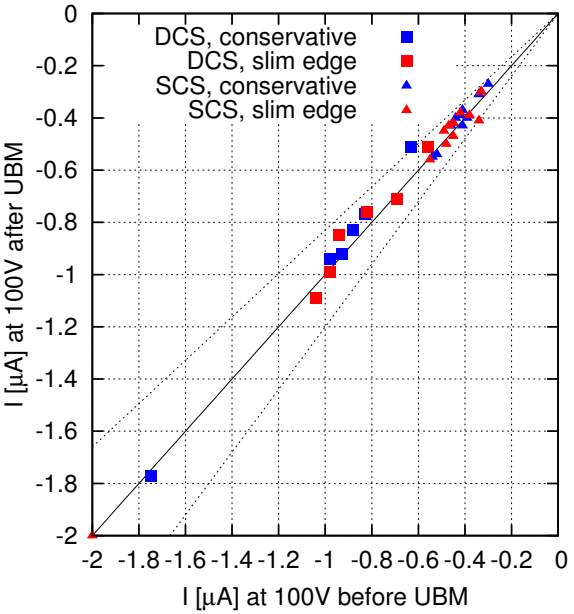


Figure 5.16.: Operation current migration plot comparing the stages before UBM measured at the sensor vendor and after UBM measured at the bump bond vendor. 36 FE-I4 sensors with a thickness of 250 μm have been tested.

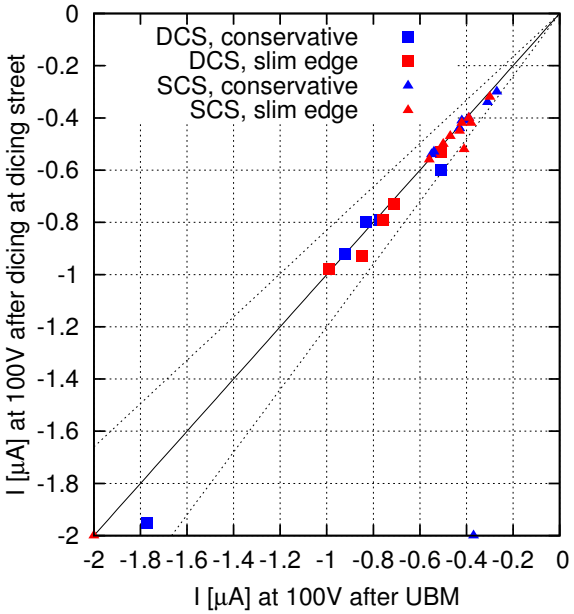


Figure 5.17.: Operation current migration plot comparing the stages after UBM and after dicing at the dicing street, both measured at the bump bond vendor. 30 FE-I4 sensors with a thickness of 250 μm have been tested.

It can be seen that all points are lying close to the diagonal line. This means that no deteriorations take place during the UBM process as it was expected. A general trend of a higher leakage current for the double chip sensors in comparison to the single chip sensors is visible. This is as well expected due to their larger area.

Figure 5.17 shows the migration plot of the stage after dicing at the dicing street compared to that after UBM. 30 sensors have been measured at these two stages. In this case there are again no systematic deviations from the diagonal line visible. This indicates that the dicing step itself works in principle. Any deteriorations would refer to mechanical damages to the bulk and would not correspond to the changed guard ring design because the remaining safety margin after this step is still large enough to ensure a controlled potential drop. This is supported by the fact that there are no different trends visible between double and single chip sensors. After this dicing step they have a different sized remaining dead space (compare Figure 5.12). If the safety margin has a distance which is critical for the breakdown behaviour, one should be

able to see a slightly worse behaviour for the single chip sensors as their distance is smaller than that of the double chip sensors.

Figure 5.18 shows the migration plot of the stage after slim edge dicing compared to that after dicing at the dicing street. The plot contains the measurements of 36 sensors. This is the most critical step as the distance from the high voltage pad to the

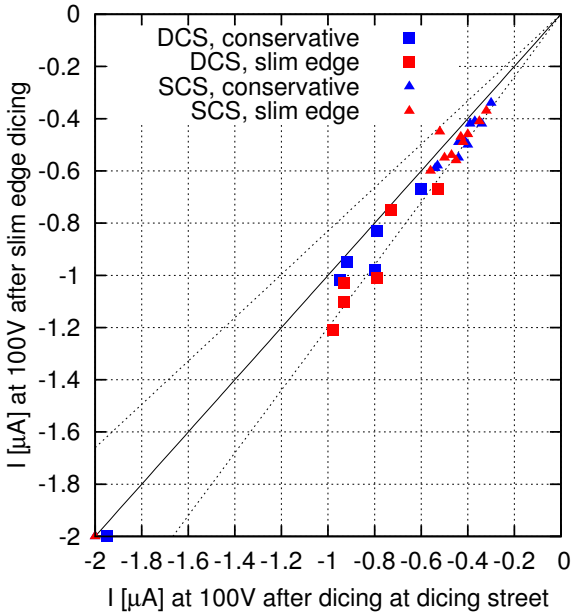


Figure 5.18.: Operation current migration plot comparing the stages after dicing at the dicing street and after slim edge dicing, both measured at the bump bond vendor. 36 FE-I4 sensors with a thickness of 250 μm have been tested.

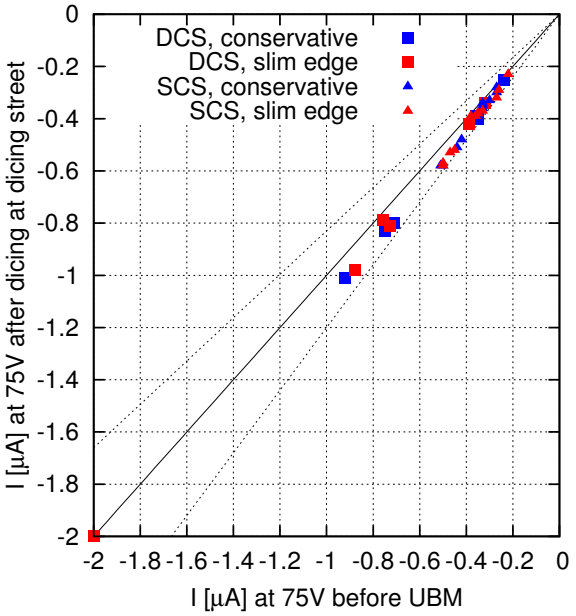


Figure 5.19.: Operation current migration plot comparing the stages before UBM measured at the sensor vendor and after dicing at the dicing street measured at the bump bond vendor. 35 FE-I4 sensors with a thickness of 200 μm have been tested.

cutting edge is reduced to the minimum value of 450 μm. If the reduced safety margin has any influence on the breakdown behaviour, it should become apparent after this dicing step. In the plot a slight trend to an increase of the leakage current is visible. It seems that all points have a systematic offset from the diagonal line. This can be an indication for different sensor temperatures in this two measurement periods. The larger fraction of all points is lying within the 20% tolerance region, the other points are still close to it.

Furthermore, it has to point to the fact that there are no systematic deviations between sensors with the conservative and the slim edge design visible. This is understandable because in both designs the p-side where the potential drop takes place is exactly the same. Hence a similar breakdown behaviour is expected.

200 µm bulk thickness

For the 200 μm thick sensors the stage after the UBM step was skipped because no deteriorations were observed for the 250 μm thick sensors. A different behaviour is not expected as the thickness should have no influence to the UBM process which is a process applied to the wafer surface. The operation current migration plot between the

stage before UBM and that after dicing at the dicing street can be seen in Figure 5.19. A total number of 35 sensors have been measured at these two stages.

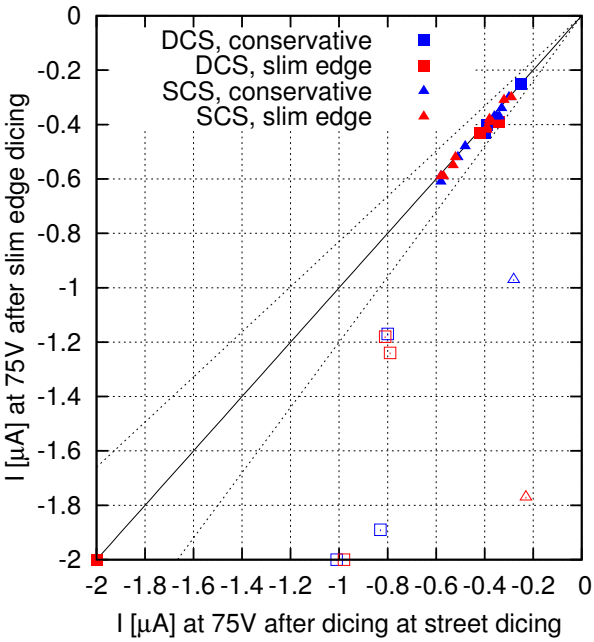


Figure 5.20.: Operation current migration plot comparing the stages after dicing at the dicing street and after slim edge dicing, both measured at the bump bond vendor. 35 FE-I4 sensors with a thickness of 200 μm have been tested. The first eight sensors which are represented by open symbols have been glued on the p-side during the dicing step. They show a significantly reduced breakdown voltage after the slim edge dicing step. The remaining sensors, represented by the filled symbols, have been glued to the n-side during the dicing step. For these ones, no deteriorations are visible anymore.

As seen for the 250 μm thick sensors this plot shows no significant deteriorations after the dicing step at the dicing street. All points are lying within the 20% tolerance region. This behaviour however changes after the slim edge dicing step (Figure 5.20). The first eight sensors which were measured show a significantly reduced breakdown voltage. They are represented by open symbols. Although the current stays below the limit of 2 μA for 6 of these 8 sensors they would already be operated in a breakdown region and thus should fail the quality assurance.

An alteration of dicing parameters such as a reduction of the cutting speed (so called feed rate) of the dicing blade did not improve the performance. Therefore, the cutting edges of the sensors were checked visually. Figure 5.21 shows exemplary light microscope pictures of the n- and p-side of the cutting edge of one sensor. It was glued with the p-side down to the tape during the dicing step. It can be seen that the bottom side shows more severe damages at the cutting edges as the top side. This observation is in line with previous experiences of IZM.

This macroscopic effect is an explanation for the bad behaviour of the sensor after this slim edge dicing step. Because the potential drop takes place on the p-side, latter is the more sensitive side of the sensor. The observed large defects in the p-side bulk supposably deteriorate the breakdown behaviour. Whereas for the 250 μm thick sensors this is obviously not the case (as seen in Figure 5.18), the sensors with thinner bulks cannot be operated after this step.

To counteract this deterioration, the remaining sensors are flipped before the dicing, i.e. the n-side is glued down to the tape. In this case the quality of the p-side is not degraded by the dicing step as severely as before. Therefore, the deterioration of the n-side should not affect the breakdown behaviour because the complete area is anyhow on ground potential. The outer guard as well as the bias grid ring which surround the active area are implantations and thus conducting. If a larger defect occurs in the outer guard, this does not matter. The filled symbols in Figure 5.20 represent these sensors glued to the n-side during the dicing. The improvement in comparison to those

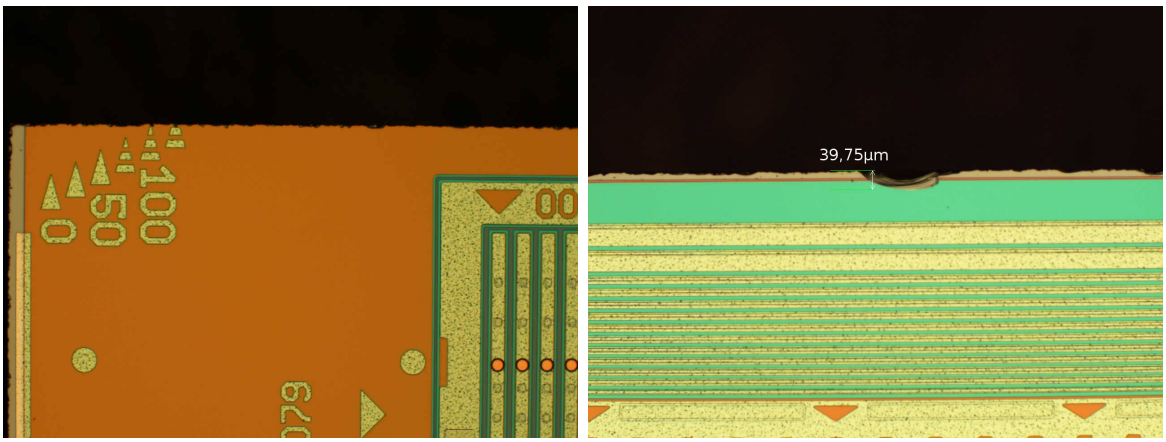


Figure 5.21.: Light microscope pictures of the sensors cutting edge after the slim edge dicing step. Top view on the n-side (left) and on the p-side (right). The sensor was glued on the p-side during the dicing step. Significant differences of the quality of the cutting edge are visible between the two sides. [IZM11]

sensors glued to the p-side is obvious. All points are located on the diagonal line or close to it, i.e. no decreases of the breakdown voltage are visible.

There are some reasons why IZM initially used to glue the sensors on the p-side. The main point is that the chipping, a result of crack propagation during the saw, occurs much more often and increased on the bottom side than on the top side. After expanding the dicing tape and releasing the dices from it, these shivers can stick out of the surface. If they are located on the pixel side, they can represent a threat to the read-out chip during and after the flip chip process. Because the UBM pillars cause an unevenness on the sensors surface the adhesive force between the sensor and the tape is reduced in comparison to a flat surface. This can provoke that the sensor is moved during the dicing step due to the strong mechanical stress. This can in turn lead to larger damages on the bottom cutting edge [Fri12].

As mentioned before, damages on the pixel side cutting edge do not affect the breakdown behaviour. A visual inspection of several sensors which have been glued on the n-side during the dicing showed that larger chippings did not occur. Furthermore, a slightly increased probability of chipping can be accepted in consideration of a non-functional sensor which was glued on the p-side. Hence it is a good compromise to glue all remaining 200 μm sensors on the n-side as well as further thinner sensors.

150 µm bulk thickness

Due to their fragility the 150 μm thick sensors have to be glued on a handling wafer during the UBM process. The handling wafer is again removed afterwards. This is a standard procedure to avoid too many wafer losses. The only disadvantage is a considerable increase of working time. As the usage of the handling wafer should not affect the quality of the wafer, a control measurement afterwards is again not necessary. Furthermore, the stage after the dicing at the dicing street was additionally skipped because the possible deteriorations between the two dicing steps have been investigated for the 200 μm thick sensors. They are as well glued on the n-side during the dicing step as no different behaviour is expected. The operation current migration plot of

the stage before UBM and that after the slim edge dicing step street can be seen in Figure 5.22. A total number of 36 sensors have been measured at these two stages.

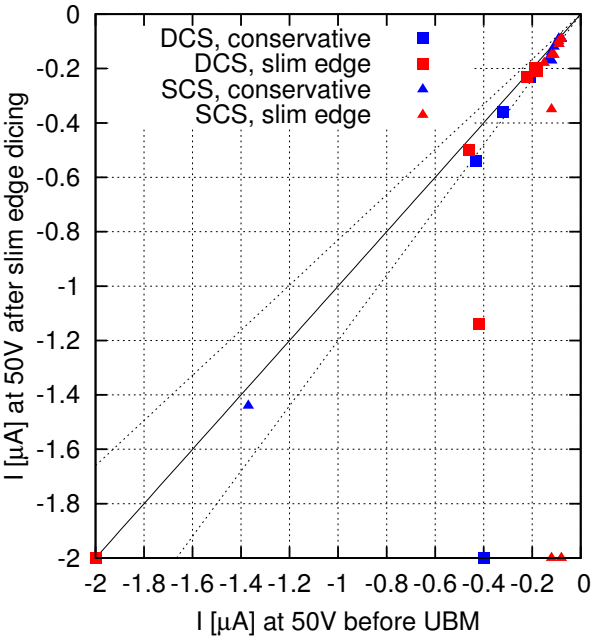


Figure 5.22.: Operation current migration plot comparing the stages before UBM measured at the sensor vendor and after slim edge dicing measured at the bump bond vendor. 36 FE-I4 sensors with a thickness of 150 μm have been tested.

It can be seen that most of the points are lying close to the diagonal line, i.e. show no deterioration of the breakdown behaviour. However 4-5 points show a significant deviation which indicates a reduced breakdown voltage. One can assume that sensors of this thickness are more susceptible for the dicing step than the thicker ones.

5.4.3. Discussion of Different Sensor Bulk Thicknesses

In order to find the appropriate sensor thickness for the IBL, several aspects have to take into account. As mentioned before in Section 5.3.3 a thinner irradiated sensor will collect more charge than a thicker one. This means a smaller thickness should in principle be favoured. On the other hand, there are several steps during the process chain which expose the wafers to mechanical stress. These steps include the wafer thinning, the wafer processing, the UBM process and the dicing. Besides the actual process steps the handling in between is a further critical step, especially if this is done automatically. From that point of view it makes sense to keep a larger thickness in order to maintain a sufficient overall process yield. Thus, a reasonable compromise has to be found.

The yield of the wafer processing at the sensor vendor showed a clear dependency of the thickness. According to the received statement [CiS12], 97 % of the 250 μm thick wafers survived the procedure. The wafers with the intermediate thicknesses of 225, 200 and 175 μm can be subsumed. Their average yield adds up to 89 % and is thus only slightly decreased compared to the standard thickness. A significant quality fall-off occurs for the 150 μm thick wafers where the yield is 44 %. This drastic yield decrease is mainly caused by the loss due to the automatic wafer handling steps but also due to the manual handling. One has to take into account that the wafers were not thinned immediately to the final foreseen thickness. There was an additional, subsequent thinning step which was done after the rounding off of the wafer edges. Thus, the edges are not absolutely

round anymore. This can result in increased stress in the wafer bulk whereby the risk of a breakage during the handling is getting higher.

As mentioned before there are handling wafers used for the UBM process at IZM in order to avoid too many wafer losses. The smallest thickness at which the wafer can be processed without a handling wafer is 200 μm. The process of the thinner wafers is thus significantly more laborious.

Figure 5.23 shows a summary of the operation current migration plot of all three investigated wafer thicknesses. To give an overview of the whole post process, the stage before UBM is compared to that after the slim edge dicing. It has to point

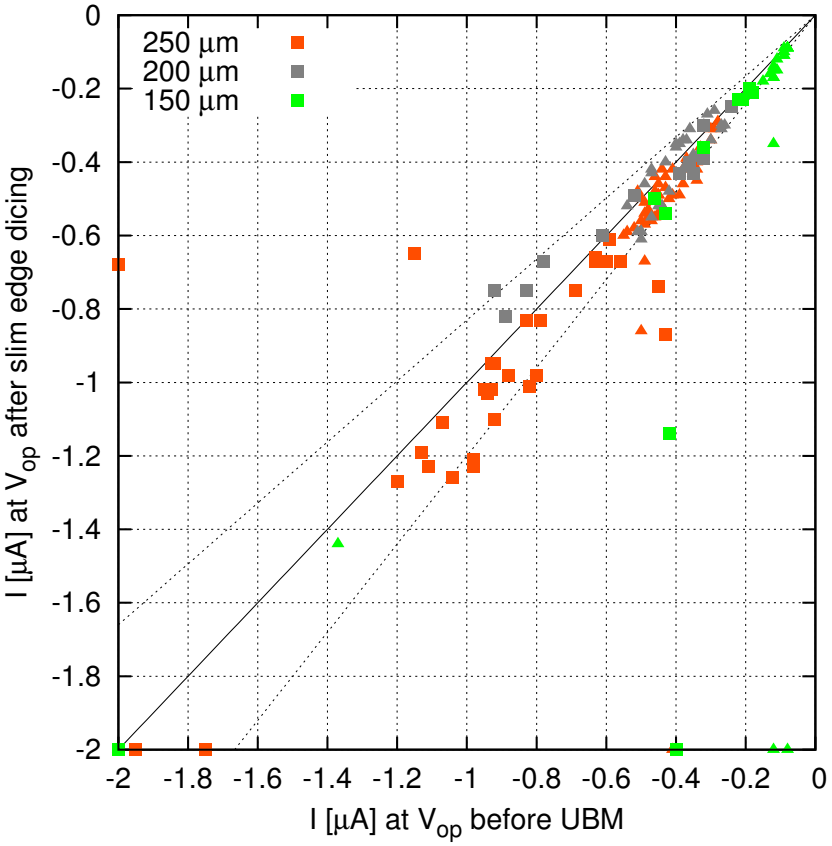


Figure 5.23.: Operation current migration plot comparing the stages before UBM measured at the sensor vendor and after slim edge dicing measured at the bump bond vendor. FE-I4 sensors with all investigated thickness of 250, 200 and 150 μm are displayed. It has to take into account that the different thicknesses involve lower operation voltages. The thicker sensors thus feature by trend a higher operation current.

out that the wafers have different operation voltages with respect to their thickness. This explains why the thicker sensors have by trend a higher leakage current. For the 250 μm thick sensors there are some deviations from the 20% tolerance region around the diagonal. Some sensors have an increased current while two even improve significantly. On the contrary the 200 μm thick sensors appear to be more stable. One explanation for that is the lower operation voltage of 75 V in comparison to 100 V. It involves the advantage that a starting breakdown is less likely for a small operation voltage than for a higher one, taking into account that the edge design is the same. Despite an even lower operation voltage of 50 V the most significantly deteriorations occur for the 150 μm thick sensors. This observation confirms the assumption that the sensors of this thickness are more susceptible for the dicing step than the thicker ones.

On the basis of the listed arguments it was decided on an IBL planar sensor thickness of 200 μm. The advantage of a supposable increased charge collection after irradiation counterbalances the possibility of a slightly increased loss of wafers during the processing steps. A further advantage of the 200 μm thickness is an improved edge efficiency performance compared to 250 μm thick sensors. It is discussed in the next Section 5.5.

5.5. Test Beam Results

Parts of Section 5.5.2 have been published in [Wit12].

5.5.1. Test Beam Operation

To study in how far the edge efficiency decreases for the slim edge sensor design, unirradiated and irradiated sensors have been operated in test beam facilities at CERN and DESY. At DESY the maximum energy of the electrons which are used for the test beam operation is 6 GeV [DESY]. The North Hall test beam area at CERN is operated with high energy pions which are produced at fixed target collisions of protons from the SPS. The pions can reach energies in the order of 100 to 200 GeV [SBA].

A detailed description of the test beam set-up, the reconstruction and analysis frameworks can be found e.g. in [Wei12]. More details concerning the IBL test beam campaign and IBL prototype module studies can be found in [IBL12]. A detailed description of the used test beam mechanics can be found in [Tro12].

The test beam set-up consists of the EUDET telescope [EUDET], the devices under test (DUT) and the data acquisition system USBPix (see [USBPix]). The DUTs are sensors which have been bump bonded to FE-I3 or FE-I4A read-out chips to form assemblies. These are glued and wire bonded to adapter cards for read-out (see Section 3.4.3, Figure 3.9). The particle tracks seen by the telescope planes can be interpolated and projected on to the DUTs and assigned to one pixel. The following analyses are using the TBmon software framework. It consists of several modular analyses which can be executed separately. The most important one is the efficiency analysis which determines a space-resolved hit efficiency by comparing the reconstructed track with the pixel response. If a reconstructed track is seen by one DUT pixel in the proximity of one and a half pixel pitches referring to the projected incidence, it is counted as a hit. A track is valid for one regarded DUT if the track causes a hit in at least one other DUT. It is then filled into a track map of the regarded DUT. If the regarded DUT also sees a hit, this hit is filled into the hit map of the DUT. The efficiency map is a simple division of the hit map by the track map. Because the spatial resolution of the telescope is better than 10 μm, it is possible to obtain a sensor hit efficiency map in subpixel resolution [Bul10].

Each hit contains the ToT information from individual pixels. Taking into account the ToT-charge calibration which is done during the assembly tuning, the ToT value can be converted into the collected charge. Analogous to the hit efficiency the analysis software is able to output a charge map showing which pixels or pixel regions are collecting which amount of charge. This represents an important additional information as the hit efficiency only reveals whether the collected charge is above or below the threshold.

For the investigation of the sensors edge area the edge efficiency analysis of TBmon is used in the coming sections. This analysis basically works as the described efficiency analysis. It focuses on the first and last sensor columns. The particular length of the edge pixel has to take into account. For the special design of the pixel shifted stepwise FE-I3 sensor (see Section 5.5.3, Figure 5.27) the analysis had to be slightly adapted.

For a subpixel resolved efficiency map all similar pixels are superimposed in order to increase the statistic. For the edge efficiency this is only possible with those pixels of

the first and last column. Thus, it is necessary to collect significantly more data than for the central sensor efficiency in order to achieve reasonable statistics.

The conventional mounting features the DUTs standing perpendicular to the beam. In order to simulate an operation as in the ATLAS pixel detector, the circuit boards including the sensor chip assemblies can be tilted in ϕ- or η-direction. The ϕ-rotation is round the long pixel side, i.e. round one pixel row. In the detector it corresponds to a tilt of the staves around the beam pipe. The tracks which are coming from the interaction point have different inclinations depending of where the sensor on the stave is hit. For the IBL the ϕ-inclination varies from 0° to 30°. Therefore, a mean ϕ-inclination of 15° can be used. The η-angle dependency is not investigated in this thesis. Studies of this topic can be found e.g. in [Rum13].

Table 5.3 shows an overview of all investigated sensor assemblies which have been successfully operated in different test beam periods.

Table 5.3.: Overview of investigated sensor assemblies which have been operated during test beam periods. The 'pss' stands for pixel shifted stepwise, the 'se' for slim edge.

sensor assembly	chip type	sensor thickness	sensor design	irradiation fluence $[10^{15}\mathrm{n_{eq}/cm^2}]$	test beam period
DO 3	FE-I3	285 μm	pss	0	PPS, CERN, Jul 2010
DO 43	FE-I3	200 μm	pss	0	PPS, CERN, Aug 2012
DO 46	FE-I3	150 μm	pss	0	PPS, CERN, Aug 2012
DO 47	FE-I3	150 μm	pss	5	PPS, CERN, Aug 2012
SCC 14	FE-I4	250 μm	IBL se	0	IBL, DESY, Feb 2011
SCC 17	FE-I4	250 μm	IBL se	0	IBL, DESY, Feb 2011
SCC 92	FE-I4	200 μm	IBL se	0	PPS, CERN, Jul 2011
LUB 2	FE-I4	250 μm	IBL se	4	IBL, CERN, Jun 2011

5.5.2. FE-I4 Based Assemblies

Results of Unirradiated Assemblies

In Figure 5.24 the hit efficiency of two 250 μm thick and one 200 μm thick sensors with the IBL slim edge design can be seen. SCC 14 was operated at a bias voltage of 90 V, SCC 17 at 150 V, both are tuned to a threshold of 3200 electrons. The thinner SCC 92 was operated at 60 V with a lower threshold of 1600 electrons. The coloured 2D plots show an overlay map of all edge pixels. One central edge pixel runs from 0 to 500 μm along the horizontal axis. It is surrounded by fractions of the neighbouring pixels. The pixel cell contours are marked in black. The end of the high voltage pad is located at 250 μm, the guard rings are affiliated on its right side. Both structures are indicated in grey.

Due to the uniform efficiency distribution along the short pixel side, a projection to the x-axis (Figure 5.24, bottom) can be used to visualize the hit efficiency drop opposite

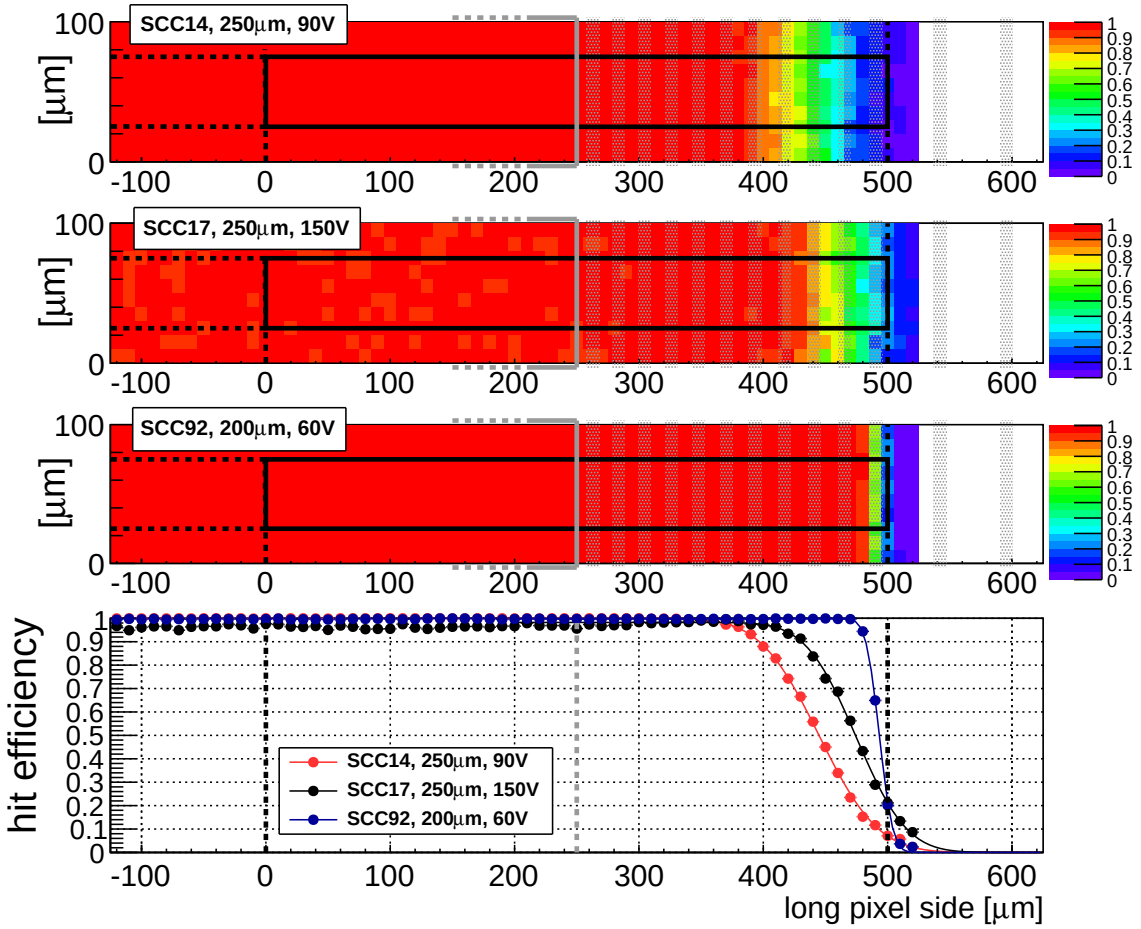


Figure 5.24.: Hit efficiency maps of the edge of three unirradiated FE-I4 assemblies with the IBL slim edge design. SCC 14 was operated at 90 V, SCC 17 at 150 V bias voltage, both sensors are 250 μm thick, the threshold is set to 3200 electrons. The 200 μm thick sensor SCC 92 was operated at 60 V, the threshold is set to 1600 electrons. The coloured 2D plots show an overlay of all edge pixels whereby red stands for an efficiency close to 1 and violet for an efficiency close to 0. The pixel cell contours are marked in black, the high voltage pad which is located at $x = 250\,\mu$m and the guard rings are indicated in grey. The plot at the bottom is a projection of the hit efficiency to the x-axis in which the S-curve like drop opposite to the guard rings becomes visible.

to the guard rings. The distributions can be fitted with a parameterised Gauss error function

$$f(x) = 0.5 \cdot P \cdot \left(1 + \mathrm{Erf}\left(\frac{x_0 - x}{\sqrt{2}\,\sigma}\right)\right) \tag{5.2}$$

with a plateau P in the inner part of the pixel and a drop to 0 at the sensor edge. The inflexion point x_0 marks the position where the efficiency drops to 50% of the plateau. The curve is symmetric with respect to this point. Thus, the efficiency decrease on the left of the point is compensated by the remaining efficiency on the right of it. For this reason this value is used as a benchmark. It can be regarded as the effective end of the pixel which yields to an effective pixel length. The σ is a degree for the steepness of the efficiency decrease, a small σ stands for a steep drop.

It can be seen that for all assemblies the plateau attains an efficiency of 1 or slightly below. This value is expected for the central region of unirradiated sensors. At the edge region the efficiencies decrease smoothly and continuously S-curve like to 0. The fit curves interpolate the edge efficiency drop very well. Within the uncertainties all points are lying on the curves.

As a default error tolerance for the determined effective pixel lengths the half bin size of 5 μm is used. In comparison the errors of the fit functions are in the order of less than a micrometer and can thus be neglected. This is as well in the order of the resolution of the telescope.

The effective pixel lengths are ascertained to be $(445 \pm 5)\,\mu$m for SCC 14 at 90 V and $(475 \pm 5)\,\mu$m for SCC 17 at 150 V. For the same bulk thickness the edge efficiency is rising with higher voltages. This behaviour is expected as after reaching the pixel side, the depletion zone should further extend laterally into the edge region. The more the depletion zone moves outwards, the more tracks are seen from the edge pixels.

The effective pixel length of SCC 92 is ascertained to be $(493 \pm 5)\,\mu$m. This means that almost the complete pixel is active although half of it protrudes the high voltage pad. This result is remarkable as the operation voltage of 60 V is extremely low. It is even lower than the designated operation voltage of 80 V for 200 μm thick sensors (compare Section 5.4.1 and Section 6.3.4). The effective pixel length is even significantly increased in comparison to SCC 17 which was operated at a higher voltage. One explanation for this improvement could be the reduced bulk thickness of SCC 92. The depletion zone expands from the high voltage pad implantation on the p-side with increasing bias voltage into the bulk. The voltage at which the depletion zone reaches the pixel implantation opposite to the high voltage pad is smaller for a sensor with a thinner bulk (compare Equation (3.1)). It could be possible that as soon as the pixel side is reached, the lateral component of the depletion zone expansion is increased compared to that case of a thicker bulk where the pixel side is not reached. However, a definite conclusion about the bulk thickness dependency cannot be made as another difference between the assemblies is the significantly lower threshold of SCC 92. This entails that considerable less collected charge is required to detect a particle track. Especially in the edge region which is characterized by an inhomogeneous field configuration and a merely partly depleted area, this different threshold could be decisive for the track detection. A further discussion can be found in Section 5.5.4.

The determined effective pixel length can be used to calculate the effective inactive edge width of the sensor. Due to the additional uncertainty of the cutting position, a more conservative error tolerance of 10 μm is reasonable. The distance from the cutting edge to the geometrical end of the pixel cell is $(200 \pm 10)\,\mu$m. For the SCC 92 sensor with an effective pixel length of $(493 \pm 5)\,\mu$m this results in an inactive edge width of $(207 \pm 10)\,\mu$m. The 250 μm thick sensors yield in values of $(255 \pm 10)\,\mu$m at 90 V and $(225 \pm 10)\,\mu$m at 150 V.

It can be seen that already for unirradiated sensors, a significant reduction of the inactive edge width is achieved for the slim edge design. In the conservative design the complete specified 450 μm between high voltage pad and cutting edge would stay inactive. By extending the pixel length by 250 μm in the slim edge design, a reduction of the inactive edge to the order of 200 μm is achieved which is significantly lower than the specified value of 450 μm given by the IBL constraints. The worse edge efficiency performance of the 250 μm thick sensors could constitute a further argument

for the usage of a bulk thickness of 200 μm for the IBL sensors. The lower threshold which is feasible with the FE-I4 read-out chip represents an important factor for the improvement of the edge efficiency.

Results of Irradiated Assemblies

An irradiated IBL prototype sensor assembly which has successfully been operated in a test beam setup is LUB 2. It is a 250 μm thick sensor with the IBL slim edge design which was irradiated at the TRIGA Mark II Reactor at JSI, Ljubljana [Lju] to about $4 \cdot 10^{15} \mathrm{n_{eq}/cm^2}$. It was operated at 400, 600, 800 and 1000 V with a threshold set to 1600 electrons. It was mounted to a ϕ-inclination of 15°. Figure 5.25 shows the 2D hit efficiency plots for the four voltages as well as a projection to the long pixel side analogous to the presented plots for the unirradiated sensors.

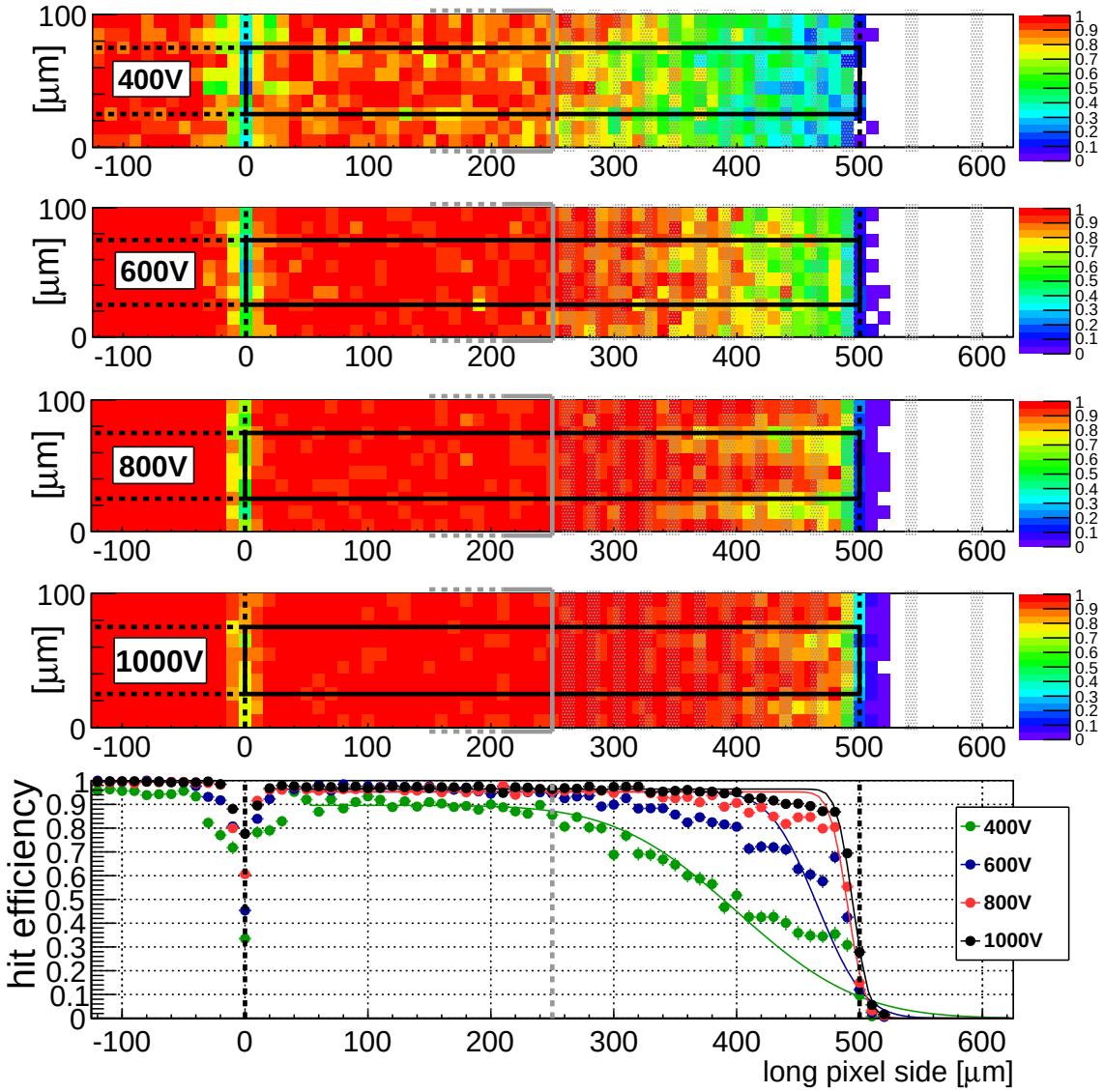


Figure 5.25.: Hit efficiency maps of the edge of the FE-I4 assembly LUB 2 with the IBL slim edge design irradiated to $4 \cdot 10^{15} \mathrm{n_{eq}/cm^2}$, operated at four bias voltages. It was tuned to a threshold of 1600 electrons. The plots are analogous to those in Figure 5.24.

The projection of the hit efficiency is again fitted with an error function in order to obtain an effective edge pixel length. It is noticeable that the measuring points do not follow perfectly an S-curve as they do for the unirradiated sensors (see Figure 5.24). Especially for 400 and 600 V larger deviations occur. The edge efficiency characteristics can rather be approximated by sequences of three linear sections. Opposite to the high voltage pad it stays on a constant plateau. Opposite to the guard rings it decreases linearly. With lower voltages the slope of the drop increases. As well does the level decrease which is reached close to the end of the pixel before the efficiency drops steeply to zero. For 800 and 1000 V the level before the steep drop is around $80 - 90\%$. The S-curve fits are matching in a better way. For 600 V the level before the steep drop is around 50%, for 400 V still at 30% efficiency.

Due to the observed deviations between the data points and the fit curve, an alternative method is used to determine the effective end of the pixel. Figure 5.26 shows a sketch to illustrate the practice for a simple example with a linear efficiency decrease. Firstly,

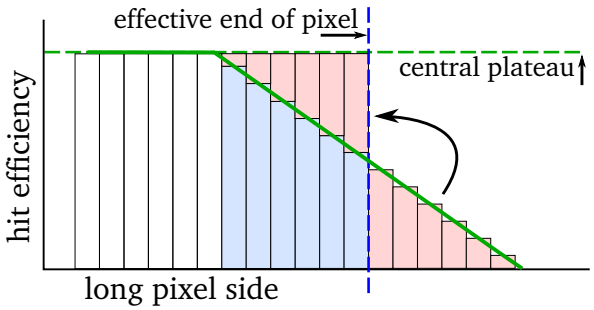


Figure 5.26.: Sketch to illustrate the identification of the effective end of the pixel by summing-up the bin entries. In the region where the efficiency (in green) drops below the central plateau, the blue bins are filled up with the entries of the outermost red bins. The blue dashed line indicates the resulting end of the pixel position.

the hit efficiency is fitted linearly in the central part of the pixel to obtain the plateau, indicated by the green dashed line. In the region where the efficiency drops below the central plateau, the corresponding blue bins are filled up to the plateau level with the entries of the outermost red bins. The last blue bin which is filled up, indicated by the dashed blue line, marks the resulting end of the pixel. It is equal to that position where efficiency drops to 50% of the plateau value. This procedure of shifting the bin contents is valid because it does not make any difference where the bin content is located or in which way it is distributed. In the analyses this method can be implemented by summing-up all bin entries of the pixel, divide it by the value of the plateau and multiply it by the bin width. The result is the effective pixel length. For an S-curve like drop as seen so far in Figure 5.24, the outcome should be the same as the error function is also symmetric with respect to the inflexion point. In comparison to the S-curve fit, the method of summing-up the bin entries features the advantage that it yields to meaningful results apart from the characteristic of how the efficiency decrease is formed.

For the present data, the two different methods to determine the effective pixel length yield to extremely identical values. The deviations for all four plots is not above $8\,\mu$m and thus smaller than the bin size. This is astonishing in view of the larger deviations of the fit curves from the data especially for 400 and 600 V. Anyhow the values of the method of the bin summation are used for the analysis because of the mentioned advantages.

In consideration of Figure 5.24 it becomes apparent that the configurations of the field and the depletion zone are different compared to the unirradiated case. As the depletion

zone expansion starts from the pixel side after irradiation it is guaranteed to have a depleted area directly beneath the pixels. These can collect charge even though the sensor bulk is not fully depleted. The operation voltage of 400 V is however too small to ensure a sufficient amount of collected charge to exceed the threshold. This is due to the fact that on the one hand the depleted volume itself is too small to generate enough charge carriers. On the other hand the voltage dependent electric field in the bulk is too weak. With a weaker field the probability increases that the drifting electrons can be trapped by radiation induced lattice defects. Even the plateau opposite to the high voltage pad is only at 90% efficiency. In the edge region it is supposable that the depleted volume diminishes with an increasing distance to the high voltage pad. This would explain the linear efficiency drop opposite to the guard rings.

With higher voltages the hit efficiency rises in the edge region as well as in the central region. Opposite to the guard rings the slope of the efficiency loss becomes more flat. This indicates that the depletion zone as well expands to the p-side which increases the probability of a detected hit. The steep efficiency drop to zero located close to 500 μm most likely occurs due to the geometric end of the pixel. If the pixels would protrude even further into the edge area, it is supposable that the flat linear efficiency drop would proceed.

In the 2D maps of Figure 5.25 it is visible that the hit efficiency is not as homogeneous along the short pixel side as for the unirradiated sensors in Figure 5.24. Especially at 800 V right of 350 μm and at 1000 V right of 400 μm there are significantly efficiency drops at the borders of the pixels in comparison to their centres. This is a clear indication for an increased charge sharing probability. If the generated charge is split to two adjacent pixels, the two charge fractions are presumably to small to exceed the threshold and the track is not detected. This effect causes a decrease of the hit efficiency especially if the amount of generated charge is only little above the threshold in the first place. These conditions are given in the region opposite to the guard rings. In the same 2D maps it is visible that the efficiency fluctuations along the short pixel side between pixel centre and pixel border are not perfectly matching with the actual positions indicated by the black box. This shift can be explained by the 15° tilt in ϕ-direction.

The data of the irradiated assembly shows a clear improvement of the edge efficiency with rising voltages. For 800 V and especially for 1000 V the main efficiency drop occurs very close to the end of the pixel. The respective effective pixel lengths are $(490 \pm 5)\,\mu$m and $(499 \pm 5)\,\mu$m. It can be declared that for the fluence of $4 \cdot 10^{15} \mathrm{n_{eq}/cm^2}$ at a bias voltage of already 800 V the complete overlapping pixel is active. This corresponds to the minimal inactive edge width of $\sim (200 \pm 10)\,\mu$m. Referred to the length of the IBL sensor, this is equal to an inactive fraction in the order of 1%.

Unfortunately, the obtained fluence of $4 \cdot 10^{15} \mathrm{n_{eq}/cm^2}$ of this assembly is not the specified IBL fluence. Nevertheless it is not anticipated that for $5 \cdot 10^{15} \mathrm{n_{eq}/cm^2}$ a significantly different behaviour of the edge efficiency will occur. As seen, already for 800 V the efficiency shows convincing results for $4 \cdot 10^{15} \mathrm{n_{eq}/cm^2}$. A possible efficiency decrease due to slightly higher radiation damages should be compensable by raising the bias voltage.

Furthermore, the IBL sensors will feature a thickness of only 200 μm which will presumably yield to an even better edge efficiency performance. For the considered irradiation fluences it is not feasible anymore to fully deplete the complete bulk volume with a

reasonable bias voltage (see Equation (3.3)). For that reason a smaller bulk thickness should not lead to any disadvantages. It would on the contrary lead to higher field strengths at same voltages in comparison to 250 μm thick sensors. This effects a lower trapping probability and thus a higher amount of collected charge.

5.5.3. FE-I3 Based Assemblies

In addition to the FE-I4 based IBL prototype assemblies, several FE-I3 based assemblies have been operated in a test beam setup. All of them have been tuned to the standard FE-I3 threshold of 3200 electrons.

Design of the Pixel Shifted Stepwise Sensor

The pixel shifted stepwise sensor is basically a FE-I3 compatible sensor. The only speciality concerns the first and the last columns. Always a group of ten of the 600 μm long edge pixels are shifted opposite to the guard rings, see Figure 5.27. The overlap relating to the high voltage pad differs from group to group by 25 μm. The overlap of the first group is $-50\,\mu$m, i.e. the high voltage pad exceeds the end of the pixels by 50 μm. The pixels of the third group end up with the high voltage pad, those of the last shifted group no. 15 protrude by 300 μm. The obtained free space between the edge and the inner pixels are filled with adapted dummy pixels. They are connected to the bias grid network to avoid any field inhomogeneities due to potential differences. As they are not read out by the front end chip they stay inactive.

This layout was designed in order to be able to investigate different pixel overlaps opposite to the guard rings with only one sensor. It can be seen whether the efficiency decrease in the edge direction is only voltage dependent or also correlated with the pixel overlap distance. On the basis of these results it is possible to evaluate whether it makes sense to shift the pixels further to the edge or if it exists a voltage dependent limit.

For the following test beam analyses always eight of the ten pixels of one shifted group are superimposed to one pixel, called slice. They are marked with black boxes in Figure 5.27. By omitting the first and last pixel of each group it is tried to avoid any interfering effects due to inhomogeneous geometries. Thus, every analysed pixel is surrounded by pixels of the same position. Furthermore, any effect of the bias ring which is as well shifted stepwise are excluded. Because in many cases only one edge column of the assembly is facing the beam, only eight pixels can be overlayed. Therefore, one has to collect significantly more data than for edge studies with standard sensors to gain sufficient statistics for a subpixel resolved plot.

Example for an Unirradiated Assembly

Figure 5.28 shows the edge efficiency of an unirradiated pixel shifted stepwise sensor assembly which was operated in a test beam setup. The example contains the data of DO 43, a 200 μm thick sensor with a bias voltage of 80 V. The coloured 2D plot shows the hit efficiency of all superimposed pixels, represented by one slice per shift distance. To increase the statistics for one bin, the track information along the short

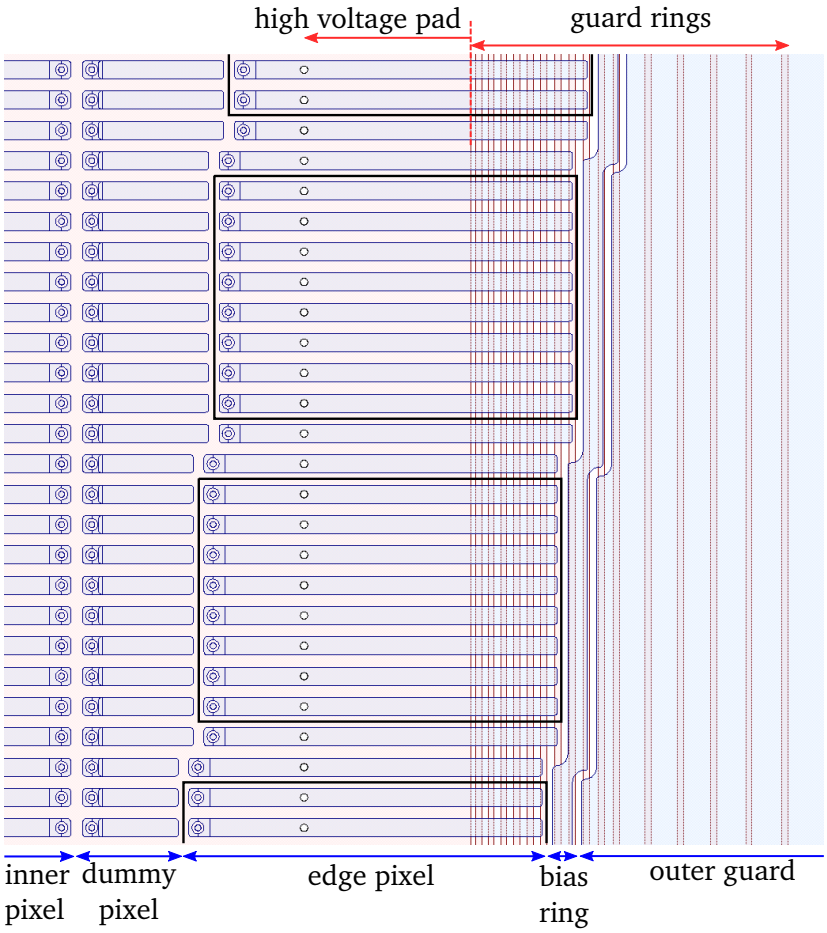


Figure 5.27.: Top view on the design of the edge columns of the pixel shifted stepwise sensor. Respectively a group of ten of the 600 μm long edge pixels are shifted opposite to the guard rings. The overlap relating to the high voltage pad differs from group to group by 25 μm. The obtained free space between the edge and the inner pixels are filled with adapted dummy pixels. They are as well connected to the bias grid network (not visible). The n^+-implantation is seen in blue, the p^+-implantation in red.

pixel side is disregarded by transferring it to the same bin. This is reasonable as only the efficiency characteristics along the long pixel side is relevant. The characteristics in the short pixel direction should anyhow be uniform for symmetrical reasons. The slices are highlighted by black boxes, the end of the high voltage pad and the guard rings are marked in grey. The lower plot in the figure shows a projection of the hit efficiency of each slice to the x-axis. Analogous to the analysis of the FE-I4 based sensors the efficiency decrease in the edge region is fitted by a Gauss error function (compare Section 5.5.2, Figure 5.24).

It becomes apparent that the first three slices do not show any data which is due to the fact that only the upper part of the sensor was placed in the beam. The characteristic triangle which is formed by the dummy pixels has as well no entries. This is expected as those pixels are not read out.

It can be seen that for all slices the plateau attains a hit efficiency of 1 or slightly below which is expected for the central region of unirradiated sensors. At the edge region the efficiency decrease smoothly and continuously S-curve like to 0. The fit curves interpolate the edge efficiency drop very well. Within the uncertainties most points are lying on the curves.

For the slices 5 to 10 the efficiency characteristics follows the same steps as the geometry of the pixels. From one slice to the next the efficiency drop at the edge is shifted as well by 25 μm. The effective pixel length stays the same. Approximately with slice 11 the starting efficiency drop does not move outwards with each step anymore. This can be seen clearly in the 2D map where the red colour marks the efficiency above 90%. For the five uppermost slices the first non-red bin is located at the same position around

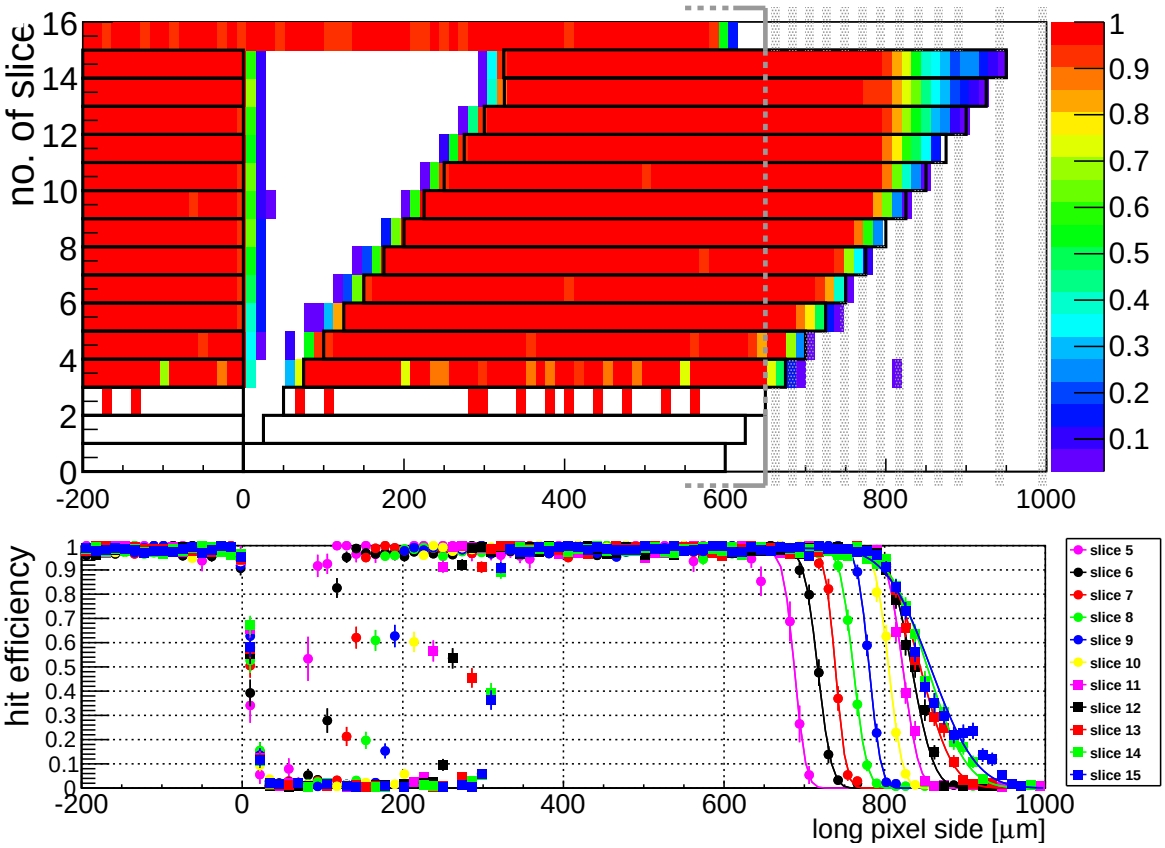


Figure 5.28.: Hit efficiency map of the edge of the unirradiated FE-I3 pixel shifted stepwise assembly DO 43 which was operated at 80 V. The sensor thickness is 200 μm. In the coloured 2D plot red stands for an efficiency close to 1 and violet for an efficiency close to 0. The slices which are marked in black represent an overlay of respectively eight pixels with the same overlap referring to the high voltage pad. Latter is located at $x = 650\,\mu$m and indicated in grey like the guard rings. The plot at the bottom is a projection of the efficiency to the x-axis in which the S-curve like drop opposite to the guard rings becomes visible. It can be seen that until slice 10 the effective end of the pixel moves outwards with respect to the pixel geometry. With slice 11 the starting efficiency drop does not move outwards with each step anymore. The effective end of the pixel still moves outwards but significantly less than the pixel geometry is shifted.

800 μm. It seems as if the position of the starting efficiency drop goes into a kind of saturation. The slope of this efficiency drop however gets smaller with each slice. This has the effect that the effective end of the pixel still moves outwards but significantly less than the pixel geometry is shifted.

Example for an Irradiated Assembly

An analogous hit efficiency plot of an irradiated sensor assembly shows Figure 5.29. The example contains the data of DO 47, a 150 μm thick sensor, irradiated with neutrons to the fluence of $5 \cdot 10^{15} \mathrm{n_{eq}/cm^2}$. It has been operated at a bias voltage of 400 V.

The third slice shows a slightly reduced performance. This is likely due to a decreased statistics resulted by a lack of beam in the lower sensor region. The other slices have

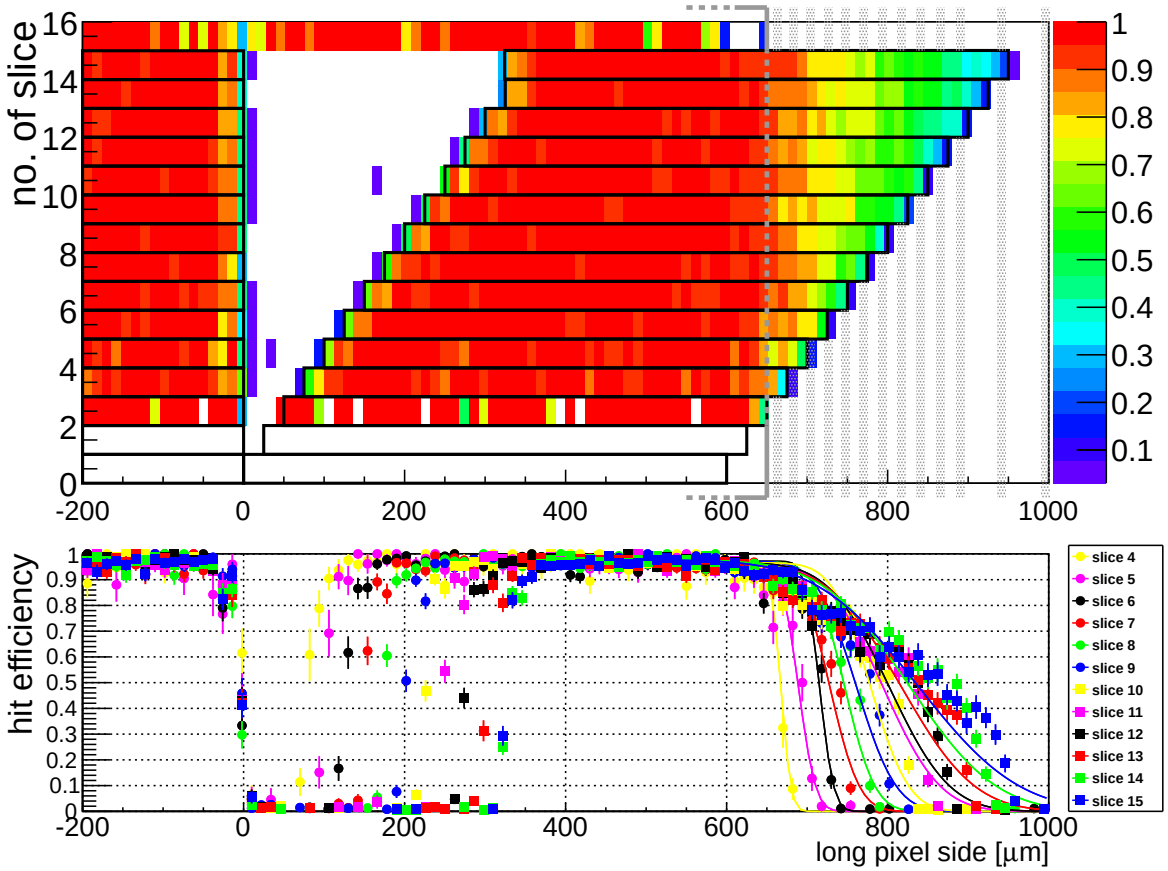


Figure 5.29.: Hit efficiency map of the edge of the FE-I3 pixel shifted stepwise assembly DO 47, irradiated with neutrons to the fluence of $5 \cdot 10^{15} n_{eq}/cm^2$. The sensor thickness is 150 μm. It was operated at a bias voltage of 400 V. The plots are analogous to those in Figure 5.28. Opposite to the guard rings the S-curve like efficiency drop translates smoothly into a linear one with a rising pixel overlap as illustrated in Figure 5.30.

plateaus on average around 97% efficiency which is quite well for a sensor with such an irradiation fluence at such a relatively low bias voltage. The LUB 2 assembly shows at 400 V a lower efficiency of around 90% in the central pixel area despite the lower fluence (see Figure 5.25). One explanation can be the smaller thickness of DO 47 which leads to higher electric fields at similar bias voltages.

At the right end of the inner and the left end of the edge pixels the orange colour indicates a region of a slightly decreasing efficiency. It already starts in front of the geometrical end of the pixels which are highlighted by the black boxes in the 2D map. This characteristic is not observed for the unirradiated assemblies as seen in Figure 5.28. In that case the pixels are homogeniously efficient on their full length opposite to the high voltage pad. One main reason for these differences of the irradiated assembly is the charge sharing probability which is highly increased at the short pixel side boarder. It leads to a significantly efficiency loss especially for lower bias voltages (compare Section 5.5.2 and Figure 5.25). One part of the split charge is draining in the dummy pixels which are grounded but inactive. The charge sharing effect at the long pixel side cannot be seen as all entries in the short pixel direction are superimposed into the same bin. Additionally, the regarded ends of the pixels incorporate the bias grid contact. The bias dot implantation represents a further drain for the charge which has

a noticeable impact on the efficiency of irradiated assemblies (see [Rum13]).

These efficiency decreases are mentionable as they seem to be a general feature in an irradiated sensor. The region of the dummy pixels is lying completely beneath the high voltage pad. Any field inhomogeneities which could cause an efficiency drop can be excluded as the area is sufficiently far away from the end of the high voltage pad. This general efficiency loss has to bear in mind when evaluating the characteristics in the edge region. Even though the bias grid is missing on the other side of the edge pixels, the efficiency loss due to charge sharing will remain. Analogous to the dummy pixels on the left side the bias ring on the right side is as well grounded and drains part of the generated charge.

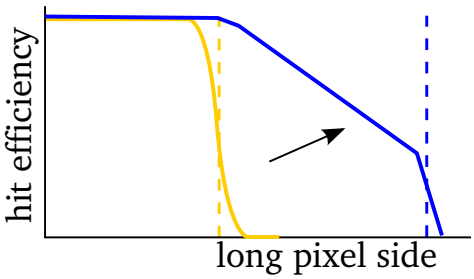


Figure 5.30.: Sketch to illustrate the edge efficiency characteristic for an irradiated assembly as seen in Figure 5.29. The yellow curve belong to pixels with a small shift, the blue one to those with a large shift. With an increasing pixel overlap the S-curve like characteristic translates into a linear one. The dashed lines indicate the positions of the geometrical ends of the pixels.

The efficiency characteristics on the right side in the edge region reveal a remarkable behaviour (see also Figure 5.30). The pixels with a small overlap (yellow) feature a continuously S-curve like decrease to 0 comparable to the unirradiated assemblies. With a rising overlap this S-curve like efficiency drop translates smoothly into a linear one (blue). The slope thereby gets more flat which results in a further expansion of the effective pixel end. The linear shaped efficiency drop of the pixels with the largest overlap look the same as seen for the irradiated FE-I4 assembly LUB 2 for low bias voltages (compare Figure 5.25). Especially for the last slice the bend correlated to the end of the pixels is visible.

Results of all Pixel Shifted Stepwise Assemblies

For all operated pixel shifted stepwise assemblies the edge efficiency drop is fitted with a Gauss error function to obtain the effective end of pixel position for each slice. As for the irradiated assemblies larger deviations between data and fit function are existent for the pixels with a larger overlap, the method of the bin summation is additionally used as described in the previous Section 5.5.2 (compare Figure 5.26). It is observed as before that the determined values of the effective end of the pixels is extremely similar for both methods.

To be able to compare all data, the effective end of the pixels is plotted against the pixel overlap in Figure 5.31, left for all assemblies. This means in comparison to the recent plots in Figure 5.28 and 5.29, the two axes are interchanged whereas the slice number is converted into the pixel overlap. Each assembly is displayed with one colour. The black diagonal line marks the position where the respective pixel would be fully efficient. The vertical error bands represent a default error tolerance of $\pm 6\,\mu$m which is the half size of the bin widths. This value is mostly significantly larger than the error of the fit function. In general the effective end of the pixel moves stepwise, parallel to the geometrical shifts for the small pixel overlaps. With increasing overlap the characteristics deviate from this linear behaviour.

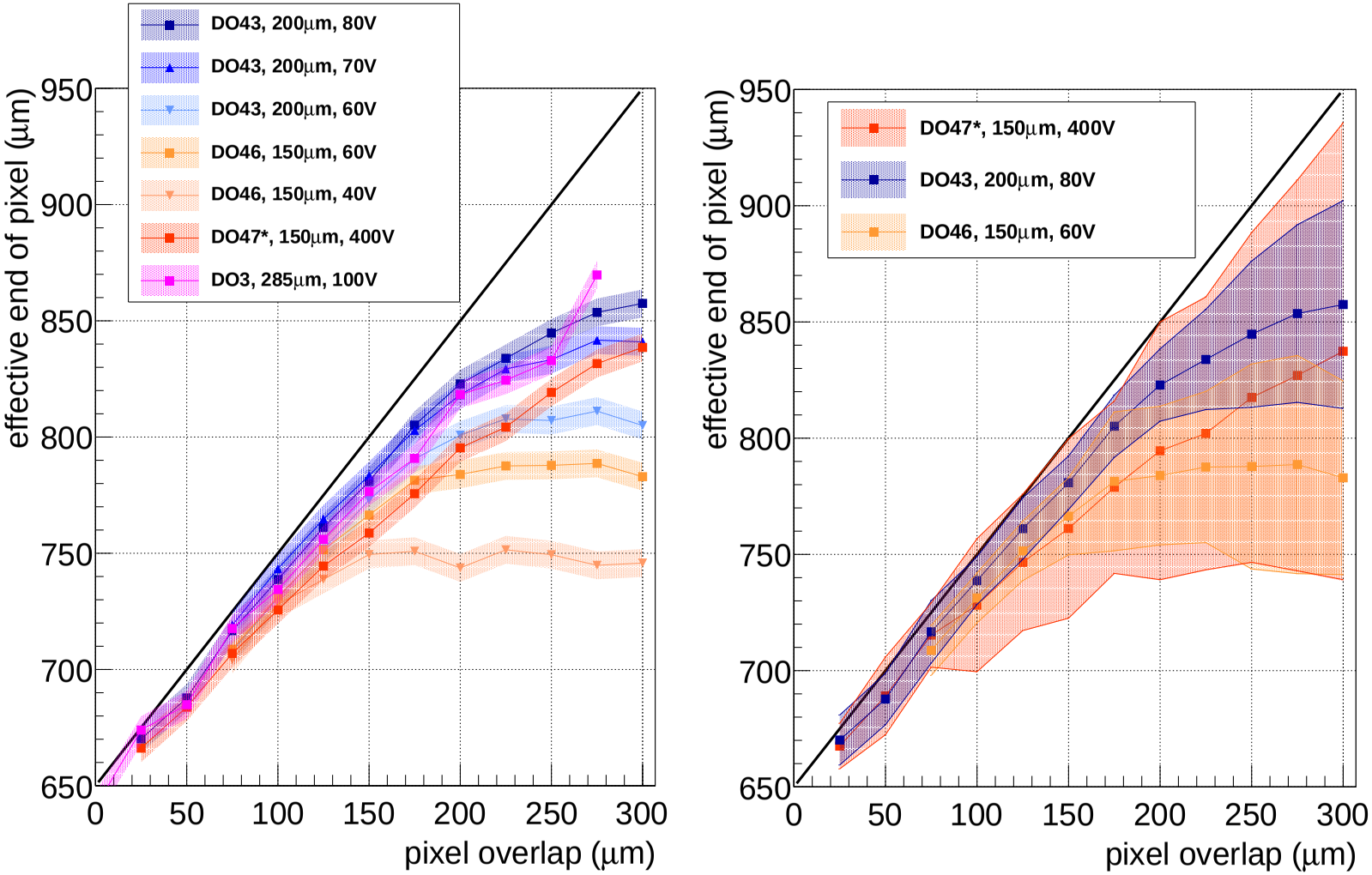


Figure 5.31.: Summary plot of all pixel shifted stepwise assemblies. The effective end of the pixels is plotted against the pixel overlap. The asterisk marks the irradiated assembly. In the left plot the vertical error bands represent a default error tolerance of $\pm 6\,\mu$m, in the right plot the values of the sigma of the Gauss error function fit.

The unirradiated DO 43 assembly with a bulk thickness of 200 μm was operated at 60, 70 and 80 V, it is displayed in blue. It is obvious that the effective end of the pixel is rising with the bias voltage. There are only small differences visible between 70 and 80 V. The curvature of the graph indicate a beginning saturation. The increased pixel overlap effects an increasing edge efficiency but the gain is diminishing. For 60 V the saturation is distinctive. The effective end of the pixel does not exceed 810 μm which is reached at a pixel overlap of 225 μm. The 150 μm thick DO 46 assembly was operated at 40 and 60 V, it is displayed in yellow. The effective end of the pixel saturates for both voltages; for 60 V around 780 μm and for 40 V around 750 μm. A comparison of the two bulk thicknesses can be made as both assemblies were operated at 60 V. It can be seen that the 200 μm thick sensor has a better edge efficiency performance than the thinner one.

It is not possible to give a definite conclusion whether a larger bulk thickness results in an increase of the edge efficiency: The DO 3 assembly has a thickness of 285 μm and was operated at 100 V, displayed in pink. On the basis of the DO 43 and DO 46 data, one could expect an even better performance as its thickness is larger and its voltage is higher. The plot however shows that the edge efficiency is comparable with that of DO 43 at 80 V.

The irradiated DO 47 assembly with a bulk thickness of 150 μm, operated at 400 V features the same trend for small pixel overlaps as the unirradiated DO 46 with the same thickness at 60 V. It though does not run into a saturation at the pixel overlap of 175 μm. It also features a beginning saturation but the curvature is even smaller than for DO 43 at 80 V. This can be explained by the fact that the depletion zone expands from the pixel side and the generated charge can always be drawn to the pixels.

In the discussed plot the only factor which is displayed is the efficiency drop to 50% of the plateau. It does not contain any information about the slope of the efficiency decrease. Because this size also represents an important information, especially in order to describe the differences between unirradiated and irradiated assemblies, it is included in a similar plot in Figure 5.31, right. In this case the vertical error bands represent the values of the sigma of the Gauss error function fit. This means they mark the positions where the fit function drops to 84% and 16% of its plateau. A small sigma value corresponds to a steep efficiency drop. Although the fit functions feature deviations from the data, they reflect the development of the steepness of the efficiency drop quite well. In order to maintain a clear plot, the data of only three assemblies at respectively one voltage is depicted.

For both, unirradiated and irradiated assemblies, the sigma is by trend increasing with the pixel overlap. It becomes obvious that the values for the irradiated assembly are significantly higher than for the unirradiated ones. For the maximum overlap the value is about twice as high. The characteristic that the efficiency decrease is getting more and more flat with increasing pixel overlap is much more distinctive for the irradiated assembly. This was already discussed on the basis of Figures 5.29 and 5.30. The S-curve like drop translates into a more flat linear one. Furthermore, this illustration makes clear that the efficiency drop to 84% which is marked by the lower error band limit runs into a saturation for all assemblies. This is even the case for the irradiated assembly where the drop to 50% of the plateau continues to increase.

It again has to be pointed out that the fit functions only represent approximations to the real efficiency characteristic. Deviations of the fitted parameters always have to

take into account especially for large pixel overlaps of the irradiated assemblies where the sigma is by trend determined to be too small, i.e. the steepness of the efficiency drop is too large.

5.5.4. Summary of Edge Efficiencies

The test beam results of this section show that the shifting of the pixels opposite to the guard rings represents a significant improvement to the edge efficiency performance of planar n^+-in-n pixel assemblies. Although the bulk underneath the pixels is not depleted homogeniously, a charge collection is observed which leads to a positive hit efficiency.

In order to compare FE-I3 and FE-I4 assemblies, those pixels of the pixel shifted stepwise assemblies are regarded which have the same overlap as the FE-I4 assemblies of 250 μm. Because the geometric lengths of the edge pixels are different, it is calculated the active length l_a of the 250 μm overlap. It represents the distance between the effective end of the pixel and the high voltage pad:

$$l_a = (\text{effective end of pixel}) - (\text{x-position of high voltage pad}) \quad .$$

In Table 5.4 this active length is displayed for all operated assemblies dependent on the differing parameters of sensor thickness, threshold and bias voltage.

Table 5.4.: Overview of all investigated assemblies which have been operated during test beam periods. The active length l_a is the distance between the effective end of the pixel and the high voltage pad. It is displayed dependent on the differing parameters of sensor thickness, threshold and bias voltage. Besides the voltage dependency for respectively one sample it can be made some further comparisons, marked by the coloured arrows. The asterisks mark the irradiated assemblies.

sensor assembly	chip type	sensor thickness [μm]	threshold [electrons]	bias voltage [V]	active length l_a [μm]
DO 3	FE-I3	285	3200	100	183 ± 6
DO 43	FE-I3	200	3200	60	157 ± 6
				70	183 ± 6
				80	195 ± 6
DO 46	FE-I3	150	3200	40	99 ± 6
				60	138 ± 6
DO 47*	FE-I3	150	3200	400	169 ± 6
SCC 14	FE-I4	250	3200	90	195 ± 5
SCC 17	FE-I4	250	3200	150	225 ± 5
SCC 92	FE-I4	200	1600	60	243 ± 5
LUB 2*	FE-I4	250	1600	400	158 ± 5
				600	211 ± 5
				800	240 ± 5
				1000	249 ± 5

A clear operation voltage dependency of the hit efficiency can be verified. For unirradiated assemblies this can be explained by the expansion of the lateral depletion zone which moves into the edge region. With an increasing lateral depletion zone the possibility is rising that sufficient charge is generated during the transit of an ionizing particle. For the DO 43 assembly with a sensor thickness of 200 μm, the active length l_a is enlarged by (38 ± 9) μm if the voltage is increased from 60 V to 80 V. A similar value is obtained for the DO 46 assembly with a sensor thickness of 150 μm if the voltage is increased from 40 V to 60 V.

A bulk thickness dependency of the edge efficiency cannot clearly be evaluated with the present data. Not only comparing data from FE-I3 and FE-I4 assemblies but also data from different FE-I3 assemblies show results which are occasionally inconsistent. The comparison of DO 43 and DO 46 leads to the assumption that a thicker sensor bulk is preferable. For the same operation voltage of 60 V, the 200 μm thick sensor features an active length l_a which is (19 ± 9) μm larger than for the 150 μm thick one (see blue arrow in Table 5.4). On the contrary, the DO 3 assembly with a sensor thickness of 285 μm features the same active length as DO 43 although it is operated at a bias voltage which is 30 V higher (see yellow arrow). The higher voltage should lead to a larger active length. It is possible that it is compensated by the larger bulk thickness which is disadvantageous. The SCC 14 assembly with a sensor thickness of 250 μm and a voltage of 90 V yields to the same active length as DO 43 at 80 V (see red arrow). In this case, no clear differences between these thicknesses can be determined. DO 43 with a sensor thickness of 200 μm performs slightly better but taking into account the uncertainties of the determined active lengths, this cannot be stated definitely. The observed behaviour of this present assemblies is only consistent if assuming that sensors with thicknesses around 200 μm yield to the best edge efficiency performance and both smaller and larger thicknesses affect a degradation. This statement is certainly not definite as the data only gives an indication.

A significant improvement of the edge efficiency can be attributed to a lower threshold. The results of the assemblies with the new FE-I4 read-out chip tuned to a threshold of 1600 electrons clearly show a better performance than others with a threshold of 3200 electrons. The unirradiated SCC 92 assembly reveals almost completely active edge pixels with the IBL design at 60 V operation voltage. In comparison to DO 43 which is tuned to the higher threshold of 3200 electrons, the active length is increased by (86 ± 8) μm at the same voltage (see green arrow).

For the irradiated sensors the depletion zone expansion starts at the pixels. In this case an efficiency decrease opposite to the guard rings is as well observed. An explanation for this can be that the depletion zone does not expand uniformly, orthogonally to the surface into the bulk. The field strength could be more distinct opposite to the high voltage pad. The irradiation induced bulk defects could thus cause more charge loss in the edge region. Anyhow the efficiency loss in the edge region can be counteracted by increasing the bias voltage as seen for the LUB 2 assembly: An increase of the bias voltage from 400 V to 1000 V yields to an extension of the active length l_a by (91 ± 7) μm. The DO 47 assembly, operated at a bias voltage of 400 V, even yields to a larger active length as the LUB 2 assembly at the same voltage (see violet arrow). This behaviour is remarkable as it is tuned to the high threshold of 3200 electrons in contrast to the threshold of 1600 electrons of LUB 2. One explanation can be the smaller sensor thickness of DO 47 of 150 μm. This yields to higher electric fields at constant voltages and thus to a larger amount of collected charge. It appears that this

effect is decisive enough to compensate the significantly higher threshold.

For the IBL sensor design the inactive edge width could be reduced to the order of 200 μm. For sensors of the next generation for future ATLAS pixel detector upgrades it is desirable that this value is further decreased. With the conventional technology this can be achieved by two alterations. One is the reduction of the distance between cutting edge and high voltage pad which can influence the breakdown behaviour and thus the quality yield. This topic is discussed at the end of Section 6.3.6. The second option is to increase the overlap of the pixels opposite to the guard rings. The FE-I3 based pixel shifted stepwise assemblies show that the gain of efficiency in the edge region can diminish with an increasing pixel overlap. Anyhow these assemblies have been operated with a high threshold of 3200 electrons. It is assumed that the low FE-I4 threshold of 1600 electrons as well results in better edge efficiencies of pixels which have overlaps of even more than 250 μm as in the IBL design.

6. IBL Sensor

On the basis of the prototype production which was outlined in sections 5.3 and 5.4, the planar IBL sensor production wafer was planned and designed. As the prototype production showed satisfactory results in quality, reliability and performance, there was no significant modification neither necessary nor desired for the main production. All process parameters have been maintained at the sensor vendor CiS.

6.1. Design of Planar IBL Sensors

6.1.1. Global Wafer Design

The substrate material of the IBL planar sensor production wafer is n-doped DOFZ silicon with a $\langle 111 \rangle$ crystal orientation and a resistivity of 2 to 5 kΩcm. The wafer is four inch in diameter and 200 μm thick. Its layout can be seen in Figure 6.1, Table 6.1 specifies an overview of the relevant structures.

Table 6.1.: Reduced overview of the structures on the IBL planar sensor production wafer of 2011. 'GR' stands for guard ring. For an explanation of OSTeR see Section 7.2.4.

	structure	properties
01	FE-I4 DCS	slim edge, 13 GR, pixel overlap 250 μm
02	FE-I4 DCS	slim edge, 13 GR, pixel overlap 250 μm
03	FE-I4 DCS	slim edge, 13 GR, pixel overlap 250 μm
04	FE-I4 DCS	slim edge, 13 GR, pixel overlap 250 μm, w/ OSTeR
05	FE-I4 SCS	different pixel shapes, segmented HV-pad, w/ OSTeR
06	FE-I4 SCS	slim edge, 13 GR, pixel overlap 250 μm
07	FE-I4 SCS	slim edge, 13 GR, pixel overlap 250 μm, w/ OSTeR
08	FE-I4 SCS	slim edge, 13 GR, pixel overlap 250 μm, w/ OSTeR
09	FE-I3 SCS	conventional design, 16 GR
10	FE-I3 SCS	different pixel shapes, 16 GR
11	FE-I3 SCS	slim edge, 13 GR, pixel overlap 250 μm
12	FE-I3 SCS	pixel shifted stepwise, 16 GR, no ganged pixels
13 - 25	GR diode	different design of GRs or active area
26 - 38	test structures	different purposes

In the usable area of the four inch diameter wafer four FE-I4 DCS are housed. The remaining space is used for four FE-I4 SCS, four FE-I3 SCS, smaller guard ring diodes and further test structures. Three of the FE-I4 SCS have the same design as the DCS.

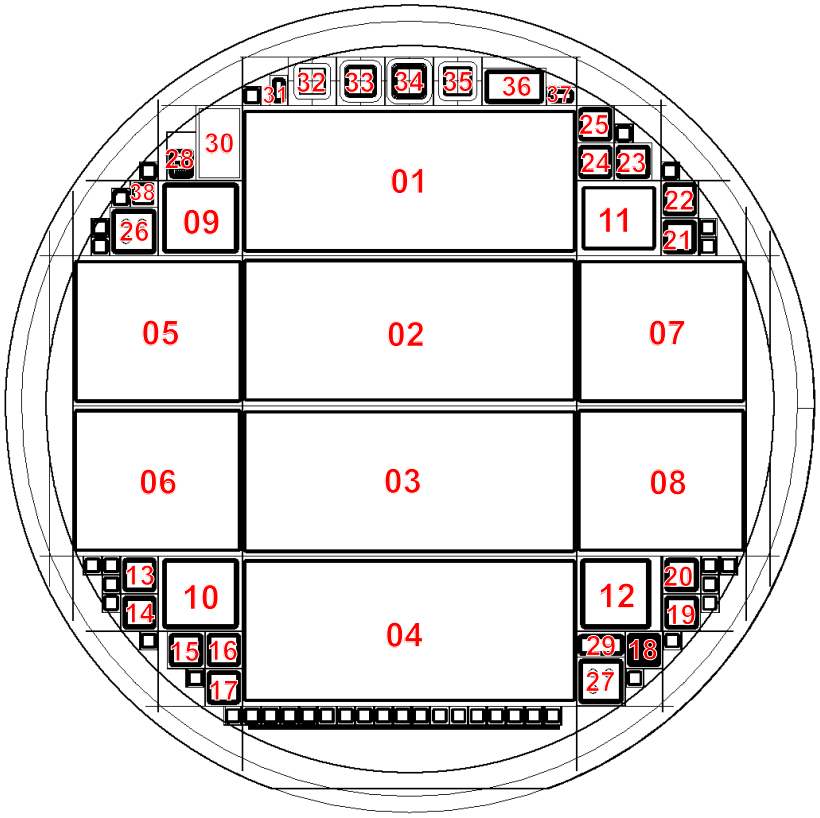


Figure 6.1.: Overview of the IBL planar sensor production wafer of 2011. View to the n-side. The structures are listed in Table 6.1.

They can be used as reference sensors for different IBL related tests as well as for studies for future applications. The FE-I4 SCS No. 05 is a test structure for investigations of different pixel implantation shapes which could be implemented in future sensors. For a detailed description see Section 7.2.2.

The FE-I3 SCS are as well implemented in different designs. For reasons of comparability the sensor No. 09 has the conventional design of the former ATLAS pixel production whilst sensor No. 11 has the same slim edge design as the IBL sensors. The sensor No. 10 features different pixel implantation shapes comparable to those of the FE-I4 sized sensor No. 05. The No. 12 is a FE-I3 based test sensor with the pixel shifted stepwise design to study the edge performance of pixels opposite to the guard rings. The design was already explained in detail in Section 5.5.3.

The further test structures include gate controlled diodes (GCD) with oxide test fields and MOSFET structures (see [ATL03]). These can be tested to control the quality of the SiO_2 and the substrate-oxide interface if deviations from the accustomed production quality is observed.

The placement of the sensors is taking into account that an easy handling during the dicing steps should be preserved. This means an additional detachment and re-taping of shards is not necessary to dice all FE-I4 DCS and SCS. Thereby, a second dicing street as needed in the prototype production design (see also Figure 5.12) is not required. By cutting along the foreseen dicing streets the DCS already have their final dimensions.

6.1.2. Final Sensor Layout

The layout of the IBL FE-I4 sensors is basically a copy of that of the prototype production. The slim edge design as seen in Figure 5.10 is used as the enlarged edge pixels opposite to the guard rings showed conclusive results of the efficiency. As discussed in Section 5.3.1 the pixels of the two central columns of the DCS are extended to 450 μm to keep the necessary gap between the Front-End chips. Due to the layout, the outer dimensions are 41300 μm $\times$ 18600 μm as seen in Figure 5.8. However, after the dicing step at the bump bond vendor the final average dimensions of several sensors was determined to be 41315 μm $\times$ 18585 μm.

High Voltage Contact Pads

The positioning of the high voltage contact pads on the p-side is an important decision which has to be done according to prior agreement with the flex design. The module flex is glued to the sensor and features designated openings with bond pads. These are connected via wire bonds to the high voltage contact pads on the sensor. Figure 6.2 shows a sketch of all of these passivation openings of the p-side of the IBL DCS. They are marked in orange. As seen, each DCS features six large and six small quadratic passivation openings. The edge lengths are respectively 3 mm and 1 mm. The specifications of the flex design have foreseen two possibilities to contact the sensor, the large and the small square at the right. At the time of the IBL wafer submission it was not clear if other positions could have represented a viable alternative. Therefore, the additional openings are included to maintain the possibility of the alternative contact positions. Furthermore, it could be an option to contact several pads to obtain a redundant high voltage supply.

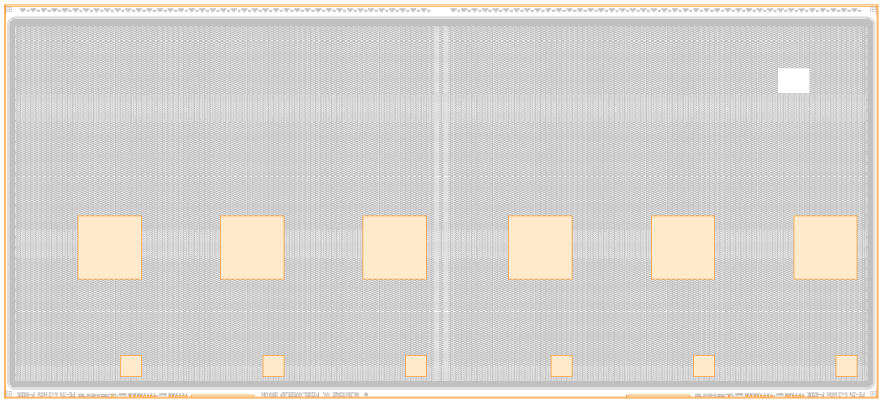


Figure 6.2.: Positioning of the high voltage contact pads on the IBL DCS. The metal is grey, the passivation opening is orange.

Fiducial Marks

The fiducial marks on the p-side of the sensor are necessary for the so-called stave loading, the mounting of the complete modules onto the staves. The alignment on the stave is done visually by means of these four metal crosses which are placed in the corners of the sensor. A sketch can be seen in Figure 6.3. The distances from the centre of the fiducial marks to the edge of the pixel matrix are as well drawn. In this case the pixel matrix does not include the 250 μm overlap of the edge pixels. The two different distances in the vertical direction are caused by the asymmetric extent of the inactive region of the sensor.

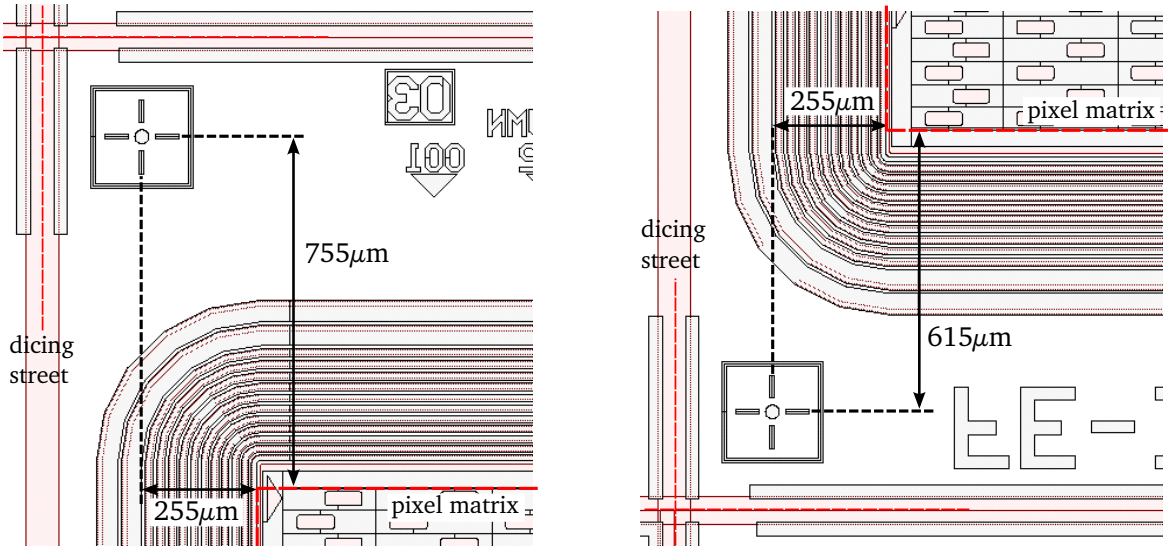


Figure 6.3.: Fiducial marks on the p-side of the IBL planar sensor. The left picture shows the end-of-column logic, the right picture the opposite side. Metal is seen in grey, p^+-implantation in red.

Scratch Pattern

In order to be able to identify a sensor after the dicing step, it is useful to include metallized scratch patterns on which the wafer number can be labelled. Respectively two of them are placed on the p-side of the IBL sensors next to the dicing street. One example can be seen in Figure 6.4. The respective sensor number is already

Figure 6.4.: Metallized scratch pattern on the p-side of an IBL sensor. In this example the engraved binary code labels the batch and wafer number 59-09.

implemented within the metal masks of the n- and p-side of each wafer. The batch and the wafer number have to be binary encoded by engraving marks into metallized squares. This can be done by hand with a pointed tool like a needle or a scalpel. In the case of a mistake, a square named 'not valid' can be marked and the second scratch pattern can be used. Because the batch numbers have six digits it is not reasonable to encode it completely. The shortened batch numbers are used which are documented in Table 6.2.

6.2. IBL Planar Wafer Production

Altogether 150 planar IBL wafers have been ordered at the sensor vendor which results in an aimed number of 600 double chip sensors. The production was originally planned to be subdivided into six batches of 25 wafers respectively. From these batches however only a number of 119 acceptable wafers was reached. This is because of wafer loss during

the processing on the one hand and the fact that some wafers delivered from the sensor vendor did not fulfil the quality criteria (see Section 6.3.2).

In order to guarantee that the desired number of 150 acceptable wafers is available, three further batches have been post processed in time. These remaining 31 wafers only undergo the reception control at the IBL sensor institute (see Section 6.3.1) and can be declared as a backup. They undergo the UBM and dicing steps only for the case that a larger sensor loss during the module and stave production emerges.

An overview of the IBL production batch numbers and the respective numbers of accepted wafers can be seen in Table 6.2.

Table 6.2.: Overview of the IBL wafer production batches. The shortened batch number is used amongst others for the scratch marks.

	batch number	shortened batch number	accepted wafers
1	310892	92	20
2	310893	93	22
3	310894	94	18
4	312059	59	20
5	312060	60	17
6	312061	61	22
7	313431	31	12
8	313432	32	11
9	313512	12	8

6.3. Quality Control

The quality assurance of the IBL sensor production is an essential process to ensure a sufficient number of acceptable DCS for module hybridisation. It should comprise several control steps to be able to retrace where and when the sensor behaviour changes. The conducted measurements are mainly an IV test which is the most important characteristic to decide on their operating ability. One CV measurement on wafer level is requisite to obtain an overview of the depletion voltages. For a comparison see also Section 5.4.

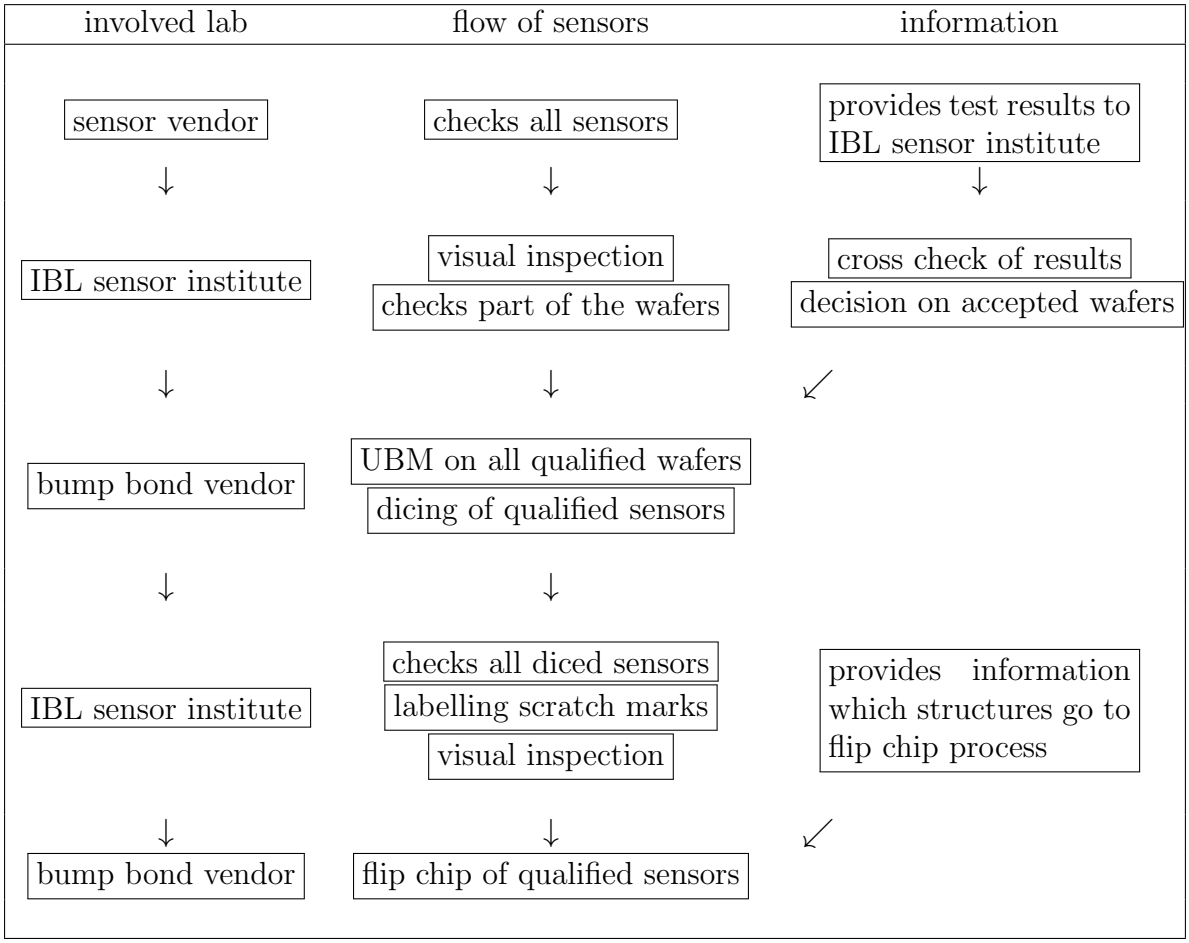
The following discussed quality assurance steps and sensor specifications already have been documented and published in two ATLAS notes [Kli11a] and [Kli11b].

6.3.1. Quality Assurance Steps

Table 6.3 shows a generalized flow chart of the quality assurance steps which have been performed for the IBL planar sensor production. The sensor vendor is CiS, the bump bond vendor IZM and the only IBL sensor institute which participated is TU Dortmund[1].

[1] TU Dortmund, Lehrstuhl Physik E IV

Table 6.3.: Flow chart of the process steps during the quality assurance of the planar IBL sensor production.



The first quality check is done by the sensor vendor who performs an output control of all produced wafers. It includes IV measurements on the FE-I4 DCS No. 01 to 04 (see Figure 6.1 and Table 6.1), the FE-I4 SCS No. 05 to 08 and on one FE-I3 SCS No. 09. Furthermore, one CV measurement can be derived from one guard ring diode No. 21. The sensor vendor provides all test results to the sensor institute.

After arrival at the sensor institute a first visual inspection is done. Five randomly chosen wafers per batch are cross checked by doing IV measurements of the same structures. On the basis of these data the reliability of the measurements of the sensor vendor can be evaluated. Besides the proof of a general comparability between the measurements of sensor vendor and IBL institute, this cross checks can be used to remeasure sensors showing an untypical IV behaviour. A further cross check consists in CV measurements which are performed on several randomly selected wafers at this stage. As it is much more facile to do a CV measurement on wafer level, this stage is in practice the only possibility to re-check the depletion voltage.

These measurements on wafer level can be easily done in-house at the sensor institute even if the available conditions do not conform to state-of-the-art clean room standards. The reason is the fact that one of the first steps of the UBM process is a cleaning of the wafers at the bump bond vendor. On the basis of the delivered and cross checked

data, the sensor institute decides which wafers fulfil the quality criteria and are hence accepted.

The qualified wafers are send to the bump bond vendor who performs the UBM process and the subsequent dicing step. The quality control after the UBM process is not considered to be necessary. The experience with the prototype production (see Section 5.4.2) showed that no significant deterioration has to be assumed for this step. The IV measurement after the dicing step however is the most important quality control of the bare sensor because it decides whether the sensor is acceptable for the flip chip process. It is carried out on all FE-I4 DCS. The performance can be done at the bump bond vendor or at the sensor institute. Latter can result in polluted sensors if the clean room conditions do not conform to the standards. The diced sensors are however laborious to clean in comparison to entire wafers. Furthermore, an additional cleaning step is not foreseen before the bump bonding. Anyhow a measurement at the sensor institute is preferred as it can be done much more flexibly in time and manpower. Inspections of firstly treated sensors measured at the sensor institute showed that a cleaning step was not necessary before the bump bonding. Hence a shipment of all diced sensors to the sensor institute is done. Prior to the measurement the scratch patterns are labelled on the diced DCS. The final step at the sensor institute is a visual inspection of all DCS.

On the basis of this final IV measurement it is decided which sensors are qualified and can be bump bonded. This quality control ensures that no non-operable module is assembled which would cause unnecessary costs. Besides the loss of a functional FE-I4 chip the flip chip process itself is quite cost-intensive.

6.3.2. Quality Criteria

The quality criteria of the IBL sensor production are adapted from the experiences made with the prototype production (see Section 5.4). As a possible distinguishing label it can be used the three signal light colours: Green for good sensors, red for bad ones and yellow for those of second quality.

The depletion voltage V_{depl} should be in the range between 15 V and 70 V. After defining an average depletion voltage for all sensors, the operation voltage is set to $V_{\text{op}} = V_{\text{depl}} + 30\,\text{V}$. The maximum allowed leakage current must not exceed $2\,\mu\text{A}$ at operation voltage. The leakage current slope is defined to be the ratio of operation and depletion current and must not exceed the value of 1.6 : $\text{slope} = I_{\text{op}}/I_{\text{depl}} \leq 1.6$.

One wafer delivered from the sensor vendor is accepted if at least two of the four DCS fulfil the quality criteria. The wafer thickness has to be in the range between $180\,\mu\text{m}$ and $220\,\mu\text{m}$. The planarity shall be better than $40\,\mu\text{m}$.

It has to stress that the mentioned quality criteria only represent the minimum requirements which have to be fulfilled. A sensor which fulfils the electrical criteria can still be excluded from the list of acceptable sensors. One reason for such a degradation is a severe deterioration after the dicing step which is seen during the visual inspection (see next Section 6.3.3). Depending on the severity of the deterioration the category can change to yellow or red. Another reason for a degradation to the yellow category is an IV characteristic which on the one hand stays within the requirements for I_{op} and the current slope but on the other hand shows a physically untypical behaviour.

Therefore, all IV curves are checked by eye before the final decision is made which sensors are qualified for bump bonding.

6.3.3. Visual Inspection

Two main visual inspections are done at the sensor institute. The first one is a reception control after the wafers arrive from the sensor vendor. Besides the general examination that no wafer is broken during the shipment it is checked that the number and the wafer numbering concur with the delivery note. During the wafer surface inspection the attention is only given to larger defects visible by eye like scratches or noticeable inhomogeneous shades.

The second visual inspection is done of the diced sensors after the last IV measurement. It is the pre-delivery inspection before the shipment back to the bump bond vendor. Because the electrical test is already done at this stage, it is only focussed to the pixel side which is surveyed with a light microscope. Any severe deteriorations on the p-side should become noticeable in the IV characteristic. This inspection aims to find any damages which do not become noticeable thereby like inhomogeneous UBM pads or larger defects on the n-side cutting edge. Figure 6.5 shows light microscope pictures of different peculiarities which have been observed on the sensors n-side.

The UBM quality has a large influence on the reliability of the bump bond connections. Therefore, it is paid attention to strips, shades or scratches on the pixel matrix. They could have occurred during the dicing step where the sensor is glued with the n-side down to the tape as well as during the IV measurement where the n-side is drawn to a metal chuck.

Figure 6.5 a) and b) are showing defects on the UBM-pads themselves. With a small optical magnification they are noticeable as the microscope light is reflected in a diffuse way in comparison to normal UBM-pads. In Figure 6.5 a) the difference between normal (bottom left) and defective pads (top right) can be seen in a large optical magnification. The defective ones possess scratches on the surface, others feature small cracks (Figure 6.5 b)). A reason for that could be a movement of the sensor on the metal chuck during the IV measurement. Apart from the surface defects, the pads do not show any deformations like indentations. They should thus not contribute to any missing bump connectivities. During the whole sensor production this effect is observed on several sensors. For most of them the defects occurred however only at a very small amount of pixels, mostly grouped together. Only five sensors show a significant spread of effected pixels.

Besides any defects on the pixel side, dirt particles can as well derogate the bump process, especially if it is located next or on a UBM pad as seen in Figure 6.5 d). Because a cleaning of the sensors is not foreseen before the bump bond step it is endeavoured to send them as clean as possible. For this reason any visible dirt or debris is flushed with clean canned air or removed with a vacuum cup tweezers shortly before closing the transport case.

The other focus during the second visual inspection is laid to the cutting edge. As discussed for the prototype production (see Section 5.4.2) the bottom side is damaged much more than the top side. Thus, larger deteriorations of the outer guard area are supposable. The attention has to concentrate especially to the short pixel side which is

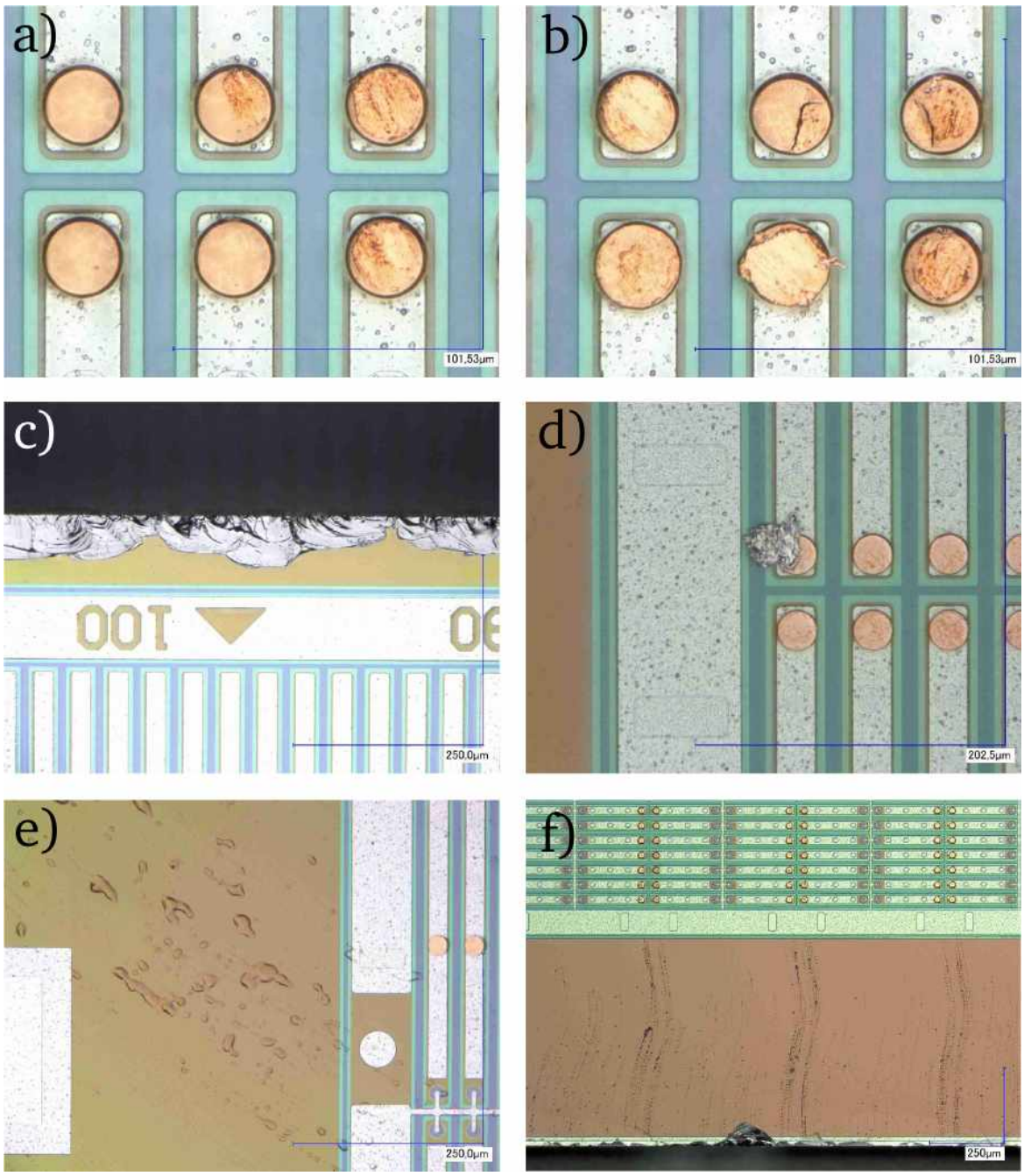


Figure 6.5.: Light microscope pictures of different peculiarities which have been observed on the sensors n-side. a) and b): small defects on the surface of the UBM pads; c): larger cracks at the slim edge dicing street; d): dirt on a UBM pad; e) and f): water residues in the edge region.

more susceptible due to the minimized safety margin. The distance between the cutting edge and the bias ring which is the first functional structure is reduced to $\sim 100\,\mu$m at this side. Hence it can happen that cracks range from the edge close to the bias ring or even into it. Cases as shown in Figure 6.5 c) in which the cracks affect the half width of the safety margin are observed frequently. A crack close to the bias ring results in a degradation of the sensor to the yellow category, a damage of the bias ring to the red category.

Figure 6.5 e) shows a kind of water residue which is especially noticeable in edge region of several sensors. It is presumably caused by the dicing procedure. Some kind of strip pattern correlating with the bump pad position are often observed (see Figure 6.5 f)). They can be caused after the dicing by the flushing water which is contaminated with small debris residues. The residues occur batchwise which leads to the assumption that those sensors have been diced in a row and treated the same way. In order to clean the affected sensors, a chemical treatment would be necessary which would lead to a large effort in time and manpower. As the bump bonding process is not affected by these water residues such a procedure is not conducted.

All deteriorations which are noticed during the visual inspections are registered and taking into account for the decision if a sensor is degraded to the yellow or red category.

6.3.4. CV Measurements

The purpose as well as the setup and the interpretation of a CV characteristic was already discussed in detail in the corresponding prototype Section 5.4.1. In the course of the IBL sensor production the only systematic CV measurements have been done at the sensor vendor to obtain the depletion voltage for each wafer. The distribution of these depletion voltages for all 150 accepted wafers of the nine batches can be seen in Figure 6.6 left.

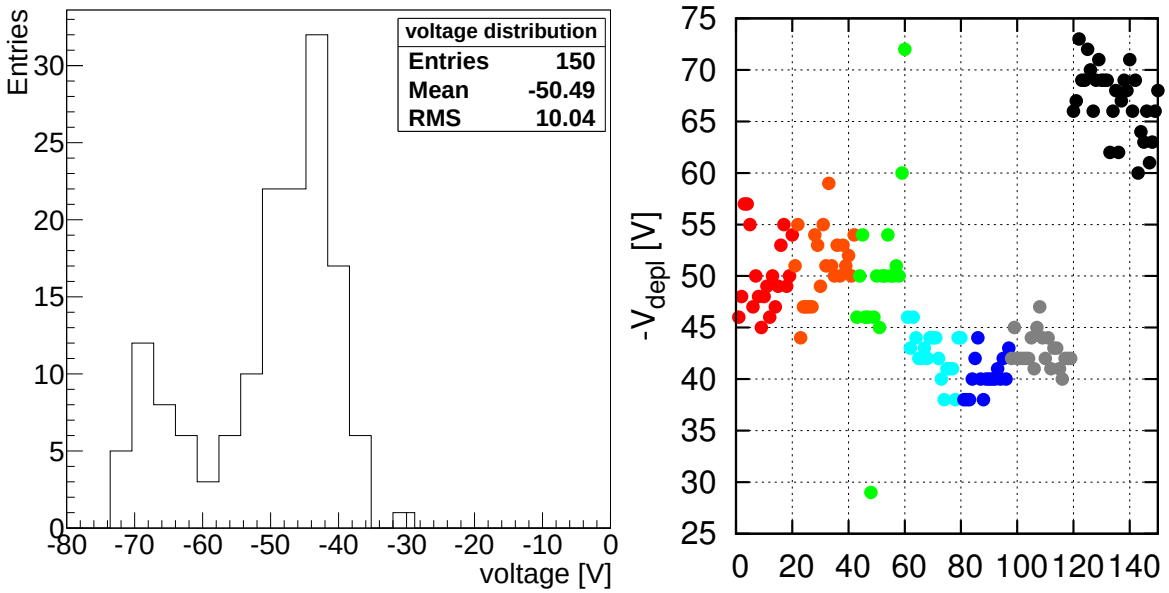


Figure 6.6.: Depletion voltages of all 150 accepted IBL wafers, measured at the sensor vendor. The left plot shows the distribution, the right plot the dependency on the wafer number. Each batch from one to six has its own colour, batches seven to nine are subsumed in black. It is noticeable that the depletion voltage of the backup batches is about 20 V higher than the average of the first six batches. This explains the second, smaller peak around 70 V in the distribution.

The histogram shows a double Gaussian distribution with one main peak around 45 V and one smaller side peak around 70 V. It is obvious that this aspect is caused by a systematic reason. On the right side of Figure 6.6 the single depletion voltages are

plotted against the number of the wafer, i.e. the changes through all batches become visible. Each batch from one to six has its own colour, batches seven to nine are subsumed in black. It becomes clear that wafers of respectively three subsequent batches possess similar depletion voltages. This means that these corresponding wafers have a related bulk resistivity, assuming the same bulk thickness for all wafers (compare Equation (3.1)). This observation is supported by the fact that always three batches have a subsequent numbering which suggest that the substrates originate from the same silicon ingot (see Table 6.2). The mean depletion voltages and the corresponding root mean square values of the subsumed batches are summarized in Table 6.4.

Table 6.4.: Depletion voltages of subsumed IBL batches.

	V_{depl}[V]	
batches	mean	RMS
1 - 3	50.4	5.3
4 - 6	41.9	2.1
7 - 9	67.0	3.3
1 - 6	46.2	5.9
1 - 9	50.5	10.0

It is noticeable that the depletion voltage of the last three batches is about 20 V higher than the average of the first six batches. This behaviour is understandable as the last batches represent the backup wafers (see Section 6.2). It was already communicated by the sensor vendor in advance that these wafers supposably have a slightly worse quality which manifests in a lower bulk resistivity and thus in a higher depletion voltage. As they only have to be post processed in case if too many sensors get unusable, an increased depletion voltage is regarded to be acceptable.

The sensor institute performs only cross check CV measurements on some randomly chosen wafers before the shipment to the bump bond vendor. Figure 6.7 shows exemplarily the CV data of six wafers of the batches 2 and 6. Two or three diodes per wafer have been measured in order to check if any deviations of the depletion voltage across the wafer is visible.

It can be seen that the fluctuations between diodes of one wafer are minimal. This is remarkable as those of the prototype production have exceeded about 10 V (compare Figure 5.14). It indicates a good substrate quality with a high homogeneity. The deviations between the different wafers are as well conspicuously small. They do not exceed 5 V even between the wafers of different batches.

Figure 6.8 shows a migration plot in order to illustrate the differences of the depletion voltages of the measurements of the sensor vendor and those of the sensor institute. The coloured points refer to the six wafers of Figure 6.7, the grey ones belong to wafers of the backup batches 7 to 9. The diagonal solid line marks the values which do not change, the dashed blue diagonal lines indicate the deviations in steps of 5 V. An explicit correlation between the values of the sensor institute and those of the sensor vendor is not existent for the wafers of the batches 2 and 6. It is likewise no uniform offset visible. The values of the sensor institute are therefore significantly lower. The differences vary from 8 up to 20 V which cannot be explained with an error in reading.

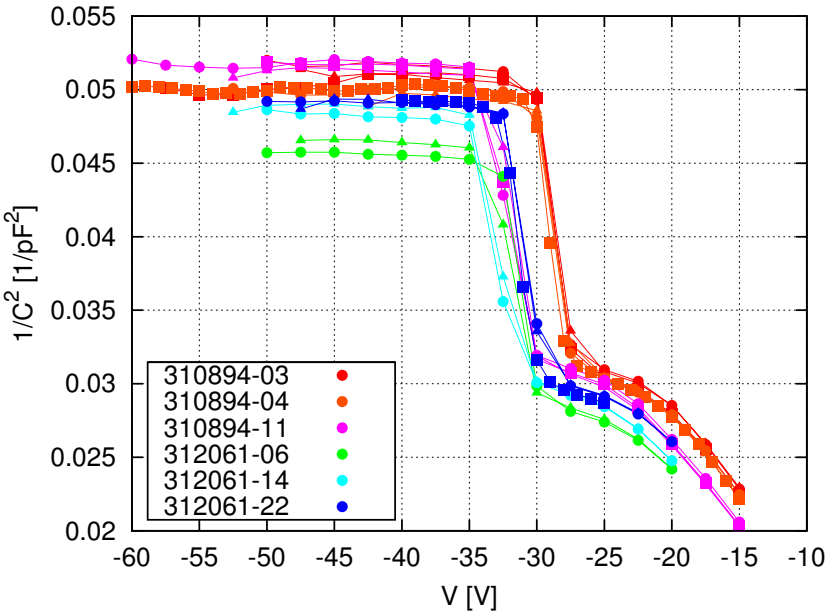


Figure 6.7.: Exemplary CV measurements of several diodes of six IBL wafers. One colour represents one wafer, one symbol stands for one diode number. The fluctuations between diodes of one wafer are minimal. The deviations between the different wafers are as well conspicuously small.

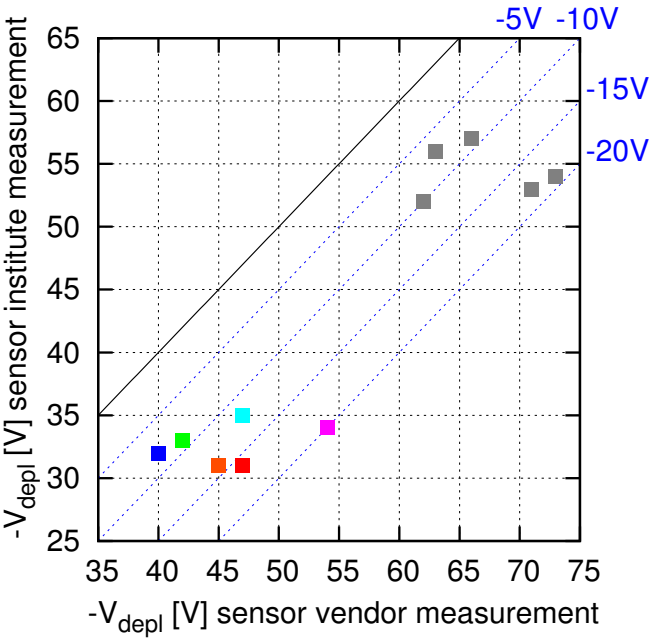


Figure 6.8.: Depletion voltage migration plot of the IBL production comparing the data of the sensor vendor and the sensor institute. The coloured points refer to the six wafers of Figure 6.7, the grey ones belong to wafers of the backup batches 7 to 9. The diagonal solid line marks the values which do not change, the dashed blue diagonal lines indicate the deviations in steps of 5 V. The systematic offset between the main and the backup batches can be observed in both data. Within the main or the backup batches an explicit correlation is not existent.

The wafers of the backup batches show similar differences, i.e. the depletion voltage offset of about 20 V between the main and the backup batches which where measured at the sensor vendor are confirmed by the data of the sensor institute. Some example plots of measurements by the sensor vendor show that the delivered values fitted to the raw data. Thus, a systematic difference in the measurement method or setup has to be assumed. A detailed explanation for these deviations could not be found.

A systematic re-measurement of all wafers at the sensor institute is time-consuming and would cause a delay in the sensor post-processing. As the UBM step represents a bottleneck during the post-process chain it is demanded to pass the wafers on to the bump bond vendor without any unnecessary delays. Furthermore, all measurements at the sensor institute show a lower depletion voltage than the values delivered by the sensor vendor. Thus, there is no risk because the assumed depletion voltage is by trend higher than the actual one.

The average depletion voltage for the planar IBL sensors is defined to be 50 V which

equates the mean value of the distribution in Figure 6.6. It is as well in the same range as the defined value for the 200 μm thick sensors of the prototype production (see Section 5.4.1). Because of the same design and specifications of the two productions it is again decided to take a safety margin of 30 V which is added to the depletion voltage. The resulting operation voltage of 80 V still guarantees that all sensors are operated fully depleted. Even the maximum depletion voltages of the backup wafers of the last three batches are lying beneath this value (see Figure 6.6, right).

6.3.5. IV Measurements

First Quality Control at the Sensor Institute

Systematic IV measurements on wafer level are done by the sensor vendor who performs an output control. All FE-I4 and one FE-I3 sensor are checked on every wafer. At the sensor institute five wafers per batch are chosen to be cross checked. The backup batches are counted as one batch. Figure 6.9 shows exemplarily the IV characteristic of two wafers containing the data of the sensor vendor in black and the sensor institute in red.

In Figure 6.9 a) both data sets show a quite similar behaviour. The absolute current values as well as the regions of the initiating breakdowns are comparable. Only the sensor 02 shows a considerably decreased breakdown voltage which results in a degradation to the red category. A reason can be a damage of the sensor which occurred during the transport. Anyway it can be assumed that the sensor was still functional and was correctly measured at the sensor vendor as the shape of the curve shows a typical IV characteristic.

A different case can be seen in Figure 6.9 b) showing the comparison of the IV measurements of a further wafer. In this example the IV characteristics of the sensor vendor feature noticeable high slopes between depletion and operation voltage for several sensors causing a classification to the red category. This kind of resistive behaviour does not represent a typical IV characteristic of an unirradiated sensor as a plateau is not identifiable. A cross check of these sensors is thus reasonable. As the data of the sensor institute represented by the red symbols show, the slope is significantly decreased and a typical plateau is visible. All sensors fulfil the quality criteria afterwards. A reason for these different curves is not obvious. The topic is discussed later.

The IV measurements can be analysed analogous to the prototype production, see Section 5.4.2. For a clearly arranged overview one uses migration plots in which the correlation between two operation currents is displayed. Figure 6.10 shows a migration plot of the operation current comparing the data from the sensor vendor with the measurements of the sensor institute. It includes 279 sensors of all 36 cross checked wafers. The batches are displayed by differently coloured symbols.

It can be seen that most of the points are located on the diagonal line or within the 20% tolerance region. An increased operation current is only visible in some single cases. Therefore, there is a large fraction of sensors where the leakage current is decreased, especially for those of the batches five and six (dark blue and grey). In total about 22% of the points are lying in the upper part of the plot outside the 20% tolerance margin. Because this kind of presentation only illustrates the single current values it is not

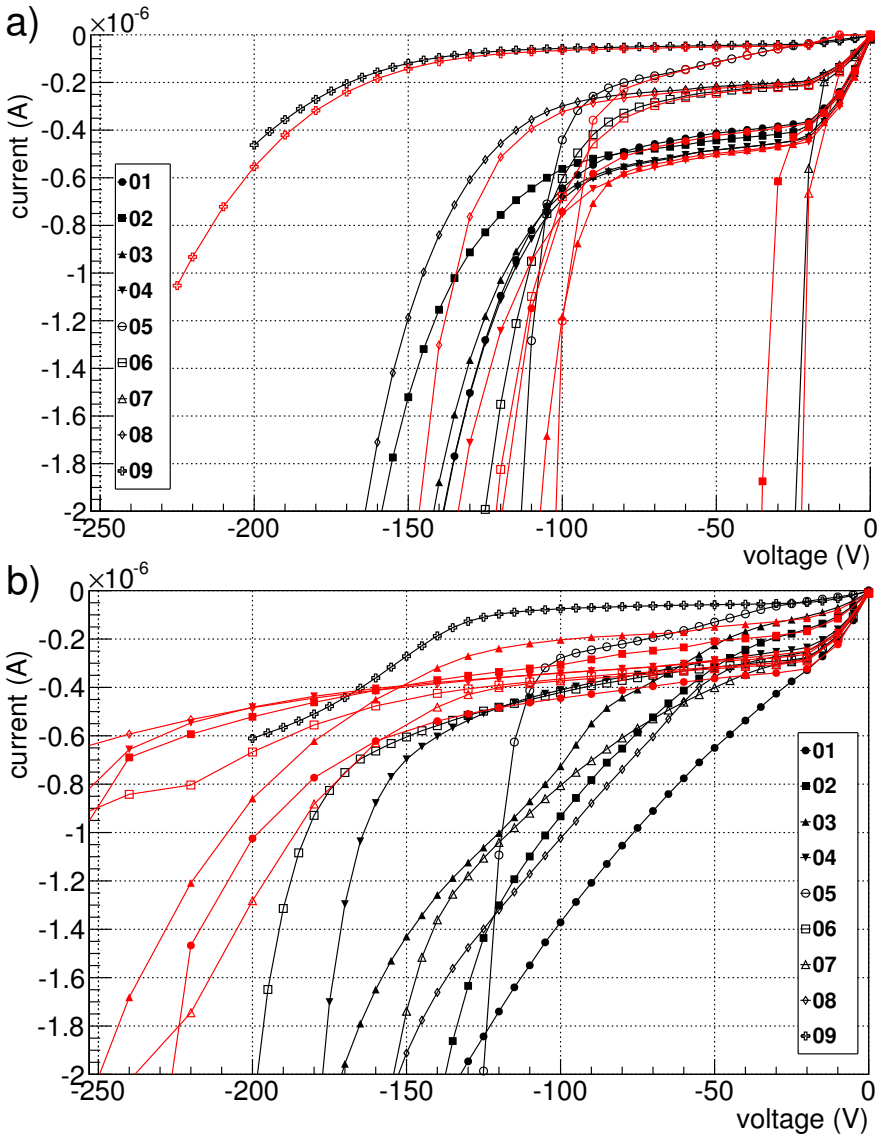


Figure 6.9.: Example of IV characteristics of two wafers cross checked at the sensor institute. One symbol stands for the same sensor number. Black symbols represent data from the sensor vendor, red ones from the sensor institute. The wafer in a) shows a comparable behaviour of all sensors. The wafer in b) features large deviations between the two data sets. The high slopes measured at the sensor vendor are significantly decreased in the data from the sensor institute.

possible to evaluate if the IV slope is increased or if the absolute leakage current is on a higher level. Latter could be explained for example by a higher ambient temperature.

In order to get an impression in how far the IV slope between depletion and operation voltage changes, the slopes of the same datasets are plotted in a migration plot in Figure 6.11.

In this plot the maximum slope is set to 1.8 to comprise also higher values. This limit is marked by the two dashed black lines. There is no significant information loss as the maximum allowed slope is 1.6. For those sensors showing a low breakdown voltage the current limit of 2 μA can be reached before the data points at depletion and operation voltages are taken. Thus, it is not possible to determine a slope. In these cases the slope is set to the default value of 2.0. This procedure implicates the advantage that two informations are included in the same plot: That whether the sensor is functional due to the operation current and the absolute slope. Furthermore, possible temperature differences between the two periods of data taking which can cause fluctuations of the absolute current do not distort the result in this presentation. An increased temperature leads to a similar increase of the two currents. The temperature dependency is compensated as the slope is the relative ratio between these currents.

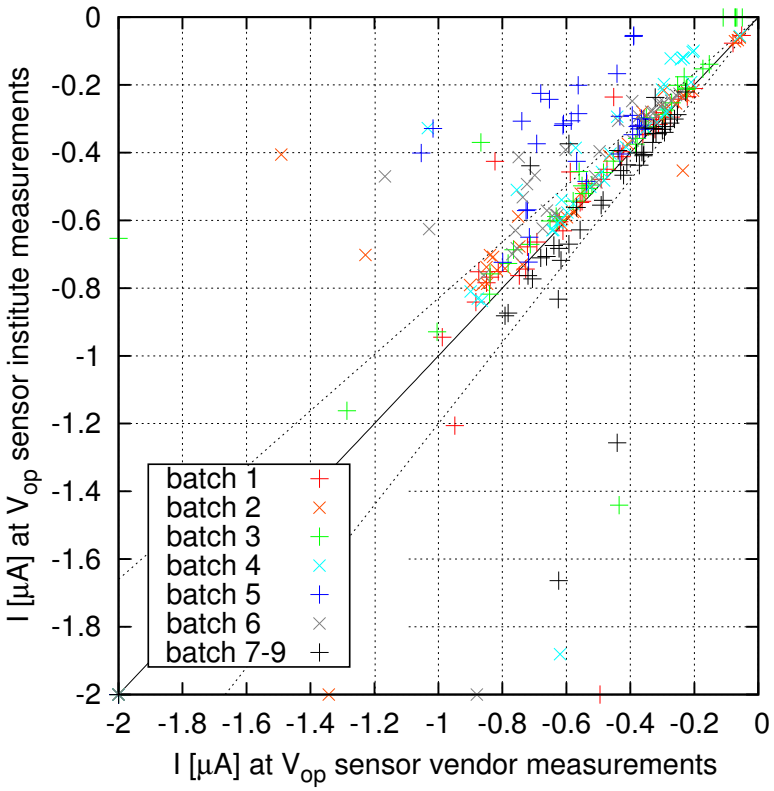


Figure 6.10.: Operation current migration plot of the IBL production comparing the data from the sensor vendor with the measurements of the sensor institute. It includes 279 sensors of all 36 cross checked wafers. The batches are displayed by differently coloured symbols. 21 points are overlayed in the bottom left corner.

Temperature fluctuations between the two relevant data points can be neglected as there are usually only several seconds between the measurements.

The plotting of the data of the sensor institute against the data of the sensor vendor helps to visualize the differences of the IV behaviours. The maximum allowed slope limit of 1.6 is illustrated by the two red lines which divide the plot into four regions. In the bottom left region the sensors fulfil the quality criteria at both stages. In the top left region they were only qualified at the sensor vendor, in the bottom right region only at the sensor institute. The top right region marks sensors which fail the quality criteria at both stages.

In Figure 6.11 the wafer batches are differentiated by the same colours as in Figure 6.10. In the slope migration plot a similar behaviour is visible as in the operation current migration plot. Most of the points are grouped close to the diagonal. With higher slope values the fluctuations between the two stages are also increased. This is understandable as a slope which is higher than 1.4 is already an indication for an initiating breakdown. Within a breakdown the increasing current can cause a local self heating of the sensor which again leads to an increase of the current. The effect is thus self-reinforcing. The IV slope of a breakdown can therefore be unstable and is unlikely to reproduce in other measurements.

Furthermore, a larger fraction of points have a slope between 1.05 and 1.25 at the sensor institute which was significantly higher at the sensor vendor. The sensors originate predominantly from the batches five and six. These deviations correlate to the decreased operation current seen in Figure 6.10. This observation supports the assumption that the corresponding IV characteristics show such a resistive behaviour as seen in Figure 6.9 b) and not a higher absolute level of the current. Because the data of the sensor vendor shows such a physically untypical characteristics it has to be assumed that changes in the measurement method or setup took place. Another explanation

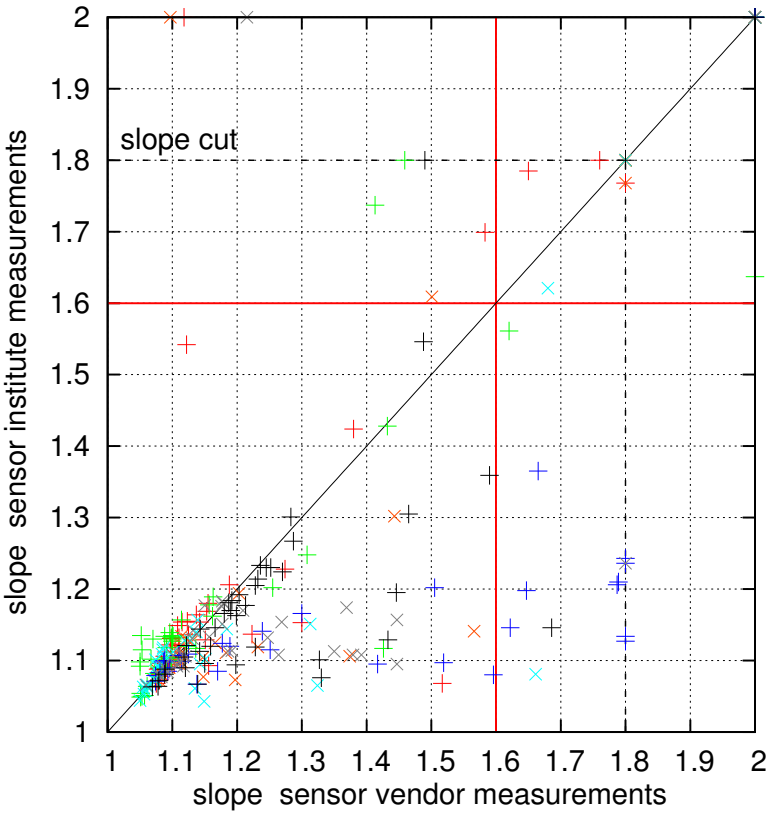


Figure 6.11.: IV slope migration plot of the IBL production comparing the data from the sensor vendor with the measurements of the sensor institute. The maximum slope is set to 1.8 to comprise also higher values. This limit is marked by the two dashed black lines. The maximum allowed slope limit of 1.6 is illustrated by the two red lines. The slope values of 2.0 are set as a default for those sensors which feature a breakdown already before the operation voltage is reached. 21 points are overlayed in the top right corner.

cannot be found as such resistive behaviours in the data of the sensor vendor only occurred interim. Following measurements again yielded to typical characteristics.

The few sporadic points lying around 1.1 to 1.2 for the measurement at the sensor vendor and significantly higher for the measurement at the sensor institute represent such cases as sensor No. 02 in Figure 6.9 a). They show a typical IV characteristic before and an early breakdown afterwards. This is an indication that they were damaged during the transport or the handling between the two measurements. Such cases are inevitable and can only tried to keep to a minimum by handling the sensors as carefully as possible.

The kind of presentation in Figure 6.11 allows easily to evaluate which sensors fulfil the quality criteria. The corresponding points therefore have to stay below the limit of 1.6 . Due to the plotting of sensor institute data against sensor vendor data the improvements and degradations are visible. There are 225 sensors out of the 279 which are functional at both stages. 13 sensors changed from category red to green, 8 sensors from green to red. The remaining 33 sensors fail the quality criteria before as well as afterwards.

Despite the relevant number of sensors showing deviations in the IV characteristic between sensor vendor and sensor institute it is decided not to extend the cross check measurements. As discussed in the previous Section Section 6.3.4 a systematic re-measurement of all sensors would cause an immense and unnecessary effort in time and manpower. Furthermore, it is demanded to pass the wafers on to the bump bond vendor without any delays. Besides, the statistic show that the sensor performance is rather improved than it is degraded. This means a sensor of the green category would be rejected more often than a sensor of the red category would be accepted. This results in turn that more wafers are rejected than accepted by mistake. However the

absolute number of wrongly chosen wafers is negligible in comparison to the amount of produced wafers. Such fluctuations are incorporated by the over production.

Second Quality Control at the Sensor Institute

The most meaningful quality control of the IBL sensors is the IV characteristic after the UBM and dicing at the bump bond vendor. It is performed on every DCS at the sensor institute after labelling the scratch marks. It was seen for sensors of former prototype productions that the IV characteristic can be influenced by the dicing step significantly. Good sensors can deteriorate but bad sensors can improve as well and become operable again. For this reason it was decided to remeasure all DCS, even those which failed the quality criteria before the UBM and dicing.

The IV curves of the DCS of two exemplary wafers are seen in Figure 6.12. The data of the sensor vendor is plotted in black, of the sensor institute cross checks in red and the data taken after the UBM and dicing step in green. Each DCS is represented by one symbol.

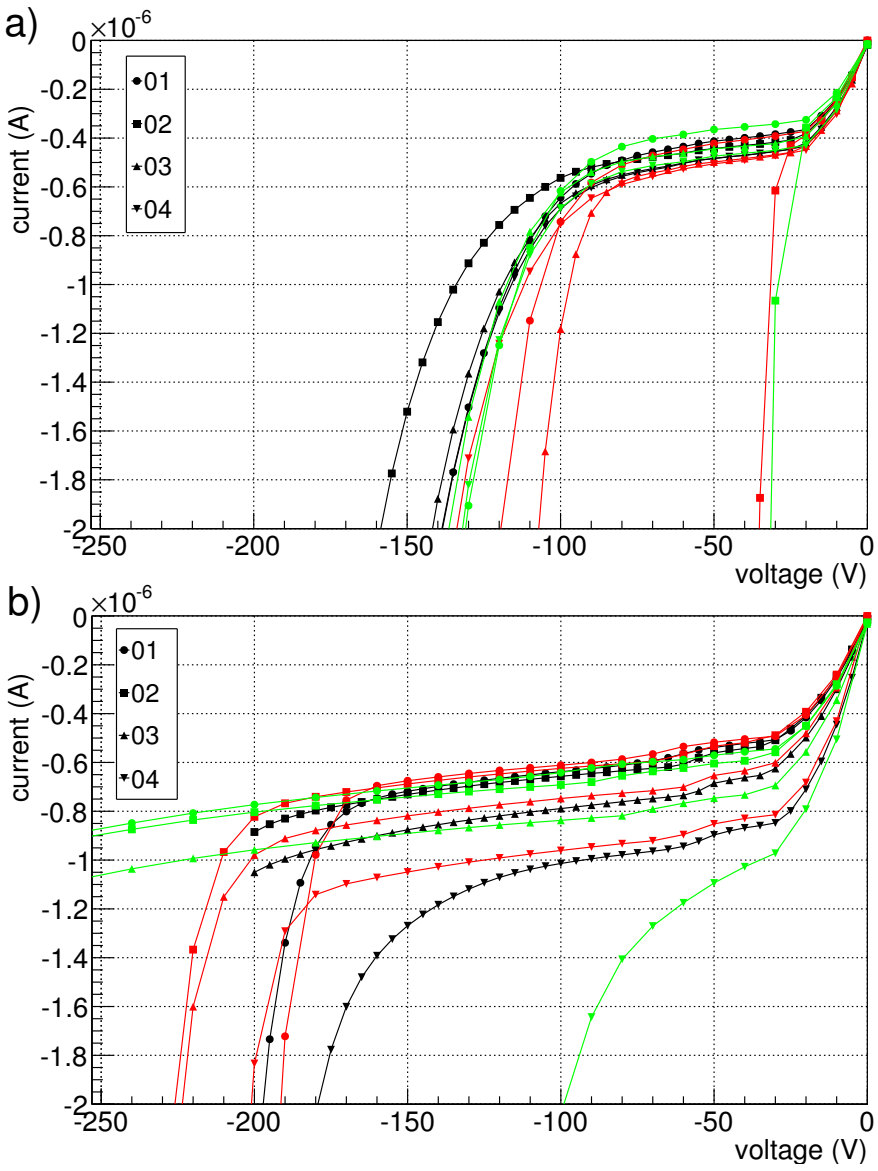


Figure 6.12.: Example of IV characteristics of the DCS of two wafers. One symbol stands for the same sensor number. Black symbols represent data from the sensor vendor, red ones from the sensor institute before UBM, green ones from the sensor institute after UBM and dicing. The wafer in a) shows a comparable behaviour of all sensors. The wafer in b) features deviations between the data sets. After the dicing step the breakdown voltage of sensor No. 04 is significantly decreased whilst the other three sensors rather improve.

The sensors in example Figure 6.12 a) show a comparable behaviour in all steps. Only the breakdown voltage of sensor No. 02 decreased comparing the data of the sensors vendor and the sensor institute. After the dicing step it stays the same. The other three sensors as well feature the same current level, breakdown voltage and curvature. The example in Figure 6.12 b) shows sensors with changes in the IV characteristic. All sensors had a similar behaviour before the UBM and dicing step with a breakdown around 200 V. Afterwards the breakdown voltage of sensor No. 04 is significantly decreased. It was apparently damaged by the mechanical stress or the handling during the dicing step. The other three sensors rather improved. It is no breakdown visible anymore up to the maximum measured voltage of 300 V. This improvement does not influence the sensor performance as the quality criteria are only relevant up to the operation voltage of 80 V. Increasing breakdown voltages beyond this limit are not incorporated in the quality control statistics. Anyhow it is remarkable as a significant amount of sensors feature such an improved behaviour. A definite reason for these changes is not obvious. The breakdown could initially be caused by a microscopic tension in the sensor bulk which is released by the dicing step.

Figure 6.13 shows a migration plot in which the operation current after the dicing is plotted against those before the UBM. The data of sensors which have been cross checked at the sensor institute before the UBM step is used to replace the data of the sensor vendor. Thus, the values on the abscissa is a combination of both data sets in order to compare the most recent and meaningful data. The plot includes all 437 sensors which are extant after the dicing step. The sensor batches are again differentiated by the same colours as in Figure 6.10. The four different sensor numbers are additionally represented by different kinds of symbols.

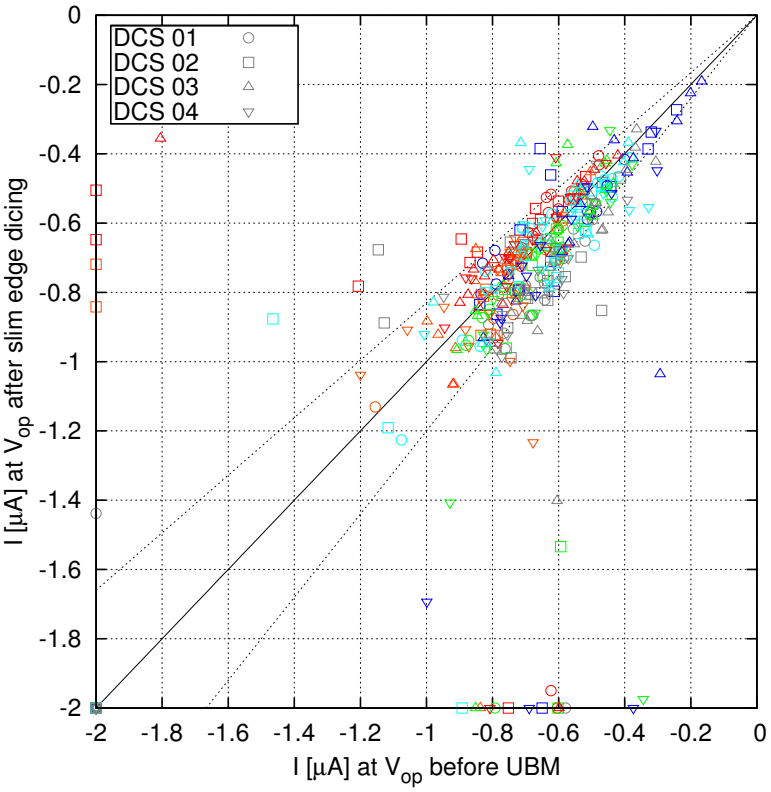


Figure 6.13.: Operation current migration plot of the IBL production comparing the data taken before the UBM with that after the slim edge dicing. The data before the UBM is a combination of the measurements of the sensor vendor and the sensor institute. It includes all 437 sensors which are extant after the dicing step. The batches are displayed by different colours. The four different sensor numbers are additionally represented by different kinds of symbols. 33 points are overlayed in the bottom left corner.

It can be seen that most of the points are located on the diagonal line or within the 20% tolerance region. Most of the remaining points are either close to the 20% tolerance region or beyond the 2 μA limit. There are only some sporadic values in

between. In order to get insight in how far the IV slope between depletion and operation voltage changes, the slopes of the same data sets are plotted in a migration plot in Figure 6.14. The cutting criterion and default value for the sensors with high slopes or early breakdown voltages is the same as for Figure 6.11.

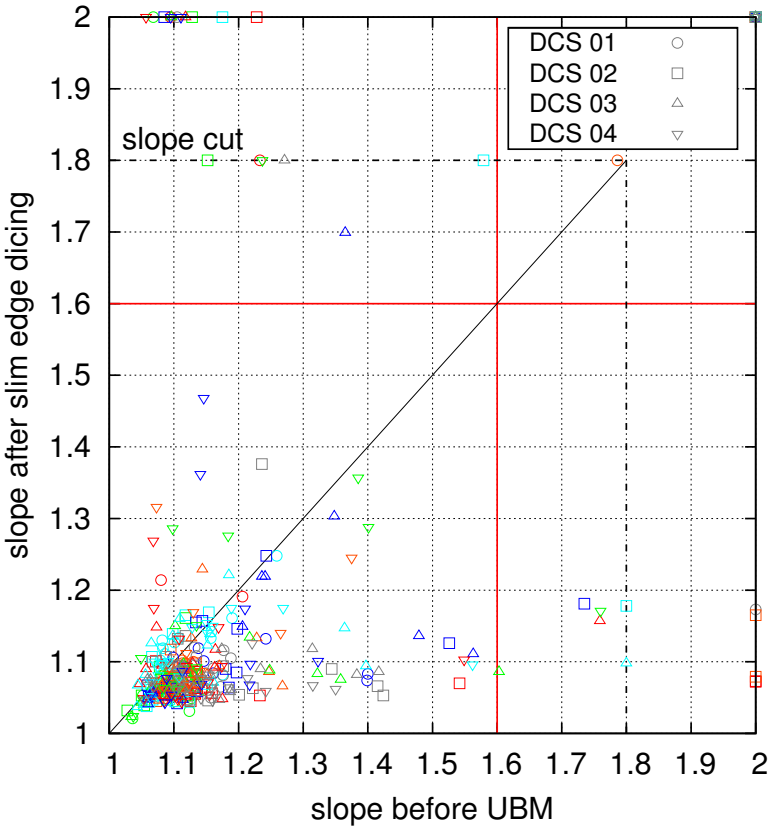


Figure 6.14.: IV slope migration plot of the IBL production comparing the data taken before the UBM with that after the slim edge dicing. The data before the UBM is a combination of the measurements of the sensor vendor and the sensor institute. It includes all 437 sensors which are extant after the dicing step. The cutting criterion and default value for the sensors with high slopes or early breakdown voltages is the same as for Figure 6.11. The colour and shape encoding of the symbols is the same as in Figure 6.13. 33 points are overlayed in the top right corner.

Most of the points are grouped around the diagonal at small slopes between 1.0 and 1.25. In consideration of tolerable small deviations it can be seen that the slope of most sensors stays the same. The improvements and degradations between the measurements before UBM and after the dicing step can be read off the quadrant in which the point is located in the plot. There are 373 sensors out of the 437 which are functional at both stages. 11 sensors changed from category red to green, 19 sensors from green to red. The remaining 34 sensors fail the quality criteria before as well as afterwards.

Systematic groupings are not noticeable, neither correlated with the batch nor with the sensor number. The only notable feature is a larger fraction of points having a slope between 1.05 and 1.15 after the dicing step which was significantly higher before UBM. The sensors originate predominantly from the batches five and six. The reason for these deviations appear to be the same as for the decreased slope seen in Figure 6.11. This effect as well occurred mainly for the same batches five and six. It is supposable that these sensors show the same resistive behaviour at the sensor vendor as those seen in the example in Figure 6.9 b). Because they have not been cross checked before the UBM step at the sensor institute the increased values are visible on the abscissa.

Taking this fact into account it can be determined that the sensor IV characteristics is by trend rather degraded than improved. This is comprehensible as the dicing step implicates considerable mechanical stress. The 19 sensors in the upper left quadrant are a clear indication for a damage during the dicing, see Figure 6.12 b). Such a sensor loss is inevitable and can only tried to keep to a minimum by handling the sensors

as carefully as possible. Experiences concerning the dicing have already been made during the prototype production, see Section 5.4.2. The most meaningful improvement was achieved by dicing the sensors upside down compared to the conventional way. A simple reduction of the cutting speed of the dicing blade did not improve the performance. Further parameters which could optimise the conventional diamond saw dicing technique are not available without a significant effort and systematic investigations. An alternative to the diamond saw dicing is discussed later in Section 7.1.

6.3.6. Summary of the Quality Control

A detailed quality assurance overview of all IBL DCS can be found in Table 6.5. It is divided into the first part of the wafer production at the sensor vendor and the second part including the UBM and dicing steps.

Table 6.5.: Quality assurance overview of all IBL DCS during the process flow. In the 'before UBM and dicing' columns (marked with *) all sensors are already omitted which are broken during the UBM and dicing process or during the transport.

		sensor vendor			UBM and dicing process									
					before*			after			before and after			
		fulfil QC			fulfil QC			fulfil QC			fulfil QC		change	
	batch	yes	no	sum	yes	no	sum	yes	no	sum	yes	no	−	+
b1	310892	68	12	80	62	12	74	62	12	74	58	8	4	4
b2	310893	76	12	88	66	11	77	66	11	77	64	9	2	2
b3	310894	64	8	72	58	6	64	55	9	64	53	4	5	2
b4	312059	70	10	80	68	10	78	69	9	78	67	8	1	2
b5	312060	62	6	68	54	6	60	50	10	60	48	4	6	2
b6	312061	83	5	88	79	5	84	77	7	84	76	4	3	1
b7	313431	47	1	48										
b8	313432	42	2	44										
b9	313512	32	0	32										
	sum													
	b1 - 9	544	56	600										
	b1 - 6	423	53	476	387	50	437	379	58	437	366	37	21	13

The 'sensor vendor' column is a combination of data from the sensor vendor and the cross check measurements at the sensor institute. The complete production yield considering all 150 accepted wafers is 90.7% for the DCS. This is equivalent to 3.6 good DCS per wafer on average. This result is exceedingly satisfactory as the estimate number was 3 good DCS per wafer. The yield is by trend continuously increasing with the batch numbers. One reason for that could be the gaining in experience and routine during the processes. The outstanding yield of the backup batches results from the fact that more wafers have been produced than being ordered. The best wafers have been chosen for acceptance.

The 'UBM and dicing process' columns are only relevant for the main batches 1 to 6. In principle these informations are already incorporated in the slope migration plot in

Figure 6.14. In the columns before UBM and dicing, all sensors are already omitted which are broken afterwards during the process steps at the bump bond vendor or during the transport. These cases are taken out in order not to falsify the statistics and thus the sensor yield. A loss of a sensor due to such exterior factors has to be disentangled from changes of its IV characteristics. In comparison to the data in Figure 6.14 the columns after UBM and dicing additionally incorporate the few cases in which a sensor fulfils the quality criteria but is anyhow degraded to the red category. This can occur if the sensor is operated at 80 V in a beginning break down which is not comprised by the quality criteria or if the visual inspection reveals a serious damage on the pixel side.

Out of the 437 DCS which are extant after the UBM and dicing process, 379 are qualified and can be used for the bump bonding process. In order to be able to calculate a yield of this post process, these numbers cannot be used as several sensors have already failed the quality criteria before. In the last four columns of Table 6.5 the sensors are categorized depending on whether their quality status stays the same or changes from green to red (−) or from red to green (+) between the stages before and after the processes. These columns correspond to the four quadrants marked in Figure 6.14.

For a reasonable yield declaration the 37 sensors which do not fulfil the quality criteria before and afterwards are disregarded as a bad sensor cannot expected to improve its behaviour. If only those sensors are regarded which fulfil the quality criteria before, 366 out of 387 are remaining which is equivalent to a yield of 94.6%. Alternatively it makes sense to include additionally the 13 sensors which improve from category red to green. This would result in 379 good sensors out of 400 which leads to a nearly similar yield of 94.8%. If those sensors are included which are broken during the UBM and dicing steps, 379 green sensors remain out of 423 which are green before. This is equal to 89.6%.

The overall yield for the production and post processing of the main batches 1 to 6 is 379 out of 476 or 79.6%. For an IBL layout with 100% planar sensors one would require 224 DCS. For this scenario the minimal yield of the module and stave production which is still tolerable is 59.1%. In case of an IBL layout with 75% planar sensors which is equal to a number of 168 this value must not fall below 44.3%. Table 6.6 shows an overview of these values. If the loss during the module and stave production increases to an extent that a sufficient number of qualified modules is not guaranteed anymore, the post processing of the backup batches would have to be initiated. If the determined post process yield of $\sim 95\%$ is applied to all batches, one would expect to have ~ 493 good sensors available for the module and stave production. The minimal tolerable yields would then be 45.4% and 34.1% respectively.

The discussed numbers confirm that the planar IBL sensor production show exceedingly well results. The yields of the wafer production as well as of the post process and dicing are convincing and should guarantee an adequate overrun of good sensors. If severe unpredictable complications occur during the module and stave production, it is still possible to counteract by post process the 31 wafers of the backup batches. One would expect more than twice as much good sensors as required for a 100% and almost three times as much as required for a 75% planar IBL scenario.

The quality criteria do not comprise the breakdown voltages of the sensors. The only criterion which is determined is whether they can be operated up to 80 V. For planar

Table 6.6.: Required and available amounts of diced IBL DCS dependent on the fraction of planar sensors in IBL and whether the backup batches are comprised or not. The number of good DCS for all batches (*) is partially extrapolated using the determined post process yield.

fraction of planar sensors in IBL	DCS required	batches included	good DCS	overrun of DCS	minimal tolerable yield of module and stave production [%]
100%	224	b1 - 6	379	155	59.1
75%	168	b1 - 6	379	211	44.3
100%	224	b1 - 9	493*	269	45.4
75%	168	b1 - 9	493*	325	34.1

n^+-in-n sensors of the next generation which are conceivable for future ATLAS pixel upgrades it is supposably advantageous to increase the operation voltage. As seen in Section 5.5.3 the edge efficiency of pixels opposite to the guard rings is depending on the bias voltage. If a larger pixel overlap is desirable in order to decrease the sensors inactive fraction, the designated operation voltage has to be increased as well. Otherwise the larger pixel shift would not yield to a higher edge efficiency.

If a higher operation voltage is demanded of the sensors with the current IBL design, the production yield is not expected to be significantly reduced. Figure 6.15 shows the distribution of $V_{2\mu A}$, the voltage at which the current limit of 2 μA is exceeded, for all IBL sensors after the dicing step. As a lot of sensors are only measured up to 300 V this value is set as a maximum although several sensors have even higher values. This means the leftmost bin represents values of 275 V and higher.

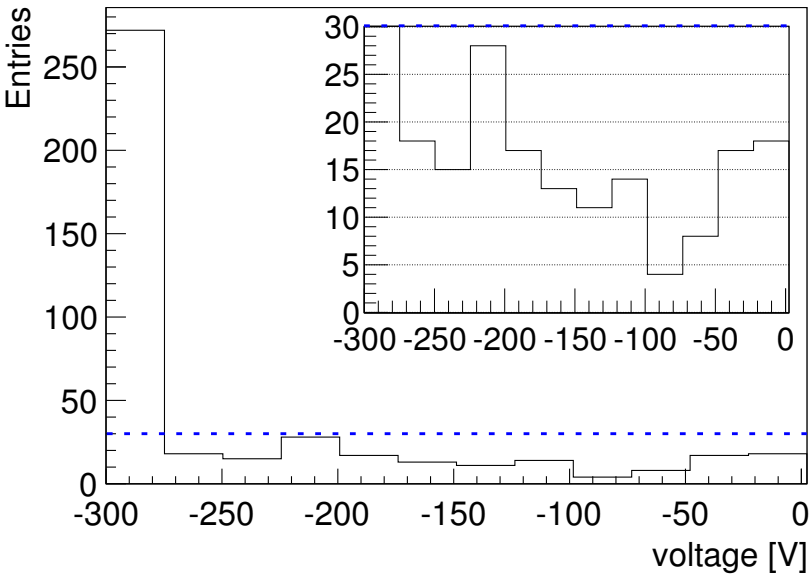


Figure 6.15.: Distribution of $V_{2\mu A}$ of all 435 IBL DCS which are measured after the dicing step. The leftmost bin represents values of 275 V and higher. The small histogram is a zoom to entries below 30.

This voltage is not equal to the breakdown voltage but it gives an upper limit of how far the operation voltage can be increased. Depending on the curvature of the IV characteristic, the maximum operation voltage is at most 50 V below this value. It is obvious that most of the voltages at 2 μA are significantly higher than the operation

voltage of 80 V. More than half of the values are comprised in the leftmost bin with more than 280 V.

If all sensors are omitted which fulfil $V_{2\mu A} \leq 110\,\mathrm{V}$, it remain 377 sensors or around 87%. This number is in the order of those which fulfil the quality criteria. If an operation voltage increase of 50 V is requested, the number of good sensors would shrink to 353. The resulting decrease of the sensor yield is acceptable. If the cut is set to $V_{2\mu A} \leq 210\,\mathrm{V}$, it still remain 321 sensors or around 74%. This yield decrease of 13% compared to the cut at 110 V is rather appreciable but it still would have to be deliberate about whether it is justifiable.

These estimations can help to plan optimizations for a new sensor edge design for future applications. Proposals for that can be found in Section 7.2.

7. Future ATLAS Pixel Upgrades

7.1. Alternative Dicing Methods

The experiences with the prototype and IBL productions showed that the conventional diamond saw dicing can be maintained for sensors with the IBL slim edge design. The cracks at the cutting edge did only exceed the 100 μm safety margin in some single cases. If the inactive edge distance is decreasing, cracks of these dimensions as seen in Figure 6.5 c) can not be tolerated anymore. As discussed in Section 7.2.1, it is supposable that the safety margin between cutting edge and pixel matrix has to shrink to the order of 50 μm.

One alternative technique to the diamond saw dicing is the laser dicing which is already often used in industry for separation of silicon wafers. Trials have been made with FE-I4 sized sensors of the IBL production which have been laser diced at IWS[1]. The dicing positions are the same as for the conventional diced sensors to retain the comparability. The laser dicing process consists of two steps. Firstly, the laser runs along the dicing

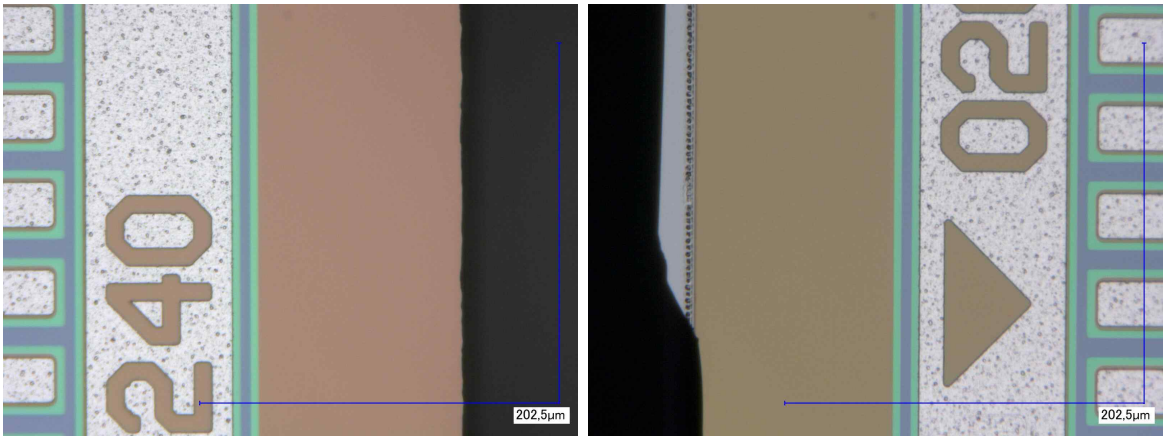


Figure 7.1.: Light microscope pictures of the n-side of the sensor cutting edge after the laser dicing. After the cleaving, the cutting edge mostly exhibit a very good quality without any deteriorations (left). In only a few cases the cleaving line does not follow exactly the laser scribing line (right). However these cases only lead to cracks with dimensions up to the order of 30 μm. The largest part of the safety margin is not affected. In the right picture the bullet holes of the laser can be seen next to the cutting edge.

street at which it penetrates only into a small fraction of the bulk. This process is equal to a scribing step. Afterwards, the sensors are cleaved along this scribing line.

[1] Fraunhofer Institut für Werkstoff- und Strahltechnik, Dresden, Germany, http://www.iws.fraunhofer.de/

Figure 7.1 shows two exemplary microscope pictures of the cutting edge. In most cases the cleaving line follows exactly the scribing line which results in a straight cutting edge in good quality (left picture). In only a few cases the cleaving line does not follow exactly the laser scribing line which causes cracks in the order of 30 μm (right picture). Compared to the cracks caused by the diamond dicing saw, these damages are significantly smaller. They can be tolerated in consideration of required safety margins of 50 μm.

Apart from the visual inspection, IV measurements are performed to monitor how the electrical behaviour changes. Taking into account the uncertainties due to the small statistic, the dicing yield is comparable with that of the IBL production. The laser dicing technique thus represents a serious alternative to the conventional diamond saw dicing for future slim edge sensors. However, continuative trials with higher statistics have to be conducted to confirm the present results.

7.2. Sensor Design Improvements

For future upgrades of the ATLAS pixel detector the different sensor technologies are facing several challenges. The massive increase of radiation exposure especially in the inner layers with fluences up to $2 \cdot 10^{16} \mathrm{n}_{\mathrm{eq}}/\mathrm{cm}^2$ will necessitate radiation hard sensors. The charge loss will have to be reduced to a minimum. For planar n^+-in-n sensors one possibility is to improve the design in order to counteract the decrease of collected charge. Besides the optimization of the pixel implantations it is a crucial question how to deal with the bias grid design.

A further point is the inactive edge of the sensors as the modules will presumably be mounted like in the IBL in a flat way on the staves without any shingling. The IBL specification of 450 μm per side of a FE-I4 sized DCS can be regarded as an extremely tolerant value. It is supposable that for sensors of the next generation this dimension is going to be scaled down to a minimum. Sensors with so called active edges represent a possibility to comply with these requirements. The following Section 7.2.1 describes imaginable edge design improvements which can or will already be implemented in the future by using the conventional technology.

7.2.1. Edge Design Improvements

On the basis of the results which are seen for the test beam edge efficiencies (Section 5.5.4) and the IBL sensor production (Section 6.3.6), it is possible to give proposals for future optimized edge designs for planar n^+-in-n sensors. It is assumed that a FE-I4 like read-out chip is used. Figure 7.2 presents different approaches. All designs are aligned to the end of the high voltage pads. The green dashed lines mark the end of the Front-End chips which is supposed to have a minimum distance of 200 μm from the sensor cutting edge.

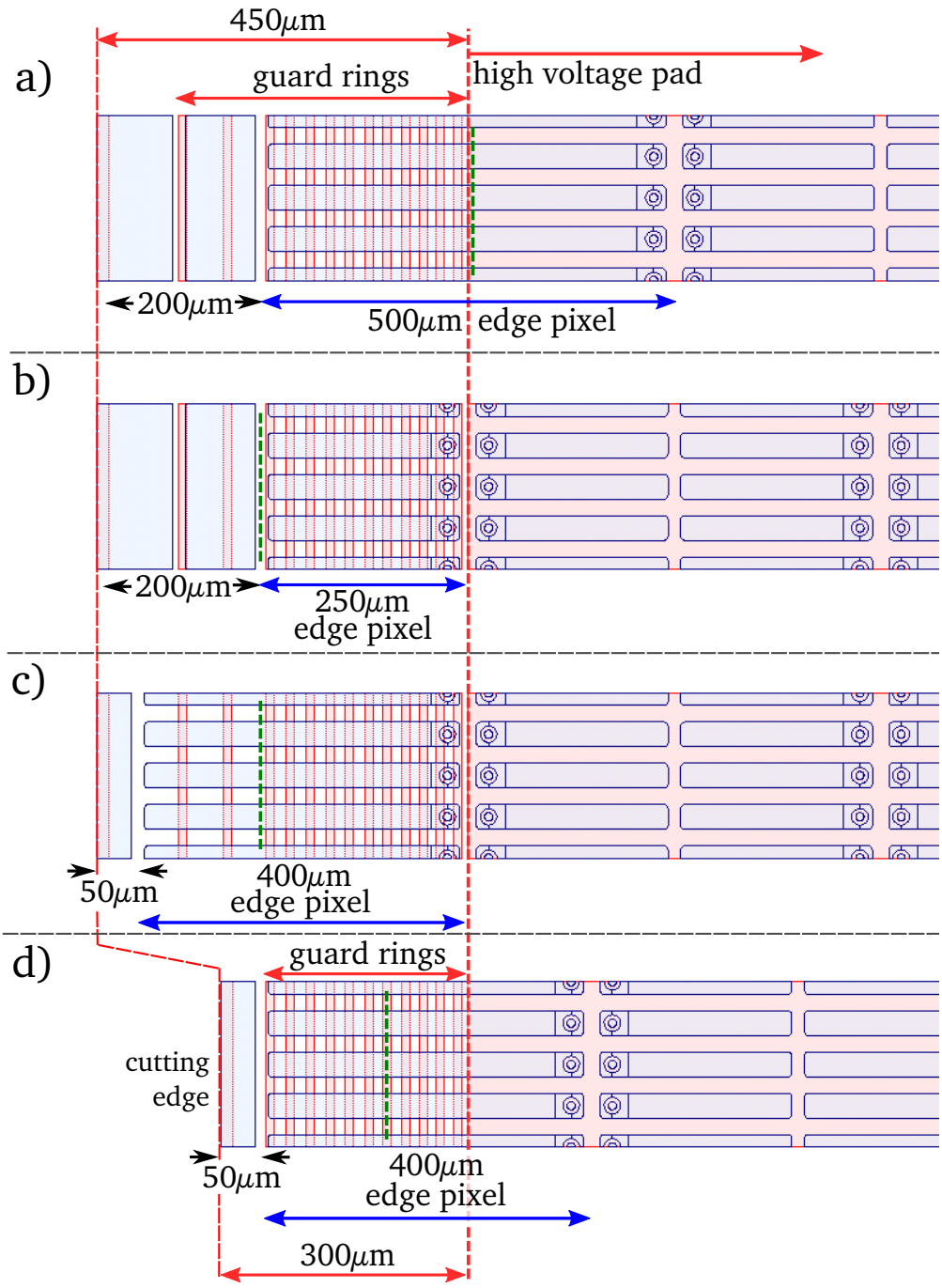


Figure 7.2.: Possible slim edge designs for planar n^+-in-n pixel sensors of the next generation compared to the IBL design a). The n^+-implantation is seen in blue, the p^+-implantation in red. The green dashed lines mark the end of the Front-End chips. For a detailed description see text.

Design a) is the current IBL layout which features 500 μm long edge pixels overlapping the high voltage pad by 250 μm. In the design b) these long pixels are split into two normal 250 μm long ones. The last pixel column is thus lying completely opposite to the guard rings. This variation will not change the edge efficiency but it implicates a significantly reduced capacitance in the edge pixels. This is advantageous for highly irradiated sensors which feature a considerable higher noise in the long pixels. Especially if intended 2×2 multi chip sensors (so-called quad sensors) require additional

ganged pixels this can help a lot. Long ganged pixels featuring four times the size of normal pixels can thus be avoided. This design is already used for quad sensors on a new planar wafer production which is submitted in 2013.

In order to further reduce the inactive edge, there are two possibilities. In design c) the normal sized edge pixels of design b) are again stretched further into the inactive area by 150 μm. The outer guard and the bias grid ring have to shrink respectively to $\sim 20\,\mu$m or alternatively merge to one 50 μm narrow n^+-implantation (as seen in the sketch) which collects the edge leakage currents. Which variant is more reasonable would have to be investigated. As the p-side is the same as for the IBL design, a different sensor production yield is not expected. Because the pixel overlap is increased to 400 μm, it is supposable that a certain part of the end of the pixel will stay inactive if the operation voltage of 80 V is kept. In order to benefit from the enlarged pixel length, the operation voltage will likely have to be increased. This will in turn have influence on the sensor production yield. In Section 6.3.6 it was mentioned that an increase of the operation voltage of 100 V can reduce the overall yield in the order of 13%.

A different approach to reduce the sensors inactive fraction is seen in Figure 7.2 d). The distance between high voltage pad and cutting edge is shrunk to 300 μm. The number of guard rings hence has to be reduced to 11. The pixel overlap with respect to the high voltage pad is 250 μm as it is for the IBL design. Because of the minimal distance between read-out chip and sensor cutting edge, the pixel length again has to be stretched to 400 μm. Due to the smaller safety margin a reduced breakdown voltage is expected. Therefore, the operation voltage of 80 V can be maintained as the pixels with an overlap of 250 μm should be completely active.

However for both possibilities c) and d) a compromise would have to be found between the efficiency of the edge pixels and the sensor production yield. Both quantities are adjustable by the defined operation voltage.

7.2.2. Modifications to Pixel Implantations

The current pixel design (seen in Figure 7.3 V0) which has been adopted from the ATLAS pixel production is laid out to minimize any field strength maxima. The implantation body is one large area with rounded corners. Investigations of other highly irradiated planar sensors [Cas10] showed evidence for a charge amplification, i.e. more charge was collected than predicted with the trapping model. This effect is supposed to increase with larger electric fields. Besides the increase of the bias voltage, one option is to reduce the sensor bulk thickness as discussed in Section 5.3.3. An alternative approach is to force field strength maxima by modifying the shape of the pixel implantations. Figure 7.3 shows different versions (V1 - V6) of FE-I4 sized pixel cells which enable to investigate this behaviour. In the standard pixel layout V0, the electric field lines run homogeniously to the large, single electrode. In the other geometries, they are bent and thus focused to smaller regions due to the divided or narrowed implantations.

In the version V1 the standard implantation is divided into four segments of comparable size. The moderated p-spray profile is maintained also between each segment. The versions V2 and V3 feature further subdivisions in which the moderated p-spray profile is not implemented due to the reduced space. Version V4 is the same as V1 with the

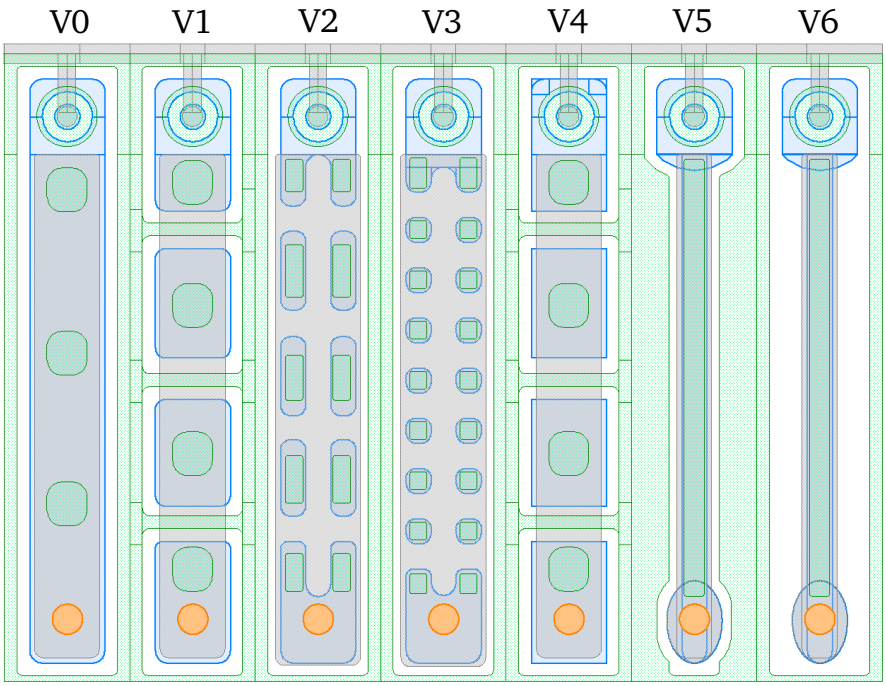


Figure 7.3.: Different versions of pixel implantation shapes to investigate in how far the electric field can be increased to collect more charge in highly irradiated sensors. V0 is the standard pixel. The n^+-implantation is seen in blue, the metal in grey, the nitride openings in green and the bump pad opening in orange.

only difference that the implantations do not have rounded but rectangular corners. In version V5 and V6 the standard pixel implant is narrowed by the factor three. The difference between the two versions is the profile of the moderated p-spray. In V5 the width of the high dose, indicated by the green nitride opening, is significantly larger than in V6.

Especially the stepwise increasing subdivision between the versions V0, V1, V2 and V3 should clarify if this approach can contribute to cause higher electric fields. In order to have a direct comparison between the performance of the different pixel versions, all of them are placed on one FE-I4 sized single chip sensor. Always 10 columns of the sensor feature the same version of pixel implantation shape, see Figure 7.4. The

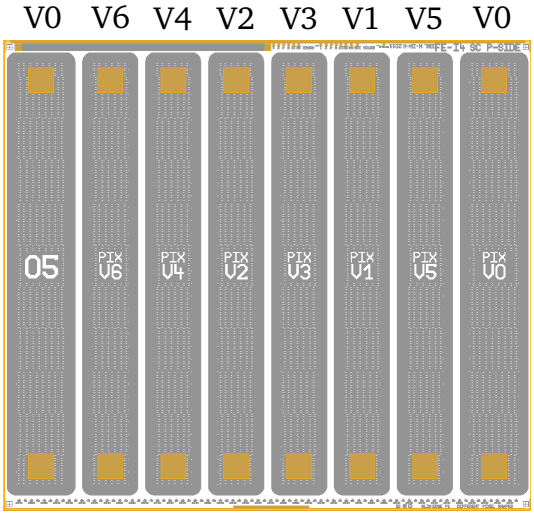


Figure 7.4.: Sketch of the p-side of the FE-I4 sized sensors featuring the differently shaped pixel implantations. The pixel versions are the same as in Figure 7.3. The p-side is divided into 8 separate high voltage pads, each surrounded by 13 guard rings. Each matrix with a different pixel version can thus be depleted separately. The metal is seen in grey, the passivation openings in orange.

standard version V0 is placed two times. Because some of the implantation designs are quite unconventional, it can not be taken for granted that they work at all. In order to avoid that the complete sensor is getting inoperative, the p-side is as well divided into 8 separate high voltage pads, each surrounded by 13 guard rings. Each matrix

with a different pixel version can thus be depleted separately. If any pixel version causes a problem, the respective part can stay inactive. This means that this structure represents basically 8 single sensors which can be read out by one FE-I4 chip. The sensor was produced on the IBL production wafer (No.05).

7.2.3. Modifications to the Bias Grid Design

Investigations of planar sensors with the current n^+-in-n pixel design revealed that a significant fraction of the charge loss takes place in the region of the bias grid. The subpixel resolved data shows that for the irradiated sensors, the charge loss below the bias grid rail can even exceed that in the bias dot implantations. The bias dots will always cause a loss of a certain amount of charge. As long as the conventional bias grid technique is maintained, this effect is inevitable. The loss underneath the metal conductor is not understood in detail up to now. One explanation can be that the metal conductor which is also on ground potential bends the field lines. It thus can cause a delay of the charge carrier which therefore can not be collected in time. A detailed discussion on this topic can be found in [Tro12].

The effect of the bias grid rail on the charge loss is even amplified as it runs at the edge of the short pixel side. At the edge of the pixel cell the charge sharing probability is significantly increased which likewise causes a charge loss. The bias grid rail is thus located at an unfavourable position. With a modification in the design the two sources of charge loss can be disentangled. This can supposably lead to an overall increase of the hit efficiency. The probability that the remaining amount of collected charge drops below the threshold is diminishing.

Figure 7.5 shows three modified bias grid versions in which this approach is implemented. The version V0 is the current design where the bias grid rail is running on the short pixel edge. In the version V1 there are two bias rails which run directly above the bias dots. The transverse conductors could be omitted so that no metal is running along the pixel edge. The bias rail is however still quite close to the end of the pixel. In the corner of the pixel cell, the charge sharing effect is understandably even more dominant. In the arrangement in V2 it is therefore tried to maximize the distance between the bias rail and the end of the pixel by shifting it to the centre of the pixels. The connection conductors to the bias dots are lying on top of the pixel implantations where they should have no influence on the collected charge. In the version V3 the bias dots are as well shifted to the centre of the pixel to maximize the distance between the end of the pixel and all sources of charge loss.

In order to have a direct comparison between the performance of the four different bias grid layouts, all of them are placed on one FE-I4 sized single chip sensor. Respectively two times 10 columns of the sensor feature the same version. The sensors are placed in a new planar wafer production which is submitted in 2013.

7.2.4. On-Sensor Temperature Resistors

Overview

For the operation of planar silicon sensors it is an important concern to have a definite knowledge about the actual bulk temperature. This applies all situations, starting from

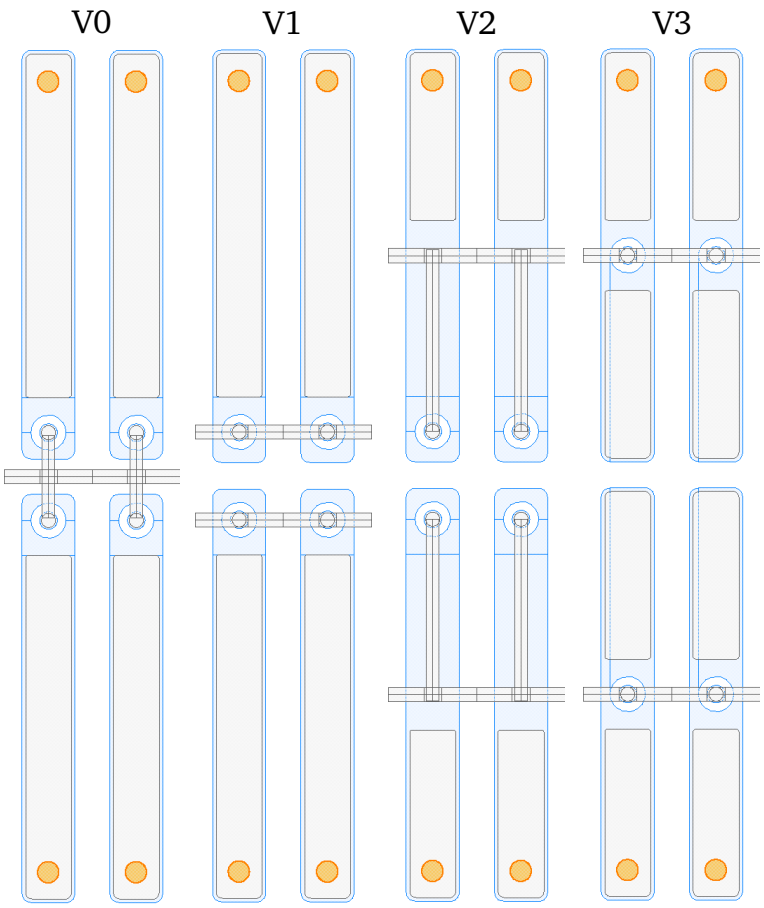


Figure 7.5.: Sketches of different bias grid layouts which should help to decrease the charge loss of irradiated assemblies. In comparison to the standard version V0, the other designs feature bias rails which are shifted from the pixel edge to the centre. With these modifications one can disentangle the charge decrease caused by the bias grid and by the increased charge sharing probability at the edges. In version V3 the bias dot is even moved to the pixel centre. The n^+-implantation is seen in blue, the metal in grey and the bump pad opening in orange.

measurements in the lab, in test beam setups to the point of operation in the complete detector. The temperature dependency of the leakage current was already discussed in Section 5.2. A further crucial aspect is the temperature dependency of the tuning of the sensor chip assembly. If an irradiated assembly is tuned at a certain temperature, the threshold as well as the ToT values are changing significantly depending on the temperature. Detailed descriptions and results can and will be found in [Lap12, Rum13, Alt14].

The present temperature monitoring is suboptimal as the probe often has no direct contact to the sensors surface. On the present ATLAS pixel modules as well as designated for the IBL modules, one NTC temperature sensor is glued on to each flex [ATL98, IBL10]. Hence between silicon and temperature probe is a non-negligible isolation. In lab or test beam measurements the temperature probe is usually glued on the aluminium carrier on which the assembly is glued. Especially for the operation of irradiated assemblies considerable differences have been observed between a temperature probe on the aluminium and another glued to the sensors surface. One reason is that the aluminium is cooled from the outside and the thermal conduction to the sensor is quite low. The heat transfer has to pass the glue between front end chip and the carrier, the chip bulk itself and the bump bonds. A gluing of a temperature probe directly on to the p-side of the sensor is challenging. It has to be guaranteed that it has direct surface contact to the sensor. Even a small gap in between can lead to a larger deviation. A removal from the sensor without damaging it is often not feasible.

An ideal temperature measurement of the sensor should take place directly on its surface or in its bulk. The first solution was easily implemented in the design of several FE-I4 sensors of the IBL wafer production. They are called On-Sensor Temperature

Resistors (OSTeR). A simple metal conductor in the shape of a meander is placed in the inactive edge region on the p-side. The conductor is $\sim 7\,\mu$m wide and in total 203 mm long. Figure 7.6 shows a sketch of the design. The metal conductors end in two $250 \times 290\,\mu$m large pads which can be contacted with a probe needle or wire bonds.

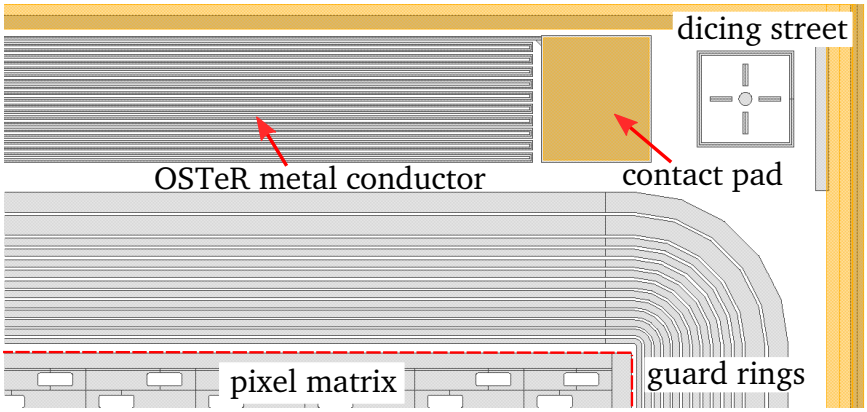


Figure 7.6.: Sketch of an OSTeR located in the corner of the p-side of an FE-I4 sized sensor. The metal is seen in grey, the passivation opening in orange.

The metal which is deposited during the wafer processing is an alloy of aluminium with 1% of silicon. For these dimensions a total resistance in the order of 700 to 800 Ω is expected at room temperature. The temperature dependency of a metal can in principle be parameterised with an exponential function as in Equation (7.1).

$$R(T) = (1 + a)^T \cdot R(0°) \tag{7.1}$$

The parameter a describes the relative change of the resistance. For the present AlSi(1%) the theoretical value is 0.00395 /K [Her13]. Within a defined range the temperature dependency can as well be parameterised by approximation with a linear function as in Equation (7.2).

$$R(T) = m \cdot T + R(0°) \tag{7.2}$$

In order to evaluate whether the OSTeRs constitute a possibility to determine the actual temperature of the sensor, one has to perform calibration measurements. They should give information about the general behaviour of the resistance. Especially the differences between different OSTeRs are significant. The performance which led to the following results was done by Sergej Schneider in the course of an internship experiment.

Measurements

For the calibration measurements, six OSTeRs are investigated which are located on diced FE-I4 single chip sensors. A picture of the setup can be found in Figure 7.7. The sensors are fixed on one aluminium block. The thermal conduction is enhanced by the use of heat transfer paste. The contact pads are wire bonded to one circuit board which serves as an adapter to the read-out cables. All sensors should have comparable temperatures as they are fixed to the same block. It is however necessary to log them as accurately as possible. For this reason each OSTeR has its own reference PT1000 temperature probe which is pressed on it via a spring. Hence it is possible to compare the measured resistance with the actual sensor temperature. The aluminium block is mounted to a heat exchanger block which is connected to a chiller. In order to be isolated from the surrounding atmosphere, the setup and the heat exchanger are

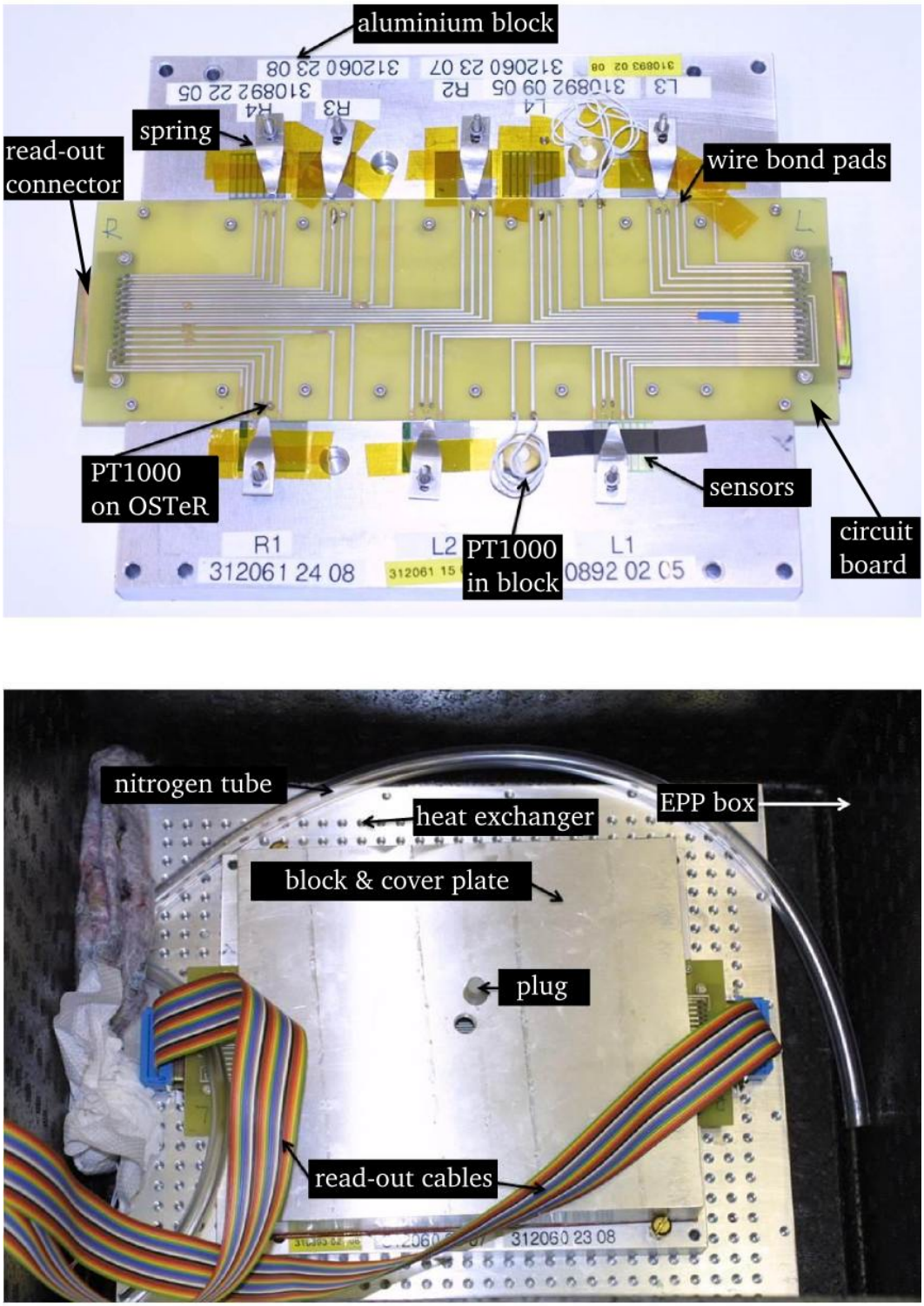


Figure 7.7.: Setup to calibrate OSTeRs on different sensors. The sensors are glued to an aluminium block and wire bonded to a circuit board which reads out the OSTeR and the PT1000 resistances (top). The block is mounted to a heat exchanger, cooled by a chiller. The sensors are protected by a cover plate. The whole setup is housed in an isolating EPP box (bottom) [Sch12].

placed in an EPP box. To prevent the sensors, the conducting paths and the wire bonds from condensed water, the top surface of the block is protected by a cover plate. Additionally the volume inside the cover plate as well as the whole box are flushed with dry nitrogen before the beginning of the measurement.

The calibration measurement consists of one run in which the temperature is changed from +35° down to −40°C in steps of 5°C. On each step the temperature stays constant for 4 hours. Figure 7.8 displays the time dependency of the six temperatures which are measured at the PT1000 probes as an example at −15°C.

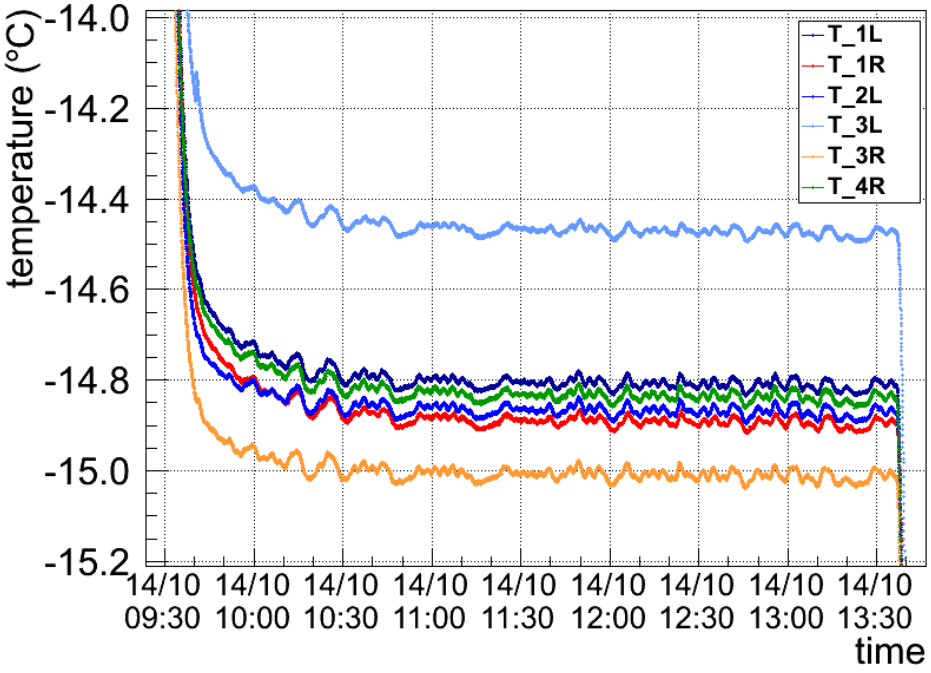


Figure 7.8.: The six temperatures measured at the PT1000 probes plotted against the time for the plateau at −15°C. After about 1.5 hours, the temperatures converge to a minimum.

It becomes apparent that it takes about 1.5 hours until the temperatures converge to a minimum. The different channels show small offsets which can be explained by differing heat connections between the sensors and the block. It is thus reasonable that each OSTeR has its own reference temperature. The fluctuations on the small scale can be regarded as synchronous between the different channels. A reason for that is the chiller which regulates its output on the basis of a reference temperature which is measured in the heat exchanger. It has however taken into account that these fluctuations are on the level of maximum 0.05°C. For these tests they can be neglected and the temperature plateaus can be regarded as sufficient constant.

One example of the time dependent resistances of the OSTeRs can be seen in Figure 7.9. The characteristic looks comparable to that of the temperature. It also takes about 1.5 hours until the resistance converges to a minimum. In the later third of the displayed time period the fluctuations are on a minimum level of 0.05 Ω.

It takes a quite long time until temperature and resistance converge to a plateau. In the first part of the time period of one temperature step it is presumable that the system is still not in a thermal equilibrium. This can cause uncorrelated deviations between the temperature measurement of the OSTeR and the PT1000. In order to eliminate any resulting unnecessary imprecisions, for the following analysis only the data of the last third of the plateau is used. The correlation between resistance and temperature of all six channels can be seen in Figure 7.10.

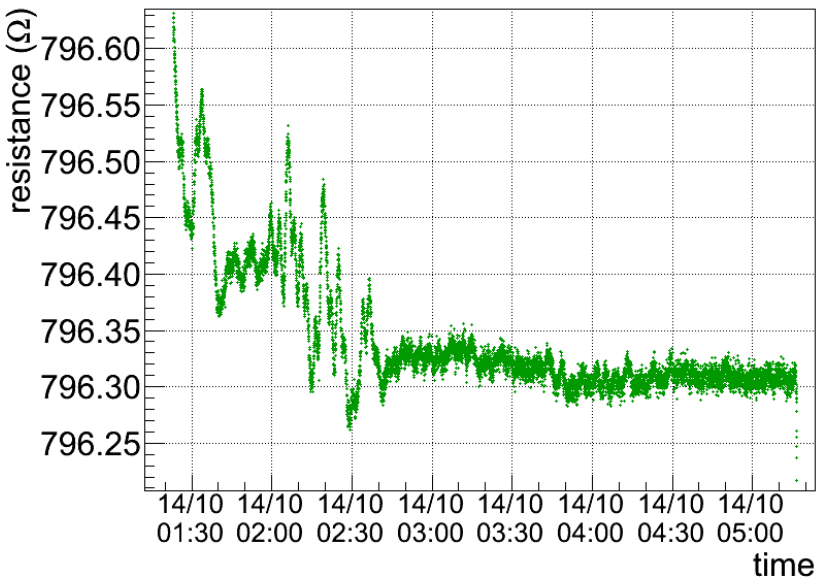


Figure 7.9.: Example of the resistance of one OSTeR plotted against the time. Analogous to the temperatures at the PT1000 probes, the resistance as well takes about 1.5 hours to converge to a minimum.

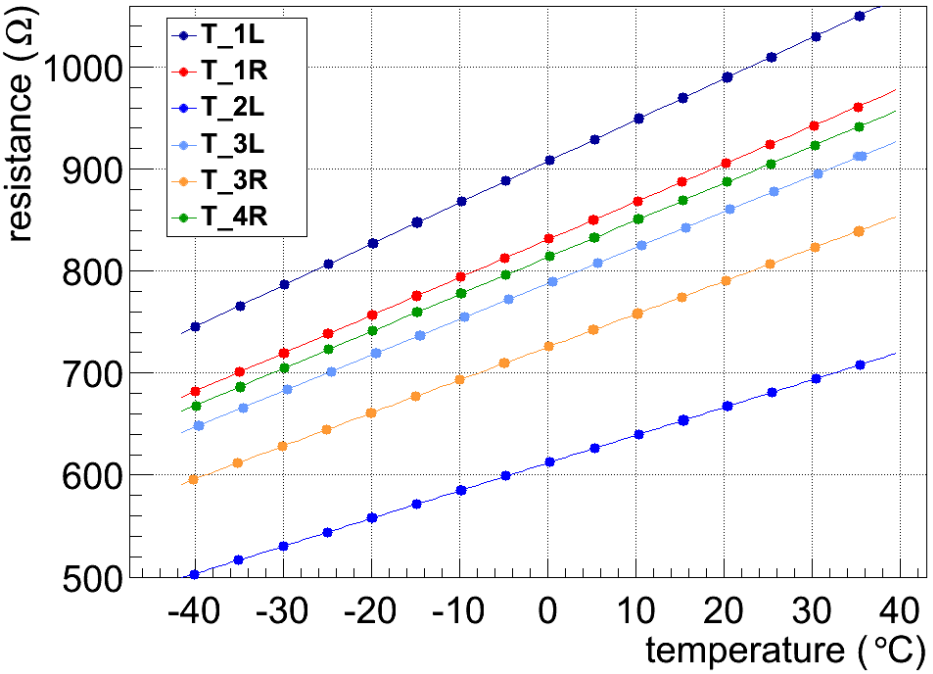


Figure 7.10.: Resistances of all six OSTeRs plotted against the respective temperatures measured at the PT1000 probes. The data result in a linear dependency which is fitted with a straight line.

The absolute resistances of the OSTeRs are highly differing. They range for example from 660 to 990 Ω at 20 °C. An exponential parametrisation like in Equation (7.1) shows significant deviations for all samples. Even including a variable offset of the temperature ($T \to T - T_0$), the fits feature a curvature which is not existent in the data. The resistances are rather lying on a straight line. Therefore, the linear approximation like in Equation (7.2) is used to fit the measurement points. The fits are as well seen in Figure 7.10. In order to see whether the two fit parameters, $R_0 = R(0°)$ and the slope m are correlated, they are plotted against each other in Figure 7.11.

The plot reveals a remarkable linear correlation between R_0 and the slope m. The fit

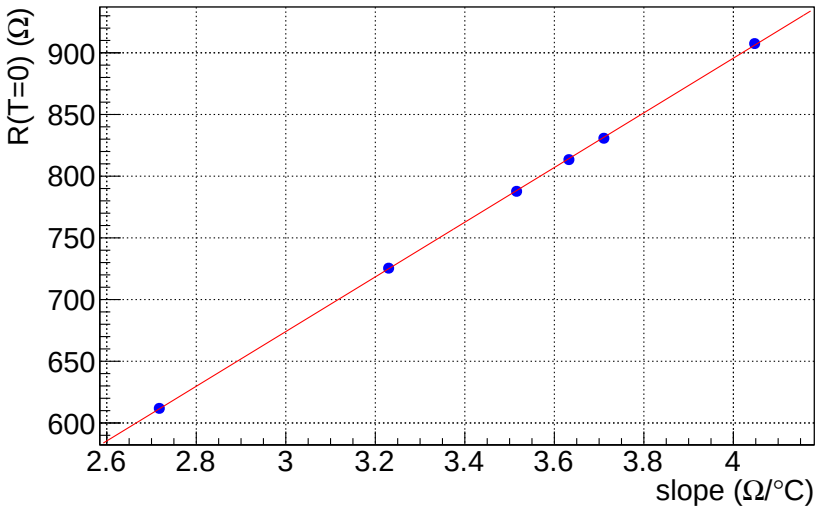


Figure 7.11.: The absolute resistance R_0 plotted against the slope m. The parameters which are determined for all six OSTeRs with Equation (7.2) feature a remarkable linear correlation. This means that the slope is rising with a rising absolute resistance.

equation results to

$$R_0 = \tau \cdot m + \rho \qquad \text{with} \tag{7.3}$$

$$\tau = (221.6 \pm 0.9)℃ \tag{7.4}$$

$$\rho = (9.3 \pm 3.3)\Omega \tag{7.5}$$

This is an important result as it confirms that the slope is rising with a rising absolute resistance. It fits to the assumption that the relative change of the electric resistivity is defined by one constant factor. In this case this factor is equal to the inverse of τ:

$$\frac{1}{\tau} = (4.52 \pm 0.02) \cdot 10^{-3}/℃ \tag{7.6}$$

This means per ℃ the resistance changes by a fixed relative value of 0.00452. It has to be pointed out that this value is in the same order of magnitude as the mentioned theoretical value for AlSi(1%) of 0.00395.

As seen for the six investigated OSTeRs the absolute resistances can highly differ. This would cause time-consuming measurements in which each sample has to be calibrated on its own. Relying on Equation (7.3) it is possible to measure one resistance value R_1 at one arbitrary constant temperature T_1 and thus calculate the slope. Rearranging Equation (7.3) and inserting $m = (R_1 - R_0)/T_1$ yields to

$$m = \frac{R_1 - \rho}{T_1 + \tau} \quad . \tag{7.7}$$

Thus, it is possible to calibrate one OSTeR with one pair of values R_1 and T_1 as it can be extrapolated to any other values R_2 and T_2. The relation

$$m = \frac{R_1 - R_2}{T_1 - T_2}$$

can be rearranged to

$$T_2 = T_1 + \frac{R_2 - R_1}{m} \tag{7.8}$$

or in combination with Equation (7.7) to

$$T_2 = T_1 + \frac{R_2 - R_1}{R_1 - \rho} \cdot (T_1 + \tau) \quad . \tag{7.9}$$

The accuracy for a calculated temperature T_2 can be estimated with the propagation of uncertainty. If the reference values R_1 and T_1 are measured a long time as done for the presented calibration test, their errors can assumed to be negligible. It is obtained for the error of T_2:

$$\sigma_{T_2} = \sqrt{\left(\frac{R_2 - R_1}{R_1 - \rho} \cdot \sigma_\tau\right)^2 + \left(\frac{-(R_2 - R_1)(T_1 + \tau)}{(R_1 - \rho)^2} \cdot \sigma_\rho\right)^2 + \left(\frac{T_1 + \tau}{R_1 - \rho} \cdot \sigma_{R_2}\right)^2} \tag{7.10}$$

If for example a resistance of $R_1 = 850\,\Omega$ is measured at $T_1 = 20\,℃$, a resistance of $R_2 = 725\,\Omega$ would correspond to a temperature of $T_2 = -15.9\,℃$. A realistic tolerance of R_2 of $\sigma_{R_2} = 3.5\,\Omega$ would thus result in a temperature tolerance of only $\sigma_{T_2} = 1\,℃$; $\sigma_{R_2} = 7\,\Omega$ yields to $\sigma_{T_2} = 2\,℃$. The dependency is by approximation linear.

These resistance tolerances are quite large in comparison to those seen for example in Figure 7.9. It has to take into account that in that setup the conditions have been much more balanced than during a usual sensor operation. The sensors self-heating and an unstable cooling power can likely lead to fluctuations of the temperatures on a short time scale. Thus, the resistance tolerance values of several Ohms can be regarded as realistic.

Conclusion

The presented measurements show that the On-Sensor Temperature Resistors constitute a possibility to obtain additional information about the sensors actual temperature. Although the absolute resistances are highly differing it is possible to calibrate one sample with only one reference pair of values by using Equation (7.3). The calibration should represent no large effort as the sensor-chip assemblies are anyhow tuned and measured extensively in the lab before the operation in test beam setups or later in the detector. The OSTeRs only have to be read out for a few hours at one known constant temperature. New versions of FE-I4 single chip cards are already implemented with additional wire bond pads to have an easy access to the OSTeR pads.

In the future it makes sense to investigate in how far the determined values of Equation (7.3) are reproducible. Especially measurements with significantly larger OSTeRs can reveal if the extremely linear correlation between $R(0°)$ and the slope can be extrapolated to higher resistances. A further step is the investigation of the behaviour after irradiation.

8. Conclusions and Outlook

In the coming years, the performance of the ATLAS pixel detector will degrade due to the massive increase of radiation damage. Especially after the Phase-I shutdown in 2017 and the related increase of the instantaneous luminosity to $2.2 \cdot 10^{34}\mathrm{cm}^{-2}\mathrm{s}^{-1}$, it will have to cope with tracks of up to 35 collisions per bunch crossing. As this is more than twice of the current design luminosity, it is inevitable to upgrade the current detector. The IBL represents an opportunity to implement this upgrade already in the current Phase-0 shutdown. It will implicate an improvement of the track pattern recognition capability, the reconstructed track accuracy and the b-tagging performance.

Due to the expected fluence of $5 \cdot 10^{15}\mathrm{n_{eq}}/\mathrm{cm}^2$ a new read-out chip is required. The former n^+-in-n design of the ATLAS pixel sensors had to be adapted to this FE-I4 chip. In a prototype wafer production, first experiences have been made with these sensors. The quality control was performed from wafer level up to the stage after dicing. One point of interest was the comparison between different sensor thicknesses. As thinner sensors ought to have a better performance after irradiation, it was investigated in how far the thickness can be optimized. A value of $200\,\mu$m seems to be the best compromise. The advantage of a supposable increased charge collection after irradiation counterbalances the possibility of a slightly increased loss of wafers during the processing steps.

An innovative method to decrease the inactive sensor edge without risking to reduce the sensor yield is a shifting of the active area opposite to the guard rings. Because this design approach was not used before, it had to be investigated in how far the efficiency of these pixels behaves. The design was already implemented in the FE-I4 sensors of the prototype production which have been operated in test beam setups. The slim edge assemblies showed excellent results with the lower threshold of 1600 electrons which is feasible with the FE-I4. Before irradiation, the pixels opposite to the guard rings can be regarded as fully efficient at the operation voltage of 80 V. After irradiation to an IBL-like fluence, the same result is observed for bias voltages of 800 V and higher. The slim edge design helped to decrease the inactive edge width to the order of $200\,\mu$m which represents a massive benefit compared to the IBL specification of $450\,\mu$m. Referred to the length of the IBL sensor, this is equal to an inactive fraction in the order of 1%.

The production of the planar IBL sensor wafers was supervised from the stage of wafer delivery to that before the flip chip process. During the quality control, the most important measurements have been coordinated, analysed and documented. The production shows exceedingly well results. The yield of the wafer production of 90.7% as well as that of the post process of 89.6% are convincing and should guarantee an adequate overrun of good sensors. Including the sensors of all wafers, it is expected to have more than twice as much good sensors as required for a 100% and almost three times as much as required for a 75% planar IBL scenario.

On the basis of the present results, it is possible to implement different post process and design optimizations for future sensors. The laser dicing technique represents a serious alternative to the conventional diamond saw dicing for sensors with a reduced inactive edge. Operated assemblies with the pixel shifted stepwise design showed that pixel overlaps of more than 250 μm present a chance to reduce the inactive edge width even more with the present conventional sensor technology. Dependencies of the effective pixel lengths on the operation voltage will have to be investigated. It is conceivable to decrease the inactive edge width to the order of 50 μm which is compatible to specifications of the ATLAS pixel Phase-II upgrade. In order to counteract efficiency decreases which are observed for HL-LHC irradiation fluences, sensors with differently shaped pixel implantations are currently investigated. One of the most crucial factors for charge loss is the bias grid. On coming wafer productions, sensors feature alterations of the bias grid layout to study in how far the design can be optimized. The calibration measurements of the On-Sensor Temperature Resistors showed that they constitute a convenient possibility to obtain information about the sensors actual temperature. They are foreseen on future sensors which can be a big facilitation for the operation in lab, test beams and in the detector. All design improvements are promising steps to make sure that planar n^+-in-n sensors will represent a serious candidate also for future ATLAS pixel upgrades.

A. Detailed Overview Tables of the Production Wafer

A.1. Prototype Production

Table A.1.: Overview of the structures on the IBL prototype production wafer.

	structure	properties
1	FE-I4 DCS	no long pixel v4, 13 GR, pixel overlap 0 μm
2	FE-I4 DCS	Slim Edge v2, 13 GR, pixel overlap 250 μm
3	FE-I4 SCS	Slim Edge v2, 13 GR, pixel overlap 250 μm
4	FE-I4 SCS	no long pixel v4, 13 GR, pixel overlap 0 μm
5	FE-I4 SCS	no long pixel v4, 13 GR, pixel overlap 0 μm
6	FE-I4 SCS	Slim Edge v2, 13 GR, pixel overlap 250 μm
7	FE-I3 SCS	Slim Edge v1, 13 GR, pixel overlap 250 μm
8	FE-I3 SCS	pixel shifted stepwise, 16 GR
9	FE-I3 SCS	conventional design v3, 16 GR, with p^+edge
10	FE-I3 SCS	Liverpool design, rd50, 6 GR on n-and p-side respectively
11	FE-I3 SCS	LAL design v2, 6 GR pixel overlap 100 μm,
12	FE-I3 SCS	no long pixel v4, 13 GR, pixel overlap 0 μm
13	FE-I3 SCS	Slim Edge v2, 13 GR, pixel overlap 150 μm
14	FE-I3 SCS	LAL design v3, 6 GR pixel overlap 300 μm,
15	FE-I3 SCS	no long pixel v4, 13 GR, pixel overlap 0 μm
16	FE-I3 SCS	Slim Edge v1, 13 GR, pixel overlap 250 μm
17	FE-I3 SCS	pixel shifted stepwise, 16 GR
18	FE-I3 SCS	conventional design v2, 16 GR, without p^+edge
19	GR diode	conventional design v1, 16 GR
20	GR diode	conventional design v1, 16 GR
21	GR diode	Liverpool design, PSI, 8 GR
22	GR diode	Liverpool design, PSI, 4 GR
23	GR diode	LAL design v3, 6 GR pixel overlap 300 μm,
24	GR diode	LAL design v2, 6 GR pixel overlap 100 μm,
25	GR diode	comb like pad v1.2, 16 GR, no moderated p-spray
26	GR diode	comb like pad v1, 16 GR, moderated p-spray
27	GR diode	comb like pad v2, 16 GR, moderated p-spray, area wide metal
28	GR diode	conventional design v1, 16 GR
29	GR diode	coplanar grid like pad v1, 16 GR, grid on n-side only
30	GR diode	coplanar grid like pad v2, 16 GR, grid on n- and p-side

Table A.2.: Overview of the structures on the IBL prototype production wafer (cont.).

	structure	properties
31	GR diode	conventional design v1, 16 GR
32	GR diode	comb like pad v1, 16 GR, moderated p-spray
33	GR diode	Liverpool design, RD50, 8 GR
34	GR diode	Liverpool design, RD50, 4 GR
35	GR diode	conventional design v1, 16 GR
36	GR diode	conventional design v1, 16 GR
37	GR diode	Liverpool design, RD50, 2 GR
38	GR diode	Liverpool design, MPI, 8 GR
39	GR diode	coplanar grid like pad v2, 16 GR, grid on n- and p-side
40	GR diode	conventional design v1, 16 GR
41	GR diode	comb like pad v1, 16 GR, moderated p-spray
42	GR diode	coplanar grid like pad v1, 16 GR, grid on n-side only
43	GR diode	conventional design v1, 16 GR
44	GR diode	conventional design v1, 16 GR
45	GR diode	LAL design, 4 GR, easily contactable
46	GR diode	LAL design, 1 GR, easily contactable
47	GR diode	LAL design, 3 GR, easily contactable
48	GR diode	LAL design, 2 GR, easily contactable
49	interpixel str.	LAL design, pixel 400, 100 and 50 μm long
50	test sensor	LAL design v4, pixel 50×50 μm, without fanout
51	GCD	ATLAS production design
52	GCD	ATLAS production design
53	MOSFET	ATLAS production design
54	MOSFET	ATLAS production design
55	Pitch Adapter	MPI HLL design v6, polysilicon
56	Pitch Adapter	MPI HLL design v6, polysilicon
57	Pitch Adapter	MPI HLL design v6, polysilicon, resistor only
58	Pitch Adapter	MPI HLL design v6, polysilicon, resistor only
59-110	GR diodes	smaller active area, 11, 12 and 13 GRs,

A.2. IBL Production

Table A.3.: Overview of the structures on the IBL planar sensor production wafer of 2011. 'GR' stands for guard ring.

	structure	properties
01	FE-I4 DCS	slim edge, 13 GR, pixel overlap 250 μm
02	FE-I4 DCS	slim edge, 13 GR, pixel overlap 250 μm
03	FE-I4 DCS	slim edge, 13 GR, pixel overlap 250 μm
04	FE-I4 DCS	slim edge, 13 GR, pixel overlap 250 μm, w/ OSTeR
05	FE-I4 SCS	different pixel shapes, segmented HV-pad, w/ OSTeR
06	FE-I4 SCS	slim edge, 13 GR, pixel overlap 250 μm
07	FE-I4 SCS	slim edge, 13 GR, pixel overlap 250 μm, w/ OSTeR
08	FE-I4 SCS	slim edge, 13 GR, pixel overlap 250 μm, w/ OSTeR
09	FE-I3 SCS	conventional design, 16 GR
10	FE-I3 SCS	different pixel shapes, 16 GR
11	FE-I3 SCS	slim edge, 13 GR, pixel overlap 250 μm
12	FE-I3 SCS	pixel shifted stepwise, 16 GR, no ganged pixels
13	GR diode	pixelated pad, 16 GR
14	GR diode	conventional design, 16 GR
15	GR diode	comb like pad v1.2, 16 GR, no moderated p-spray
16	GR diode	comb like pad v1, 16 GR, moderated p-spray
17	GR diode	comb like pad v2, 16 GR, moderated p-spray, area wide metal
18	GR diode	coplanar grid like pad v2, 16 GR, grid on n- and p-side
19	GR diode	pixelated pad, 16 GR
20	GR diode	conventional design, 16 GR
21	GR diode	conventional design, 16 GR
22	GR diode	coplanar grid like pad v1, 16 GR, grid on n-side only
23	GR diode	comb like pad v1.2, 16 GR, no moderated p-spray
24	GR diode	comb like pad v2, 16 GR, moderated p-spray, area wide metal
25	GR diode	comb like pad v1, 16 GR, moderated p-spray
26	GCD	ATLAS production design
27	GCD	ATLAS production design
28	MOSFET	ATLAS production design, p-side
29	MOSFET	ATLAS production design, n-side
30	test structure	for doping profile measurements
31	omegapix sensor	LAL design v4, pixel 50 μm $\times$ 50 μm, without fanout
32	GR diode	LAL design, 1 GR, easily contactable
33	GR diode	LAL design, 3 GR, easily contactable
34	GR diode	LAL design, 4 GR, easily contactable
35	GR diode	LAL design, 2 GR, easily contactable
36	interpixel str.	LAL design, pixel 400, 100 and 50 μm long
37	omegapix sensor	LAL design v4, pixel 50 μm $\times$ 50 μm, without fanout
38	test sensor	for Uni Bonn, 250 μm $\times$ 50 μm pixels

B. Test Beam Results

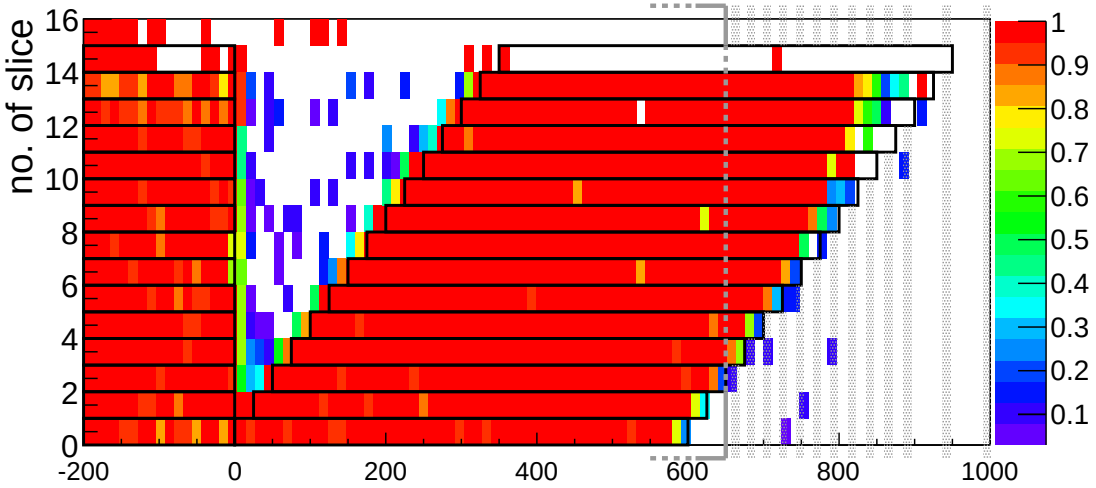


Figure B.1.: Hit efficiency map of the edge of the unirradiated FE-I3 pixel shifted stepwise assembly DO 3 which was operated at 100 V. The sensor thickness is 285 μm. The plot is analogous to those in Figure 5.28.

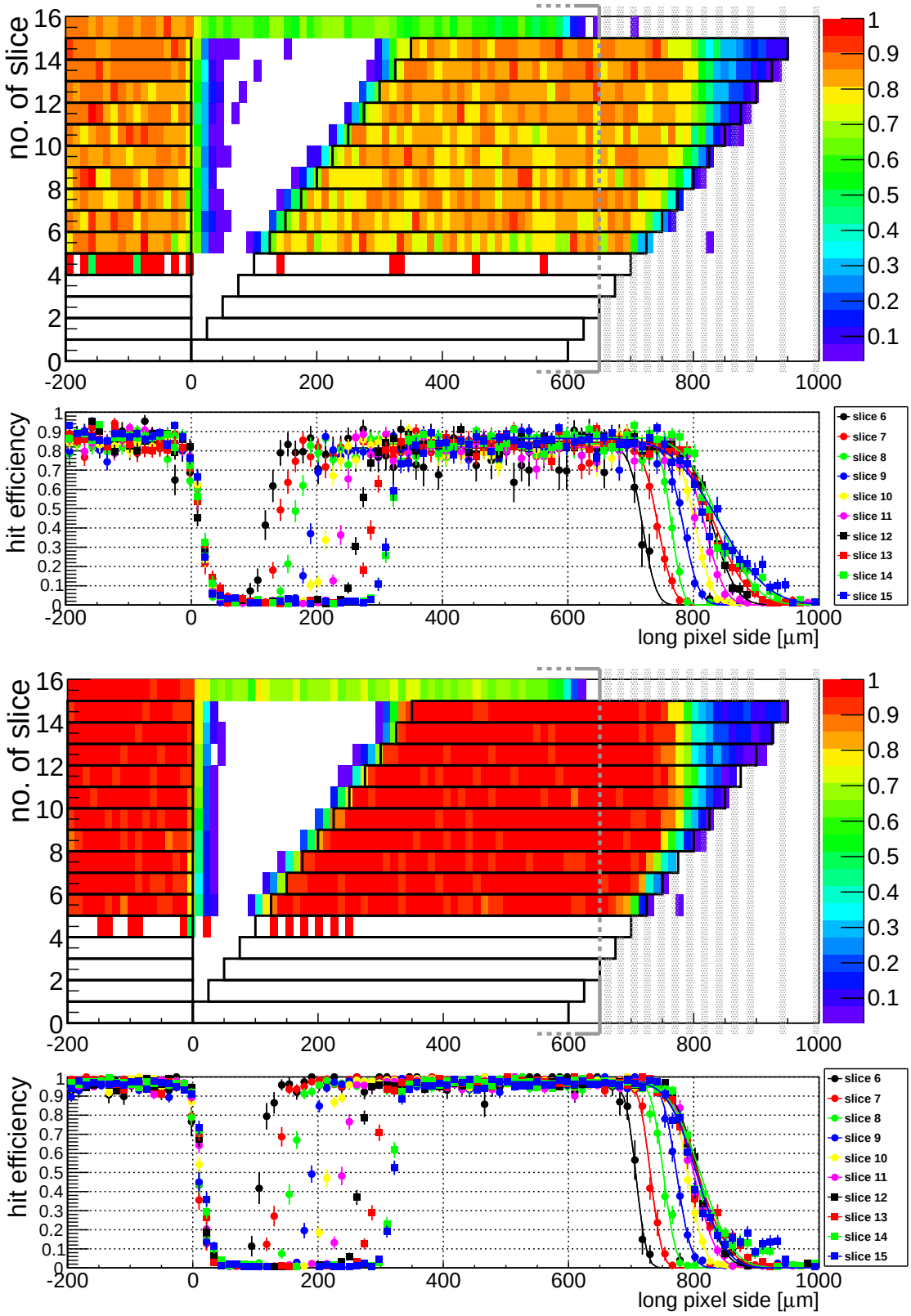


Figure B.2.: Hit efficiency map of the edge of the unirradiated FE-I3 pixel shifted stepwise assembly DO 43 which was operated at 70 V (top) and at 60 V (bottom). The sensor thickness is 200 μm. The plots are analogous to those in Figure 5.28.

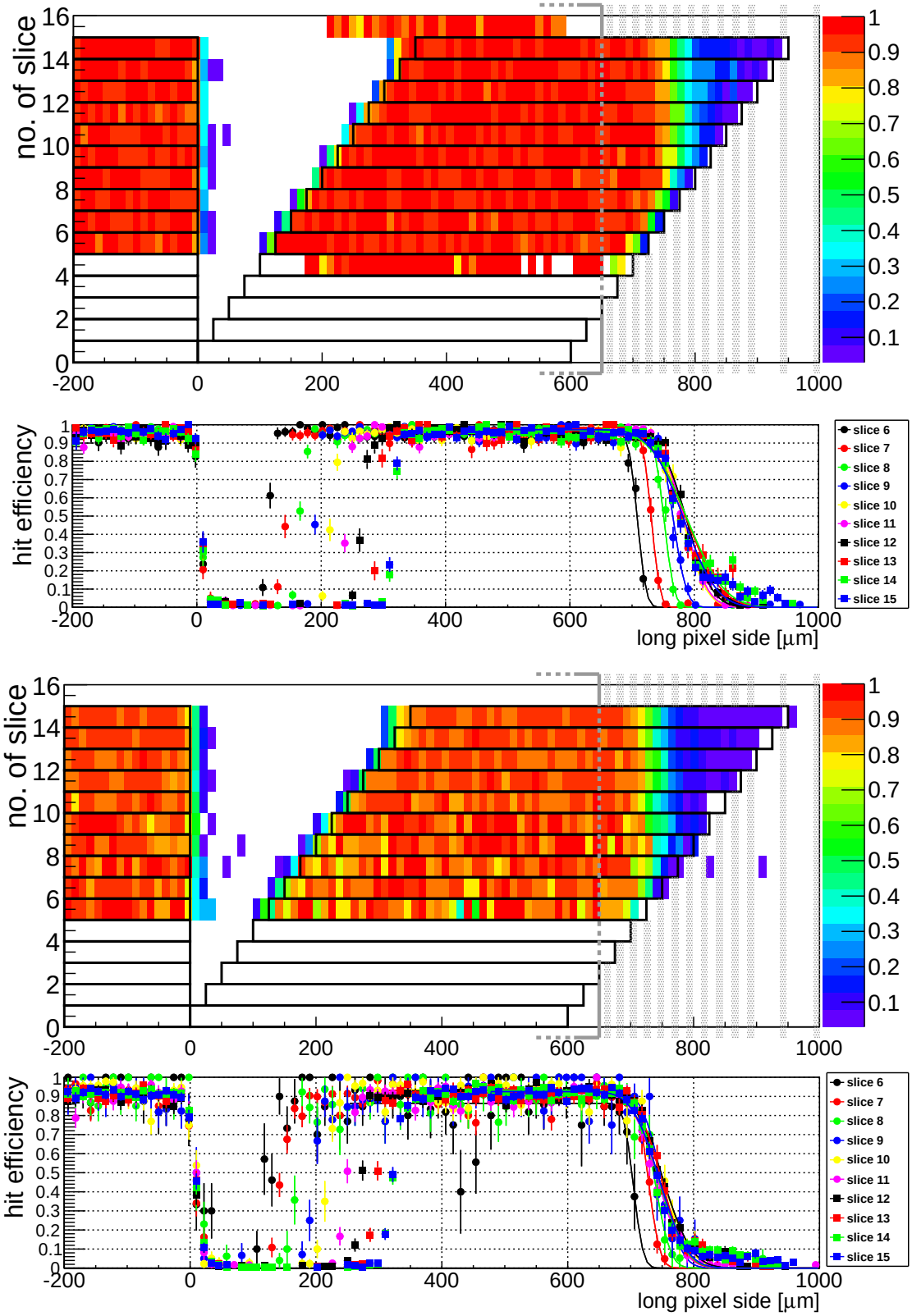


Figure B.3.: Hit efficiency map of the edge of the unirradiated FE-I3 pixel shifted stepwise assembly DO 46 which was operated at 60 V (top) and at 40 V (bottom). The sensor thickness is 150 μm. The plots are analogous to those in Figure 5.28.

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C. Goessling, R. Klingenberg, D. Muenstermann and T. Wittig
Evaluation of the breakdown behaviour of ATLAS silicon pixel sensors after partial guard-ring removal
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S. Altenheiner, C. Goessling, J. Jentzsch, R. Klingenberg, T. Lapsien, D. Muenstermann, A. Rummler, G. Troska and T. Wittig,
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