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TOPICAL REVIEW

Semiconductor nanowires

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Abstract
Semiconductor nanowires (NWs) represent a unique system for exploring phenomena at the nanoscale and are also expected to play a critical role in future electronic and optoelectronic devices. Here we review recent advances in growth, characterization, assembly and integration of chemically synthesized, atomic scale semiconductor NWs. We first introduce a general scheme based on a metal-cluster catalyzed vapour–liquid–solid growth mechanism for the synthesis of a broad range of NWs and nanowire heterostructures with precisely controlled chemical composition and physical dimension. Such controlled growth in turn results in controlled electrical and optical properties. Subsequently, we discuss novel properties associated with these one-dimensional (1D) structures such as discrete 1D subbands formation and Coulomb blockade effects as well as ballistic transport and many-body phenomena. Room-temperature high-performance electrical and optical devices will then be discussed at the single- or few-nanowire level. We will then explore methods to assemble and integrate NWs into large-scale functional circuits and real-world applications, examples including high-performance DC/RF circuits and flexible electronics. Prospects of a fundamentally different 'bottom-up' paradigm, in which functionalities are coded during growth and circuits are formed via self-assembly, will also be briefly discussed.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

Great advances in integrated circuit technologies have been accomplished during the past four decades that resulted in electronic devices with higher device density, faster clock rate and lower power consumption [1]. However, as the devices reach deep sub-100 nm scale, conventional scaling methods which maintain the device's basic structure while shrinking its size face increasing technological and fundamental challenges. For example, device size fluctuations will result in a large spread in device characteristics at the nanoscale, affecting key parameters such as the threshold voltage and on/off current. Increasing demand on the resolution of the equipment and expenses of building and operating the facilities also pushes the traditional approach towards its practical limit and hinders device scaling from reaching true atomic level [2, 3].

To sustain the historical scaling trend beyond CMOS, novel one-dimensional (1D) structures, including carbon nanotubes (CNTs) and semiconductor nanowires (NWs), have been proposed as the active components (as well as interconnects) in future nanoscale devices and circuits. In this case, the critical device size is defined during the growth (chemical synthesis) process and can be controlled with atomic scale resolution. To date, great efforts and

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progress have been made in the field of CNTs, although CNT based applications are still hindered by difficulties to produce uniform, semiconducting nanotubes. On the other hand, semiconductor NWs can be prepared with reproducible electronic properties in high-yield, as required for large-scale integrated systems. Furthermore, the well-controlled NW growth process implies that materials with distinct chemical composition, structure, size and morphology can be integrated [5]. Such an ability to build specific functions into the system during growth may in turn lead to bottom-up assembly of integrated circuits [5], which offers the potential of parallel production of massive number of devices with similar material and electrical/optical properties. Drastically different from the 'top-down' paradigm commonly used in today's semiconductor industry, this 'bottom-up' paradigm, analogous to the way that nature works, may prove to be a suitable solution to the technological challenges as devices approach atomic size.

From a fundamental physics point of view, the low-dimensional nanowire structure is an ideal platform to probe properties which may be inaccessible or hard to achieve in larger devices, due to the reduced device size and ideal material properties. For example, discreteness of electrons comes into play when the Coulomb energy associated with the addition of an individual electron becomes larger than the thermal energy; 1D quantum wires and zero-dimensional quantum dots (QDs) form when the relevant device size is comparable to the de Broglie wavelength of the carriers. As a result, the electrical and optical properties in these nanoscale devices are determined not only by the materials composition but can also be tailored by the specific device geometry.

2. Growth of NWs

2.1. The vapour–liquid–solid growth method

Semiconductor NWs are generally synthesized by employing metal nanoclusters as catalysts via a vapour–liquid–solid (VLS) process (figure 1) [6]. In this process, the metal nanoclusters are heated above the eutectic temperature for the metal–semiconductor system of choice in the presence of a vapour-phase source of the semiconductor, resulting in a liquid droplet of the metal/semiconductor alloy. The continued feeding of the semiconductor reactant into the liquid droplet supersaturates the eutectic, leading to nucleation of the solid semiconductor. The solid–liquid interface forms the growth interface, which acts as a sink causing the continued semiconductor incorporation into the lattice and, thereby, the growth of the nanowire with the alloy droplet riding on the top.

The gaseous semiconductor reactants can be generated through decomposition of precursors in a chemical vapour deposition (CVD) process or through momentum and energy transfer methods such as pulsed laser ablation [7] or molecular beam epitaxy (MBE) [8] from solid targets. So far, CVD has been the most popular technique. In CVD–VLS growth, the metal nanocluster serves as a catalyst at which site the gaseous precursor decompose, providing the gaseous semiconductor reactants. In the case of SiNW growth (figure 1), silane (SiH_4) and Au nanoparticles are normally used as the precursor and catalysts, respectively. Besides group IV materials, compound

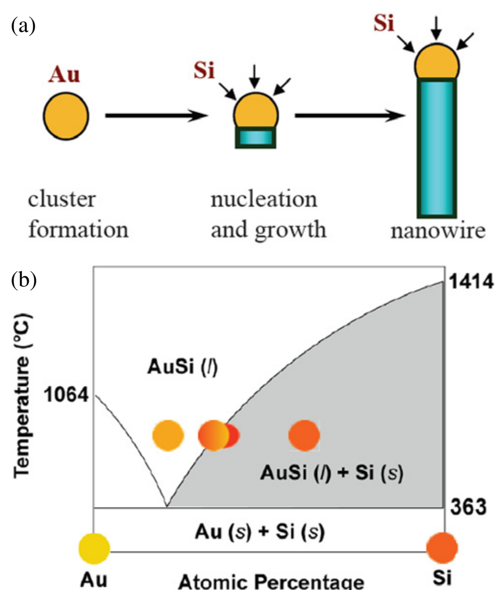

Figure 1. Schematic of VLS growth of Si nanowires (SiNWs). (*a*) A liquid alloy droplet AuSi is first formed above the eutectic temperature (363 °C) of Au and Si. The continued feeding of Si in the vapour phase into the liquid alloy causes oversaturation of the liquid alloy, resulting in nucleation and directional nanowire growth. (*b*) Binary phase diagram for Au and Si illustrating the thermodynamics of VLS growth.

III–V and II–VI NWs have also been produced with the VLS method, in which pseudobinary phase diagrams for the catalyst and compound semiconductor of interest are employed. In the compound semiconductor case, metal-organic chemical vapour deposition (MOCVD) [9] or pulsed laser ablation [10] are typically used to provide the reactants.

There are two competing interfaces during nanowire growth, the liquid/solid interface between the eutectic and the nanowire and the gas/solid interface between the reactants and the exposed surface of the growing nanowire. Precipitation through the first interface results in the VLS growth and axial elongation of the nanowire, while dissociative adsorption on the second interface results in vapour–solid growth and thickening in the radial direction. Either mechanism can be dominating in an actual growth process, depending on the detailed growth condition such as the pressure, flow rate, temperature, reactant species and background gases that are by-products of growth reactions. For example, in the above-mentioned SiNW growth process, low temperature growth can reduce the rate of direct thermal dissociation of silane; hence, axial nanowire growth is favoured. Hydrogen has also been found to mitigate radial growth through suppression of either the adsorption of the reactants by terminating the Si surface [11] or of the dissociation of silane [12, 13]. The use of H_2 as the carrier gas also passivates the NW surface in a manner similar to that observed in thin-film growth [14] and reduces roughening along the NW. Uniform NWs with negligible diameter variation can thus be achieved through careful control of the growth conditions, including the employment of local heaters to reduce uncontrolled decomposition of silane [15]. On the other hand, tapered NWs are products from simultaneous growth in both the axial and radial directions

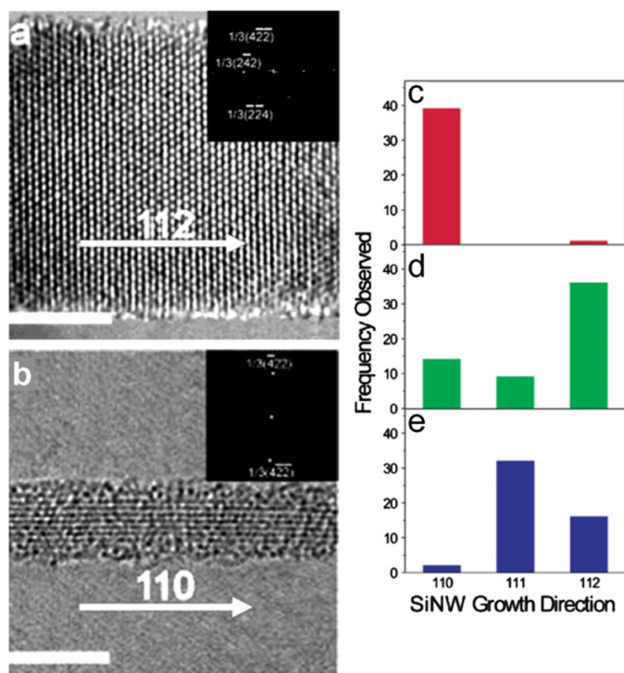

Figure 2. (*a*) and (*b*) HRTEM images of SiNWs with diameters of 12.3 nm (*a*) and 3.5 nm (*b*). Sale bar: 5 nm. (*c*)–(*e*) Histogram of the growth directions for SiNWs with diameters from 3 to 10 nm (*c*), from 10 to 20 nm (*d*) and from 20 to 30 nm (*e*). Adapted from [11].

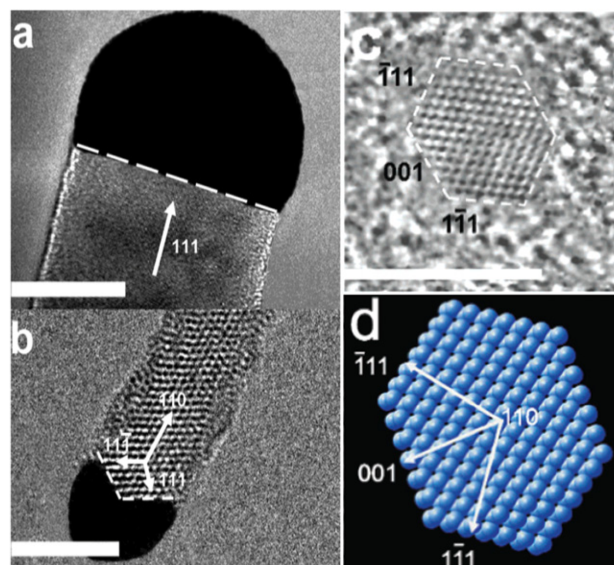

Figure 3. (*a*) HRTEM image of the catalyst alloy/NW interface of a SiNW with a ⟨111⟩ growth axis. Scale bar: 20 nm. (*b*) HRTEM image of a catalyst alloy/NW interface of a SiNW with a ⟨110⟩ growth axis. Scale bar: 5 nm. (*c*) HRTEM cross-sectional image (scale bars: 5 nm) and (*d*) equilibrium shapes for the NW cross sections predicted by Wulff construction. Adapted from [11].

and are generally not desirable for most electrical and optical applications.

In the CVD–VLS growth process the diameter of the nanowire is determined by that of the starting nanocluster, and uniform, atomic-scale NWs can be obtained in a well-controlled growth process as nanoclusters with diameters down to a few nanometres are now commercially available. Wu *et al* reported growth of uniform SiNWs with diameters down to 3 nm [11] using SiH_4 as the precursor and H_2 as the carrier gas. Wu performed detailed high-resolution transmission electron micrography (HRTEM) studies on these SiNWs and observed that the NWs are single-crystalline with little or no visible amorphous oxide even at this scale. The resulting SiNWs show narrow size distributions of 13.2 ± 1.7 nm, 5.9 ± 1.1 nm, and 4.6 ± 1.2 nm, respectively when gold nanoclusters of diameters of 10 (9.7 ± 1.5) nm, 5 (4.9 ± 0.7) nm, and 2 (3.3 ± 1) nm are used. The increase in the NW diameters compared with those of the starting nanoclusters was attributed to the supersaturation of silicon in gold nanoclusters during the formation of the liquid droplet prior to nucleation, an effect observed previously with *in situ* observations of the growth of germanium NWs [16].

The crystallographic orientation of the NW during VLS growth is chosen to minimize the total free energy, as the process is thermodynamically driven. The total free energy includes the 'bulk' energy of the SiNW, the Au/Si interface energy and the Si/vacuum interface energy. In Wu's study, the growth directions of SiNWs with different diameters are carefully examined [11]. A histogram of the growth directions of the SiNWs is shown in figure 2. Prior studies of VLS growth on micrometre-scale silicon whiskers have shown that the growth is primarily along the ⟨111⟩ direction, since the solid–liquid interface parallel to a (111) plane possesses lowest free-energy [6]. The predominant ⟨111⟩ growth direction (figure 2(*e*)) and the single (111) plane at the catalyst/NW interface (figure 3(*a*)) were indeed observed on VLS-grown SiNWs as well, with diameters larger than 20 nm [11]. On the other hand, ⟨110⟩ becomes the predominant growth direction for NWs with diameter smaller than 10 nm (figure 2(*c*)). This phenomenon can be explained by the fact that the Si/vacuum surface energy becomes increasingly dominating when the surface/volume ratio is increased as the nanowire diameter is decreased, as the Si/vacuum surfaces parallel to ⟨111⟩ axis consist of the lowest free-energy (111) and (100) planes (figures 3(*c*) and (*d*)). Interestingly, ⟨110⟩ growth does not arise from the formation of a liquid/solid (110) interface. As shown in figure 3(*b*), the catalyst/NW interface now consists of two low energy {111} planes, whereby the ⟨111⟩ and ⟨11 − 1⟩ directions combine to yield a growth axis of ⟨110⟩. Such observations are consistent with the thermodynamic picture of the VLS growth mechanism. The ⟨112⟩ growth direction, which is observed for a substantial fraction of intermediate-diameter SiNWs (figure 2(*d*)), can be explained as a 'transitional' direction between the ⟨111⟩ and ⟨110⟩ growth directions since the (112) plane is a stepped plane between the (111) and (110) planes [17].

2.2. Nanowire heterostructures

Compared with nanostructures fabricated from other approaches such as vapour–solid growth [18] or solution based liquid–solid growth [19], the VLS process offers one key advantage—heterostructures can be achieved at the individual device level in a controlled fashion. Both axial heterostructures (figures 4(*c*) and (*e*)), in which sections of different materials with the same diameter are grown along the wire axis [20, 21], and radial heterostructures (figures 4(*d*) and (*f*)), in which

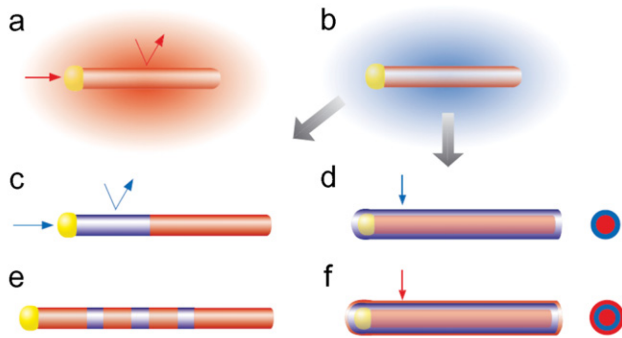

Figure 4. Nanowire heterostructure synthesis. (*a*) Preferential reactant incorporation at the catalyst (growth end) leads to 1D axial growth. (*b*) A change in the reactant leads to either (*c*) axial heterostructure growth or (*d*) radial heterostructure growth depending on whether the reactant is preferentially incorporated (*c*) at the catalyst or (*d*) uniformly on the wire surface. Alternating reactants will produce (*e*) axial superlattices or (*f*) core-multi-shell structures [25].

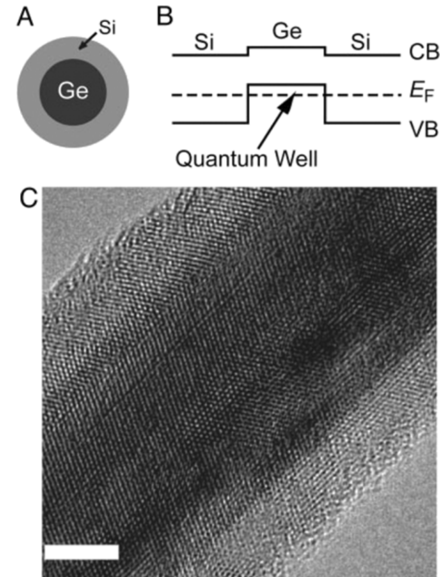

Figure 5. Ge/Si core/shell NWs. (A) Schematic of a cross-section through the Ge/Si core/shell nanowire. (B) Band diagram for a Si/Ge/Si heterostructure. The dashed line indicates the position of the Fermi level, E_F. (C) HRTEM image of a Ge/Si core/shell nanowire with 15 nm Ge (dark grey) core diameter and 5 nm Si (light grey) shell thickness. Scale bar: 5 nm [23].

core/shell and core/multi-shell form along the radial direction [22–24], have been realized on VLS–CVD grown NWs.

To understand the rational formation of nanowire heterostructures within the context of the VLS method, consider the possible effects of a change in reactant vapour once nanowire growth has been established (figure 4). If vapour decomposition/adsorption continues exclusively at the surface of the catalyst nanocluster site, crystalline growth of the new semiconductor will continue along the axial direction (figure 4(*c*)). On the other hand, if the decomposition of the new vapour/reactant on the surface of the semiconductor nanowire cannot be neglected, a shell of material will grow on the original nanowire surface (figure 4(*d*)). Repeated changing of reactants in a regime favouring axial growth will lead to the formation of a nanowire superlattice, as shown in figure 4(*e*), while changing reactants in a radial-growth regime will result in core-multi-shell radial structures, as shown in figure 4(*f*). It is important to mention that there are few constraints on the composition of the shell growth; any material suitable for planar film deposition can be deposited on the surface of a nanowire, and crystalline radial heteroepitaxy [22] can be achieved as the nanowire surface is crystalline.

2.2.1. Radial nanowire heterostructures. Radial core/shell heterostructures can be achieved if dissociation of the reactants is promoted at the grown nanowire surface (figure 4(*d*)) [22], analogous to the layered growth of planar heterostructures. Compared with NWs in the simple homogeneous form, core/shell heterostructure NWs offer better electrical and optical properties as they can now be tailored through band structure engineering. For example, similar to the formation of two-dimensional electron [26] and hole gases [27] in high-electron mobility transistors (HEMTs), 1D electron and hole gases can be achieved in core/shell heterostructure NWs. Lu *et al* observed that a 1D hole gas [23] will be formed if a Si shell is epitaxially grown on top of a Ge core, as shown in figure 5. The valence band offset of ca 500 meV between Ge and Si at the heterostructure interface [27, 28] then serves as a confinement potential for the quantum well, and free holes will accumulate in the Ge channel when the Fermi level lies below the valance band edge of the Ge core (figure 5(B)). In the Ge/Si core/shell nanowire heterostructure, the pseudomorphic strain in the epitaxial core and shell materials is relaxed along the radial direction [22], yielding a type II staggered band alignment [27]. The light hole and heavy hole bands are expected to split due to the effects of strain and confinement [27]. This hole-gas system will be discussed in detail in section 3.2, as novel phenomena and high-performance transistors are realized on such core/shell NWs.

Other types of core/shell nanoires have also been studied. For example, GaN based core/multi-shell NWs [24, 29] have been grown using MOCVD. High-efficiency light-emitting diodes were obtained on these core/multi-shell structures using bandstructure engineering and modulation doping [24, 29]. In a different approach, silicon/silica core/shell NWs were produced through thermal oxidation of as-grown SiNWs [30, 31]. By treating either the silica shell or the silicon core as a sacrificial material, silica nanotubes [31] or parallel array of silicon NWs with controlled spacing [30] have been demonstrated, respectively.

2.2.2. Axial nanowire heterostructures. Unlike radial heterostructures in which the shell growth does not involve reaction with the nanocluster catalyst, axial nanowire heterostructures can be obtained by alternative introduction of vapour phase reactants that react with the same nanocluster catalyst, as illustrated in figures 4(*c*) and (*e*). A critical requirement of the axial nanowire heterostructure growth is then that a single nanocluster catalyst can be found which is suitable for growth of the different components under similar conditions. For a wide range of III–V and IV materials, Duan *et al* observed [10] that Au nanoclusters can meet this requirement. Using Au nanoclusters as catalysts and a laser-assisted catalytic growth, Gudiksen *et al* [20] have successfully obtained GaAs/GaP axial

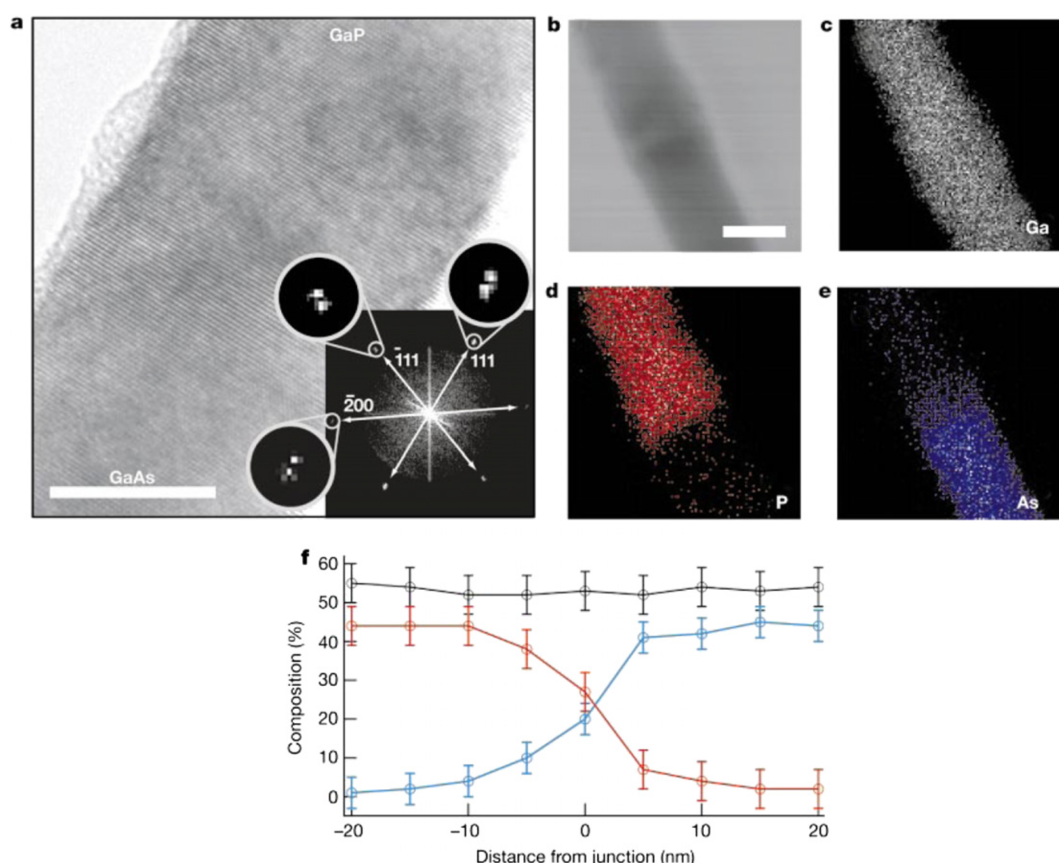

Figure 6. Axial GaAs/GaP nanowire heterostructures. (*a*) HRTEM of a GaAs/GaP junction grown from a 20 nm gold nanocluster catalyst. Scale bar: 10 nm. Inset, two-dimensional Fourier transforms of the entire image. (*b*) TEM image of another junction. Scale bar, 20 nm. (*c*)–(*e*) Elemental mapping of the Ga (shown grey), P (red) and As (blue) content of the junction shown in (*b*). (*f*) Line profiles of the composition through the junction region, showing the change in composition as a function of the distance. Ga: black, P: red and As: blue [20]. (Colour online.)

nanowire heterostructures (superlattices) with GaAs and GaP targets at temperatures of 700–850 °C at 100 Torr in a continuous argon flow.

Figure 6(*a*) shows a TEM image of a typical GaAs/GaP junction region obtained by Gudiksen. The nanowire axes was found to lie along the ⟨111⟩ direction, in agreement with previous studies of single-component systems [7, 10, 32]. Two-dimensional Fourier transforms calculated from high-resolution images containing the junction region (figure 6(*a*), inset) show pairs of reciprocal lattice peaks along the different lattice directions, while such transforms calculated from the regions above and below the junction (not shown) exhibit only single reciprocal lattice peaks. Analysis of these peak data yields lattice constants, indexed to the zinc blende structures of GaP and GaAs, of 0.5474 ± 60.0073 nm and 0.56686 ± 0.0085 nm and are in good agreement with the values for both GaP (0.5451 nm) and GaAs (0.5653 nm), respectively.

Local elemental mapping of the heterojunction by energy dispersive x-ray spectroscopy (EDS) was carried out to probe composition variations across the heterostructure junction (figures 6(*b*)–(*e*)). The elemental maps show that Ga is uniformly distributed along the length of the NW, while P (figure 6(*d*)) and As (figure 6(*e*)) appear localized in the GaP and GaAs portions of the nanowire heterostructure, respectively. Quantitative analysis of the P and As composition variation (figure 6(*f*)) however, shows, that the junction is not atomically abrupt but rather makes the transition between GaP and GaAs phases over a length scale of 15–20 nm. This length scale is consistent with the hypothesis that the ∼20 nm diameter Au catalyst must re-alloy with GaP after initial GaAs growth. The observed composition variation has several potentially important implications. First, composition variation at the interface can relieve strain and may enable the defect-free junctions and superlattices that were observed in the GaAs/GaP system which has a relatively large lattice mismatch. Second, the observed composition variation could be substantially reduced in smaller-diameter NWs when abrupt interfaces are required in certain photonic and electronic applications. For example, a 5 nm diameter nanowire superlattice should have variations of 5 nm across the junction interfaces. Alternatively, it should be possible to use different nanocluster catalysts or variations in the growth temperature when reactants are switched to obtain sharper interfaces.

By repeating the modulation process, nanowire superlattices can be produced in which the number of periods and repeat spacing can be readily varied during growth. For example, Gudiksen *et al* demonstrated a 21-layer GaAs/GaP superlattice with arbitrary repeat spacing, with the lengths of the segments controlled by the number of pulses delivered to each

target. In an independent study, the Yang group at UC Berkeley combined thermal CVD using silicon tetrachloride ($SiCl_4$) with the laser ablation of a solid germanium target to produce Si–SiGe NWs [33]. Wire growth was at 850–950 °C and 1 atm total pressure, with a $SiCl_4/H_2$ mole ratio of 0.02. InP–InAs superlattices with very abrupt interfaces were produced by the Samuelson group at Lund University using ultra-high vacuum chemical beam epitaxy [34]. Wire growth catalysed by Au particles was performed at 420 °C and ca 3 Torr using trimethylindium (TMIn), tertiarybutylphosphine and tertiarybutylarsine precursors. To create heterojunctions, the TMIn source was turned off, the group V source turned on after a 5 s pause and the TMIn turned on again after another 5 s. HRTEM images were consistent with interface widths of a few atomic layers, though elemental analysis was not performed. The monolayer sharpness of the interfaces was attributed to the high vapour pressures of the group V source materials in combination with the low growth rate (ca 1 ML s^{-1}). Such nanowire superlattices offer potential as novel thermoelectric devices [35], resonant tunnelling diode (RTD) devices [36], QD devices [37,38] or simply as optical nanobarcodes in which information is coded in the length and spacing of the direct bandgap GaAs segments.

Besides semiconductor heterostructures, metal/semiconductor axial heterostructures and superlattices have also been demonstrated recently [39]. Wu *et al* observed that NiSi, a bulk metal, can be transformed from Si via solid phase reaction with Ni. As a result, metallic NiSi NWs were produced by first evaporating Ni on SiNWs, followed by heating the sample above the NiSi transisiton temperature [39]. A temperature of 550 °C was used in Wu's study. HRTEM studies verified the resulting wires are single-crystalline NiSi, and transport measurements verified the resistivity is consistent with the bulk NiSi value. Using the same approach, Wu obtained NiSi/Si metal/semiconductor axial heterostructures by selectively patterning Ni on SiNWs using a pre-defined mask, followed by the solid phase reaction process to create NiSi segments at the selected locations. In this case, the interface at the Si/NiSi heterostructure is not limited by diffusion through the catalyst nanocluster and can be atomic sharp [39]. Compared with devices using external microscale leads and interconnects, the NiSi/Si metal/semiconductor heterostructure offers an intriguing solution in which the metallic regions can be used as local contacts to the active semiconductor regions as well as interconnects, hence achieving much higher device density.

2.2.3. Branched nanowire structures. Branched and tree-like nanowire structures may be obtained if after the initial nanowire growth, metal catalyst nanoclusters are deposited again on the surfaces of the grown NWs (the trunks), and reactants are introduced once more to facilitate nucleation and directional growth of nanowire branches. Epitaxial growth of the branches can occur if the trunk and branches are composed of similar materials and no amorphous overcoating (e.g. oxides) is developed before the branch growth. Branched NWs and 'nanotrees' were independently studied by Wang *et al* in the case of Si and GaN and Dick *et al* in the case of GaP [40] using MOCVD and a sol–gel method to deposit Au catalyst nanoclusters on the nanowire trunks.

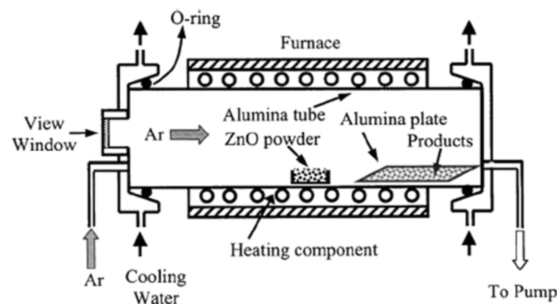

Figure 7. Schematic diagram of the horizontal tube furnace for growth of ZnO nanostructures. Reprinted with permission from [62].

2.3. Growth of metal oxide NWs

Besides the VLS approach, a simple thermal evaporation/vapour transport deposition approach has also been shown to be effective in growing 1D structures, in particular metal oxide (e.g. ZnO, In_2O_3 and SnO_2) NWs. Such NWs have been studied in applications ranging from optoelectronics devices [41–44], field-effect transistors [45,46], ultra-sensitive nanoscale gas sensors [45, 47–50] and field emitters [51, 52]. In particular, ZnO NWs have attracted a lot of interest due to the large exciton binding energy (60 meV), high electromechanical coupling constant and resistivity to harsh environment [53].

The first attempt to produce ZnO NWs was based on an electrochemical method using anodic alumina membranes (AAM) [54]. Later on, high-density, ordered ZnO nanowire arrays were obtained using AAM in a vapour-deposition process [55]. However, the AAM approach is typically limited to generating polycrystalline NWs. To produce single-crystalline 1D ZnO nanostructures, a number of methods have been explored such as thermal evaporation/vapour transport deposition [18, 56], hydrothermal process [57], MOCVD [58, 59], pulsed laser deposition [60] and MBE [61].

Among all methods used to grow metal oxide NWs, thermal evaporation/vapour transport deposition has gained the most popularity. The thermal evaporation technique is based on a simple process in which source materials in the condensed or powder form are first vapourized at an elevated temperature; the resulting materials in vapour phase then condense under the right conditions (temperature, pressure, atmosphere, substrate, etc) to form the desired product [62]. The processes are usually carried out in a setup as shown in figure 7, which includes a horizontal tube furnace, a quartz or alumina tube, gas supplies and control system.

Single-crystalline ZnO NWs grown with the thermal evaporation method (referred also as the physical vapour deposition method) were first reported in 2001 [18], with an average diameter of about 60 nm. In 2002, Yao *et al* reported mass production of ZnO NWs, nanoribbons and needle-like nanorods by thermal evaporation of ZnO powders mixed with graphite [63]. Yao found that temperature was the critical experimental parameter for the formation of different morphologies of ZnO nanostructures. Banerjee *et al* succeeded in producing grams of ZnO NWs via thermal evaporation of ZnO powder in a tube furnace at high temperatures [64]. The graphite flakes were found to be the key

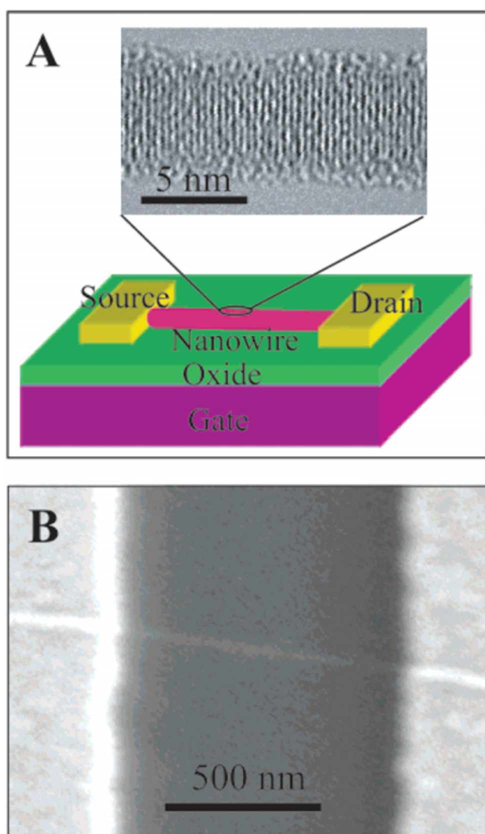

Figure 8. (A) Schematic of a SiNW FET showing metal source and drain electrodes. (Inset) HRTEM of a 5 nm diameter SiNW. (B) Scanning electron micrograph of a SiNW FET device [66].

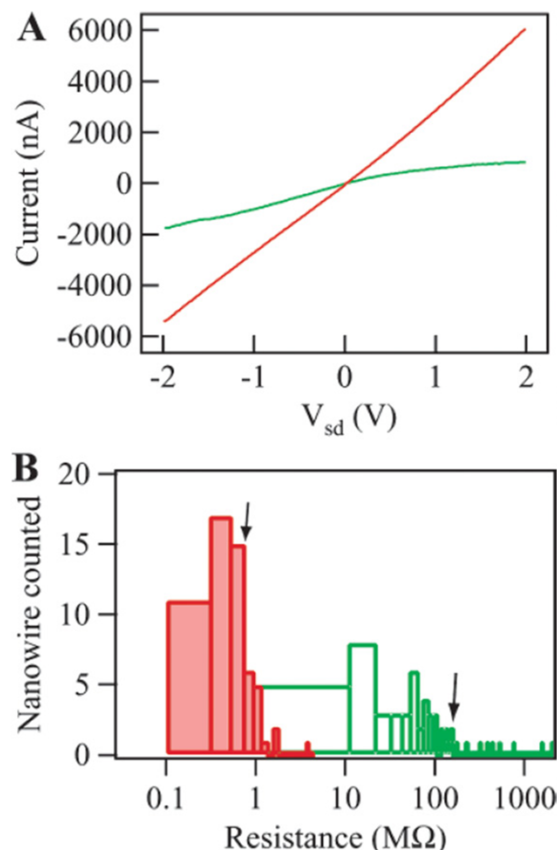

Figure 9. (A) I versus V_{sd} measured on the same SiNW before (green) and after (red) thermal annealing. (B) Histogram of Ti-contacted SiNW resistance determined from measurements before (open green bars) and after (filled red bars) contact annealing [66]. (Colour online.)

ingredient for large-quantity growth and can be easily removed by oxidation at ∼700 °C for 1–3 h in O_2 flow.

Recently, Wan *et al* reported that single crystalline ZnO NWs in the kilogram range can be obtained through direct thermal evaporation of metal zinc pellets (purity: 99.999%) at 900 °C in a quartz tube [65]. Such an approach provides an effective method for large-scale industrialization without the need of metal catalysts, graphite additives or vacuum. Oxygen ambient was found to be critical for the morphology of the synthesized ZnO products. For example, tetrapod-like ZnO nanostructures were the only product that can be grown in air ambient. However, if Zn pellets were evaporated in 1–5% oxygen, massive wire-like ZnO nanostructures can be obtained.

3. Nanowire electronic devices

3.1. Homostructure nanowire devices

3.1.1. Field-effect transistor devices. Silicon NWs (SiNWs) have been most extensively studied partly due to the dominance of Si devices in the semiconductor industry and partly due to the well-developed recipes to grow SiNWs with controlled size and doping level. In a typical device geometry, the SiNWs are first transferred into liquid suspension after growth via gentle sonication, then dispersed on a degenerately doped Si substrate with a SiO_2 overgrowth layer, as shown in figure 8. Devices in the form of field-effect transistors can then be studied after source–drain electrode formation which is normally carried out by e-beam or photo-lithography, with the degenerately doped Si substrate serving as the back gate [66].

Unlike conventional MOSFETs in which the source/drain contacts are formed by degenerated doped Si, metal contacts are commonly used in a nanowire device. In this regard, a nanowire FET device is essentially a Schottky barrier device [67–69]. Typically positive Schottky barriers are observed at the metal/semiconductor interface due to the combined effect of metal work function and Fermi level pinning by surface states [70]. As a result, the device performance is to a large degree affected by the contact properties [68,69]. For example, Cui *et al* observed [66] that after thermal annealing which was believed to improve the source/drain contacts, the average transconductance of the SiNW devices increased from 45 to 800 nS and the deduced average mobility μ increased from 30 to 560 $cm^2 (V s)^{-1}$.

In Cui's study, boron-doped (p-type) SiNWs with diameters in the 10–20 nm range were used. The nanowire FETs were fabricated using Ti S/D contacts, and transport characteristics were studied as a function of annealing. Ti was used since it is known that Ti can form a stable conducting silicide with a low Schottky barrier height on p-type silicon [71]. Figure 9(A) shows the current (I) versus source–drain voltage (V_{sd}) behaviour of a typical Ti-contacted SiNW device before and after thermal annealing. In general, the

I–V_{sd} curves become more linear and symmetric, and the transport behaviour becomes more stable after annealing, with the measured conductance increasing by 3-fold. To characterize the reproducibility of these observations, similar measurements were made on over 50 devices. These results are summarized in a histogram showing the frequency that different values of two-terminal resistance were observed (figure 9(B)). Before annealing, the resistance shows a large distribution ranging from ∼MΩ to larger than GΩ with an average of 160 MΩ. In contrast, the resistance after annealing has a narrower distribution of 0.1–10 MΩ with an average of 0.62 MΩ; that is, a 260 fold improvement in the two-terminal conductance. The increased two-terminal conductance and stability can be attributed in part to better metal SiNW contacts, although passivation of defects at Si–SiO_x interface, which can occur during annealing [72], may also contribute to the observed enhancements.

The mobility of the nanowire devices can be extracted from the measured tranconductance $g_m = dI/dV_g$. At low biases, the following relationship governs transport in an ideal FET device [70]:

$$g_m = \frac{\mu C}{L^2} V_{sd}, \tag{1}$$

where C is the total gate capacitance and L is the channel length of the device. On the other hand, the measured transconductance g_{ex} with finite source/drain contact resistances is reduced from its intrinsic value g_{in} to [73]

$$g_{ex} = \frac{g_{in}}{1 + g_{in} R_s + (R_s + R_d)/R_{in}}, \tag{2}$$

where R_s and R_d are, respectively, the source and drain contact resistance, and R_{in} is the intrinsic nanowire resistance. From equation (2), it is clear that contact resistances can greatly influence the performance of nanowire transistors, and the extracted mobility using equation (1) may not reflect the true intrinsic mobility of the device. For example, in the extreme case when $R_s \gg 1/g_{in}$, $g_{ex} \sim 1/R_s$ and becomes independent of g_{in}. Such a scenario can occur either when the contacts are poor or when high performance transistors are desired such that even a small R_s is unfavourable due to the large g_{in}.

Zheng *et al* [74] carried out detailed studies on SiNW FETs with a geometry similar to that illustrated in figure 8. The SiNWs used in this study were n-type (doped with phosphorus). As expected, the nanowire devices exhibited depletion mode n-type MOSFET behaviour, as illustrated in figure 10. Interestingly, Zheng observed that the heavily doped devices (Si/P = 500) exhibit an apparent larger transconductance compared with the lightly doped devices (Si/P = 4000), at the same device geometry and bias voltage conditions. This observation, however, contradicts the predictions of equation (1), as the heavily doped NWs would suffer from increased impurity scattering and possess a lower mobility, as previously observed in bulk materials [70].

To understand this discrepancy, four-probe measurements [74] were carried out to study the effects of the contacts on g_m and μ, as illustrated in figure 11. As seen in figure 11(B), for the heavily doped sample (Si/P = 500), I–V_{sd} curve obtained from the four-probe measurement essentially coincides with

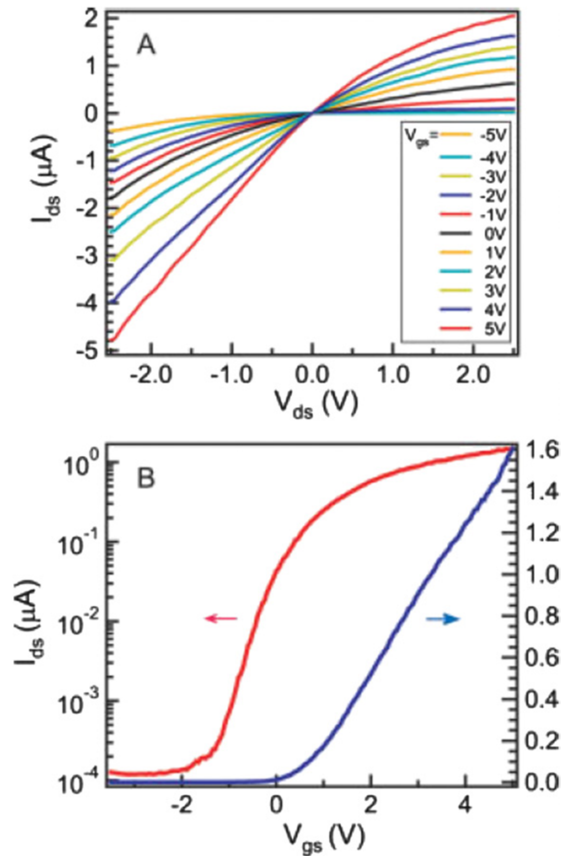

Figure 10. Electrical transport in a lightly doped n-type SiNW device. (A) I_{ds} versus V_{ds} curves recorded at different V_g. (B) I_{ds} versus V_g curve at V_{ds} = 1 V in linear (blue) and logarithmic scale (red), respectively [74]. (Colour online.)

that obtained form the two-probe measurement, indicating that the contact resistances are negligible. This can be understood from the fact that depletion width at the metal/semiconductor Schottky barrier is thin in the heavily doped samples, which in turn facilitates tunnelling and minimizes the contact resistance, in the same way as how effective Ohmic contacts are obtained in planar MOSFET devices [70]. As a result, the measured transconductance g_{ex} reflects the intrinsic transconductance g_{in}, and mobility values can be extracted from equation (1). On the other hand, for the lightly doped device (Si/P = 4000) in figure 11(C), the two-probe resistance is much larger than the four-probe resistance, indicating that contact resistance is substantial: the total resistance is ca 1 MΩ from the two-probe data, while the nanowire intrinsic resistance is only 300 kΩ from the four-probe data. After correction of the contact resistance effects using equation (2), Zheng found that the estimated intrinsic transconductance can be up to four times larger than the value deduced from the raw data. In figure 11(D) the average mobility values obtained on a number of devices are plotted versus the doping level. The extracted mobility decreases from 260 to 95 $cm^2 V^{-1} s^{-1}$ as the doping level increases, after correction of the series resistance effects. Significantly, these values are in good agreement with values reported for bulk Si [75], assuming the doping concentration is determined by the reactant ratio used to synthesize the NWs.

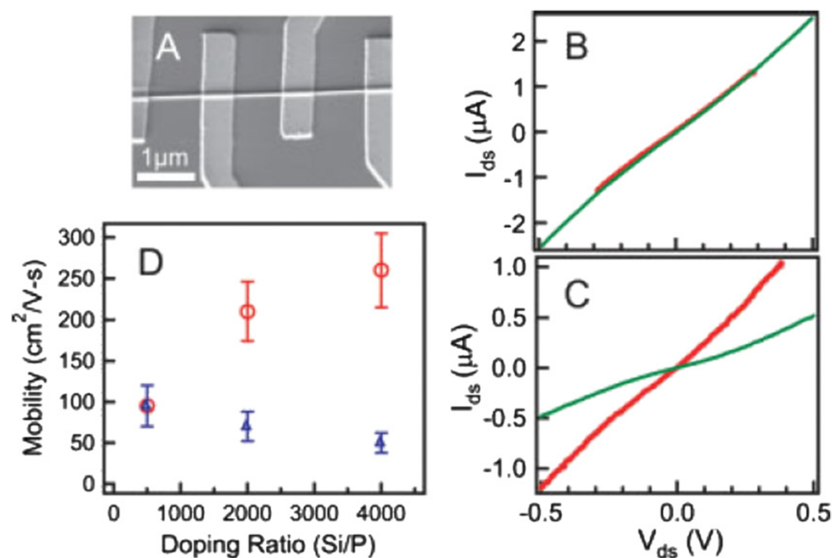

Figure 11. (A) SEM image of a typical SiNW device with four contacts used in the four-probe transport measurement. (B, C) I_{ds} versus V_{ds} data recorded on a SiNW using two-probe (thin green) and four-probe (thick red) contact geometries; the Si/P ratio is 500 : 1 for (B) and 4000 : 1 for (C). (D) Measured (blue triangles) and intrinsic (red circles) mobility values versus doping level [74]. (Colour online.)

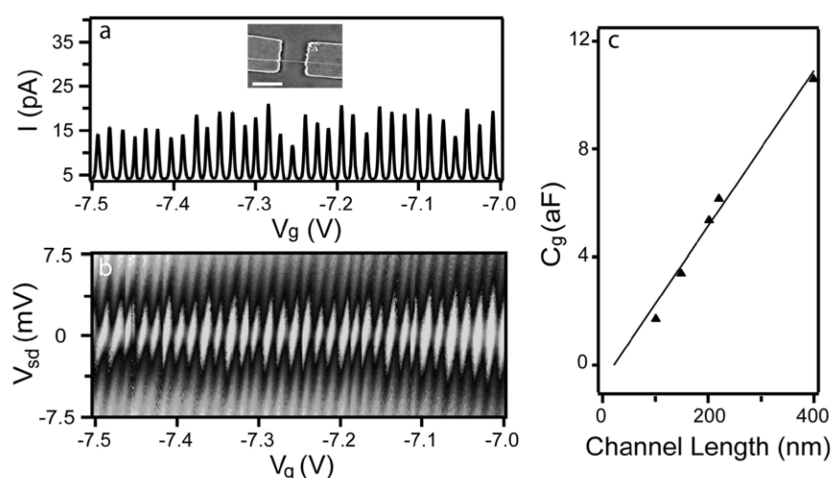

Figure 12. (*a*) CB oscillations observed at 4.2 K with $V_{sd} = 0.5$ mV. Inset: scanning electron microscopy (SEM) image of the device. Scale bar: 500 nm. (*b*) Greyscale plot of $\partial I/\partial V_{sd}$ versus V_{sd} and V_g recorded at 4.2 K; the light (dark) regions correspond to low (high) values of $\partial I/\partial V_{sd}$. (*c*) Gate capacitance versus source–drain separation (channel length) for 5 representative devices showing single-island CB behaviour. The line is a fit to the data with a slope of 28 ± 2 aF μm^{-1} [69].

3.1.2. Single-electron devices. Zhong *et al* realized that the Schottky barriers at the metal/Si contacts can serve as tunnel barriers [69]. At low temperatures the nanowire device effectively acts as a single-electron transistor (SET) when the charging energy e^2/C becomes larger than the thermal energy $k_B T$, where C is the total capacitance of the SET [76]. SET behaviour was first observed on InP nanowire devices [77] in an earlier study,. However, the tunnel barriers in these devices were formed by random defect potentials along the nanowire channel, resulting in multiple, randomly formed islands in series, with little control of the device parameters [77].

In Zhong's study, single crystal p-type SiNWs with diameters of 3–6 nm were synthesized by gold-nanocluster mediated VLS growth, using silane and diborane [11, 69, 78]. Unlike the studies on InP NWs [77], Zhong observed single island behaviour with the two tunnel barriers formed at the patterned S/D contacts, as evident in figure 12. In figure 12(*a*), current (I) versus gate voltage (V_g) data recorded with a 0.5 mV source–drain bias (V_{sd}) at 4.2 K was plotted for a device with source–drain separation of 400 nm. The I–V_g curve exhibits regular oscillations over a broad range of V_g, in which the current peaks are separated by regions of zero conductance with an average peak-to-peak separation of 0.015 ± 0.001 V. The heights of the observed peaks vary with V_g, although this variation has no obvious periodicity. The position and heights of the peaks are very reproducible on repeated V_g scans in this and similar devices. These observations indicate that the results are intrinsic to transport through the SiNWs and are moreover, consistent with the Coulomb blockade (CB) phenomena resulting from single charge tunnelling through a single quantum structure (e.g. the SiNW) with discrete energy levels [76, 79]. To define better the length-scale of the SiNW structure responsible for the CB oscillations, Zhong measured

the differential conductance ($\partial I/\partial V_{sd}$) versus V_{sd} and V_g for the device in figure 12((a). These data (figure 12(b)) show a set of well-defined conductance 'diamonds' in which the current is 'blocked' for values of V_{sd}–V_g in the light-coloured diamond regions due to the CB phenomena [76, 79]. In total, 33 CB diamonds were observed in figure 12(b). The regular closed diamond structure provides strong evidence of transport through a single quantum structure and not multiple QDs connected in series, which would exhibit a more complex overlapping diamond structure [79]. Key device parameters, including the gate capacitance, C_g and gate coupling factor, $\alpha = C_g/C$, where C is the total capacitance, can also be obtained from this measurement to be 10.7 aF and 0.33, respectively [69].

Data exhibiting closed diamonds consistent with transport through single QDs were obtained by Zhong on small-diameter SiNW devices with source–drain separations ranging from ca 100 to 400 nm [69]. Importantly, these data show that C_g scales linearly with source–drain separation (figure 12(c)) and, moreover, the average value of C_g determined from the data, 28 ± 2 aF μm^{-1}, agrees well with that calculated based on the device geometry. These results verify that the relevant dot size is defined by source–drain electrodes, since a QD size-scale set by structural variations or dopant fluctuations would give a smaller capacitance value and be independent of the source–drain separation. Small deviation of the gate capacitance from the estimated value were observed when the channel length is <100 nm and can be explained by screening from the source/drain electrodes when the channel length becomes comparable to the thickness of the gate dielectric [69].

In addition, variations in the current peak height versus V_g in figure 12(a) suggest transport is carried out through coherent energy states in the SiNW devices with the energy level spacing ΔE larger than the thermal energy $k_B T$. In this so-called 'quantum regime', peak heights are determined by the coupling of the individual quantum states to the metal contacts at the Fermi level [76]. To investigate this point further, Zhong characterized $\partial I/\partial V_{sd} - V_{sd} - V_g$ at a higher resolution for a 3 nm diameter SiNW device with a 100 nm source–drain separation, as shown in figure 13(a). The data exhibit well-defined peaks in $\partial I/\partial V_{sd}$ that appear as lines running parallel to the edges of the CB diamonds and are consistent with the formation of discrete single particle quantum levels extending across the SiNW device. Analysis of the data yields ΔE values for the first 6 levels of 2.5, 1.9, 3.0, 2.0, 2.0 and 2.9 meV. These values are in good agreement with $\Delta E = 2.5$ meV estimated using a 1D hard wall potential: $\Delta E = (N/2)\hbar^2\pi^2/m^*L^2$, where N is the number of holes, m^* is the silicon effective hole mass and L is the device length [69].

Temperature-dependent I–V_g measurements of the conductance peaks were also carried out. The representative data in figure 13(b) show that peak current decreases rapidly as the temperature is increased from 1.5 to 10 K and is approximately constant above 30 K. This behaviour is once again consistent with coherent tunnelling through a discrete SiNW quantum level that is resonant with the Fermi level of the metal contacts [76, 79]. Moreover, the temperature at which the peak becomes constant, 30 K, yields an estimate of $\Delta E \approx 3$ meV that agrees with the value determined from CB data and 1D model. The temperature dependence of the conductance peak width (W) also agrees well with predictions based on the coherent tunnelling through a single QD [76,79], as $\alpha W = 3.52 k_B T/e$ in the quantum regime ($k_B T < \Delta E$) and as $\alpha W = 4.35 k_B T/e$ in the classical regime ($\Delta E < k_B T < U$), where α is the gate coupling factor defined earlier.

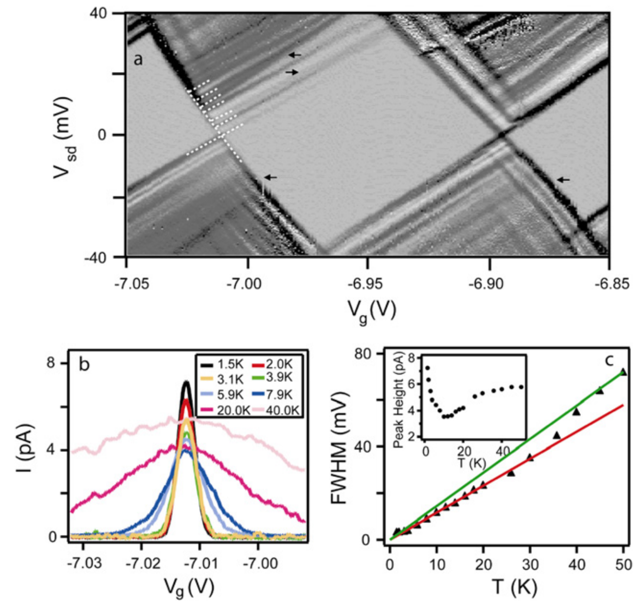

Figure 13. (a) $\partial I/\partial V_{sd}$–$V_{sd}$–$V_g$ data recorded at 1.5 K. Dark lines (peaks in $\partial I/\partial V_{sd}$) running parallel to the edges of the diamonds correspond to individual excited states. (b) Temperature-dependant I–V_g curves recorded with $V_{sd} = 50\,\mu$V. (c) Conductance peak widths in (b), determined from the full-width at half-maximum of the peak height, versus temperature. Solid lines correspond to theoretical predictions for peak widths versus temperature in the quantum regime ($\Delta E > k_B T$, red) and the classical regime ($\Delta E < k_B T$, green). Inset: temperature dependence of the conductance peak height [69]. (Colour online.)

The significance of observing coherent transport through a single island over length scales of several hundred nanometres lies in that it indicates these synthesized SiNWs are clean systems with little/no structural/dopant variations. This is in stark contrast to NWs fabricated by top-down lithography approaches, in which low-temperature studies have confirmed serially-connected QDs arising from variations in the potential due to structural and/or dopant fluctuations [80, 81]. In the SiNW case, smooth surfaces are favoured during the growth process which lowers the total free energy. Indeed, HRTEM shows [11, 69] that the SiNWs have a roughness of only ca 1–2 atomic layers over a length scale of 100 nm. Furthermore, dopants introduced during nanowire growth are likely driven to the surface of these molecular scale SiNWs, hence minimizes the charged impurity scattering as well, as reported for semiconductor nanocrystals [82].

3.2. Heterostructure nanowire devices

We have shown so far that contacts to homostructure NWs are usually dominated by Schottky barriers, a phenomenon verified by both room-temperature and low-temperature measurements. On the other hand, transparent Ohmic contacts are often desired, for example, to obtain high-performance transistor devices and to probe the intrinsic properties of

the nanowire itself. Transparent Ohmic contacts to the nanowire channel can be achieved in band-structure engineered heterostructure NWs. For example, in the Ge/Si core/shell nanowire heterostructure [23], the Fermi level, pinned inside the Si bandgap, may still lie below the Ge valence band due to the large band offset between Ge and Si (figure 5). This band line-up results in Ohmic contacts (i.e. negative Schottky barriers) to the Ge channel. Furthermore, since holes can be injected electrically from the contacts due to the energy band line-up, a hole gas can be formed in the Ge core even when both the core and shell are undoped, and the nanowire works as a depletion type device [23]. The Ge/Si core/shell NWs thus possess two key advantages compared with single component NWs: (1) transparent contacts to the conduction channel can be readily obtained and (2) dopant scattering can be eliminated. These improvements will open the door to a number of applications and studies, ranging from probing fundamental properties in low-dimensional systems to high-performance transistor devices [23].

The predicted improvements in the Ge/Si nanowire heterostructures were verified experimentally by Lu *et al* [23]. As seen in figure 14(*a*), contacts to the hole gas remain transparent even at low temperatures and when the device is close to be depleted, verifying the band line-up in figure 5. Furthermore, due to strong radial confinement of the holes in the Ge channel, discrete 1D subbands are formed and can be probed by transport measurements [83]. For each 1D subband, the energy dependence of density-of-states and group velocity cancel each other, resulting in an energy-independent conductance. The conductance for a spin-degenerate 1D subband is then a constant, $2e^2/h$, if no scattering occurs inside the channel [83]. In figure 14(*a*), the differential conductance ($\mathrm{d}I/\mathrm{d}V_{\mathrm{sd}}$) is plotted against the gate voltage V_{g} for a 170 nm long nanowire device. A back gate was used in this case. At 4.7 K, a conductance plateau was observed at a value close to $2e^2/h$ when the gate voltage was continuously varied, consistent with predictions from ballistic transport through the first 1D subband. This is an important observation, which implies the nanowire device is effectively a 1D device with only a single 1D subband participating in transport. Furthermore, the carriers move ballistically through the channel with little scattering, and the carrier mean free path is longer than the channel length.

To access multiple 1D subbands, Lu *et al* improved the gate coupling to the channel using a thin AlO_x dielectric layer and a top metal gate geometry so that higher Fermi energies can be achieved before gate leakage becomes substantial [23]. In figure 14(*b*), the differential conductance ($\mathrm{d}I/\mathrm{d}V_{\mathrm{sd}}$) obtained on a 14 nm diameter, top-gated nanowire device is plotted versus the bias voltage V_{sd} at different gate voltages V_{g}, with no offset added in the plot among the curves. The plateau region appears as dark regions where several G–V_{sd} curves at different gate voltage V_{g} overlap each other, since on the plateaus the conductance G is insensitive to changes in V_{g}. Up to four conductance plateaus at small bias (a–d) are clearly observed in this device. At larger bias, 'half-plateaus' (f–h) are also observed when the source and drain potentials cross different subbands [84, 85]. The energy level spacing can then be directly measured from the onset of the half-plateaus and are found to be consistent with predictions using cylindrically confinement potential [23].

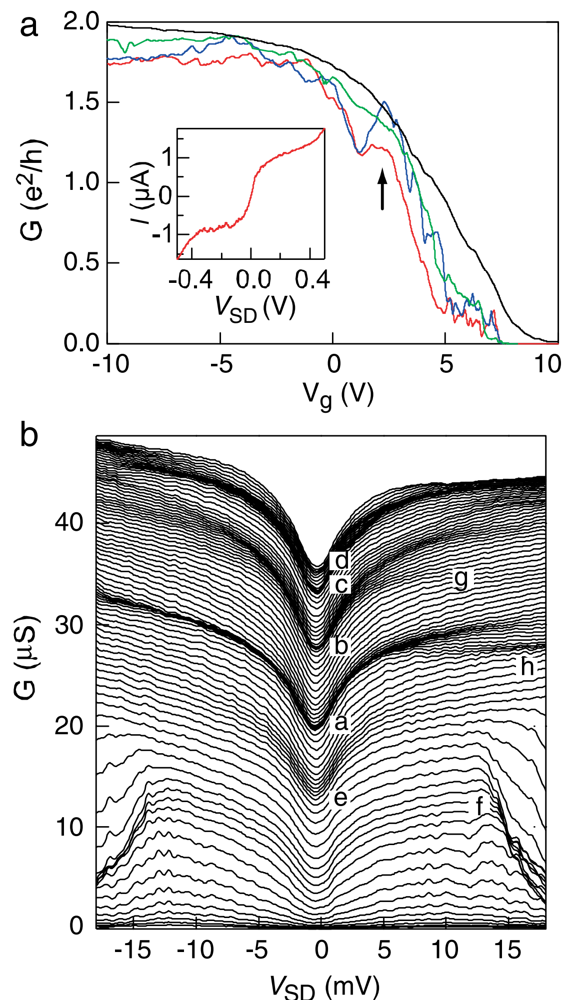

Figure 14. Transport through 1D subbands in Ge/Si nanowire devices. (*a*) G–V_{g} data recorded for a device ($L = 170$ nm) measured at different temperatures: black, green, blue and red correspond to 300 K, 50 K, 10 K and 4.7 K, respectively. (Inset) I–V_{sd} curve recorded at $V_{\mathrm{g}} = 10$ V. (*b*) G–V_{sd} plots for another device recorded at $V_{\mathrm{g}} = 0.8$ to -3.5 V in 50 mV steps with no offset applied ($T = 5$ K). Plateaus, labelled (a–g), appear dark because of accumulation of the G–V_{sd} traces. Adapted from [23]. (Colour online.)

The back-gated device in figure 14(*a*) also exhibited an interesting temperature-dependence behaviour. Notably, the basic shape of the G–V_{g} curve is preserved up to room temperature (300 K), and increasing temperature yields little change in the value of the conductance, although the slope becomes somewhat smeared. This implies that even at room temperature only a single 1D subband participates in transport and that the mean free path exceeds the channel length of 170 nm; that is, transport through the Ge/Si nanowire remains ballistic at this length scale at room temperature.

These results contrast data from planar 2DHG devices, where the mobility decreases dramatically with increasing temperature due to scattering with acoustic phonons [86]. In a 1D system, acoustic phonon scattering is expected to be suppressed due to the reduced phase space for back-scattering [87]. In Ge/Si NWs, the acoustic phonon scattering rate can be estimated using Fermi's golden rule as $(1/\tau_{\mathrm{ap}}) = (\pi k_{\mathrm{B}} T \Xi^2/\hbar\rho v_{\mathrm{s}}^2) D(E_{\mathrm{F}})$, where Ξ is the

deformation potential, ρ is the mass density and v_s is the velocity of sound. The density of states can be calculated as $D(E) = (\sqrt{2m^*}/\pi\hbar\sqrt{E})(1/\pi r^2)$ for the first subband using the effective mass for heavy holes, $m^* = 0.28m_e$ [27, 70], where m_e is the free electron mass. $\tau_{ap} \sim 4.9 \times 10^{-12}$ s was estimated at room temperature for a 10 nm core diameter nanowire at $E_F = 10$ meV, using an average sound velocity of 5400 m s^{-1} and deformation potential of 3.81 eV for Ge [27, 88]. The mean free path calculated using this value of τ_{ap} and the Fermi velocity, $v_F = \sqrt{2E_F/m^*} \sim 1.1 \times 10^5$ m s^{-1}, is 540 nm. This estimate is consistent with the experimental results and, moreover, suggests that room-temperature ballistic transport in Ge/Si NWs is possible on a 0.5 μm scale, assuming other scattering processes are suppressed. Room-temperature ballistic transport has been reported previously in metallic and semiconducting CNTs [89, 90] and was attributed to the topological singularity at $k = 0$ due to its unique band structure in metallic nanotubes [91, 92]. Reduced acoustic phonon scattering in 1D explains room-temperature ballistic transport in Ge/Si NWs, although a more detailed theoretical analysis, including the confinement effects of phonon modes, will be needed to quantify the limits of this interesting behaviour.

The small size and long mean free path of the 1D hole gas offer unique opportunities to explore new phenomena in nanoscale, low-dimension systems. For example, a small feature has been found to be always present below the first conductance plateau in the Ge/Si system, as illustrated by the arrow in figure 14(*a*). Such a feature, termed the '0.7 structure' from its height with respect to the full conductance on the plateau, has been observed previously on quantum point contacts and quantum wires formed in clean 2D electron gas samples [84, 93, 94]. This feature is generally believed to be caused by spontaneous spin polarization in low-dimensional interacting electron gas systems [93] due to the formation of a spin gap [94] or a localized spin [84]. Temperature-dependence data in figure 14(*a*) show that the 0.7 feature initially increases in magnitude and then broadens as temperature is increased to 50 K, consistent with the spin-gap hypothesis [94]. These results suggest that the 0.7 structure is not restricted to electron gas samples but is a universal phenomenon in 1D systems. In this regard, the heavier effective mass of holes in Ge/Si NWs will yield a larger interaction parameter compared with electrons [95, 96]; this together with the strong confinement effects and a uniform confinement potential along the channel should make Ge/Si heterostructure NWs an ideal platform to study such novel effects in the future.

At room temperature, these Ge/Si NWs are expected to be suitable in ultra-high performance transistor applications, due to the long mean path and transparent contacts to these devices. To further explore their potential, Xiang *et al* fabricated transistor devices using thin HfO_2 or ZrO_2 high-κ gate dielectrics and metal top gate electrodes [97] (figures 15(*a*) and (*b*), so that gate coupling in the transistor devices is further improved. Atomic layer deposition (ALD) was used to deposit a thin high-κ dielectric film using Tetrakis (dimethylamino) hafnium [$Hf(N(CH_3)_2)_4$] or tetrakis (dimethylamino) zirconium as precursors [97]. Following the fabrication of source/drain contacts, a second electron beam lithography step was used to define the top gate. The conformal top gate structure was confirmed by cross-sectional transmission electron microscopy (TEM) images, as shown in figure 15(*b*). Compared with previous back-gated devices, the top gate structure approaches an ideal cylindrical gate geometry and together with the high-κ dielectrics produces a much more efficient gate response [98].

A large number of Ge/Si NWFET devices with L varying from 1 μm to 190 nm were fabricated and measured. Essentially all the devices exhibited high performance behaviour and testify to the reproducibility of the Ge/Si NWs and contacts to this material. Representative data obtained from a device with a channel length, $L = 1\,\mu$m, and a total diameter of 18 nm (device A) and another device with $L = 190$ nm (device B) are plotted in figures 15(*c*)–(*e*). The I_d–V_g transfer curve recorded for device A at $V_{ds} = -1$ V (figure 15(*d*)) shows that the NWFET has a peak transconductance, $g_m = dI_d/dV_g$, of 26 μS and a maximum drain current I_{dmax} of 35 μA at $V_g = -2$ V. An even better performance was achieved for device B due to the reduced channel length, with $g_m = 60\,\mu$S, and $I_{dmax} = 91\,\mu$A. These values represent the best performance reported to date in single semiconductor NWFETs [12, 66].

To compare the performance of NWFETs with planar devices in which a single voltage V_{dd} sets the range of V_g and V_{ds}, a universal definition of the on and off current values needs to be adopted. Following conventions in planar devices, the on and off current values are defined as the values measured at $V_g(\mathrm{on}) = V_T - 0.7V_{dd}$ and $V_g(\mathrm{off}) = V_T + 0.3V_{dd}$, so that 30% of the V_g swing above the threshold voltage V_T is applied to turn the device off, while the remaining 70% sets the operation range of the on state. Similar methods have been proposed in benchmarking nanoscale FET devices in general [99, 100]. Using this convention, $g_m = 60\,\mu$S, $I_{on} = 37\,\mu$A ($V_{dd} = 1$ V) were obtained for device B. These values correspond to scaled g_m and I_{on} of 3.3 mS μm^{-1} and 2.1 mA μm^{-1}, respectively, using the total nanowire diameter as the device width. Notably, these values are 3–4 times better than the values of 0.8 mS μm^{-1} and 0.71 mA μm^{-1} recently reported in state-of-the-art, sub-100 nm silicon p-MOSFETs employing high-κ dielectrics [101]. The geometric gate capacitance per unit area in the NWFETs was estimated to be at most 29% larger than in Si p-MOSFETs [97]. Therefore, the large improvement in g_m and I_{on} cannot be accounted for by the increase in gate capacitance alone. Moreover, the hole mobility for device B, 730 cm^2 (V s)$^{-1}$, extracted from the peak $g_m = 3\,\mu$S at 10 mV bias using the charge control model represents more than a factor of 10 improvement over that of the Si pMOSFET with HfO_2 gate dielectric (50–60 cm^2 (V s)$^{-1}$) [101] and is also more than twice the reported mobility of Ge and strained SiGe heterostructure PMOS devices [102, 103]. Improved mobility was consistently observed for Ge/Si NWFETs with channel lengths from 0.19 to 1 μm, with an average of 640 cm^2 (V s)$^{-1}$. These improvements over planar device structures, obtained with benchmarked transistor data, clearly verify the performance benefit in clean Ge/Si heterostructure NWs.

The subthreshold region of the I_d–V_g data was also analysed and yields values of the slope, $S = [d(\log_{10} I_d)/dV_g]^{-1}$, of 105 mV/decade and 100 mV/decade for the $L = 1\,\mu$m and 190 nm NWFETs, respectively, at

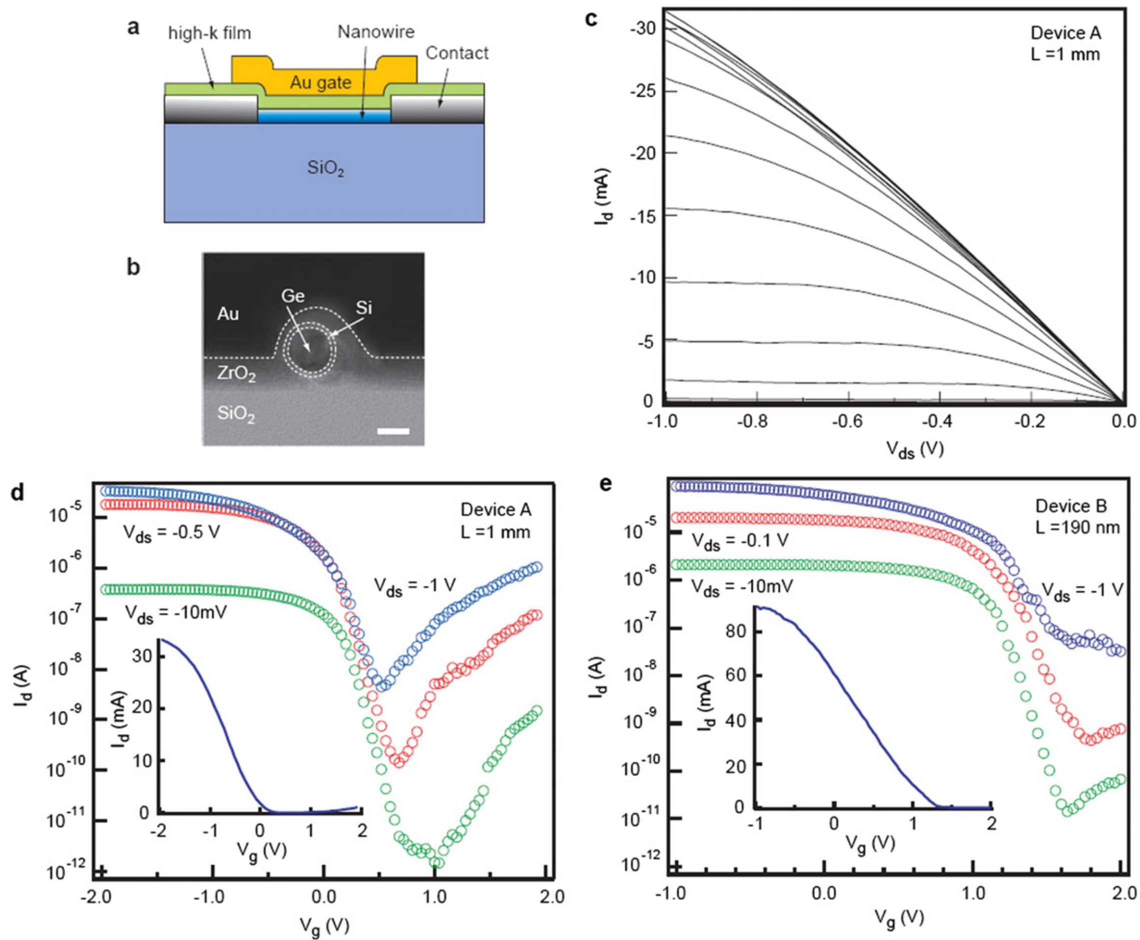

Figure 15. (*a*) Schematic and (*b*) cross-sectional TEM image of a top-gated Ge/Si core/shell nanowire FET device. (*c*) I_d–V_{ds} data for device A ($L = 1\,\mu$m) with $V_g = -2$–2 V in 0.25 V steps from top to bottom. (*d*) I_d–V_g for device A, with blue, red and green data points corresponding to V_{ds} values of -1 V, -0.5 V and -0.01 V, respectively. Inset, linear scale plot of I_d versus V_g measured at $V_{ds} = -1$ V. (*e*) I_d–V_g data for device B ($L = 190$ nm) with blue, red and green data points corresponding to V_{ds} values of -1, -0.1 and -0.01 V, respectively. Inset: Linear scale plot of I_d versus V_g measured at $V_{ds} = -1$ V. Adapted from [97]. (Colour online.)

$V_{ds} = -1$ V (figures 15(*d*) and (*e*)). The observed S values show little bias voltage dependence for both devices, an indication that good control of short channel effects [104] can be obtained on the NW devices down to at least $L = 190$ nm. In general, an FET with a small S is essential for modern logic circuits as it reduces the off-state current and minimizes static power dissipation. The value of S can be estimated [70] by $2.3k_B T/e\alpha$, where α is the gate-coupling factor, which yields a room-temperature minimum ($\alpha = 1$) of 60 mV dec^{-1}. The values of S determined for the $L = 1\,\mu$m and 190 nm Ge/Si NWFETs are superior to the best value (140 mV dec^{-1}) reported previously [105] for NWFETs but still larger than the theoretical minimum. The non-ideal gate coupling ($\alpha < 1$), which causes this larger S, is likely due to a finite trap state density at the NW/high-κ interface [106]. Optimization of the high-κ deposition process during fabrication or growth of a cylindrical high-κ shell on the Ge/Si NW prior to fabrication should yield improved interface quality and enable ideal subthreshold behaviour in the future in these NWFETs.

The performance of the Ge/Si nanowire devices are also compared with planar Si devices using the intrinsic delay benchmark [100], $\tau = CV/I$, where C is the gate capacitance, $V = V_{dd}$ and I is the on current I_{on}. As defined, τ represents the fundamental *RC* delay of the device and provides a frequency limit for transistor operation that is relatively insensitive to gate dielectrics and device width and thus represents a good parameter for comparing different types of devices [104]. Xiang *et al* found that the Ge/Si nanowire devices show clear speed advantage at a given L versus Si p-MOSFETs, and length scaling of τ is also more favourable for the Ge/Si NWFETs than for the Si MOSFETs [97]. Such a difference can be attributed to a suppression of scattering in the quasi-1D quantum confined Ge/Si NWs versus MOSFETs [23], although additional studies will be needed to support this hypothesis.

4. Assembly and integration techniques

As can be seen in the case of Ge/Si core/shell NWs, the quasi-1D transport nature and clean material structure of the nanowire system result in superior device performance, compared with even state-of-the-art planar devices [97]. However, the discussions so far are limited to the individual device level. To fully explore the potential of NW building blocks for integrated devices and circuits, efficient and scalable strategies are needed to assemble large amount of NWs into increasingly complex architectures. In this regard, two

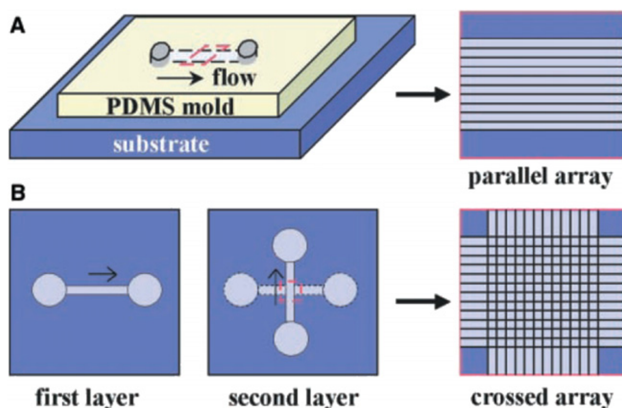

Figure 16. Schematic of the fluidic flow alignment process. (A) NW assembly was carried out by flowing a NW suspension with a controlled flow rate for a set duration inside the channel formed between the PDMS mould and a flat substrate. (B) Multiple crossed NW arrays can be obtained by changing the flow direction sequentially in a layer-by-layer assembly process [109].

key gradients are involved in the large scale assembly and integration of nanowire devices. First, methods are needed to assemble NWs into highly integrated arrays with controlled orientation and spatial position. Second, approaches must be devised to assemble NWs on multiple length scales and to make interconnects between nano-, micro- and macroscopic worlds. To date, several different approaches have been adopted to address these issues and are briefly reviewed in this chapter.

4.1. Fluidic flow-directed assembly technique

The first successful demonstration of rational assembly of NWs was achieved with the electric field assembly technique developed by Duan *et al*, by noting that NWs tend to align with the direction of an applied electric field [107]. Duan showed that individual wires can be positioned to bridge pairs of diametrically opposed electrodes and form a parallel array. Crossed nanowire structures can also be achieved by changing the direction of the electric field in a layer by layer fashion [107]. However, electric field assembly suffers from several limitations, including (1) the need to pattern microelectrode arrays used to produce aligning fields and (2) the deleterious effect of fringing electric fields at the submicron length scales resulting in misalignment. To address theses issues, a simple, fluidic flow-directed assembly method was independently developed by the Lieber group at Harvard and the Yang group at UC Berkeley.

In the fluidic flow-directed assembly method, nanowire alignment is achieved by passing a suspension of NWs through a microfluidic channel, for example, formed between a poly(dimethylsiloxane) (PDMS) mould [108, 109] and a flat substrate (figure 16(A)). Virtually all NWs can be aligned along the flow direction at an adequate flow rate, leaving an array of parallel NWs assembled on the substrate surface within the microfluidic channel [109]. The alignment can be readily extended to over hundreds of micrometres and is limited only by the size of the fluidic channel being used. The alignment of NWs within the channel flow can be understood within the framework of shear flow [110, 111]. Specifically, the channel flow near the substrate surface resembles a shear flow, and linear shear force aligns the NWs in the flow direction before they are immobilized on the substrate.

The average NW surface coverage can be controlled by the flow duration. Huang found that the NW density increases systematically with the flow duration at a constant flow rate [109]. For example, a flow duration of 30 min produced a density of about 250 NWs per 100 mm or an average NW–NW separation of $\sim$ 400 nm, and NW spacing on the order of 100 nm or less can be achieved with an extended deposition time.

Using a layer-by-layer deposition process, more complex crossed NW structures can be obtained with the fluidic flow assembly approach (figure 16(B)). The layer-by-layer approach requires that the nanowire–substrate interaction is sufficiently strong so that sequential flow steps will not affect the existing patterns, a condition that can be achieved by modifying the substrate surface with proper functional chemical groups. For example, crossbar structures with high yield have been demonstrated by alternated flow in orthogonal directions in a two-step assembly process [109].

The fluid flow alignment technique offers several advantages compared with pervious attempts. First, it is an intrinsically parallel process without the need for patterned electrodes. Second, this approach is applicable for virtually any elongated nanostructure including CNTs and DNA molecules. Third, it allows for the directed assembly of geometrically complex structures by simply controlling the angles between flow directions in sequential assembly steps. For example, equilateral triangles have been assembled in a three-layer deposition sequence [109]. Finally, since each layer is independent in the flow alignment process, a variety of homo- and hetero-junction configurations can be obtained by simply changing the composition of the NW suspension used in each step [107, 112]. However, controlled assembly of NWs with the fluidic flow method at larger scales ($>$ centimetre) is less practical and remains to be demonstrated.

4.2. Langmuir–Blodgett (LB) assembly technique

For hierarchically organizing NW building blocks *en masse* into integrated arrays tiled over large areas, an alternative solution-based approach was developed by the Lieber group and the Yang group [113–115]. This approach (figure 17) exploits the LB technique [116] to uniaxially compress a NW-surfactant monolayer on an aqueous subphase, thereby producing aligned NWs with controlled spacing. The compressed layer is then transferred in a single step to a planar substrate to yield parallel NWs covering the entire substrate surface [113]. Similar to flow alignment, this sequence of steps can be repeated one or more times to produce crossed and more complex NW structures, where the NWs can be the same or different in sequential layers.

In the study carried out by Whang *et al* [113], stable NW suspensions in non-polar solvents were produced using the surfactant 1-octadecylamine, which coordinates reversibly to NW surfaces. The NW suspensions were then spread on the surface of the aqueous phase in a LB trough and compressed. During compression, NWs become aligned along their long axes with the average spacing (centre-to-centre distance) controlled by the compression process. Wafers covered with

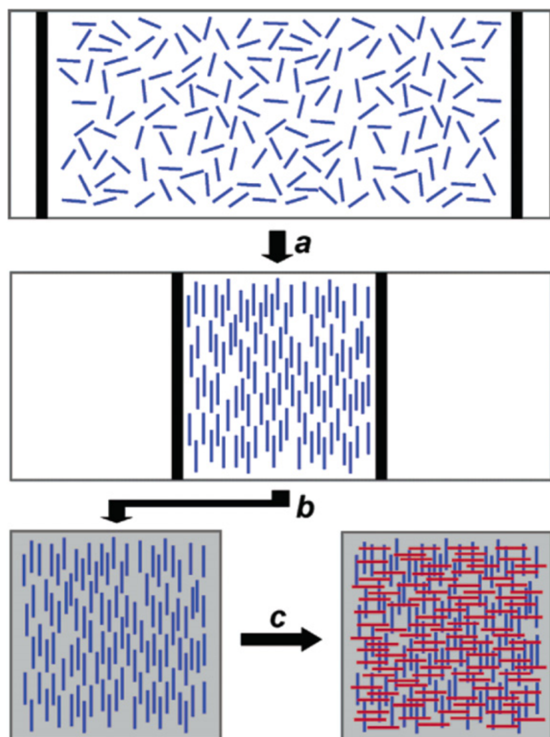

Figure 17. Schematic of the LB alignment process. (*a*) NWs (blue lines) in a monolayer of surfactant at the air–water interface are compressed in a LB trough to a specified pitch. (*b*) The aligned NWs are transferred to the surface of a substrate to make a uniform parallel array. (*c*) Crossed NW structures are formed by uniform transfer of a second layer of aligned parallel NWs (red lines) perpendicular to the first layer (blue lines) [113]. (Colour online.)

aligned NWs with areas up to 20 cm^2 were demonstrated [113], and this approach can in principle be applied to even larger area substrates [117]. Significantly, the spacing of the transferred NWs can be well controlled ranging from micrometre scale to close-packed structures during the compression process [113]. In general, the transferred NW arrays have similar quality for spacings from ca 2 μm (the largest studied) to 200 nm. Compression to spacings below ca 200 nm leads to increasing aggregation due to strong inter-NW attractive forces, although aligned close-packed monolayer structures can be transferred [113]. This latter capability was explored to produce ultra-high-density NW arrays with NW spacing on the nanometre scale, by first compressing NWs coated with a sacrificial layer, followed by removing the sacrificial layer once transferred [30]. For example, core/shell Si/SiO_2 NWs, in which the oxide shell thickness can be controlled precisely during NW growth [113], were compressed to close packed structures and the resulting parallel wire pattern after removing the SiO_2 shell was subsequently transferred to the Si substrate [113].

The aligned NW structures exhibit features similar to a nematic liquid crystal phase, including fluctuations in the average alignment direction and poor end-to-end registry. These non-uniform features are distinct from the precise structures familiar to conventional top-down fabrication. These issues, however, may not represent serious impediments to making integrated and interconnected devices. This is because interconnected finite-size arrays of nanoscale devices are more desirable than monolithic structures for integrated nanosystems, since hierarchical organization reduces the probability that small numbers of defects will cause catastrophic failure in the whole system [118]. Hence, by adjusting the array size to be less than the average NW length it is possible to minimize the number of NWs that fail to span the width of an array due to poor end-to-end registry. As a result, the solution based method enables the specific NW building block, NW pitch, NW orientation, array size, array orientation and array pitch, to be controlled independently for sequential depositions and thus offers a flexible pathway for bottom-up assembly of NW and nanotube materials into integrated and hierarchically organized structures.

5. Nanowire circuits

5.1. NW crossbar circuits

Implementation of the nanowire devices in ultra-high density, large-scale application will likely in turn require the implementation of novel architectures [1]. This includes both nano-architectures at the circuit level that link large numbers of devices with each other and with external systems to perform memory and/or logic functions as well as system architectures that allow the circuits to communicate with other systems and operate independently of their lower-level details. In particular, since traditional defect-free oriented processes will likely no longer be feasible at the molecular scale, the new architectures must be defect-tolerant [119]. Reconfigurable architectures [1], particularly crossbar structures [118,120–126] in which active devices are formed at the intersections when two sets of wires cross each other, have been demonstrated to possess desirable properties at both the nano-architecture as well as the system-architecture level.

In an earlier proof-of-concept study, Duan *et al* [107] and Huang *et al* [127] have shown that prototype logic circuits can be achieved on crossed nanowire p/n junctions. In these studies, the cross-wire structures were achieved via flow-alignment, and devices at the single to few NW levels were examined. To implement desired hierarchical patterning of arrays of aligned and crossed NWs at centimetre scale, Whang *et al* developed a technique in which locating individual NWs to the desired positions is no longer required [113]. In Whang's approach, a monolayer of aligned NWs was produced first via the LB approach. Photolithography was then used to define a pattern over the entire substrate surface which sets the array dimensions and array pitch. Finally, NWs outside the patterned array were removed by gentle sonication, resulting in arrays of parallel NWs at desired locations (figure 18).

To produce crossed NW arrays, sequential layers of aligned NWs were transferred in an orthogonal orientation and were patterned in the same fashion as described above (figure 18) [30,113]. figure 18(C) shows an image of a 10 μm $\times$ 10 μm square array with a 25 μm array pitch, and demonstrates that such a method provides ready and scalable access to ordered arrays over large areas. The nanowire array exhibits order on multiple length scales: 40 nm diameter NWs, 0.5 μm NW spacing, 10 μm array size, 25 μm array pitch repeated over centimetres—that is representative of the substantial control

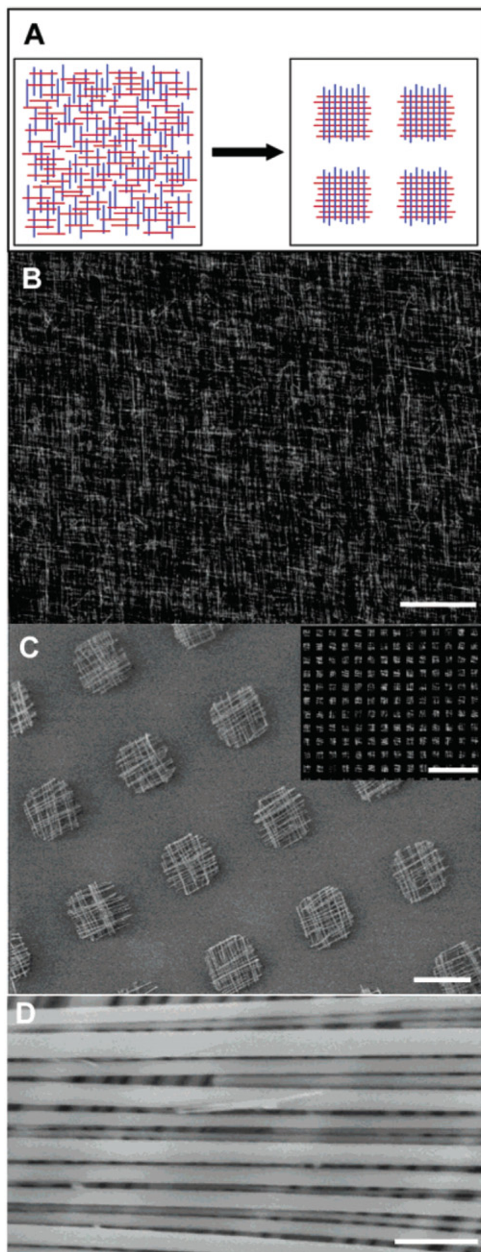

Figure 18. (A) Hierarchical patterning of crossed NW arrays by photo-lithography, where NWs are removed from regions outside of the defined array pattern. (B) Dark-field optical micrograph of crossed NWs deposited uniformly on a 1 cm × 1 cm substrate. Scale bar: 50 μm. (C) SEM image of patterned crossed NW arrays. Scale bar: 10 μm. (Inset) Large area dark-field optical micrograph of the patterned crossed NW arrays. Scale bar: 100 μm. (D) SEM image of an ultra-high density crossed NW array. Scale bar: 200 nm [113].

enabled by the LB approach. Array geometries and tiling patterns more complex than square structures are also believed to be achievable [113].

5.2. Address decoders

In order to communicate and control the very large number of NWs used in each crossbar array with a limited number of conventional, microscale control wires, address decoders are necessary which serve as a needed interface. Address decoders are logic circuits that can use an address code to select and transmit signals from multiple input wires to a single output wire (or from a single input wire to one of several output wires). The scaling advantage of a decoder is that it only requires n pairs of address wires to select and control 2^n NWs, e.g. ten pairs of address wires can in principle control 1024 (2^{10}) NWs. As a result, 20 pairs of address wires might be sufficient to completely address a 1 Mbit crossbar memory [118].

DeHon *et al* [120] proposed that if modulation doping along the nanowire axis can be achieved that results in controlled shifts in the threshold voltages V_T, individual NWs can be uniquely addressed with a set of microscale control wires. Furthermore, DeHon argued that if the coded NWs are chosen at random from a sufficiently large population, a large fraction (>99%) of the selected NWs will have unique addresses, even without knowledge of the specific locations of the coded regions [120]. Such a stochastic decoding scheme is ideally suited for nanowire-based crossbar applications, since during the assembly (flow-alignment or LB alignment) process, the registry of the NWs is generally lost, resulting in arrays of aligned albeit randomly positioned NWs.

Zhong *et al* obtained the first prototype nanowire decoder in which the shifts in V_T were achieved through surface modification at the corresponding crosspoints [128]. In a recent study, Yang *et al* demonstrated that modulation doping of the NWs can be achieved during growth, hence paving the way for an all-nanowire-based system [15]. A local substrate heater (versus a tube furnace reactor) was used in Yang's study to minimize spontaneous dissociation of the precursors away from the catalysts, since coating of doped Si over the nanowire surface will interfere with the axial modulation doping effects. Furthermore, the growth was carried out in a H_2 atmosphere, which further suppresses the decomposition of silane and inhibits deposition on the nanowire surface [12, 13]. To verify that modulation doping was indeed achieved along the nanowire growth direction, Yang used scanning gate microscopy (SGM) [20, 129] to measure gate response of different regions within a single nanowire. In such a study, a conducting atomic force microscopy probe with an applied voltage (V_{tip}) functions as a spatially localized gate, which enables the conductance of the nanowire with pre-fabricated source and drain contacts to be varied and mapped. Results obtained from SGM studies on modulation doped n-type SiNWs are shown in figure 19, in which the dark regions correspond to lightly-doped n regions which show excellent gate response and bright regions correspond to heavily-doped n^+ regions which show little gate response [15]. The SGM studies clearly verified that modulation doping along the nanowire axis can be achieved with full control of the size, spacing and number of the modulated regions during the growth process. Prototype crossed nanowire/microscale-control-wire decoder arrays were also fabricated and tested in Yang's study, and behaviours of such devices were shown to follow DeHon's proposal [15, 120].

The demonstration of modulation doping, along with the success in producing axial and radial nanowire heterostructures [20, 22, 23], implies that specific functions can be built into the system during growth, instead of having to be defined by intermediate lithographic patterning and/or electrical contacts fabricated after growth. For example, many of the wiring

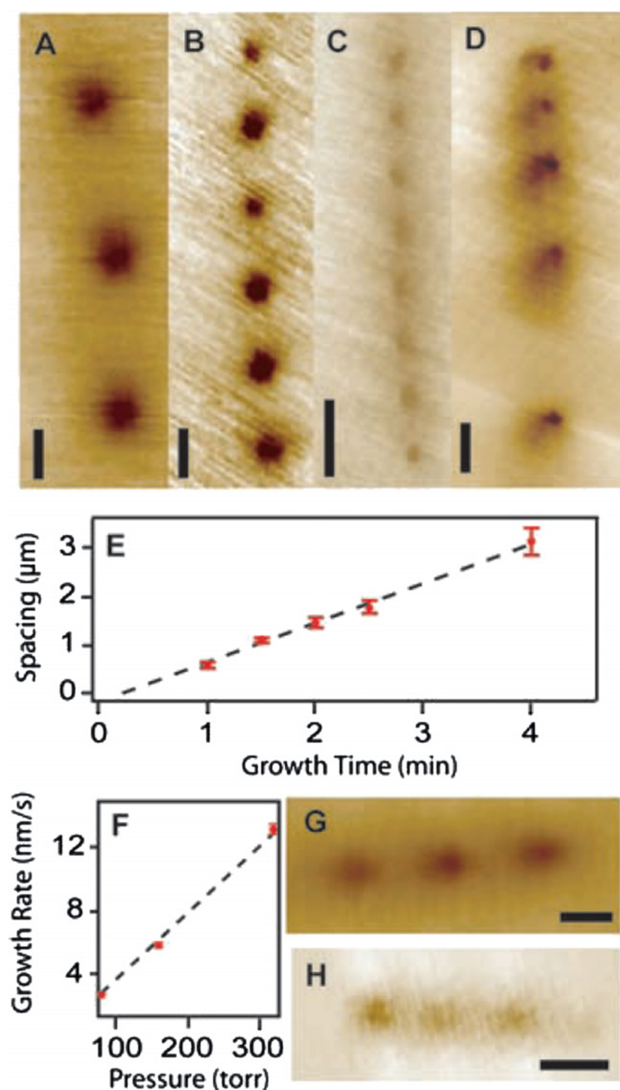

Figure 19. SGM images of n^+–$(n\text{-}n^+)_N$ NWs where (A) $N = 3$, (B) $N = 6$ and (C) $N = 8$. The growth times for the n/n^+ regions are 1/3 min, 1/1 min and 0.5/0.5 min, respectively. (D) SGM image of a $N = 5$ nanowire device. The growth time for the n regions is 0.5 min and n^+ sections are 0.5, 1, 2 and 4 min. Scale bars: 1 μm. (E) Repeat spacing versus growth time at total pressure of 320 Torr. (F) Growth rate versus growth pressure. SGM images of n^+–$(n\text{-}n^+)_3$ modulation-doped NWs synthesized with total pressures of (G) 160 torr and (H) 80 torr. The growth time for each n and n^+ region is 15 s. Scale bars: 100 nm [15].

steps normally created by lithography can now be encoded by varying the doping sequence of the NWs so that the only post-fabrication lithographic steps would be those involved in making external input and output contacts to the much fewer control wires. The ability to encode the system in a controlled fashion also opens opportunities to functionalize different segments along the wire with specific binding molecules and may eventually lead to the realization of the ultimate bottom-up integrated circuits—nanocircuits produced exclusively via self-assembly without involvement of top-down fabrication techniques.

5.3. NW devices on non-crystalline substrates

Another potential application of nanowire-based electronics is devices on non-crystalline substrates such as plastics and glass. Devices made on these low-cost and lightweight substrates serve as the basis for a large and rapidly growing class of electronics applications, including flat-panel displays, smart cards and wearable displays [130–133]. Compared with existing approaches based on amorphous silicon and organic semiconductors, the single-crystalline nanowire-based devices offer much higher mobility and device performance. Furthermore, even though comparable mobility may be obtained on polycrystalline silicon devices, the additional steps and higher-temperature processing required to achieve high-quality polycrystalline silicon represent limitations in the implementation of polycrystalline silicon transistors on large-scale glass and plastic substrates [133].

One key advantage of solution-based assembly methods of high-performance semiconductor nanowire devices is the ability to separate the high-temperature material growth stage from the low-temperature device fabrication stage. In the first stage, the synthesis of NW building blocks is carried out under conditions optimized to yield high-quality single-crystal materials, where the desired electronic and/or photonic functions are defined by material composition, structure and diameter. Since the growth stage is independent of the second stage in which active devices are fabricated, there is no need to be concerned with thermal and other substrate limitations, in contrast to direct thin-film deposition methods. In the device fabrication stage, the NWs are isolated as stable solution suspensions, and deposition and patterning of devices are carried out as discussed earlier. In this sense, the use of NW suspensions has the same processing advantages as the use of organic semiconductors [134, 135], except that material properties are greatly improved in the NW case. Different functions can also be introduced on the same substrate through sequential transfer of NWs with desired properties [109, 127, 136], and advanced lithography is no longer necessary in these applications. For example, a layer of aligned NWs produced by the flow alignment or Lanmuir–Bloggett assembly method can be treated effectively as a thin-film material, and devices can be fabricated using the same techniques as in a conventional thin-film transistor process.

Using this approach, McAppline *et al* demonstrated logic and photonic devices on glass and plastic substrates using single-crystalline Si and GaN NWs [136]. The measured mobility of the SiNW devices is independent of the substrate ($\sim$200–300 $\mathrm{cm^2(V\,s)^{-1}}$) and is 2–3 orders better than that obtained in amorphous Si or organic devices [137, 138]. Furthermore, the performance of devices fabricated on a plastic substrate shows little degradation when bent (figure 20), verifying the potential of nanowire-based devices in applications such as flexible displays. In a separate study, Duan *et al* reported fabrication of thin-film transistors on a plastic substrate using aligned SiNWs and demonstrated the performance advantage of nanowire thin-film transistors compared with amorphous silicon and organic thin-film transistors [139]. Following the same approach, Friedman *et al* recently demonstrated a three-state ring-oscillator using silicon NWs [140]. Flow alignment and conventional photo-lithography were used to fabricate the device. The ring-oscillator was composed of more than 100 NWs and exhibited an oscillation frequency of ca 11 MHz on Si substrate. Significantly, contrary to conventional planar

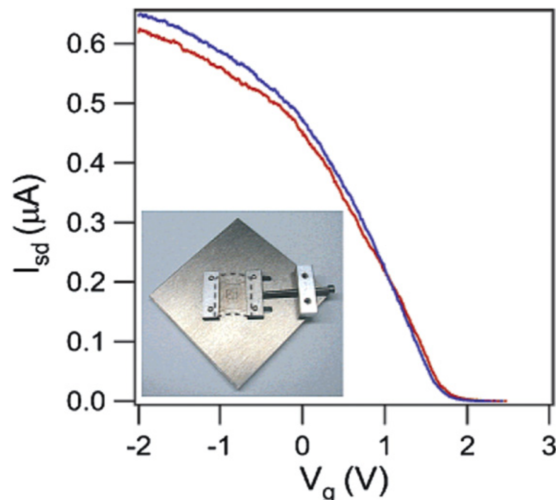

Figure 20. I versus V_g data recorded when the NW/plastic device was flat (blue) versus bent to a radius of curvature of 0.3 cm (red) [136]. (Colour online.)

devices which exhibit degradation in device performance when transferred to non-crystalline substrates, Friedman observed that the nanowire ring-oscillators in fact exhibited higher operating frequencies when fabricated on glass substrates. This observation can be explained from the insensitivity of nanowire devices to substrates and the reduction in the stray capacitance on the insulating glass substrate compared to conducting Si substrate [140].

6. Conclusion

The area of semiconductor NWs has been constantly gaining interest and momentum among science and engineering communities since the late 1990s. In this review, we attempted to summarize progresses made in this field during the last several years, ranging from nanowire growth with precise control at the atomic level to device characterization that probes novel properties in 1D systems and novel device structures, and to integration and assembly methods of large numbers of NWs for practical applications. The key ingredients in the semiconductor nanowire system include the single-crystalline nature of the material, strong quantum confinement effects due to the small diameter and the ability to carry out tailored growth with desired shape, size and material composition (including radial and axial nanowire heterostructures). The separation of high-temperature growth and low-temperature device fabrication processes also implies that nanowire devices are well suited to applications on non-crystalline substrates such as flexible electronics.

Because of their high carrier mobility and large surface area, semiconductor NWs have also been studied in a variety of applications besides high-performance electronics, including dye-sensitized solar cells [141], label-free, ultra-sensitive bio- [142, 143] and chemical sensors [49, 144]. By exploiting the optical cavity and/or waveguide properties of the semiconductor material, nanowire-based on-chip photonic devices and circuits have been demonstrated as well, including light-emitting diodes [107], lasers [146–149], active waveguides [150, 151] and integrated electro-optic modulators [150, 152]. Such topics are beyond the scope of this review and interested readers are referred to the corresponding references listed above.

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