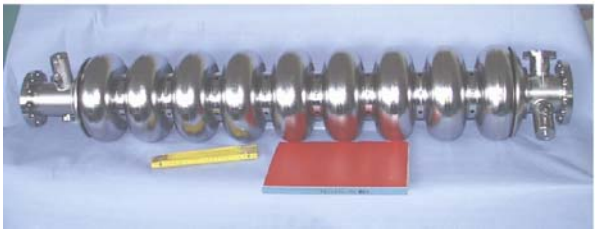

SRF 

# FPGA and optical network based LLRF distributed control system for TESLA-XFEL Linear Accelerator

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*1) Institute of Electronic Systems, Nowowiejska 15/19, 00-665 Warsaw, Poland*
Stefan Simrock
*2) Deutsche Elektronen-Synchrotron (DESY), Notkestrasse 85, 22607 Hamburg, Germany*

## Abstract

The work presents a structural and functional model of a distributed low level radio frequency (LLRF) control system for the TESLA-XFEL accelerator. The design of a system basing on the FPGA chips and multi-gigabit optical network was debated. The system design approach was fully parametric. The major emphasis is put on the methods of the functional and hardware concentration to use fully both: a very big transmission capacity of the optical fiber telemetric channels and very big processing power of the latest series of the, DSP enhanced and optical I/O equipped, FPGA chips. The subject of the work is the design of a universal, laboratory module of the LLRF sub-system. Initial parameters of the system model under the design are presented.

**Keywords:** Super conducting cavity control, signal conversion, FPGA, DSP, optics fibers, FPGA with optical I/O, free electron laser, FEL

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**ABSTRACT**

The work presents a structural and functional model of a distributed low level radio frequency (LLRF) control system for the TESLA-XFEL accelerator. The design of a system basing on the FPGA chips and multi-gigabit optical network was debated. The system design approach was fully parametric. The major emphasis is put on the methods of the functional and hardware concentration to use fully both: a very big transmission capacity of the optical fiber telemetric channels and very big processing power of the latest series of the, DSP enhanced and optical I/O equipped, FPGA chips. The subject of the work is the design of a universal, laboratory module of the LLRF sub-system. Initial parameters of the system model under the design are presented

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## 1. INTRODUCTION

The TESLA – XFEL project bases on the nine-cell super conducting niobium resonators to accelerate electrons and positrons. The acceleration structure is operated in standing p-mode wave at the frequency of 1,3 GHz. The RF oscillating field is synchronized with the motion of a particle moving at the velocity of light across the cavity [9].

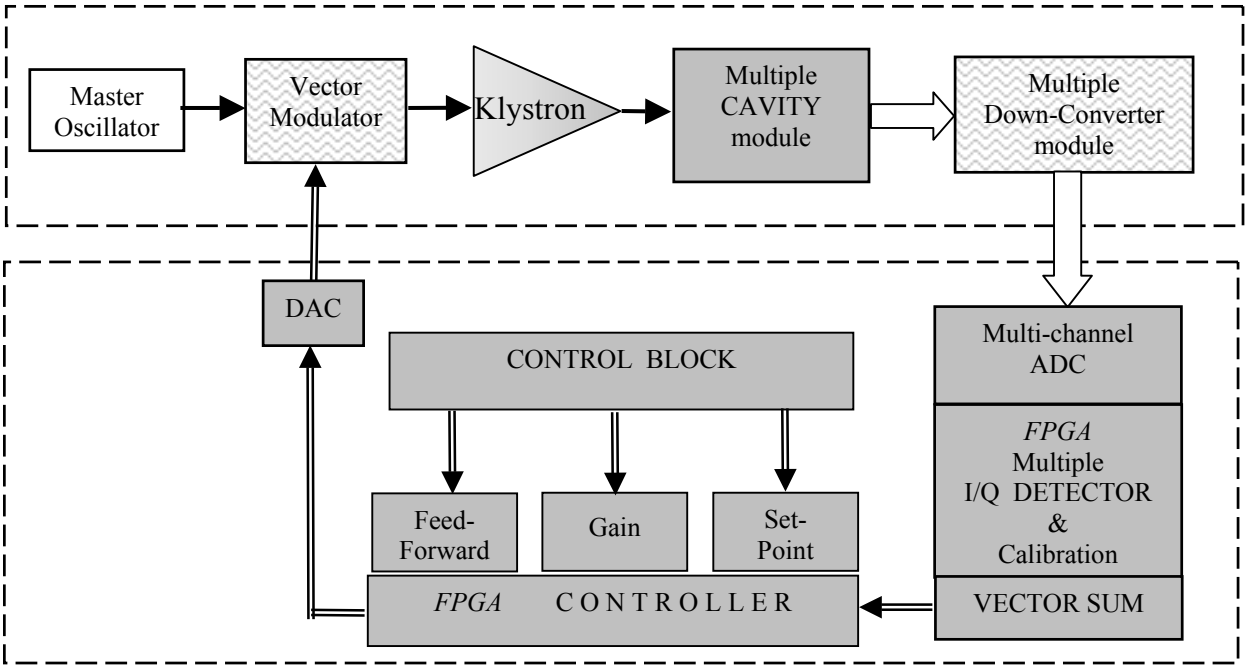


Fig. 1. General functional block diagram of LLRF Multiple Cavity Control System

The LLRF – Low Level Radio Frequency control system [1,2,3,4] has been developed to stabilize the pulsed accelerating fields of the resonators (see fig. 1). The control section, powered by one klystron, may consist of many cavities. One klystron supplies the RF power to the cavities through the coupled wave-guide with a circulator. The fast amplitude and phase control of the cavity field is accomplished by modulation of the signal driving the klystron from the vector modulator. The cavities are driven with the pulses of 1.3 ms duration and the average accelerating gradients of 25 MV/m. The RF signal of each cavity is down-converted to an intermediate frequency of 250 KHz preserving the amplitude and phase information. The ADC and DAC converters link the analog and digital parts of the system.

A very dynamic development of the programmable FPGA circuits, which has been observed during the last years, stimulated their wide applications the real-time LLRF systems [5,6]. The major driving factor behind the widening applications is a considerable lowering of the chip costs relative to the available number of the logical cells, the aggregated capacity of the memory blocks and the aggregated processing power of the inbuilt DSP components. This factor is constantly changing the FPGA circuits into the universal building blocks of any advanced photonic and electronic system design.

The DSP equipped FPGA chips, when used in the LLRF system, allow for realization not only the basic functional tasks but also for building of the whole new layers of diagnostics and communications [6]. The newest generations of the FPGA circuits promise even for more as they have integrated modules of very fast communication interfaces with signal multiplexing and demultiplexing in the direct I/O configuration. These I/Os may be either electrical (e.g. differential LVDS or PECL) or optical (e.g. gigabits fiber link)[10].

The paper debates the structural and functional model of a universal, LLRF control (also measurement and diagnostic in the near future) system, which bases on the FPGA chips of the newest generation. The newest predicted features and development tendencies in the FPGAs were taken into account. It was assumed that the system design should enable a relatively easy and cheap system modification (hardware upgrade without exchange) for some prolonged period of time after the commissioning. Here, the modification capability means the efficient adaptation to the changing and extending requirements of the (free electron laser, superconducting cavity) control process. The system should also have the possibility to change the type of the FPGA chip, without rebuilding essentially the framework architecture. After some time of the development it is unavoidable to change the system generation, but the parameterization and inbuilt flexibility of the design avoids excessive costs of the prototyping process (of the LLRF system).

## 2. STRUCTURAL AND FUNCTIONAL MODEL OF LLRF SYSTEM

The LLRF system (for the SC cavity) may be considered, from the side of the data flow and processing, as a *multichannel, synchronous, pipelined hardware concentrator,* having the following features:

- *Multichannel* – The need to be multichannel is a fundamental requirement, because the system is expected to control nondependently up to several tens of cavities. The multi-parameter field control in the particular cavities requires the presence of nondependent, synchronous readout channels in the system. Some cavity parameters should also be measured by the system to develop its control potential and extend diagnostic capability. The feature of being multichannel enables building of multilevel system. The channels are integrated in a vector sum in the second tier of the system.

- *Synchronous* – This feature assures a simultaneous (and parallel, in a multichannel system) data processing for the same moment of time, marked by the central system clock of the accelerator. All the system events have to be situated extremely precisely in relation to the accelerator clock. The system time perturbations have to be taken into account. The perturbations may originate from the signal jitter, dispersion and attenuation, differences in the length of transmission lines causing differential latencies, unexpected exceptional events, etc.

- *Pipelined* – This design approach stems from the complexity of the used system control procedures and algorithms. The signals are numerically processed in the steps. The data granularity is enabled for the separate moments of time. The data can be distinguished for all channels, all moments of time and all stages of the signal processing in the LLRF control and measurement loop. The moments are determined by the central system clock of the accelerator.

Such a system approach, taking into account the results of the above considerations, to the model design of the SC cavity LLRF as data concentrator is presented in fig.2. The data concentration process embraces in this case the whole

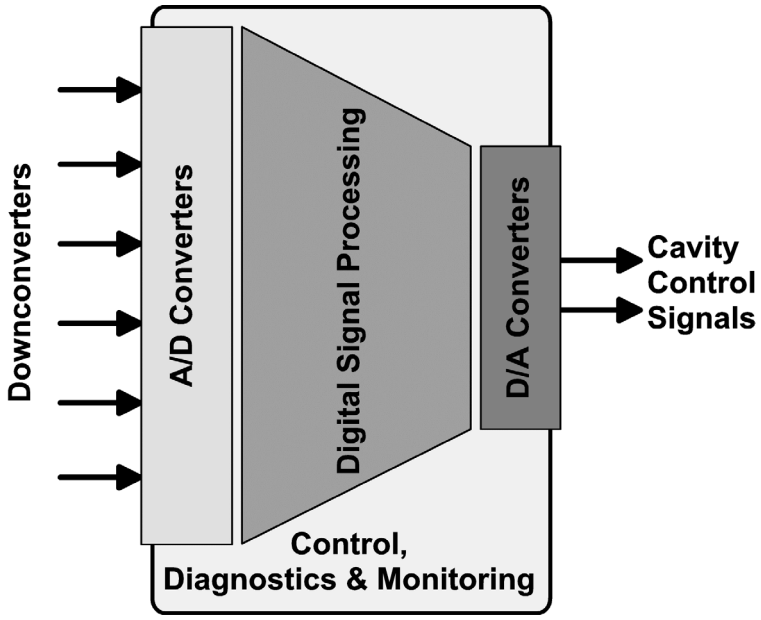


Fig. 2. A general functional structure of the data concentration process in the SC cavity LLRF control system

DSP range. It starts from the outputs of the ADCs up to the outputs of the DACs. The signal flow process may be considered in two different categories:

- *Functional concentration* – The concentration of many functions, in an (almost) single chip system (or reversely, dissipation among a few separate networked chips), stems from the properties and complexity of the DSP algorithm. The algorithm calculates the results from the multichannel data input in parallel. An example of this feature is that the vector sum is calculated using the parallel data from the ADCs (see fig. 1),

- *Hardware concentration* – A massive concentration of the hardware processing power in the central node (hub) of the SC cavity LLRF control system is a derivative of the need for the functional concentration. The aim of the hardware concentration is to gather a considerable number of complex physical signals in a single data processing object to be treated numerically. An example of this feature is that the structure of many ADCs is connected to a single, powerful enough, FPGA chip.

The design of the, FPGA and photonics based, SC cavity LLRF control system, which is the subject of consideration presented in this work, uses the above features. The design approach considers the system as a distributed data concentrator structure, where the concentration is done for the functional and hardware levels. A simple experimental model of such a system was proposed. It is assumed that the LLRF system would be re-configurable (on the considered functional and hardware levels) in the widest possible extent. The reconfiguration capability embraces the following parameters:

- The number of the input and output channels. The frequency of the I/O channel sampling. The frequency of the DSP.

- Splitting of the pipelined signal processing to the concentration tiers. The tiers include the functional and hardware levels. The aim of the splitting is to optimize the available (usually scarce) optical transmission bandwidth and the signal processing rate as well as the system costs.

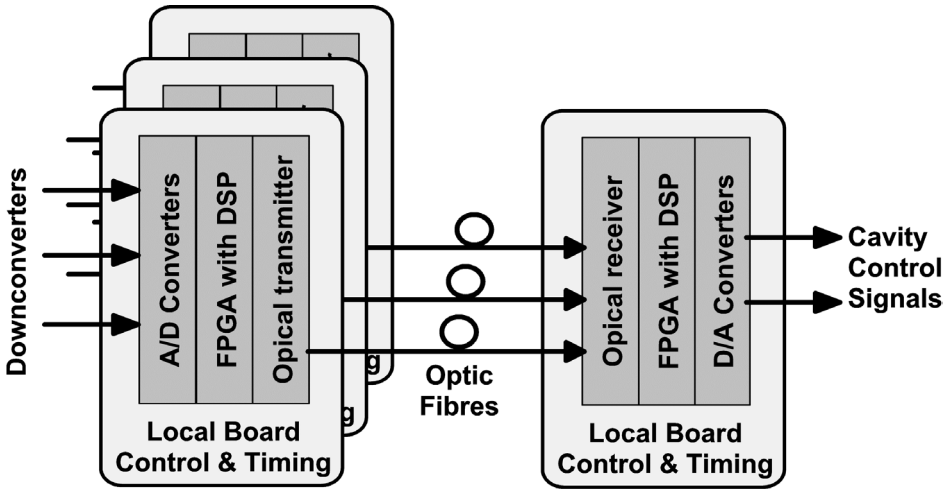


Fig. 3. A general functional structure of the (data and functions) concentration process in the LLRF system

Fig. 3 presents a hardware model of the distributed LLRF system basing on the FPGA chips, which are mutually connected via the network of optical links. The realization of this solution is possible due to the new features implemented in the latest series of the programmable circuits. These features are: the embedded, dedicated DSP blocks of considerable processing power, large RAM memory and the blocks of serial gigabit transmission. The latter are designed to work directly with the popular and comparatively cheap optical fiber multi-gigabit transceivers. From the functional side, the proposed solution enables an easy modification of the system structure. The parameterized structure functions are: the number of the input channels and data processing. A standardized and, thus, universal character of the applied fiber optic links enables realization of mutual (direct) functional connections between the particular PCBs. The need of the current system modification may be narrowed to a part of the design, instead of the whole.

## 3. PARAMETERIZATION ASPECTS OF LLRF SYSTEM

A simple reconfiguration possibility of the LLRF system, postulated in the previous chapter, stems from the elementary (of the low granularity) parameterization of the design. Small, elementary, functional blocks are connected via a broadband optical fiber network. The optical network is here a universal interface to the fast data distribution. Figs. 4 and 5 present the basic parameters of the functional blocks of the LLRF system and the throughput of the optical network.

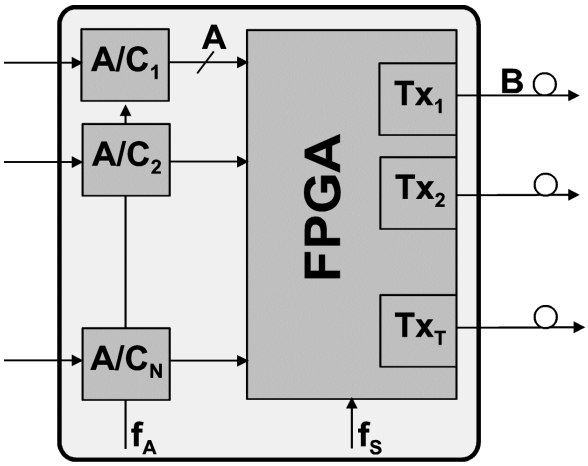


Fig. 4. Parameterization of the ADC-DSP block

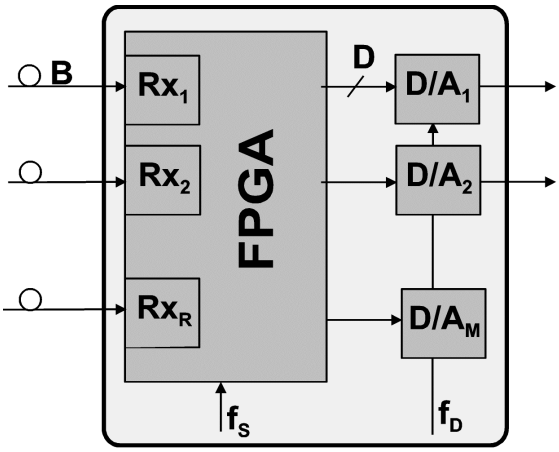


Fig. 5. Parameterization of the DSP-DAC block

The bandwidth of the data stream from the ADCs in the ADC-DSP block may be calculated from the following expression:

$$ADC_{BAND} = N * A * f_A$$

where: $N$ is a number of the ADCs, $A$ is a number of conversion bits of the ADC, and $f_A$ is a frequency of the sampling.

Assuming that the full bandwidth $ADC_{BAND}$ is distributed to the block DSP-DAC, then, the required optical fiber bandwidth $Tx_{BAND}$ must fulfill the following relation:

$$Tx_{BAND} \geq ADC_{BAND} \Rightarrow (T * B) \geq (N * A * f_A)$$

where: $T$ is a number of the required optical fiber channels, and $B$ is the transmission rate expressed in [bits/s]. The proposed solution, in this case, with the multiplication of the optical fiber channels (parameter $T$) stems from the possibility to use some of the FPGA chips with the embedded SERDES blocks. The fast SERDES (serializer/deserializer) modules possess the aggregated throughput of several Gbps.

The optical fibre receiving link in the DSP-DAC block, possesses, from the assumption, the channels of the same transmission characteristics as the transmitting one. The aggregated receiving bandwidth may be calculated from the condition:

$$Rx_{BAND} \geq C * Tx_{BAND} \Rightarrow (R * B) \geq (C * N * A * f_A)$$

where: $C$ is a number of the ADC-DSP modules connected via the optical fiber network to a single DSP-DAC module.

The bandwidth of the output data stream from the D/A converters in the DSP- DAC block may be obtained from the relation:

$$DAC_{BAND} = M * D * f_D$$

where: $M$ is a number of D/A converters, $D$ number of conversion bits of the converter, $f_D$ frequency of sampling.

A conclusion may be drawn from the above relations that the most critical components are:

- *ADC channels concentration* - in a single block, typically situated on a single PCS. This is due to the technological difficulties and the required aggregated bandwidth of fiber optic transmission.
- *Multiplication of optical fiber links* – in order to provide the required bandwidth of transmission. This forces the use of a big number of the receivers in the DSP-DAC module (parameter R).

The next chapter presents chosen methods of the functional and hardware concentration. These methods are expected to minimize certain critical parameters of the LLRF system.

## 4. CHOSEN CONCENTRATION METHODS FOR LLRF SYSTEM

This chapter discusses the four representative methods of the functional and hardware concentration in the LLRF system, in order to obtain the optimal usage of the optical fibre bandwidth and to optimize the implementations of the data processing, control and diagnostics in the FPGA chips.

The results were presented on an example, for certain work conditions, of the LLRF systems of TESLA accelerator. The, FPGA based (Xilinx Virtex V3000), cavity controller was implemented earlier [6,11,12,13].

| | |
|---|---|
| Number of input channels | (parameter $N$)..... 32 |
| Number of output channels | (parameter $M$)..... 2 |
| Sampling frequency of ADC | (parameter $f_A$)..... 40 MHz |
| Sampling frequency DAC | (parameter $f_D$) ..... 40 MHz |
| Frequency of DSP process | (parameter $f_S$)..... 1 MHz |
| Word width in DSP processing | ..... 18 bitów |

### 4.1. DATA CONCENTRATION FROM ADC

This kind of the concentration process relies on the transmission, via optical links (to the DSP-DAC module) of the original data provided by all 32 ADCs situated in the ADC-DSP module. It is the concentration version imposing minimal functional requirements on the ADC-DSP module (no necessity to do any DSP operation). In this modest case, the module may be equipped with a cheap and popular FPGA chip like Cyclone (by Altera) or Spartan (by Xilinx). As a consequence, the LLRF processing algorithm modification in the DSP layer does not include the ADC-DSP module. This solution requires a large optical transmission bandwidth. A detailed analysis result was gathered in table 1 for the sampling frequency $f_A=40MHz$.

| Number of ADC-DSP modules (parameter $C$) | | ADC channels (parameter $N=8$) | | | | | ADC channels (parameter $N=16$) | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Resolution of ADC (parameter $A$) | | 8 | 10 | 12 | 14 | 16 | 8 | 10 | 12 | 14 | 16 |
| standard SERDES transmission (parameter $B=3.125Gb/s$) | parameter $Tx_{BAND}$ [Gb/s] | 2.56 | 3.20 | 3.84 | 4.48 | 5.12 | 5.12 | 6.40 | 7.68 | 8.96 | 10.24 |
| | parameter $T$ | 1 | 2 | 2 | 2 | 2 | 2 | 3 | 3 | 3 | 4 |
| | Bandwidth occupancy [%] | 81.92 | 68.27 | 81.92 | 95.57 | 81.92 | 81.92 | 81.92 | 98.30 | 95.57 | 93.62 |
| | parameter $Rx_{BAND}$ [Gb/s] | 10.24 | 12.80 | 15.36 | 17.92 | 20.48 | 10.24 | 12.80 | 15.36 | 17.92 | 20.48 |
| | parameter $R$ | 4 | 8 | 8 | 8 | 8 | 4 | 6 | 6 | 6 | 8 |

Tab.1 Optical transmission bandwidth for chosen parameters of the LLRF system with the indirect concentration method.

The results in the table 1 show that, only in the case of $N=8$ and $A=8$, the bandwidth of a single optical link is sufficient to transmit all the data from the ADC-DSP module. In all other cases, the optical links multiplication is required, and the maximum mux value is $T=4$. The main factor influencing the bandwidth is the sampling frequency, which is here $f_A=40MHz$. The next chapter presents a solution in which the required optical fiber link bandwidth may be considerably lowered.

### 4.2. MODULATED SIGNALS CONCENTRATION I/Q

The concentration of the modulated I/Q signals in the ADC/DSP module enables reduction of the sampling frequency from $f_A=40MHz$ to $f_S=1MHz$ for each measurement channel. In this case, each channel has to possess the nondependent, programmable correction components. The following parameters are subject to the correction: amplification changes, stabilization of the reference level, signal averaging block, low-pass filtering, etc. These solutions require the use of the faster and the bigger FPGA chips than in the previous case. The DSP blocks in these FPGAs are required too. This kind of processing serves only for conditioning of the measurement signal. It does not embrace within its extent the LLRF control algorithm. This solution leads to the reduction of the required optical fiber bandwidth, what was presented in tab. 2 for the sampling frequency $f_S=1MHz$.

| Number of ADC-DSP modules (parameter $C$) | | ADC channels (parameter $N=8$) | | | | | ADC channels (parameter $N=16$) | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Resolution of ADC (parameter $A$) | | 8 | 10 | 12 | 14 | 16 | 8 | 10 | 12 | 14 | 16 |
| standard SERDES transmission (parameter $B=3.125Gb/s$) | parameter $Tx_{BAND}$ [Gb/s] | 0.06 | 0.08 | 0.10 | 0.11 | 0.13 | 0.13 | 0.16 | 0.19 | 0.22 | 0.26 |
| | parameter $T$ | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Bandwidth occupancy [%] | 2.05 | 2.56 | 3.07 | 3.58 | 4.10 | 4.10 | 5.12 | 6.14 | 7.17 | 8.19 |
| | maximum $f_S$ [MHz] | 48.83 | 39.06 | 32.55 | 27.90 | 24.41 | 24.41 | 19.53 | 16.28 | 13.95 | 12.21 |
| | parameter $Rx_{BAND}$ [Gb/s] | 0.26 | 0.32 | 0.38 | 0.45 | 0.51 | 0.26 | 0.32 | 0.38 | 0.45 | 0.51 |
| | parameter $R$ | 4 | 4 | 4 | 4 | 4 | 2 | 2 | 2 | 2 | 2 |

Tab. 2 Optical transmission bandwidth for chosen parameters of the LLRF system in the concentration of modulated I/Q signals

The concentration of the modulated signals I/Q enables normalization ($T=1$) of the number of optical fibre transmitters for the ADC-DSP modules and the number of optical fiber receivers ($R=C$) in the DSP-DAC module, which is respective to the number of the transmitting modules. The bandwidth occupancy does not cross the value of 10%, what means the possibility to increase the I/Q signal modulation frequency from the existing now *250kHz* even to *5MHz* without the necessity to modify the structure of the optical fiber network. The consideration, in a further perspective, of much faster processing algorithms, involves the use of very advanced technologically and big, thus, expensive, FPGA chips. The next chapters present the solution embracing the process of concentration on the level of the LLRF control algorithm. The tasks fulfilled in a single FPGA chip may be realized in a few smaller chips in the fully distributed processing structure. The structure has an optical network as a backbone.

### 4.3. I/Q SIGNAL CONCENTRATION AFTER DETECTION

The concentration of the I/Q signals after detection in the ADC-DSP module enables performing of a part of the LLRF control algorithm on the level of the ADC-DSP block. The process stores, however, the overall control on each measurement channel in the DSP-DAC module. The considered method of concentration requires the use of FPGA chips equipped with the DSP blocks. The ADC-DSP block may realize a considerable part of the diagnostics and monitoring of the particular channels, apart form doing its regular task of functional processing. In this case, the costs of diagnostics and monitoring implementation may be considerably distributed among a number of FPGA chips. The required optical transmission bandwidth depends on the width of the word used in the DSP algorithm. Tab.3 presents the values of the required optical transmission bandwidth for a few exemplary values of the width of DS word.

| Number of ADC-DSP modules (parameter $C$) | | ADC channels (parameter $N=8$) | | | | | ADC channels (parameter $N=16$) | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Width of DSP word [bits] | | 18 | 24 | 30 | 36 | 42 | 18 | 24 | 30 | 36 | 42 |
| standard SERDES transmission (parameter $B=3.125Gb/s$) | parameter $Tx_{BAND}$ [Gb/s] | 0.07 | 0.10 | 0.12 | 0.14 | 0.17 | 0.14 | 0.19 | 0.24 | 0.29 | 0.34 |
| | parameter $T$ | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Bandwidth occupancy [%] | 2.30 | 3.07 | 3.84 | 4.61 | 5.38 | 4.61 | 6.14 | 7.68 | 9.22 | 10.75 |
| | maximum $f_S$ [MHz] | 21.70 | 16.28 | 13.02 | 10.85 | 9.30 | 10.85 | 8.14 | 6.51 | 5.43 | 4.65 |
| | parameter $Rx_{BAND}$ [Gb/s] | 0.29 | 0.38 | 0.48 | 0.58 | 0.67 | 0.29 | 0.38 | 0.48 | 0.58 | 0.67 |
| | parameter $R$ | 4 | 4 | 4 | 4 | 4 | 2 | 2 | 2 | 2 | 2 |

Tab. 3 Optical fibre link transmission bandwidth for chosen parameters of the LLRF system in the concentration method for I and Q signals.

The method debated in this chapter does not allow for reducing the optical transmission bandwidth because the values of I and Q must be transmitted for all channels nondependently. The further possibility to reduce the transmission bandwidth may be obtained by splitting the control algorithm, what is presented in the next chapter.

### 4.4. CONCENTRATION OF LOCAL VECTOR SUMS

A much bigger functional concentration is obtained by performing the calculations of the local vector sum already on the level of the ADC-DSP module. All the control, monitoring and diagnostics of particular channels have to be also implemented in the ADC-DSP module. A much bigger reduction of the optical bandwidth is obtained, because the vector sum are transferred. The transmission bandwidth depends on the width of the DSP word was presented in tab. 4.

| The width of DSP word [bits] | | 18 | 24 | 30 | 36 | 42 |
|---|---|---|---|---|---|---|
| standard SERDES transmission (parameter $B=3.125Gb/s$) | parameter $Tx_{BAND}$ [Gb/s] | 0.01 | 0.01 | 0.02 | 0.02 | 0.02 |
| | Bandwidth occupancy [%] | 0.29 | 0.38 | 0.48 | 0.58 | 0.67 |
| | maximum $f_S$ [MHz] | 173.61 | 130.21 | 104.17 | 86.81 | 74.40 |
| | parameter $Rx_{BAND}$ [Gb/s] | 0.02 | 0.02 | 0.03 | 0.04 | 0.04 |

Tab. 4 Optical transmission bandwidth for chosen parameters of LLRF system in the method of concentration of local vector sums.

## 5. UNIVERSAL RESEARCH MODEL OF DISTRIBUTED LLRF SYSTEM

The realization of the eventual solution of the distributed LLRF control system basing on the FPGA chips and optical fiber network will be preceded by the investigation of the laboratory model. The aim is to create the numerous structures of the system, and investigate the scalability, efficiency and reliability. The hardware and software layers are subject to practical analysis [7,8] for various models of concentration debated in the previous chapter.

Fig. 6 presents a functional structure of the universal research module basing on the FPGA Stratix GX chip by Altera [10]. The module possesses a symmetrical construction and was equipped in:

- Four A/D converters (parameter *N=4*) of the resolution of 14-bits (parameter *A=14*),
- Four D/A converters (parameter *M=4*) of the resolution of 14-bits (parameter *D=14*),
- Four optical transmitters (parameter *T=4*) of the bandwidth 3.125Gb/s (parameter *B=3.125*),
- Four optical receivers (parameter *R=4*) of the bandwidth 3.125Gb/s (parameter *B=3.125*),

The frequency of the analog channels processing equals to: $f_A=f_D=40MHz$. The frequency of DSP is $f_S=1MHz$ what is in respect to the requirements of the TESLA-XFEL accelerator.

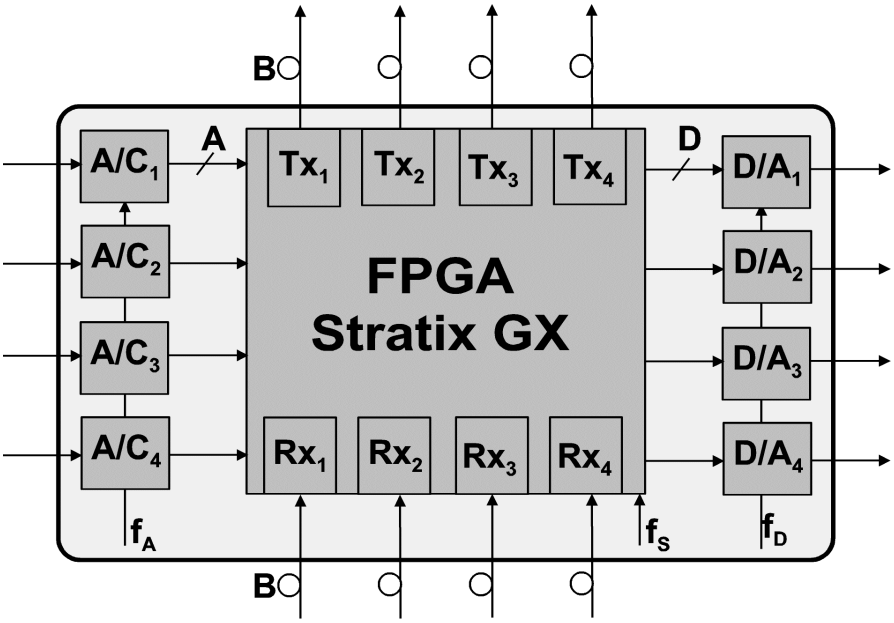


Fig. 6. A general functional structure of the universal module of the LLRF system

## 6. CONCLUSIONS

The work presents a structural and functional model of a distributed LLRF control system for the TESLA-XFEL accelerator. The model bases on the, DSP and communications functions equipped, FPGA chips and very fast, multigigabit, synchronous optical fiber data distribution system. The system design enables uniquely its scaling and realization of various methods of data and processing power concentration on the functional and hardware levels.

The obtained functional solutions lower considerably the required transmission bandwidth for the data. They provide the use of a single optical fiber channel, even at increasing the LLRF control algorithm frequency nearly 20 times. The implementation methods of the new LLRF control algorithm, in a distributed version, were described. This implementation results practically in the possibility to distribute the system processing power into a few smaller FPGA chips.

The solutions, presented in this work, allowed preparing a universal model of the hardware module for the SC cavity, LLRF control system. The module enables building of a fully scalable system structure in a broad range of technical functions and parameters. The debated functional and hardware concentration ideas were realized practically and are subject to further investigations of their practical performance.

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