The ATLAS Level-1 Central Trigger Processor (CTP)

- **Introduction**
- **Functionality and Implementation**
- **Tests and Results**

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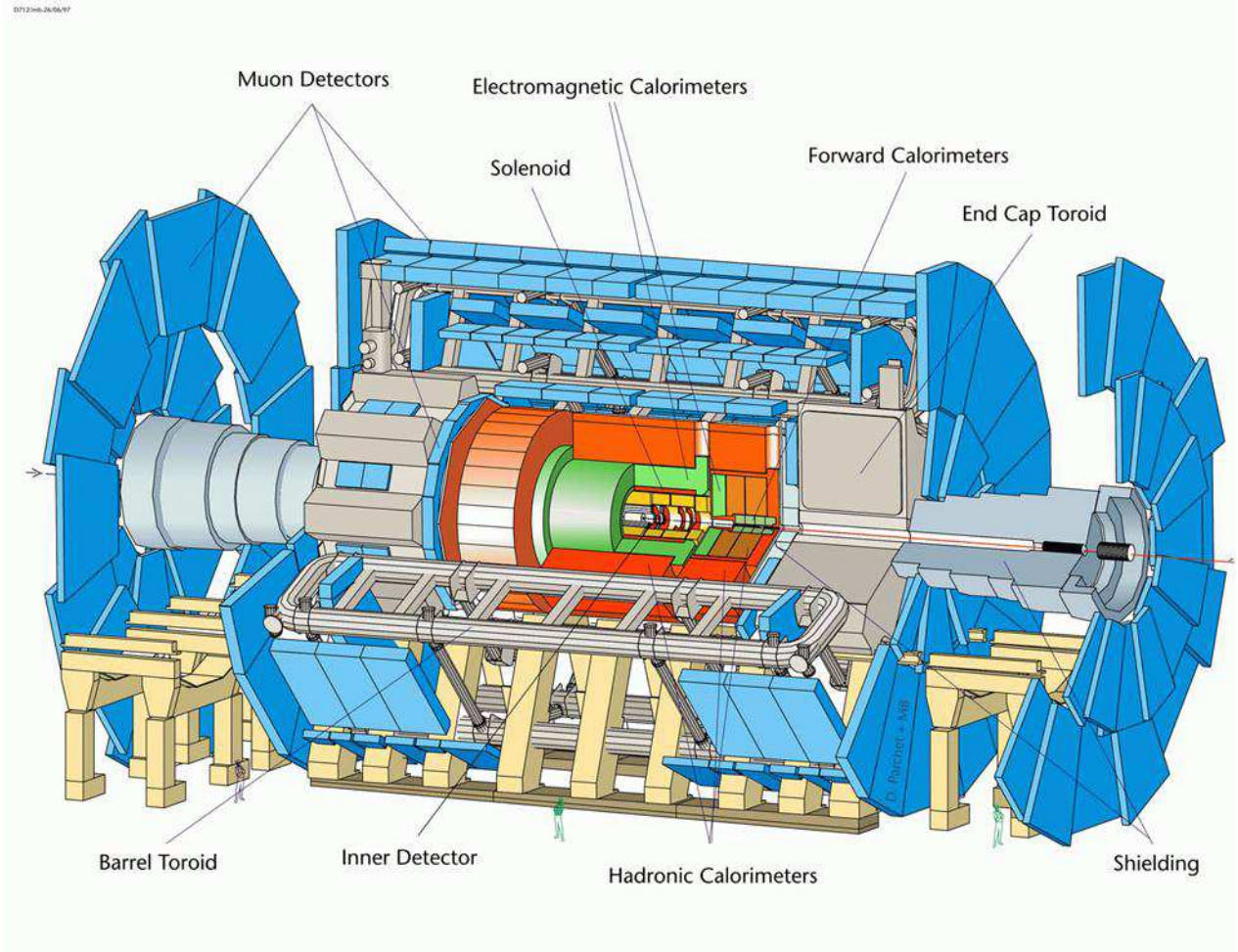
→ See also presentation "The ATLAS Level-1 Trigger Timing-in" by T. Pauly

The ATLAS Experiment (1)



General-purpose Experiment at CERN's **Large Hadron Collider (LHC):**

Proton-proton collisions at 14 TeV centre-of-mass energy

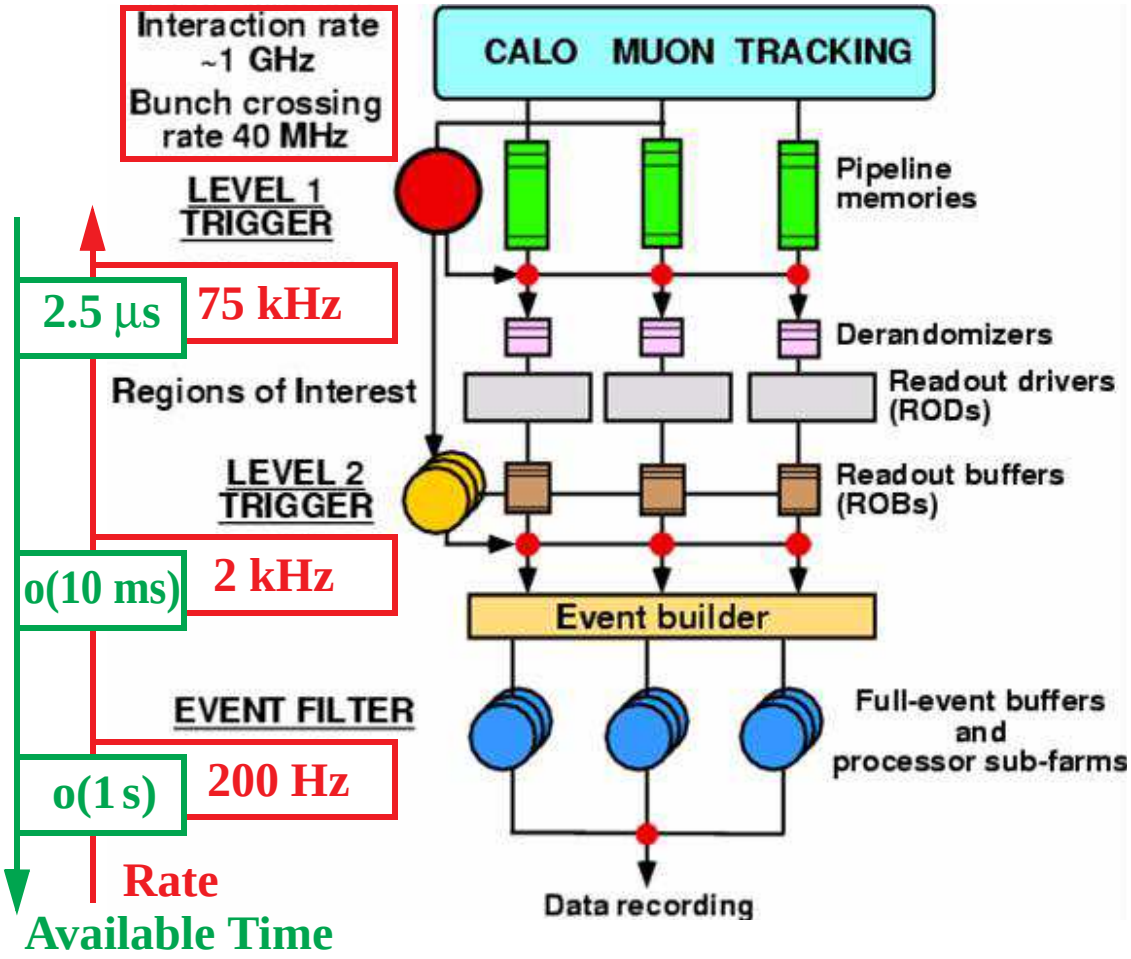
About 25 collisions per bunch crossing (**BC**) every 25 ns (40 MHz)

⇒ Interaction rate of 1 GHz

The ATLAS Experiment (2)

Installation of the 8th and final coil of the ATLAS barrel toroid

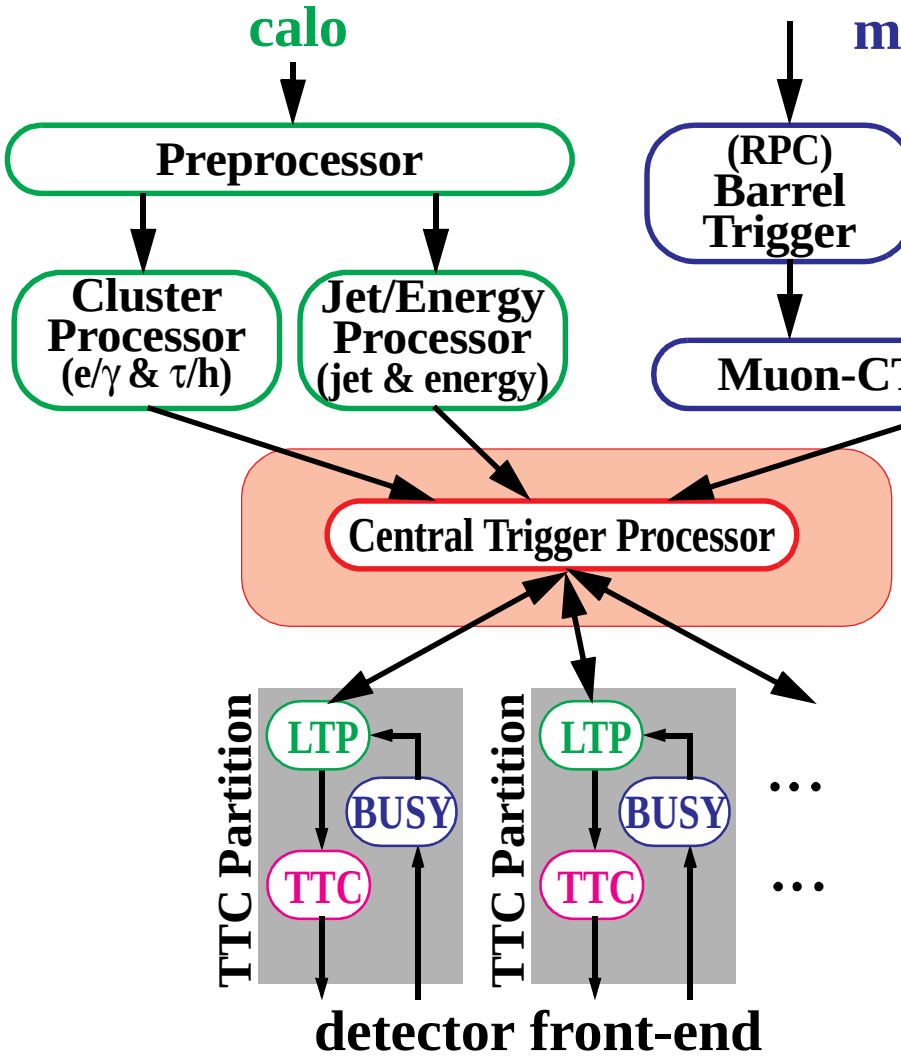
The Trigger/DAQ System



Level-1 Trigger:
Electronics +
Firmware

Level-2 Trigger
+ Event Filter:
Computers
+ Networks
+ Software

The Level-1 Trigger System



RPC = Resistive-Plate Chambers

TGC = Thin-Gap Chambers

LTP = Local Trigger Processor
+ multiplexing module

TTC = Timing, Trigger and Control

BUSY = Tree of ROD_BUSY modules

ATLAS has ~ 40 TTC Partitions

→ *A new LTP multiplexing module has been specified in order to allow concurrent combinations of TTC Partitions for stand-alone tests*

The Central Trigger Processor (1)

- **Trigger Input:**

  - **Multiplicities** from Calorimeter and Muon Triggers:
    electrons/photons, taus/hadrons, jets, and muons;

  - **Energy flags** from Calorimeter Trigger:
    ΣE_T , E_T^{miss} , ΣE_T^{jet}

  - **Calibration requests** from sub-detectors

  - Other **specialized triggers**: scintillators, beam pick-ups, etc.

  $\Rightarrow$ Up to a total of **160 trigger inputs** at any one time

  Plus **internal triggers** (generated in CTP):
  random triggers, prescaled clock, bunch crossing groups

The Central Trigger Processor (2)

- **Level-1 Accept (L1A):**
  - Derived from trigger inputs according to a **trigger menu:**
    - Up to **256 trigger items** are made from combinations of conditions on the trigger inputs, e.g.

      1EM10 ≡ at least one electron/photon with $E_T \geq 10$ GeV

      1MU6 ≡ at least one muon with $p_T \geq 6$ GeV/c

      XE20 ≡ missing energy of at least 20 GeV
    - Each trigger item has a mask, a priority[1] and a prescaling factor
      [1] **for preventive dead-time:**

      high priority: as little deadtime as possible

      low priority: comparatively high deadtime
    - **L1A is the OR of all trigger items**

  - An **example** of a trigger menu might contain

    1MU6 **mask = ON, priority = LOW, prescaling = 1000**

    2MU6 **mask = ON, priority = HIGH, prescaling = 1**

    1EM20 AND XE20 **mask = ON, priority = LOW, prescaling = 1**

    ...

The Central Trigger Processor (3)

- **Additional Functionality:**
  - **Trigger-type** word (8 bits) accompanying every L1A
    Sent promptly via the TTC system to the front-end electronics
  - **Dead-time** in order to prevent front-end buffers becoming full
  - **Region-of-Interest (RoI)** for the Level-2 Trigger and
    event data for the **Read-out System (ROS)** and for **monitoring**
    Provides much more information than the trigger-type word, allowing a detailed understanding of why the event was selected
  - **Time-stamp** (GPS-based UTC time) accompanying every L1A
  - **Timing signals**, e.g. Event Counter Reset (ECR), ...
  - **Scalers** in order to provide monitoring of rates and of deadtime
- **Constraints:**
  - **Trigger latency target, i.e. from trigger input to L1A:**
    100 ns ≡ 4 BC
  - **Trigger menu changes with physics/beam/detector conditions**

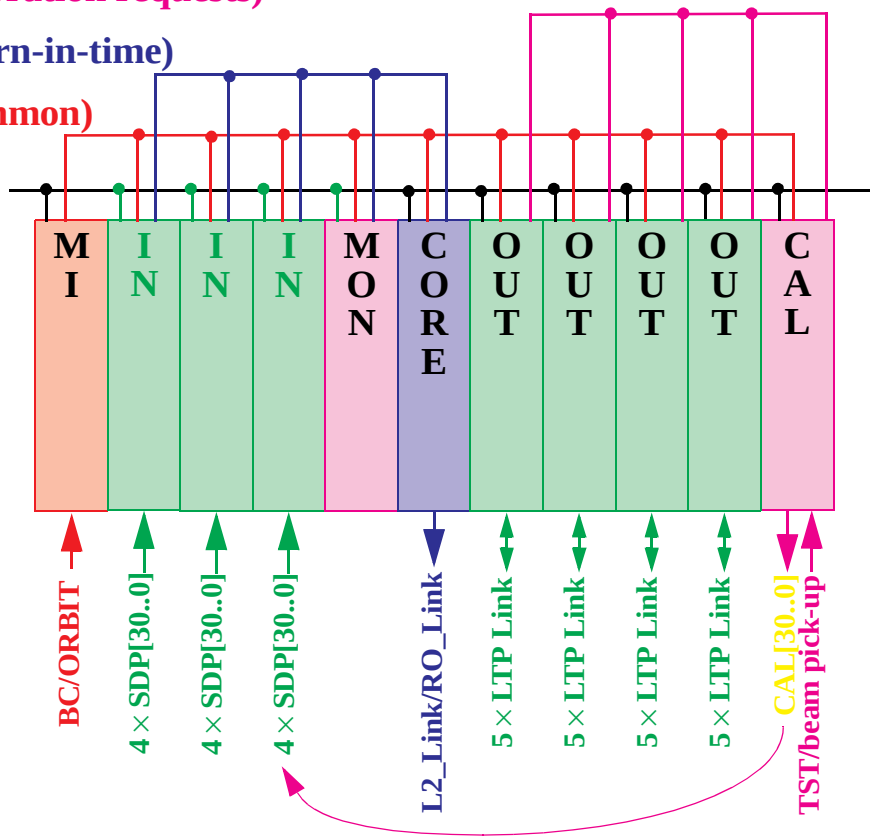
The Design of the CTP

CAL bus (calibration requests)

PIT bus (pattern-in-time)

COM bus (common)

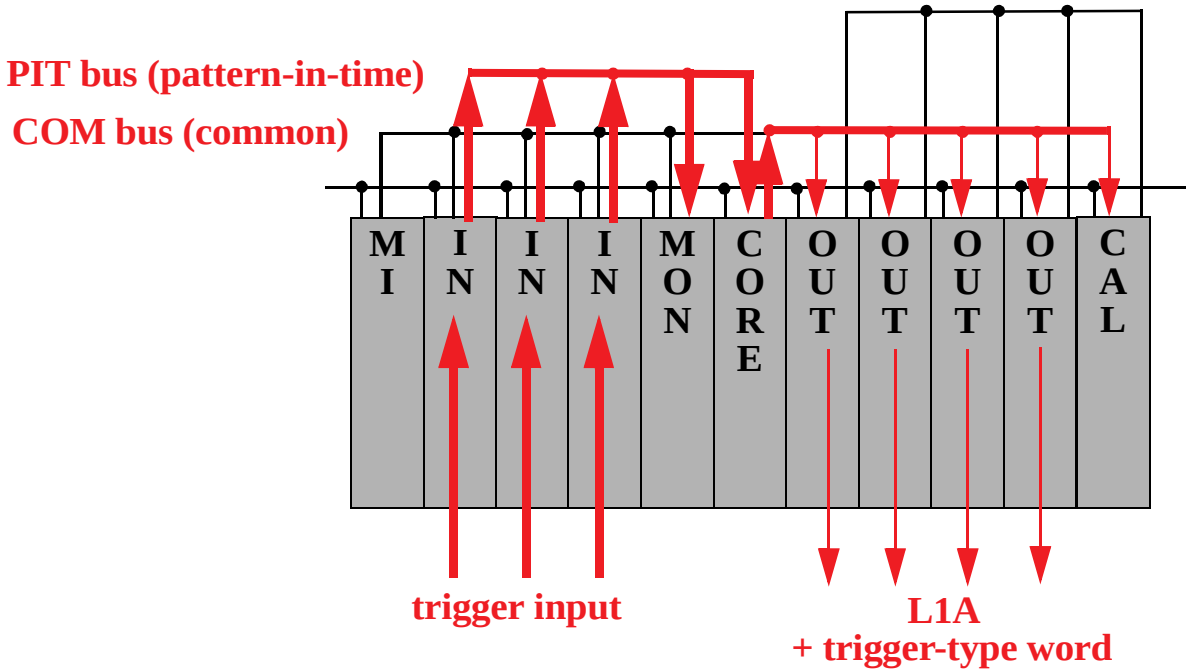
VMEbus



9U VME64x
+ custom backplanes

CTP_MI	(Machine Interface)	Timing
CTP_IN	(Input Module)	Trigger input
CTP_MON	(Monitoring Module)	Bunch-to-bunch monitoring
CTP_CORE	(Core Module)	Trigger menu + Readout&Monitoring + Time stamp
CTP_OUT	(Output Module)	Trigger fan-out
CTP_CAL	(Calibration Module)	Sub-detector calibration requests

The Trigger Path of the CTP

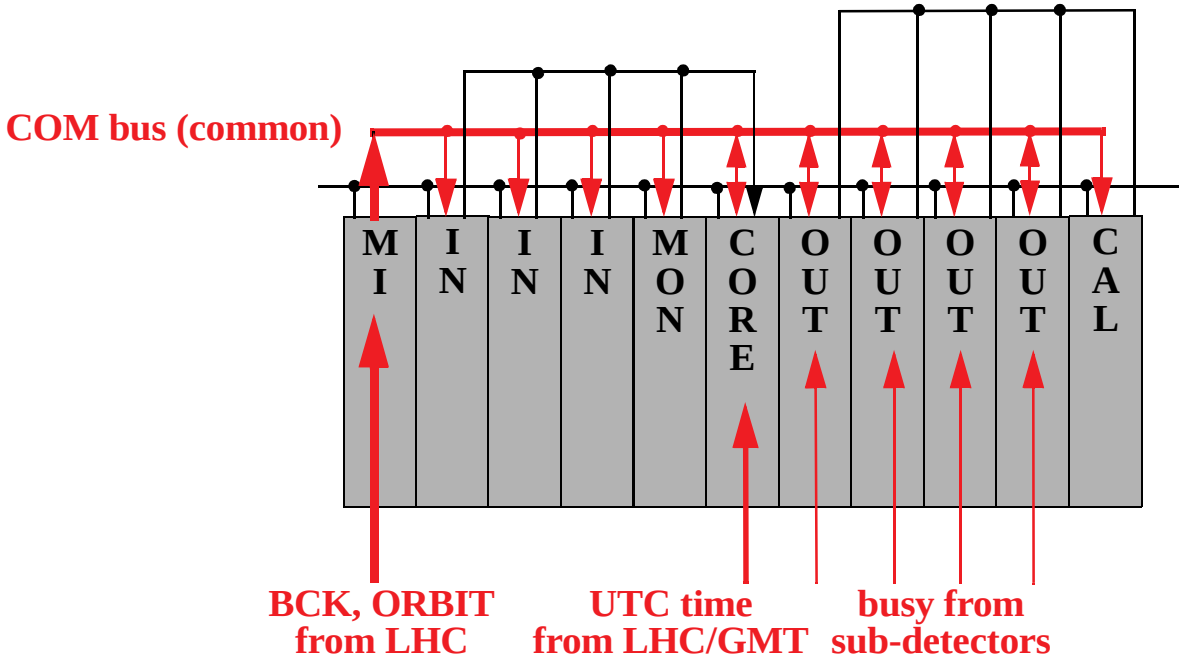


CTP_IN modules receive, synchronize (phase) and align (BC) the trigger inputs, and route them to the **PIT bus (Pattern-In-Time)**

CTP_CORE module receives and synchronizes the PITs, compares with trigger menu and generates **Level-1 Accept (L1A)**, sends L1A to the COM bus

CTP_OUT receives L1A from the COM bus and fans it out to sub-detector LTPs

The Timing Path of the CTP



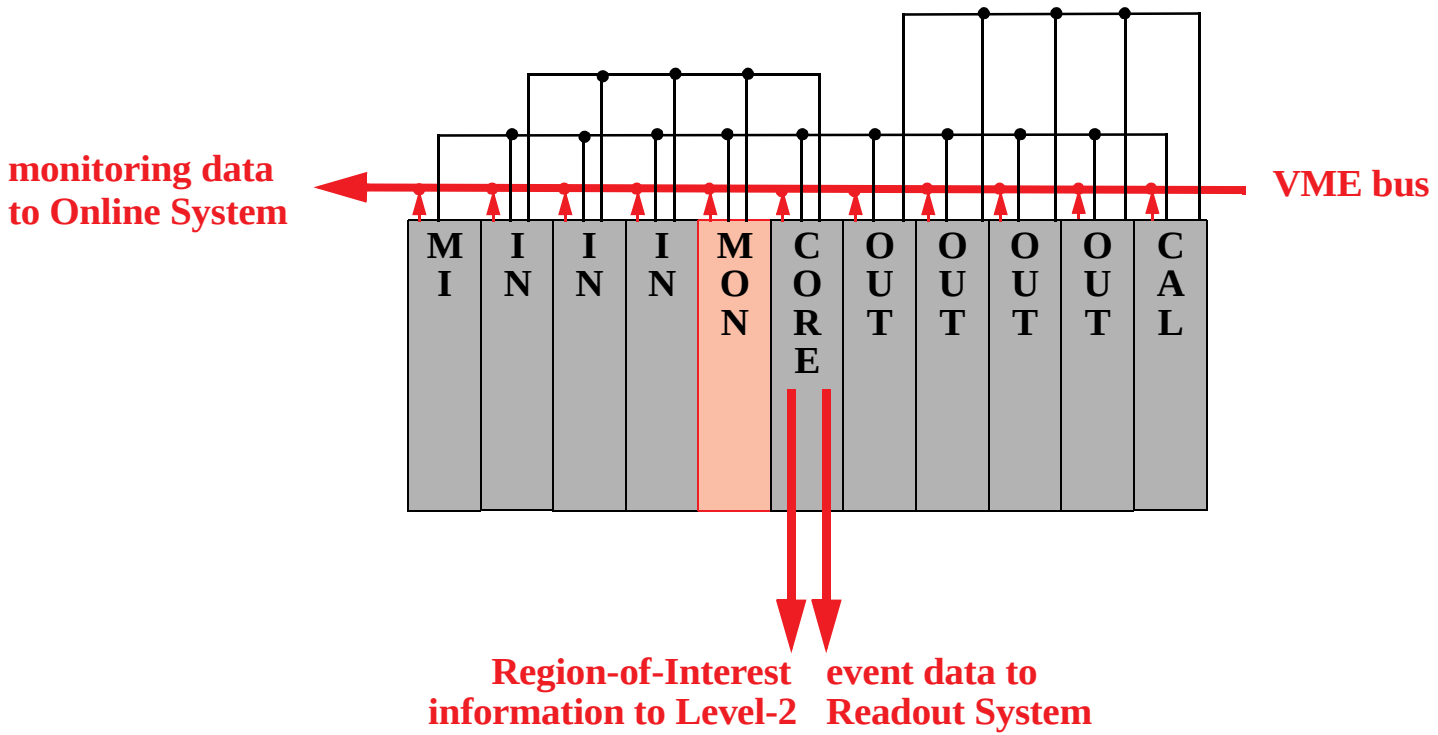
CTP_MI module receives timing signals from LHC, generates additional timing signals and sends all to the COM bus

CTP_OUT modules receive busy signals from sub-detector LTPs and send them to the COM bus

CTP_CORE module receives GPS-based UTC time from **LHC GMT (General Machine Timing)** timing system

All CTP modules receive timing signals from the COM bus

The Readout & Monitoring of the CTP



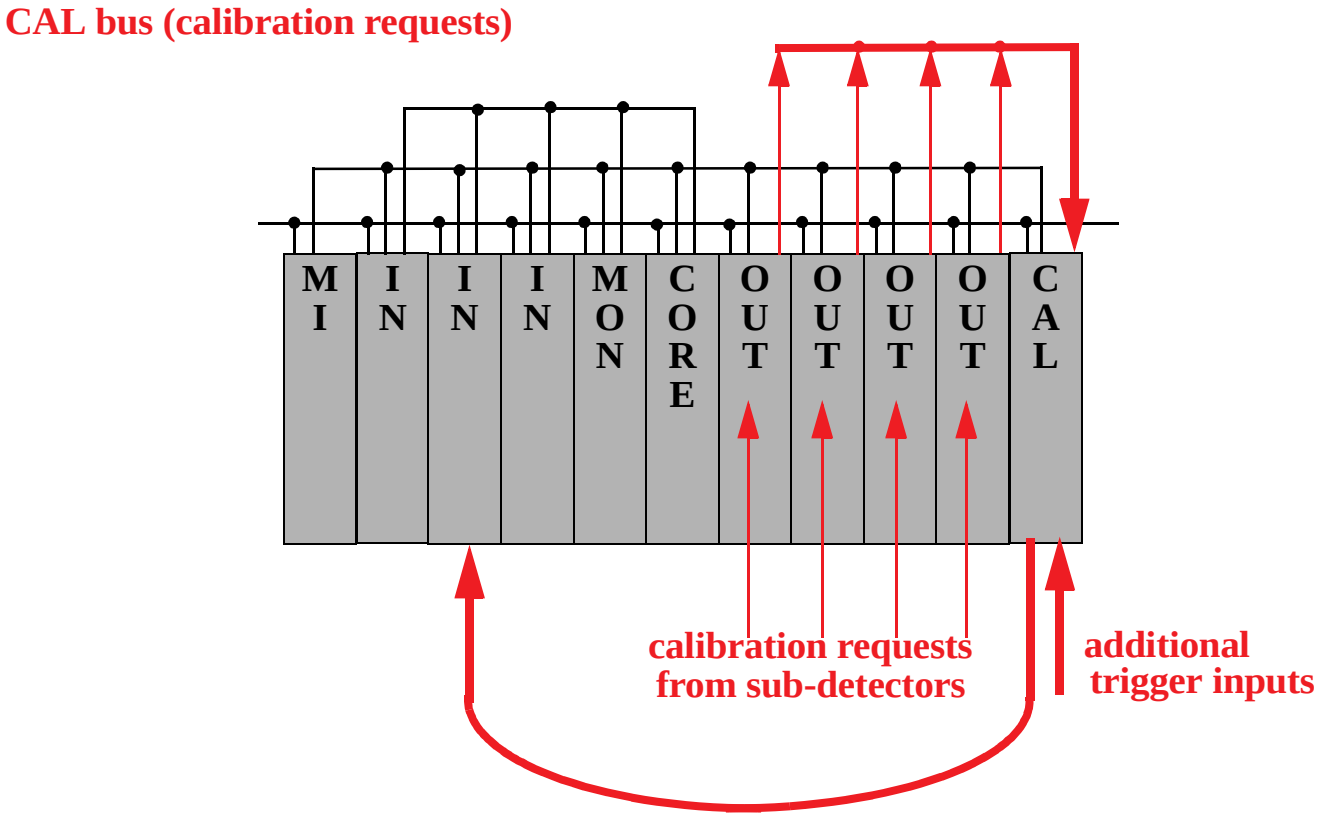
CTP_CORE module sends Region-of-Interest (RoI) information to the Level-2 Trigger and event data to the Readout System & monitoring

CTP_MON produces a bunch-by-bunch histogram of signals from the PIT bus

CTP modules provide other monitoring data to the VMEbus, in particular,

- CTP_IN: samples and scalers of trigger inputs
- CTP_CORE: scalers of trigger items and of deadtime
- CTP_OUT: scalers of deadtime of sub-detectors

The Calibration Requests in the CTP



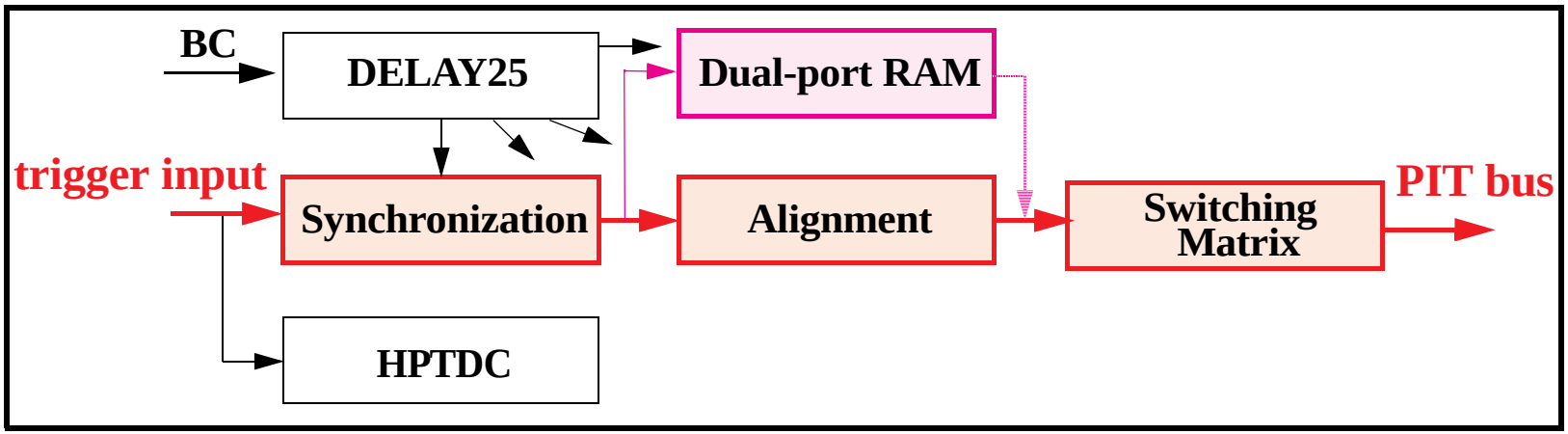
CTP_OUT modules receive calibration requests from sub-detector LTPs and send them to the CAL bus

CTP_CAL time-multiplexes calibration requests, receives additional trigger inputs and sends all to a CTP_IN module

The CTP Input Module (CTP_IN)

→ Trigger Path:

- Measure phase of trigger inputs
  using CERN High-Performance TDC (**HPTDC**)
- Adjust clock of CTP_IN module
  using CERN **DELAY25** (**PHOS4** on older version)
- Store synchronized data in **diagnostic memory** (dual-port RAM)
- Adjust BC alignment of trigger inputs using **pipeline** in FPGA
- **Select and route** trigger inputs to be sent to PIT bus using a CPLD

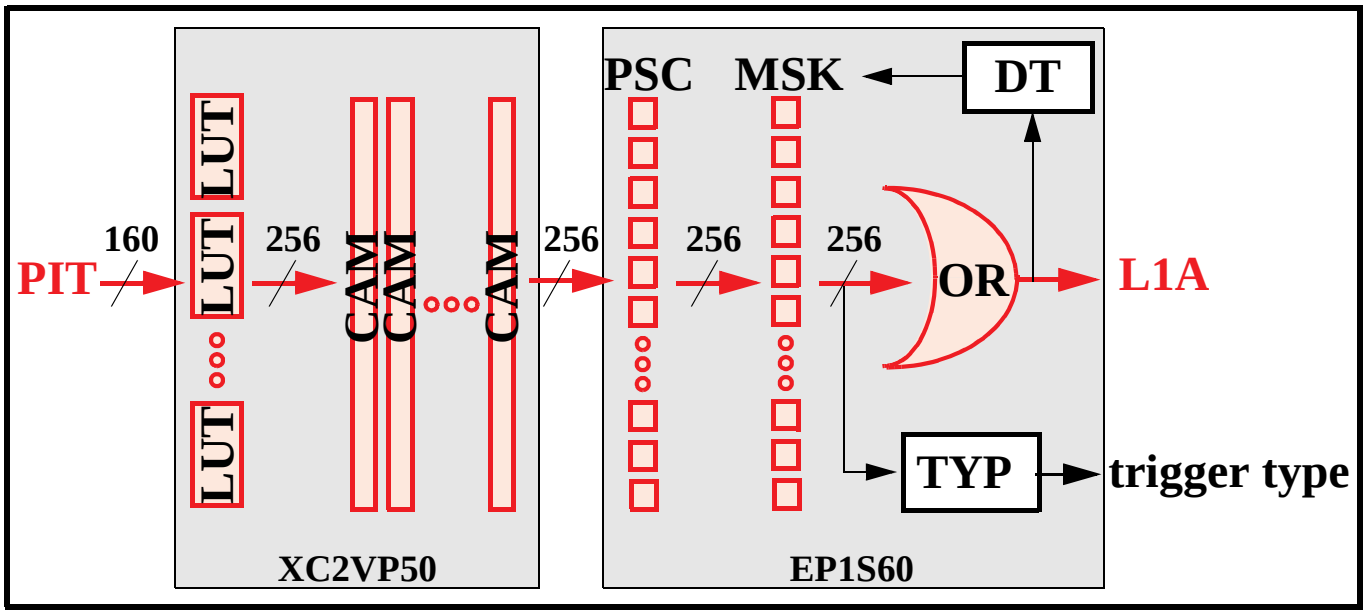


Trigger Path of CTP_IN Module

The CTP Core Module (CTP_CORE) (1)

→ Trigger Path:

- Combine Pattern-In-Time (**PIT**) using **Look-up Tables (LUT)**, and **Content-Addressable Memories (CAM)** to form **256 trigger items**
  Each CAM contains a 256-bit word and is ternary,
  i.e. allows bit-wise matching of "***0***", "***1***" or "***don't care***"
- Prescale (**PSC**, 24 bit), mask (**MSK**, mask + dead-time + busy), and OR the trigger items to generate **Level-1 Accept** (**L1A**)
- Generate preventive dead-time (**DT**) and trigger-type word (**TYP**)



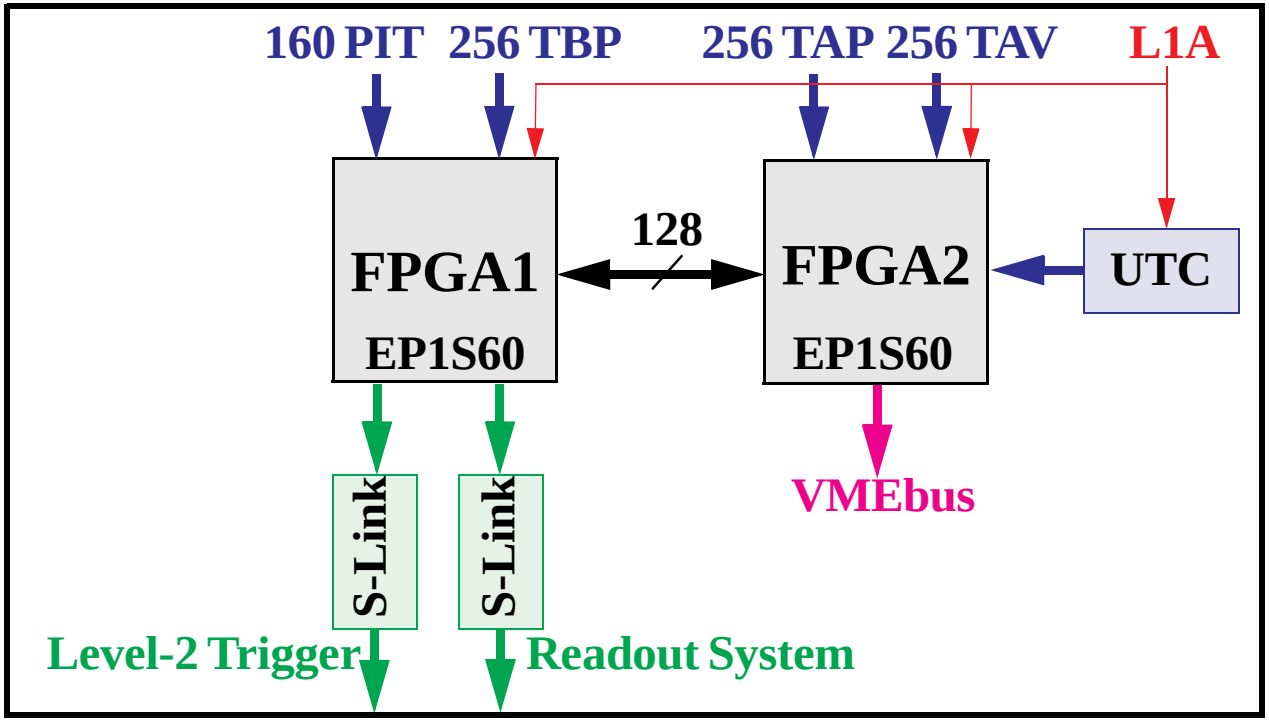
Trigger Path of the CTP_CORE Module

The CTP Core Module (CTP_CORE) (2)

→ Readout & Monitoring:

Copied into FIFOs for every L1A **(+ programmable window around L1A)**:

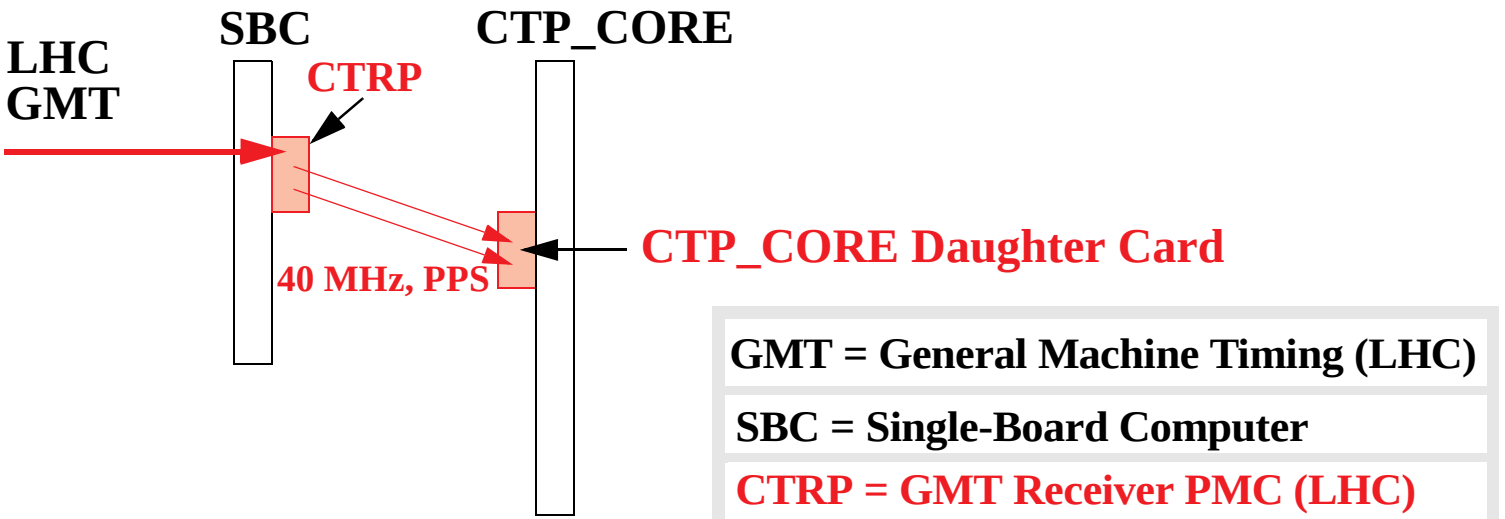
- 160 signals from the **PIT** bus + 12 internal triggers
- 256 trigger items before prescaling (after LUT and CAM) (**TBP**)
- 256 trigger items after prescaling (**TAP**)
- 256 trigger items after veto (**TAV**)
- 64-bit **UTC** time-stamp (based on GPS) with 5-ns jitter



Readout & Monitoring of the CTP_CORE Module

The CTP Core Module (CTP_CORE) (3)

→ Time Stamping:



GMT = General Machine Timing (LHC)

SBC = Single-Board Computer

CTRP = GMT Receiver PMC (LHC)

PPS = Pulse Per Second

→ Use **LHC General Machine Timing (GMT)** (CERN/AB/CO) system, which contains GPS-based precise UTC time

CTRP card (CERN/AB/CO) on single-board computer receives GMT signal

CTP_CORE daughter card receives 40.00 MHz and pulse-per-second from CTRP card and contains 200.00 MHz counter
At every L1A it produces a time-stamp with relative precision of 5 ns

→ ***Measure absolute time precision, expect much better than 1 μs***
→ ***Use other information from GMT, e.g. cycle type, beam energy***

The Testing of the CTP

- **Test beam programme during Autumn 2004:**

  Combined beam tests for prototypes and final modules
  of all ATLAS sub-detectors and trigger and data acquisition

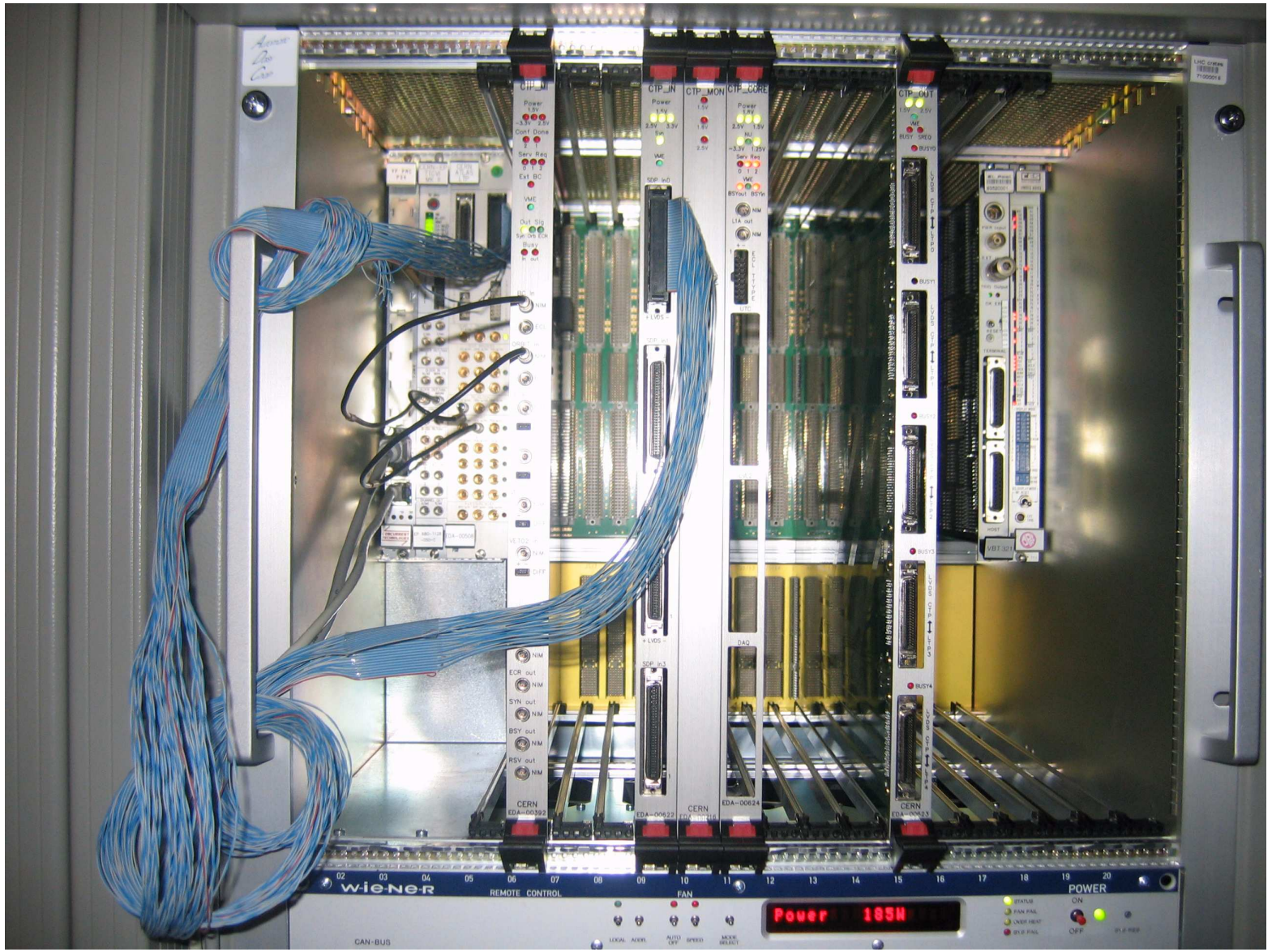
  Trigger Input:

Calorimeter Trigger:	1 CABLE: 4×3 bit e/γ + 4×3 bit jet multiplicities
	1 CABLE: 1 bit total E_T
Muon Trigger:	1 CABLE: 6×3 bit muon multiplicities, from MUCTPI, 1 Sector Logic RPC or TGC
Scintillators:	1 CABLE: 3×1 bit scintillators (via LTP → CTP_IN)
	⇒ total of 46 bits

- **Full-system stand-alone tests in Laboratory:**

  - **Use LTP to emulate trigger input:**
    pattern generator and dedicated cable with **16 (out of 31) signals** + parity
  - Full chain: LTP → CTP (→ LTP)
  - Alternatively use MUCTPI for trigger input

The CTP Full-System Tests (1)



The CTP Full-System Tests (2)

- **Timing-In:**

→ Arrival of trigger inputs at CTP_IN:

- **synchronization** (phase) w.r.t. to local clock,
  local clock can be shifted by DELAY25 (PHOS4)
- **alignment** (BC) w.r.t. to latest trigger input, uses pipeline

Method A (Phase):

- measure phase of trigger inputs with HPTDC

Method B (Data):

- capture trigger inputs in diagnostic memory and
  compare with expected data
- reduce clock delay until data errors appear

Method C (Parity):

- same as method B (or in addition to method B) but using parity error

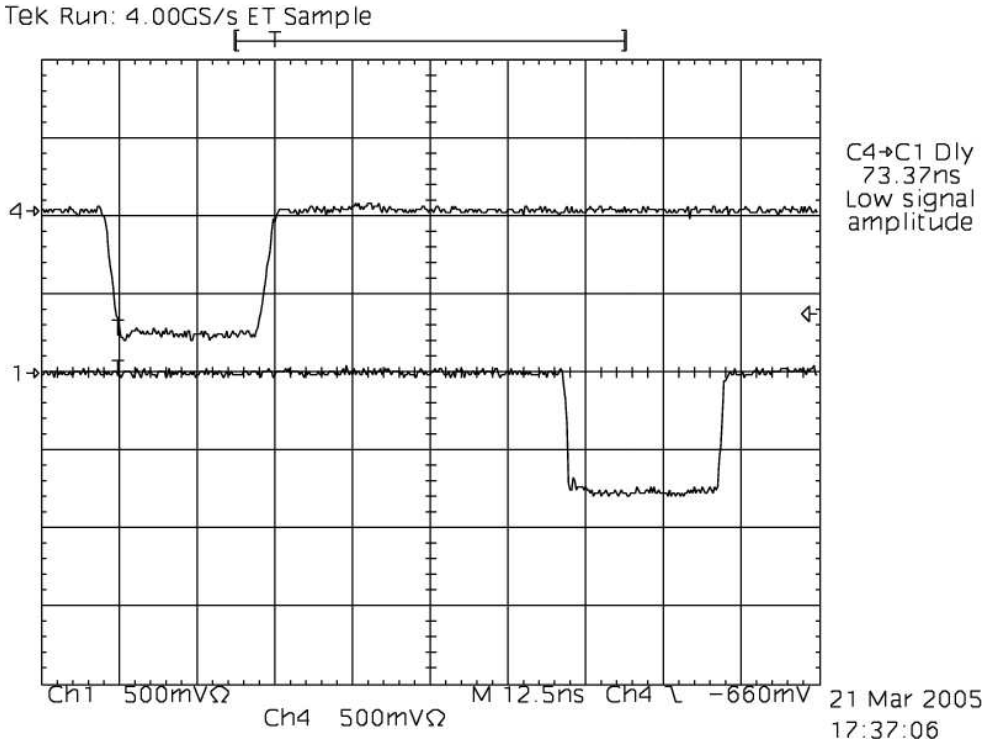
⇒ Automatic procedure:

Sample all trigger inputs, adjust phase synchronization,
and BC alignment if expected data are known

→ CTP_CORE timing is fixed w.r.t. to CTP_IN(s)

The CTP Full-System Tests (3)

- **Trigger Formation:**



"C4": B-GO<1> = PIT<43> signal at the front-panel output of LTP
+ 17 ns after PIT<43> signal at CTP_IN front-panel input

"C1": L1A signal at front-panel output of CTP_CORE
+ 1 ns before L1A signal at CTP_OUT LVDS connector

⇒ **total latency ≈ 91 ns**

including some safety margin for timing-in:

⇒ ***CTP latency ≈ 95 ns (latency target was 100 ns)***

The CTP Full-system Tests (4)

- **Control and Monitoring:**

  Use common ATLAS ROD Crate DAQ,
  i.e. configuration and run controllers

  (see also presentation "VMEbus Processor Hardware and Software Infrastructure in ATLAS" by M. Joos)

  Use trigger database and trigger menu compiler for configuration of event-selection criteria, etc.

  (see also presentation "Configuration of ATLAS Trigger" by R. Spiwoks)

  Use run controllers with low-level hardware-access software

  Monitoring software is currently under development:
  - event sampling
  - integrating scalers, bunch-to-bunch scalers, deadtime scalers
  - global values, including temperature and voltage

Conclusion

CTP has been used during Autumn 2004 test beam and full-system tests to generate triggers with real and emulated trigger inputs

Measured CTP latency is ~ 95 ns (< 100 ns)!

Work on the CTP to be finished:

- **test of CTP Core module firmware for readout&monitoring**
- **design and manufacturing of CTP Calibration module**
- **monitoring software**

CTP will be installed in underground counting room and available for ATLAS commissioning from Autumn 2005