The ATLAS Level-1 Central Trigger Processor (CTP)

R. Spiwoks[1], S. Ask[1], N. Ellis[1], P. Farthouat[1], P. Gällnö[1], J. Haller[1], A. Krasznahorkay[1,2], T. Maeno[1], T. Pauly[1], H. Pessoa Lima Jr.[3,4], I. Resurreccion Arcas[1], G. Schuler[1], J.M. de Seixas[3], R. Torga Teixeira[1], T. Wengler

1) CERN, Geneva, Switzerland
2)University of Debrecen, Debrecen, Hungary
3) Brazilian Center for Research in Physics, Rio de Janeiro, Brazil
4) Federal University of Rio de Janeiro, Rio de Janeiro, Brazil

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Abstract

The ATLAS Level-1 Central Trigger Processor (CTP) combines information from calorimeter and muon trigger processors and makes the final Level-1 Accept (L1A) decision on the basis of lists of selection criteria (trigger menus). In addition to the event-selection decision, the CTP also provides trigger summary information to the Level-2 trigger and the data acquisition system. It further provides accumulated and bunch-by-bunch scaler data for monitoring of the trigger, detector and beam conditions. The CTP will be presented and results will be shown from tests with the calorimeter and muon trigger processors connected to detectors in a particle beam, as well as from stand-alone full-system tests in the laboratory which were used to validate the CTP.

I. The Level-1 Trigger System

The ATLAS Level-1 trigger [1] is based on multiplicity information from clusters found in the calorimeters and from tracks found in dedicated muon trigger detectors. The overview of the ATLAS Level-1 trigger is shown in Figure 1.

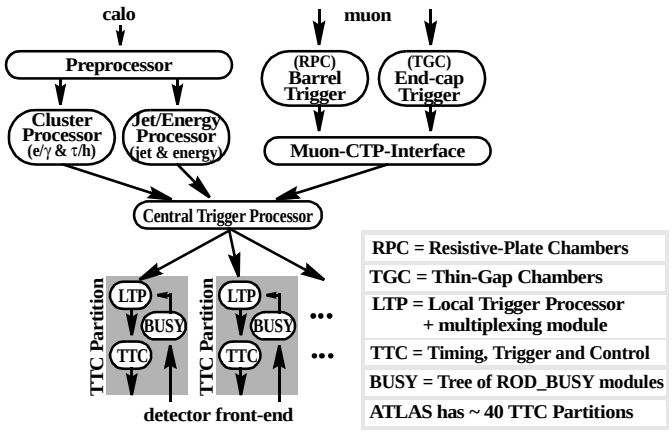

Figure 1:The Overview of the ATLAS Level-1 Trigger

The calorimeter [2] and muon [3],[4] trigger processors provide trigger information to the CTP. The CTP forms the Level-1 Accept (L1A) and fans it out to the TTC partitions of the experiment. Each TTC partition contains one Local Trigger Processors (LTP) [5], a TTC system proper [6], and a tree of ROD_BUSY modules [7]. The CTP provides trigger summary information to the Level-2 trigger system and to the data acquisition system [8]. It is configured, controlled and monitored by the Atlas Online system [9].

The LTP provides the facility to run with the trigger and timing signals from the CTP, but can also generate the signals locally. In order to allow several combinations of TTC partitions to run independently of the CTP, a new LTP interface module is being developed. It will allow to perform concurrent calibration runs of the calorimeter detectors with the calorimeter trigger, and of the muon detectors with the muon trigger, without requiring any recabling.

II. The Functionality of the CTP

A. The Trigger Formation

The CTP receives trigger information from the calorimeter and muon trigger processors. The trigger information consists of multiplicities for electrons/photons, taus/hadrons, jets, and muons, and of flags for total transverse energy, total missing energy, and total jet transverse energy. The CTP also provides internal triggers from random generators, for bunch crossing groups, and pre-scaled clocks.

All triggers and their thresholds are programmable. Several thresholds are used concurrently for each type of trigger information. A total number of 160 input bits are taken into account by the CTP at any given time. The total number of input bits can be higher because of selection at the input to the CTP.

1 MU6	mask = ON, priority = LOW, pre-scaling =	1000
2MU6	mask = ON, priority = HIGH, pre-scaling =	1
1EM10 AND XE20	mask = ON, priority = LOW, pre-scaling =	1
...		

Figure 2:An Example of an Excerpt of a Level-1 Trigger Menu

The CTP generates a L1A derived from the trigger inputs according to the Level-1 trigger menu. The Level-1 trigger menu consists of 160 trigger items each of which is a combination of one or more conditions on trigger inputs. E.g. if *"EM10"* symbolizes the trigger input for electrons/photons with a transverse energy of at least 10 GeV, then *"1EM10"* symbolizes the condition of there being at least one electron/photon above that threshold. Several of these conditions can be combined to make a trigger item. Each trigger item also has a mask, a priority, and a pre-scaling factor. The priority is for the preventive dead-time generated by the CTP, see Section II.B. High-prior-

ity items see as little deadtime as possible, while low-priority items see a comparatively higher deadtime. The L1A is the logical OR of all trigger items. An example of an excerpt of a Level-1 trigger menu is shown in Figure 2.

B. Additional Functionality

The CTP not only generates the L1A but also provides with each L1A an 8-bit trigger type word which is sent promptly via the TTC system to the detector front-end electronics and which indicates the type of trigger. It can be used for event data processing. The CTP further generates deadtime in order to prevent front-end buffers becoming full. Two leaky-bucket algorithms limit the number of L1As to be generated in a period of time. The number and period are programmable. The two algorithms can be used to defined two priorities of trigger items. The CTP also provides mechanisms for generating the event counter reset (ECR).

The CTP sends, at every L1A, Region-of-Interest (RoI) information to the Region-of-Interest Builder (RoIB) in the Level-2 trigger system for guidance of the Level-2 trigger algorithms. It also sends, at every L1A, trigger summary information to the Read-Out System (ROS) of the data acquisition system. This information is a superset of the RoI information and can contain several bunches before and after the triggering bunch for debugging and monitoring purposes. The trigger summary information provides much more information than the trigger-type word and allows detailed understanding of why the event was selected. The CTP also provides a GPS-based UTC time stamp in the trigger summary information. This allows to correlate the event to other events taken in particle or astrophysics experiments all over the world, see also Section III.C.

The CTP also provides monitoring data: snapshots of incoming data, bunch-by-bunch monitoring of inputs, see Section III.C, and scalers of trigger inputs and trigger items before and after pre-scaling integrated over all bunches.

C. The Constraints

The formation of the trigger is required to be performed within four bunch crossings from input into the CTP until output of the L1A out of the CTP. This corresponds to a latency of 100 ns.

The Level-1 trigger menu used for the trigger formation is expected to change frequently depending on the physics, beam and detector conditions. High flexibility has to be provided for the trigger formation.

III. The Implementation of the CTP

A. Overview

The CTP consists of the following modules:

- up to three input (CTP_IN) modules,
- a core (CTP_CORE) module for trigger formation, read-out and monitoring, and time stamping,
- a bunch-by-bunch monitoring (CTP_MON) module,
- up to four output (CTP_OUT) modules connecting to the LTPs in the TTC partitions of the detectors,
- a machine interface (CTP_MI) module for timing signals, and
- a calibration (CTP_CAL) module for calibration requests from the detectors.

The CTP modules are housed in a 9U VME64x crate. In addition to the standard VMEbus, the CTP modules also use dedicated buses for synchronized and aligned trigger inputs (PITbus, PIT = pattern in time), for the common timing and trigger signals (COMbus), and for the calibration requests from the detectors (CALbus). The overview of the implementation of the CTP is shown in Figure 3.

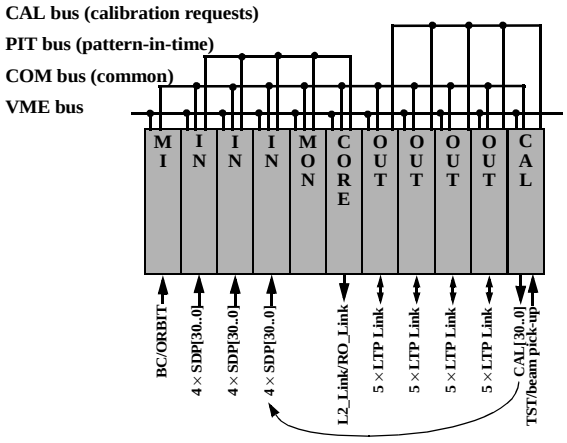

Figure 3:The CTP Design with its Modules, Backplanes, and Signals

In the following sections only the CTP input module and the CTP core module will be presented in some detail. For the other modules refer to [10].

B. The CTP_IN Module

The block diagram of the trigger path of the CTP input module is shown in Figure 4.

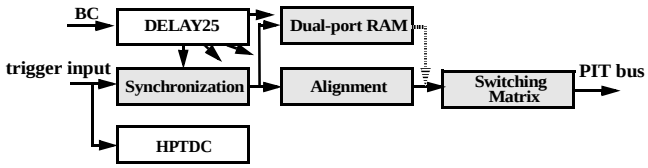

Figure 4:The Trigger Path Diagram of the CTP_IN Module

The CTP_IN module receives trigger inputs from the trigger processors, like the calorimeter or muon trigger processors or other sources. It measures the phase of the trigger inputs using a CERN High-Performance TDC (HPTDC) [11]. The clock of the CTP_IN module can be adjusted using the CERN DEAY25 chip [12]; on an older version of the CTP_IN module the CERN PHOS4 chip [13] was used.

The synchronized trigger inputs can be stored in diagnostic memory (dual-port RAM) for debugging and monitoring. They are aligned with respect to the bunch crossing they originate from using pipelines in an FPGA. The CTP_IN module selects and routes trigger inputs to be sent to the PITbus using a

switching matrix implemented in a CPLD.

C. The CTP_CORE Module

The block diagram of the trigger path of the CTP_CORE module is shown in Figure 5.

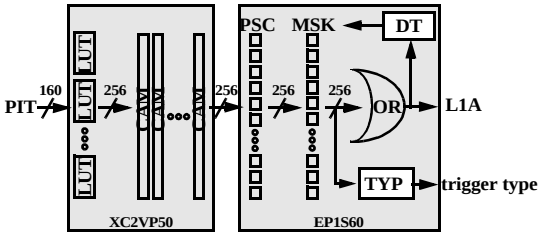

Figure 5:The Trigger Path of the CTP_CORE Module

The CTP_CORE module receives the pattern in time from the PITbus and combines them using Look-up Tables (LUT) and Content-Addressable Memories (CAM) to form 256 trigger items. Each CAM contains a 256-bit word and is ternary, i.e. allows bitwise matching of “0”, “1” or “don’t care”. The 256 trigger items are prescaled using 24-bit prescalers (PSC) and masked with a general mask, deadtime and busy (MSK) before they are ORed to generate the Level-1 Accept (L1A), Preventive deadtime (DT) is generated from the L1A and the trigger-type word from the trigger items after masking (TYP).

The CTP_CORE module sends RoI information to the RoIB of the Level-2 trigger system, and trigger summary to the ROS of the data acquisition system. The readout and monitoring of the CTP_CORE module is shown in Figure 6.

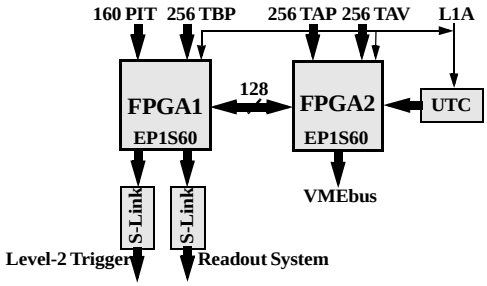

Figure 6:The Readout and Monitoring of the CTP_CORE Module

For every L1A data in a programmable window before and after the L1A and from each stage of the processing are written into FIFOs embedded in two FPGAs. The data captured include:

- 160 PIT signals and the 12 internal triggers,
- 256 trigger items before prescaling (TBP),
- 256 trigger items after prescaling (TAP),
- 256 trigger items after veto (TAV), and a
- 64-bit time UTC time-stamp from the time-stamping system.

The time stamping of the CTP_CORE module is based on the LHC General Machine Timing (GMT) [14] system which contains a GPS-based precise UTC time. The GMT signal is received using a CTRP card [14] on the single-board computer in the CTP crate. The CTRP card produces a 40.000 MHz and a 1 Hz signal (“pulse-per-second”) which are sent to a daughter card on the CTP_CORE module. The daughter card contains a 1 Hz counter, and a 200 MHz counter. At every L1A it produces a 64-bit time-stamp with a relative precision of 5 ns. The time stamping system is shown in Figure 7.

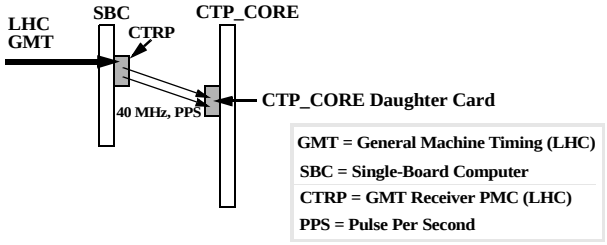

Figure 7:The Time Stamping of the CTP_CORE Module

IV. Tests and Results

The CTP has been tested in the ATLAS testbeam programme during Autumn 2004. The aim of the test beam programme was to run prototypes and final modules of all ATLAS detectors and trigger and data acquisition in a combined way. A total of 46 trigger input bits were received at the CTP from the calorimeter trigger, the muon barrel and end-cap triggers, and from scintillators in the beam.

The tests of the CTP were then continued in the laboratory using an LTP to emulate the trigger input. A total of 16 trigger input bits can be generated in a fully programmable way. The full chain from trigger to CTP to LTP could also be tested. The Muon-CTP-Interface could be used as a trigger input, alternatively to the LTP. The CTP full-system stand-alone set-up is shown in Figure 8.

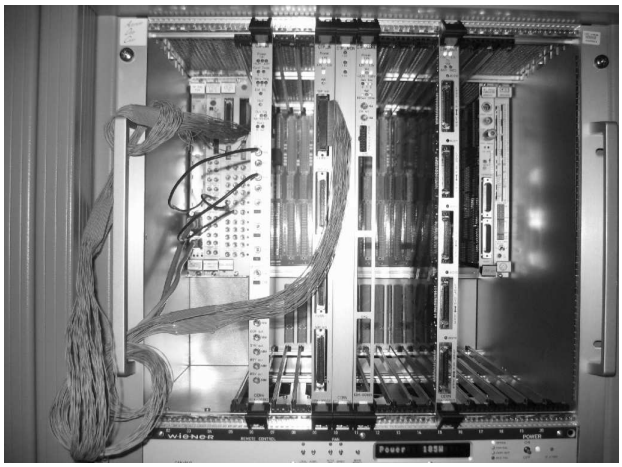

Figure 8:The Full-System Stand-Alone Test of the CTP

Timing-in of the trigger inputs is a very important aspect of the functionality of the CTP. Trigger inputs arriving at the CTP_IN(s) have to be synchronized in phase with respect to the local clock which can be shifted using the DELAY25 (or PHOS4). Trigger inputs are aligned in BC with respect to the same bunch crossing using pipelines. Several methods were tried for the timing-in:

- In **method A (Phase)** the phase of the trigger inputs in measured using the HPTDC.
- In **method B (Data)** the diagnostic memories of the CTP_IN(s) are used to capture the incoming data and to compare them to expected data. The clock phase is reduced until data errors appear.
- **Method C (Parity)** is similar to method B and can be used in addition to it. It uses the parity error of the trigger input on the CTP_IN.

An automatic procedure was developed which samples all trigger inputs and adjusts the phase synchronization and the BC alignment, supposing that the expected data are known. The timing of the CTP_CORE module with respect to the CTP_IN modules is a constant of the CTP.

The latency of the CTP from input to the CTP_IN and output of the CTP_OUT was measured. Figure 6 shows such a measurement. Signal “C4” is the B-GO<1> signal of the LTP which is used as PIT<43> on a CTP_IN. This signal is taken at the front-panel output of the LTP and arrives 17 ns after the signal the front-panel input of the CTP_IN. Signal “C1” is the L1A signal at the front-panel output of the CTP_CORE and arrives 1 ns before the signal at the LVDS connector of a CTP_OUT. Considering this and adding a safety margin for several cables on the CTP_IN, and for several CTP_INs, the latency is about 95 ns. This has to be compared to the required maximum latency of 100 ns.

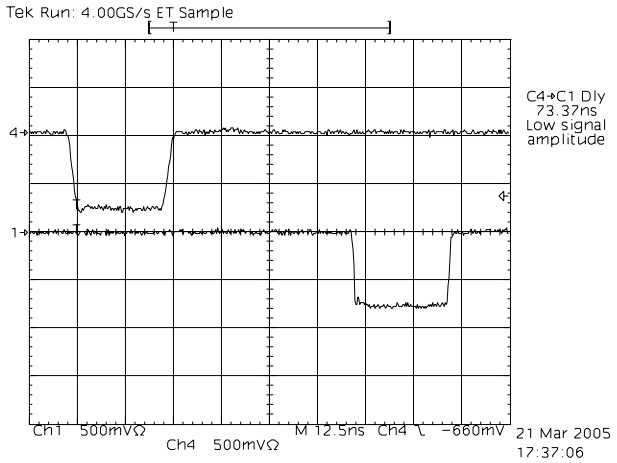

Figure 9:The Latency Measurement of the CTP
(Read text for explanation of the signals)

The CTP uses the common ATLAS ROD Crate DAQ [15] for configuration and control. A trigger database and a trigger menu compiler are used for the configuration of the event-selection criteria [16]. Software run controllers are used with low-level hardware-access libraries to control the CTP modules. Monitoring software is currently under development for event sampling, reading of integrating scalers, bunch-by-bunch scalers, and deadtime scalers, as well as for global values, including temperature and voltage.

V. Conclusion

The CTP has been used during Autumn 2004 test beam and full-system tests in the laboratory to generate triggers with real and emulated trigger input. The latency of the CTP was measured to be 95 ns, which is below the required 100 ns. Some work on the CTP, in particular, the test of the CTP core module firmware for readout and monitoring, the design and manufacturing of the CTP calibration module, and the development of the monitoring software, needs to be finished. The CTP will be installed in the underground counting room of ATLAS and it will be available for commissioning of the detectors and the triggers from Autumn 2005.

VI. References

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[10] P. Borrego Amaral et al., The ATLAS Level-1 Central Trigger System, IEEE Trans. on Nucl. Sci., Vol. 52, No. 4, August 2005.

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[14] The LHC General Machine Timing (GMT) is developed at CERN/AB/CO group.

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[16] See R. Spiwoks et al., “Configuration of the ATLAS Trigger”, these proceedings.