# The ATLAS Level-1 Trigger Timing Setup

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*Abstract* — **The ATLAS detector at CERN's LHC will be exposed to proton-proton collisions at a bunch-crossing rate of 40 MHz. In order to reduce the data rate, a three-level trigger system selects potentially interesting physics processes. The first trigger level is implemented in electronics and firmware. It aims at reducing the output rate to less than 100 kHz. The Central Trigger Processor (CTP) combines information from the calorimeter and muon trigger processors and makes the final Level-1-Accept (L1A) decision. It is a central element in the timing setup of the experiment. Three aspects are considered in this article: the timing setup with respect to the Level-1 trigger, with respect to the experiment, and with respect to the world.**
**Trigger signals from the muon and calorimeter trigger processors have to be synchronized in phase with respect to the local clock, and aligned in terms of the bunch crossing they originate from. The Level-1 latency is defined as the time between the collision and the arrival of the L1A at the sub-detectors. It is fixed and less than 2.5 usec. During this time, the data from all sub-detectors are stored in front-end pipeline buffers. In order to guarantee read-out of the same collision, the pipeline lengths must be carefully tuned in order to match the Level-1 latency using several strategies with and without particle beam. The CTP further calculates a UTC time stamp derived from a GPS-based time-stamping system with a stability of 5 nsec and high absolute time precision. The time stamp will allow us to correlate ATLAS events with those in other particle-physics or astronomic detectors at CERN or elsewhere.**

## I. Introduction

The ATLAS Level-1 (LVL1) trigger [1] is based on multiplicity information from clusters in the calorimeters and from tracks in dedicated muon trigger detectors, as well as global transverse energy information from the calorimeters. An overview of the ATLAS LVL1 trigger is shown in Fig. 1.

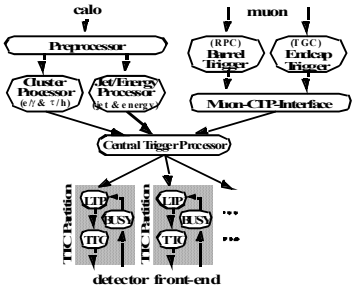


Figure 1: Overview of the ATLAS Level-1 Trigger.

The calorimeter [2] and muon [3], [4] trigger processors provide trigger information to the Central Trigger Processor (CTP) [5]. The CTP forms the LVL1 Accept (L1A) and fans it out to Timing, Trigger and Control (TTC) partitions. In the ATLAS experiment there are about 40 TTC partitions. Each partition contains one Local Trigger Processor (LTP) [6], a TTC system [7] proper, and a busy tree which allows one to throttle the generation of L1As and which is based on the ROD_BUSY module [8]. The CTP provides trigger summary information to the Level-2 (LVL2) trigger system and to the data acquisition system [9]. It is configured, controlled and monitored by the Online system [10].

## II. The Level-1 Trigger

The Level-1 Trigger consists of the calorimeter trigger, the muon trigger, the CTP, and the sub-detector front-end TTC partitions. The calorimeter trigger is described in [2], the muon trigger in [3] and [4]. The following sections describe the CTP, and the LTP which is the master of a TTC partition.

### *A. The Central Trigger Processor (CTP)*

The CTP [5] receives trigger information from the calorimeter and muon trigger processors. This consists of multiplicities for electrons/photons, taus/hadrons, jets, and muons, and of flags for total transverse energy, total missing transverse energy, and total jet transverse energy. Additional inputs are provided for special triggers such as a minimum-bias trigger based on scintillator counters.
The CTP generates L1As derived from the trigger inputs according to the LVL1 trigger menu. The menu consists of up to 256 trigger items each of which is a combination of one or more conditions on the trigger inputs and the internal triggers provided by the CTP, i.e. two random triggers, two pre-scaled clocks, and eight triggers for programmable groups of bunch crossings. Each trigger item further has a mask, a priority, and a pre-scaling factor. The L1A is the logical OR of all trigger items. The CTP generates the L1A within 100 nsec, i.e. from input of the trigger information to output of L1A signal. This corresponds to a latency of four bunch crossings (BCs).

The CTP consists of several different modules which are housed in a single 9U VME64x crate. In addition to VMEbus, the CTP modules use custom buses for the synchronized and aligned trigger inputs (PITbus, PIT = pattern in time), for the common timing and trigger signals (COMbus), and for the

sub-detector calibration requests (CALbus). An overview of the design of the CTP is shown in Fig. 2.

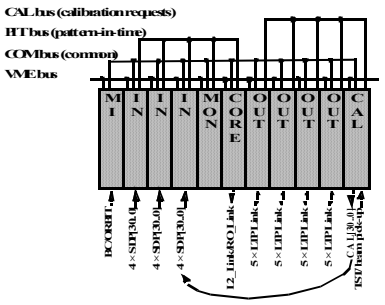


Figure 2: The Central Trigger Processor (CTP).

The CTP machine interface module (CTP_MI) receives timing signals from the LHC via the TTCmi [7], or generates them locally. The CTP_MI sends the timing signals to the COMbus.

The CTP input module (CTP_IN) receives trigger inputs from the trigger processors and other sources. It synchronizes the trigger inputs with respect to the internal clock, checks their parity, and aligns them with respect to the bunch-crossing identifier. The CTP_IN selects and routes trigger inputs to be sent to the PITbus.

The CTP core module (CTP_CORE) receives and synchronizes the trigger inputs from the PITbus. It combines them with internal triggers to build trigger items according to the LVL1 trigger menu and forms the L1A. The CTP_CORE sends the trigger results to the COMbus.

The CTP monitoring module (CTP_MON) receives and synchronizes the trigger inputs from the PITbus. It decodes and selects the trigger inputs to be monitored. The CTP_MON scales trigger information on a bunch-by-bunch basis.

The CTP output module (CTP_OUT) receives timing and trigger signals from the COMbus and fans them out to the sub-detector LTPs. The CTP_OUT also receives busy signals and calibration requests from the LTPs. It masks and monitors the busy signals, and provides them to the COMbus. It provides the calibration requests to the CALbus.

The CTP calibration module (CTP_CAL) time-multiplexes the calibration requests on the CALbus and sends them to the CTP_IN. The CTP_CAL also contains other external inputs for beam pick-up monitors and test triggers which are sent via cable to the CTP_IN.

### *B. The Local Trigger Processor (LTP)*

The LTP [6] is the interface between the CTP and the sub-detector front-end TTC partitions. Every TTC partition has one LTP which is its master and which allows the TTC partition to be run in either of two different modes:

- In global mode the TTC signals from the CTP are used. The TTC partition is part of the main ATLAS run.
- In local mode the TTC signals from the local inputs or the pattern generator are used. The TTC partition is run stand-alone.

In addition, it is possible to connect several TTC partitions using their local outputs and local inputs in order to allow stand-alone running of combinations of different TTC partitions.

The LTP essentially consists of a programmable switch allowing one to interconnect any input to any output and a pattern generator as shown in Fig. 3.

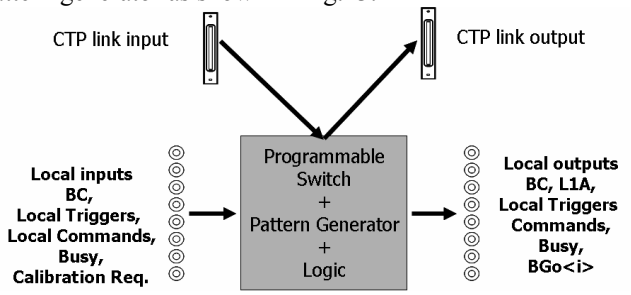


Figure 3: Simplified block diagram of the LTP.

The interface to the CTP is provided by a differential link. Several LTPs of the same sub-detectors are daisy-chained in order to reduce the number of connections to the CTP. The LTP has local outputs for the TTCvi [7] of the TTC partition. In addition, it has local outputs for sub-detector-specific use or for combining several TTC partitions. The local inputs can be used for local mode. The pattern generator allows one to generate internal signals for each BC. It is implemented using a 1 MWord RAM which can be written using VMEbus and which is read out at the BC frequency.

## III. TIMING SETUP WITH RESPECT TO THE LEVEL-1 TRIGGER

Trigger Signals between the calorimeter and muon trigger processors on one side and the CTP on the other side have to be timed in considering two aspects:

- The phase synchronization, which defines the phase of the incoming trigger signals with respect to the local BC clock: setup times have to be respected in order for the trigger signals to be correctly taken into account by the CTP.
- The Bunch-Crossing Identifier (BCID) alignment, which defines the BCID relation of all incoming trigger signals with each other: earlier arriving trigger signals have to be delayed by multiples of BC in order for all trigger signals to be aligned at the same BCID.

Both types of timing in are schematically shown in Fig. 4.

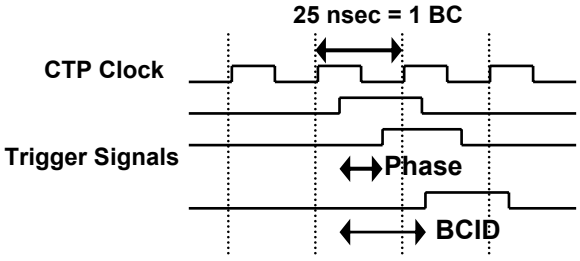


Figure 4: Phase Synchronization and Bunch-crossing Identifier Alignment of Trigger Signals.

In order to perform the phase synchronization the CTPIN module contains CERN HPTDCs [11] which allow one to measure the phase of the incoming trigger signals, see Fig. 5.

After the phase of all trigger signals has been measured, a CERN PHOS4 [11] or CERN DELAY25 [12] chip, depending on the generation of CTPIN module, is used in order to displace the local clock so that the setup time of the CTPIN module for the trigger signals is respected. In addition, the measurement of the phase will be continued during running for monitoring purposes.

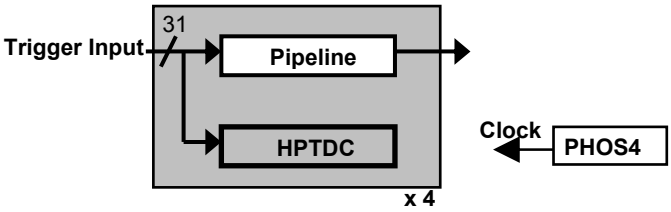


Figure 5: Schematic View of Part of the CTP Input Module.

In order to perform BCID alignment the calorimeter and muon trigger processors send test patterns which are synchronized with the Bunch Counter Reset (BCR) signal, which defines BCID = 0. Alternatively, other synchronization signals can be used as long as those signals have a known or measured timing relation with the test pattern. The CTPIN module contains diagnostic memories for capturing the incoming trigger signals. Comparison between captured and expected trigger signal patterns is used to define the alignment. The CTPIN module has one pipeline for each trigger signal with a programmable length of up to 63 BCs. This corresponds to BCID alignments of up to 1.6 usec.

## IV. Timing Setup with respect to the Experiment

The read-out of the ATLAS experiment at the level of the Level-1 trigger is based on a fixed latency, see Fig. 6. Signals from the sub-detectors are held in synchronous pipeline buffers until the arrival of the L1A signal. When this signal arrives the data are read out and transmitted to the next level of data acquisition. For this to work correctly and for complete events to be built from all sub-detectors, the pipeline lengths must be aligned in order to read data coming from the same BC. After the Level-1 trigger, the data are provided with a Level-1 identifier and an additional BC identifier. The read-out is then asynchronous and based on these identifiers.

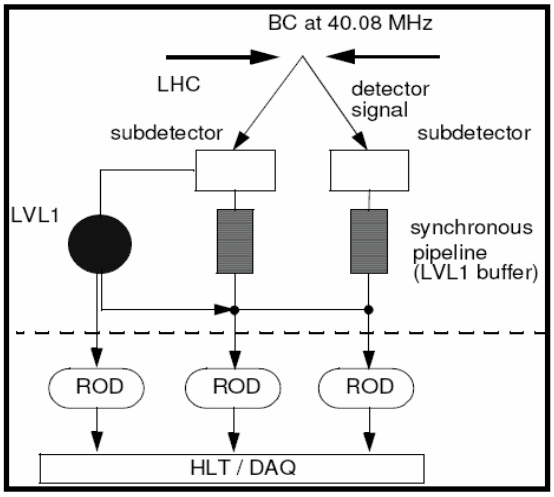


Figure 6: Level-1 Latency and Read-out at Level-1.

In order to define the timing setup with respect to the experiment several methods have to be used, often in combination:

- Latencies have to be measured or calculated. This is, in particular, important for the time of flight of particles, for signal cables lengths and for latencies of all electronics modules.
- Latencies can be measured using test pulses which are sent a known time before a corresponding Level-1 Accept. The test pulses can be used to inject data at several levels of the front-end electronics. This method can be used at the level of the whole experiment using the CTP, or at the level of individual TTC partitions using the LTP.
- The timing setup can be measured using the beam structure of the LHC. A statistical method with low trigger thresholds allows one to collect data over some time and then compare it with the timing structure of the LHC beams which is shown in Fig. 7.

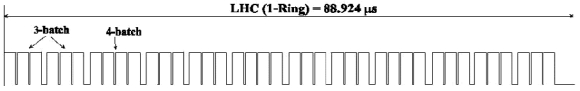


Figure 7: LHC Beam Structure.

In addition to the methods described above, there are also two detectors which directly observe the beam:

- Silicon-counter hodoscopes [13] are placed in the two end-cap regions of the experiment. They can be used to define a minimum-bias trigger consisting of the coincidence of signals on both sides.
- Beam pick-ups [14] are placed 175 m on both sides of the experiments, see Fig. 8. They can be used to define a filled-bunch trigger which can be used as reference for the timing structure of the LHC beam. In addition, they can be used to monitor the phase between the LHC clock and the LHC bunches.

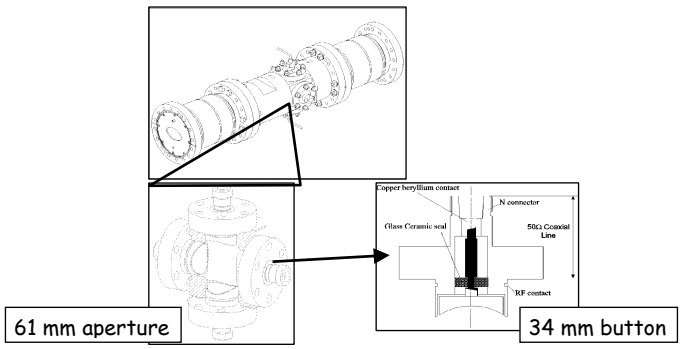


Figure 8: Beam Pick-ups.

## V. Timing Setup with respect to the World

In order to compare events observed in the ATLAS experiment with other events observed in other particle physics or astronomic experiments at CERN or elsewhere every event accepted at the Level-1 trigger is tagged with a precise time-stamp. This time-stamp is provided by a GPS-based UTC time stamp transmitted over the LHC General Machine Timing (GMT) system [15].

The schematic view of the time-stamping system is shown in Fig. 9. The LHC GMT signals are received by a CTRP card which is provided by the CERN/AB/CO group. The card is of PMC format and is attached to the single-board computer which controls the CTP. The CTRP card is programmed to deliver a Pulse-Per-Second (PPS) signal and a 40.00 MHz clock locked with the PPS. These signals are fed to a daughter card on the CTP Core Module which uses the PPS signal for a seconds counter, and the 40MHz clock to lock a 200 MHz counter. At arrival of a L1A the values of the seconds and of the 200 MHz counter are read and stored in the event record which is transmitted to the data acquisition system.

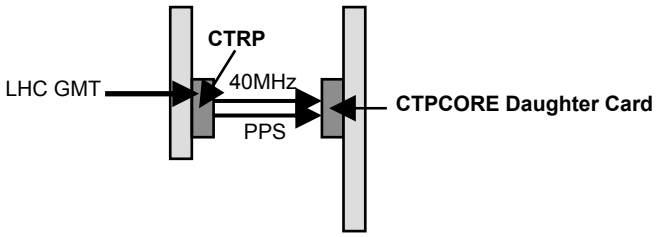


Figure 9: Schematic View of the Time-stamping System of the CTP.

The relative timing precision of the time-stamping system is 5 nsec. The absolute precision depends on the calibration of the LHC GMT system with the GPS timing reference. It is expected that an absolute precision of about 25 nsec could be achieved.

## VI. Conclusions

Several aspects of the timing setup of the ATLAS Level-1 trigger are presented. The CTPIN module provides the tools necessary to define the synchronization and alignment of the trigger signals from the muon and calorimeter trigger processors. The CTP and LTP will be used for the timing setup of the experiment using measurement and calculation of latencies, test pulses and a statistical method using the timing structure of the LHC beam. In addition, the CTP contains a GPS-based time-stamping system which allows correlating ATLAS events with events all over the world.

## Acknowledgments

We would like to thank our colleagues from the CERN/AB/CO group for providing us with the LHC GMT timing signal, the CTRP card, the driver and their help.

## References

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