EUROPEAN ORGANIZATION FOR NUCLEAR RESEARCH
ORGANISATION EUROPEENNE POUR LA RECHERCHE NUCLEAIRE

CERN - AB Department

AB-Note-2005-017-RF

PS BOOSTER BEAM TESTS OF THE NEW DIGITAL BEAM CONTROL SYSTEM FOR LEIR

M. E. Angoletta, A. Blas, J. Bento, J.H. DeLong*, A. Findlay,
P. Matuszkiewicz, F. Pedersen, A. Salom-Sarasqueta.

Abstract

We have been developing a scaled-down prototype of the new digital beam control and cavity servoing system for CERN’s Low Energy Ion Ring (LEIR). The system hardware and software, developed as part of a CERN-BNL collaboration, are based on new all-digital technology already deployed at BNL's AGS Booster. The system relies on VME modules, carrying Digital Signal Processors (DSPs) as well as Field Programmable Gate Arrays (FPGAs), and daughter cards. New concepts deployed include software implementation through DSPs & FPGAs of reference-functions and timings generation. Additionally, a user-selectable digital data acquisition functionality provides diagnostic and troubleshoot access points, a new feature which is very useful in a digital system. The scaled-down prototype implements frequency program, radial steering, phase and radial loop capabilities and has been tested in CERN's PS Booster (PSB) during the 2004 run. The measured time constants of the different loops agree with the design values. In addition, the generation of reference functions and timings by software, as well as the digital data acquisition scheme have been validated at DSP level. In this paper we describe the prototype used in the PSB tests, both hardware and software, and the operational results obtained. Finally, we present an outline of the final LEIR system and of the roadmap for applying the same technology to other CERN accelerators.

* Brookhaven National Laboratory, Upton, USA

Geneva, Switzerland
November 2005

1. INTRODUCTION

A new digital beam control and cavity servoing system is under development for CERN's Low Energy Ion Ring (LEIR) [1]. During the PS Booster (PSB) 2004 run a set of tests with beam were performed by means of a scaled-down prototype of the LEIR system. These tests expanded a previous series of tests [2] carried out in summer 2003. With respect to the system used in 2003, the new prototype deploys new hardware as well as new FPGA and DSP code. Phase loop, radial loop, radial steering and frequency program are implemented and the beam can be successfully steered and accelerated until extraction. Moreover, the overall DSP software structure is very similar to that planned for LEIR.

LEIR and PSB, with their rather high revolution frequency f_{REV} and synchrotron frequency f_S, are the most challenging CERN machines in terms of required bandwidth for the beam phase loop. Beam testing in the PSB is convenient as fully parasitic tests may be run. The PSB is an attractive benchmark since its $\mathrm{f_S}$ and $\mathrm{f_{REV}}$ are comparable to LEIR's design values. Table 1 summarizes PSB and LEIR (for Pb^{54+} only) main parameters.

Parameter		**unit**	**LEIR (Pb^{54+})**	**PSB (p^{+})**
Injection	$f_{REV,I}$	[MHz]	0.361	0.599
	$f_{S,I}$	[kHz]	0.600	2.000
	T_I	Mev/u	4.2	49.62
	ctime, ct_I	ms	~ 200	275
Extraction	$f_{REV,E}$	[MHz]	1.423	1.746
	$f_{S,E}$	[kHz]	2.000	0.470
	T_E	Mev/u	72.2	1374.2
	ctime, ct_E	ms	2600	810
Cycle length, t_C		s	3.6	1.2
Acceleration time, t_{ACC}		s	~ 1	0.5

Table 1: *Main parameters for the PSB and LEIR (Pb^{54+}, nominal beam) typical cycles.*

The LEIR cycle lasts 3.6 seconds [1]; the design f_{REV} range is 0.361 MHz (injection) to 1.423 MHz (extraction), the whole acceleration phase taking about 1 s. The expected $\mathrm{f_S}$ range is 600 Hz to 2 kHz. In the 1.2 s PSB proton beam cycle [3] the acceleration phase takes about 0.5 s and f_{REV} values range between 0.599 MHz and 1.7458 MHz. The actual f_S ranges between 2 kHz and 470 Hz. The time from each cycle start is known as ctime; injection occurs at 275 ms and extraction at 810 ms. Figure 1 compares the behaviour of f_{REV} and momentum p for a typical proton cycle in the PSB to the same for an expected Pb^{54+} LEIR cycle. The x axis value is the ctime expressed in milliseconds.

In these tests, the beam controlled with the scaled-down prototype was made to circulate in the PSB ring four for users that do not use this ring, typically user EASTA. The PSB ejection kicker is disabled, hence the beam is dumped instead of being injected in the PS. The beam circulating in the ring is kept at a low intensity (typically of the order of 10^{11} protons) to avoid triggering the Beam Loss Monitor alarm. Occasionally and for few shots only a higher intensity is allowed in the ring.

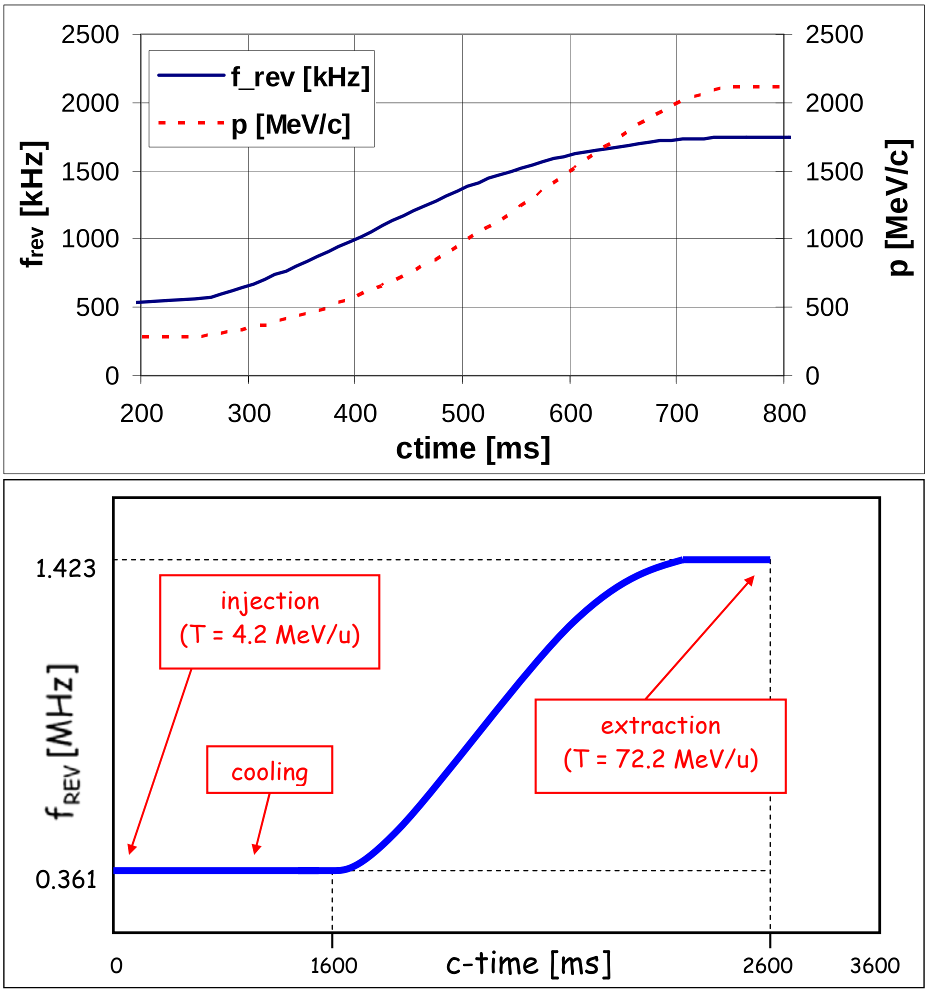


Figure 1: *Plot of the typical revolution frequency and momentum behaviour during a 1.2 seconds proton cycle in the PSB and of the expected 3.6 seconds-long Pb^{54+} LEIR cycle.*

2. SYSTEM OVERVIEW

The scaled-down beam control system prototype implements phase loop, radial loop, radial steering and frequency program capabilities via FPGA and DSP software. It controls the voltage modulation of the ring 4 CO2 cavity in the PSB. This is very convenient as this ring is available for completely parasitic tests [2]. Figure 2 gives an overview of the beam control system prototype installed in the PSB Beam Observation Room (BOR).

The system comprises one DSP carrier board carrying three daughtercards, namely:

a) a four-channels, two-sites Digital Down Converter (DDC), performing digitisation, low-pass filtering and decimation of analogue signals;

b) a one-site Master Direct Digital Synthesiser (MDDS), generating, under DSP control, a high-frequency analogue clock signal from a 100-MHz clock reference;

c) a one-channel, one site Slave Direct Digital Synthesiser (SDDS), generating, under DSP control, an analogue signal from the MDDS-generated clock reference.

The DDC daughtercard receives signals from the BR4.UPH14L4 Phase Pick-Up (PU), the BR4.CO2 Cavity and the BR4.UES Radial PU, located in PSB sectors 14, 7 and 12 respectively, as shown in Figure 3. The output of the system is generated by the SDDS and goes to the CO2 Cavity.

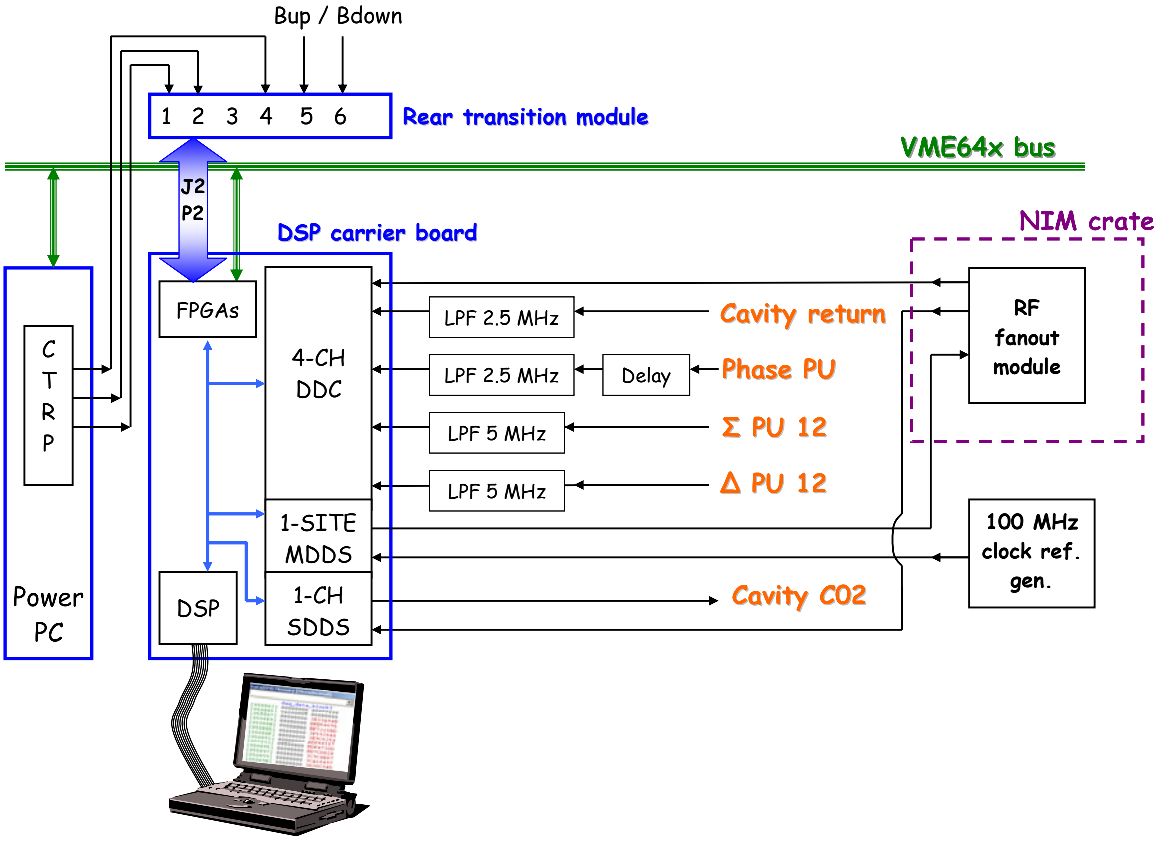


Figure 2: *Schematics of the beam control system installed in the PSB for the 2004 run. The system implements frequency program, phase-loop, radial loop and radial steering functionalities.*

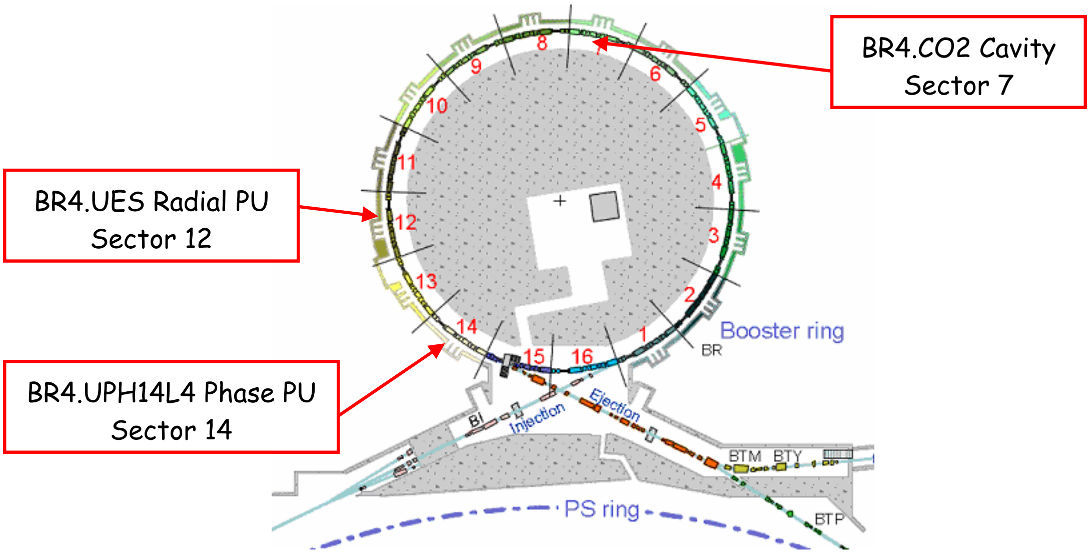


Figure 3: *Location of the elements used (PUs, cavity) in the PSB layout.*

The MDDS clock is fed to the DDC and SDDS via a standard RF fanout module, installed in a NIM crate. Its frequency

$$f_{MDDS} = h_{MDDS} \cdot f_{REV}, \qquad (1)$$

where f_{REV} is the revolution frequency calculated by the DSP, is updated every 11 μs by the DSP itself. Here the MDDS harmonic h_{MDSS} is chosen to be equal to 16.

With reference to Figure 2, a rear transition module allows feeding the system with additional analogue inputs, which are passed to the FPGAs on the DSP carrier board via the VME64x J2/P2 connector. The *Bup* and *Bdown* signals give the variation of the bending magnetic field *B* in units of 10^{-5} T and are used to implement a B-train counter. A CTRP timing receiver module [4], carried by the PowerPC, generates machine-related timings and one fixed-frequency clock (called DSP sample clock) and feeds them to the DSP carrier board via the rear transition module. The SDDS generates the cavity drive signal as the 16th sub-harmonic of the MDDS clock. The cavity voltage amplitude is controlled via the PSB standard hardware and function generator module.

In Figure 2 the phase PU, radial PU and cavity return signals are first passed through low-pass filters (LPF) with 2.5 and 5 MHz cutoff frequencies. They are then digitized in the DDC module with a sampling frequency equal to f_{MDDS}. These signals are further down-converted and digitally filtered by the DDC as described in paragraph 3.1. Finally, the DSP uses them for implementing phase and radial loops. For the phase loop, signals from the BR4.CO2 cavity and the BR4.UPH14L4 phase PU are processed to calculate the phase difference. An analogue delay of 310 ns is applied to the phase PU signal. For the radial loop, the beam radial position is calculated from Delta and Sum signal coming from the radial PU. The phase and radial loop sampling frequencies are 90 kHz and 12.7 kHz, respectively. The phase loop is closed typically at a ctime of 275.3 ms and the radial loop at a ctime of 282 ms.
A laptop is used for downloading the new code to the FPGAs located on the motherboard and on the daughtercards. The DSP is operated from the same laptop: the code is compiled and downloaded to the DSP, output data are shown on the screen or saved to a file. A picture of the experimental setup installed in the PSB BOR is shown in Figure 4.

Again with reference to Figure 2, the CTRP feeds the rear transition module with three timing signals, namely:

a) the cycle start, at ctime = 0 ms. This is a Pulse-to-Pulse Modulation (PPM) signal that starts the DSP activity.
b) The B-train count start, at ctime = 1 ms. This is a pulse which starts the FPGA-implemented B-train counter.
c) The DSP sample clock, which is a signal (sine- or square-wave) with frequency of 90 kHz.

Spare PSB RF timings were used, namely BAX.SFBQUAD for a) and BAX.EFBQUAD for b). The timing BAX.SBCLI was used to switch the cavity modulation control from the analogue beam control system to the new digital prototype version.

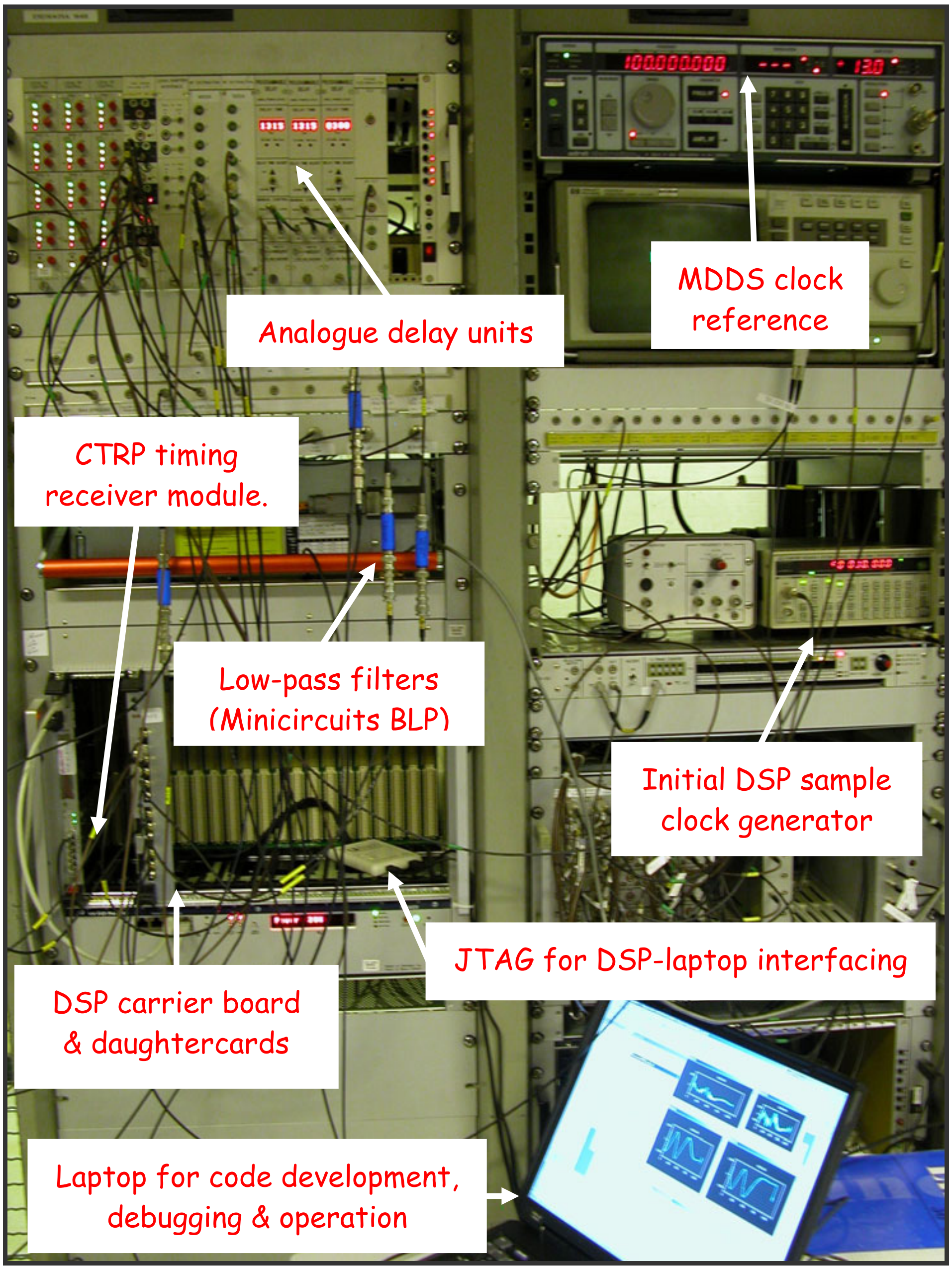

Analogue delay units
MDDS clock reference
CTRP timing receiver module.
Low-pass filters (Minicircuits BLP)
Initial DSP sample clock generator
JTAG for DSP-laptop interfacing
DSP carrier board & daughtercards
Laptop for code development, debugging & operation

Figure 4: *Equipment setup in the PSB BOR.*

3. HARDWARE AND FPGA SOFTWARE DESCRIPTION

Figure 5 shows a picture of the DSP carrier board with the daughtercards installed, emphasising the Altera FPGAs that implement the signal processing.
The DSP carrier board, 1-site MDDS and 1-channel SDDS are the same used for the summer 2003 tests [2]. The only novelties for fall 2004 tests are the 4-channel DDC daughtercard and FPGA code. Both are described in paragraph 3.1. The FPGA code on the DSP carrier board FPGAs has also been upgraded, as detailed in paragraph 3.2.

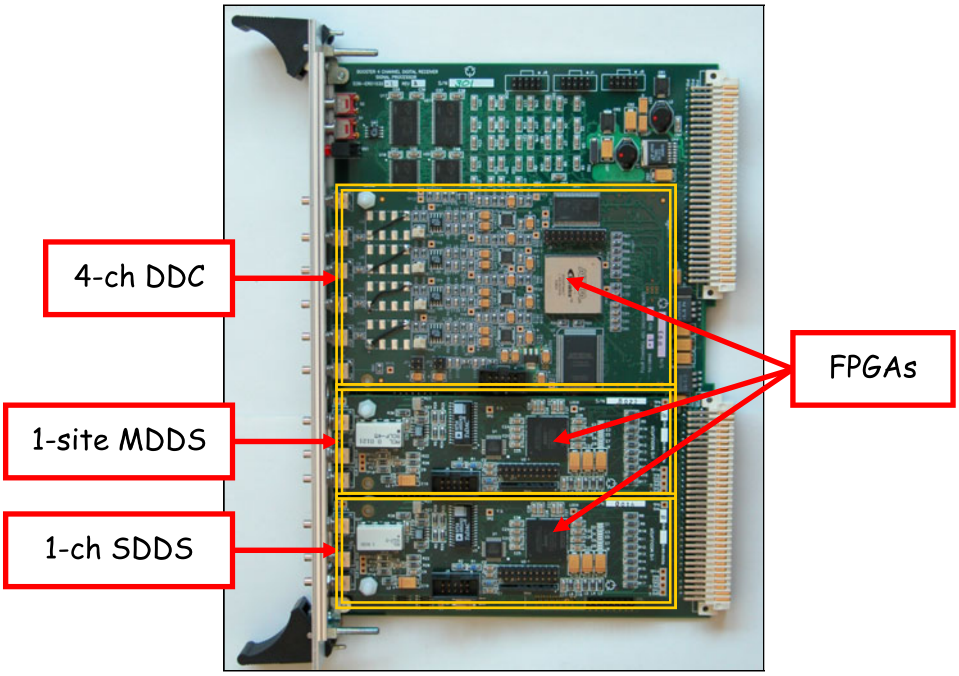


Figure 5: *DSP carrier board with the three daughtercards installed.*

3.1 DDC board and CIC filter

Figure 6 gives a schematic view of the four-channel DDC daughtercard. The on-board ADCs are Analog Devices' AD9245, 14 bit resolution devices capable of sampling at a rate of up to 80 MHz and clocked by the MDDS clock. The synchronous load line is not used and, in the tests described here, the on-board anti-alias filter has been removed and replaced by an external filter. The SRAM block memory includes 256 k memory locations of 16 bits each and in the LEIR version it will store DDC diagnostic information. However, it was not used for the fall 2004 tests. The EPC4 block is Altera's enhanced FPGA configuration device and is used for storing configuration data for the DDC FPGA.

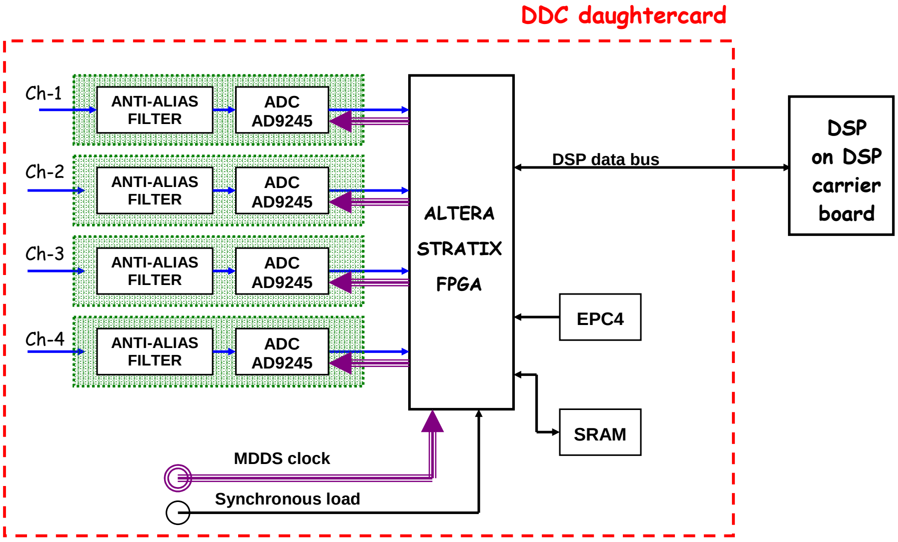


Figure 6: *Schematic view of the four-channel DDC daughtercard.*

The FPGA code implements a programmable DDC, which includes a decimating Cascaded-Integrator-Comb (CIC) filter. An advantage of implementing the DDC in FPGA over using a commercial chip is that the DDC can be designed so as to keep the group delay very short, an important characteristic for implementing a feedback loop. The FPGA code has been conceived and implemented at CERN, and a prototype version was used in the fall 2004 PSB tests. The major difference between prototype and final version is that in the former the DDC setup is hard coded in the FPGA while in the final version it is controlled by the DSP. In addition, the synchronisation between different channels on the same daughtercard is obtained by driving them by the same Numerical Control Oscillator (NCO). Figure 7 shows the structure of one of the four channels, the others reproducing the same structure. Three blocks compose the DDC, namely the NCO, the Complex Mixer and the Low-Pass Filter. The NCO uses the MDDS clock, the local oscillator harmonic H_{LO} and a Look-Up Table (LUT) to generate a quadrature sine wave, with programmable frequency and phase. The Complex Mixer block consists of two digital multipliers and the Low-Pass Filter block is made of two configurable CIC filters, whose main role is to remove the unwanted high frequency components from the mixing stage. The output of a DDC channel consists of two 32-bit values, which are the In Phase (I) and Quadrature (Q) part of the filtered signal.

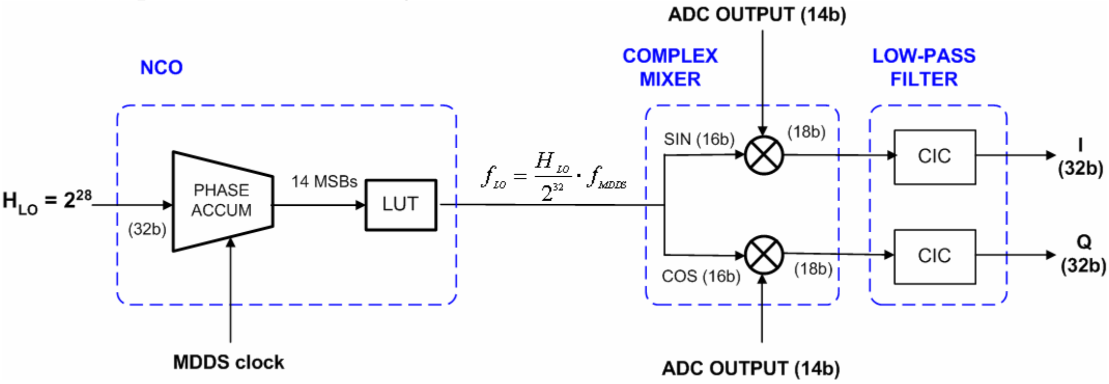


Figure 7: *Schematics of the FPGA code for one DDC channel, emphasising three main blocks: NCO, Complex Mixer and Low-Pass Filter. The structure is the same for each channel.*

The CIC filter is a low-pass filter whose frequency response is fully determined by three parameters, namely:

a) N = number of cascaded integrator and decimator stages;
b) R = decimation ratio;
c) M = number of delays in the cascaded differentiator stages.

The Decimating CIC structure, shown in Figure 8, consists of three main sections: a cascade of N digital integrators, a decimating section and a cascade of N digital differentiators (also called combs). The time elapsed between two consecutive samples at the CIC output $T_{DDC\text{-}OUT}$ corresponds to the sampling period T_S multiplied by the decimation factor R. By imposing limited data storage and no multipliers, the CIC filter implementation uses fewer resources than the Finite Impulse Response (FIR) and the Infinite Impulse Response (IIR) filters.

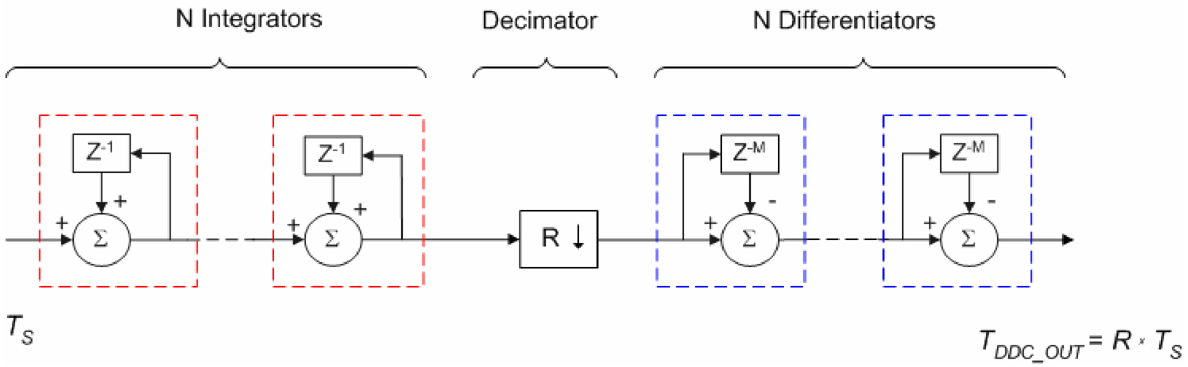


Figure 8: *CIC filter: schematic view.*

The averaging time t_{AVGN} for one CIC filter stage (N=1) and the total group delay $t_{DDC\text{-}GRP\text{-}DELAY}$ due to the CIC filter are given by:

$$t_{AVGN} = T_S \cdot R \cdot M \tag{2}$$

$$t_{DDC-GRP-DELAY} = \frac{N}{2} \cdot t_{AVGN} \tag{3}$$

Table 2 summarises the CIC filter parameters used for the fall 2004 PSB tests. Two different setups were used, for the phase and for the radial loop respectively. In both cases, however, the CIC filter is implemented as a single stage (N = 1).

Signal	***N***	***R***	***M***
Channel 1 (cavity return signal, used in the phase loop)	1	1	32
Channel 2 (phase PU signal, used in the phase loop)	1	1	32
Channel 3 (Σ radial PU signal, used in the radial loop)	1	64	32
Channel 1 (Δ radial PU signal, used in the radial loop)	1	64	32

Table 2: *Summary of the CIC filter parameters used for the fall 2004 PSB tests.*

In the phase loop, R is set to 1 to obtain the lower possible $T_{DDC\text{-}OUT}$. The number M of delays in the differentiator stage is set to 32 so as to integrate over two revolution turns and to improve the signal-to-noise ratio. In the radial loop, the values of R and M used correspond to 128 revolution turns of integration time. The main objective is to improve the signal-to-noise ratio, a very important task especially for the small Radial PU Δ signal. The price to pay is a higher group delay, which is anyhow compatible with the radial loop bandwidth.

Table 3 summarises the group delays and CIC filter output sample rates obtained with the filter setup used in the fall 2004 tests for the phase and radial loop, respectively. Values are given for the injection and extraction revolution period $T_{REV} = 1/f_{REV}$.

	T_{REV} [μs]	T_S [μs]	**Phase loop**			**Radial loop**		
			t_{AVGN} [μs]	$t_{DDC\text{-}GRP\text{-}DELAY}$ [μs]	$T_{DDC\text{-}OUT}$ [μs]	t_{AVGN} [μs]	$t_{DDC\text{-}GRP\text{-}DELAY}$ [μs]	$T_{DDC\text{-}OUT}$ [μs]
Inj.	1.68	0.11	3.35	1.67	0.10	214.4	107.2	6.7
Ext.	0.57	0.03	1.14	0.57	0.04	73.2	36.6	2.3

Table 3: *Summary of the group delay $t_{DDC\text{-}DELAY}$ and CIC output data rate $t_{DDC\text{-}OUT}$ for the phase and radial loops.*

DDC-to-DSP communication was achieved by means of a no-handshake asynchronous protocol via the DSP data bus shown in Figure 6. The DSP always read I before Q to guarantee data coherence. I and Q were stored in the DDC memory at the time when I was read and not updated until the entire I and Q reading sequence had ended.

3.2 DSP-carrier board FPGA software

The FPGA software was upgraded to implement a counter and generate an interrupt on the DSP. These functionalities are essential for the deployed DSP software. The DSP carrier board receives a constant-frequency signal through the rear transition module. This signal is called DSP sample clock, it is generated by either a signal generator or a CTRP timing receiver and its frequency is 90 kHz in the tests described here. Figure 9 gives a schematic view of the DSP sample clock counter and the DSP interrupt scheme.

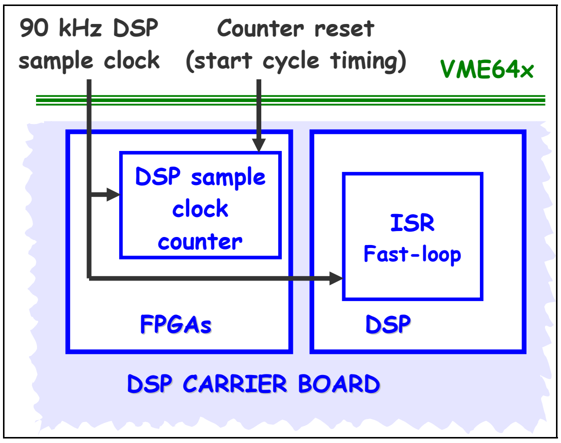


Figure 9: *Schematic view of the DSP sample clock counter and the DSP interrupt generation scheme. Two FPGAs on the DSP carrier board are used.*

One of the FPGAs on the DSP carrier board generates a DSP interrupt coincident with the rising edge of the DSP sample clock. This interrupt is serviced by the fast-loop routine described in paragraph 4.1. A different FPGA counts the number of rising edges and is reset by the start-cycle timing. Knowing the DSP clock period allows the DSP sample clock counter output to be converted to a precise time in the beam cycle.

4. DSP SOFTWARE DESCRIPTION

The DSP implements frequency program, radial steering, phase and radial loops capabilities. The DSP software has been greatly changed and improved with respect to the summer 2003 test version [2]. Moreover, it uses a novel approach to the generation of vector-based reference-functions and timings, indicated here as soft-GFAS and soft-timings, respectively. These are functions traditionally generated by VME hardware. Another novelty is DSP-Oasis, a user-selectable digital data acquisition function providing diagnostic and troubleshoot access points to check real-time data and to save them for later analysis. This is based on the new Oasis system developed for LHC [5]. The general DSP software organisation is outlined in paragraph 4.1. Paragraphs 4.2 through 4.7 describe the major software components used during the tests and give some test results. The code structure is now the same as that planned for LEIR. The PSB tests code mainly differs from the LEIR version in that only one DSP board was used instead of three. As a consequence, one DSP has to carry out functions that will be performed by three DSPs in the LEIR version. Therefore the PSB beam control actions were carried out with a period longer than that planned for LEIR. A second consequence is that the DSP-to-DSP communication could not be tested. The system will be integrated in the AB/CO infrastructure as soon as the Fesa2 architecture [6] becomes available. The Real Time Task (RTT) will be implemented under this architecture. The RTT will run on a PowerPC and will interface the user (application level) with the DSP (hardware level). In the fall 2004 PSB tests a part of the DSP code simulated the RTT execution, by initialising the external memory with user-defined control values. A drawback of this operation mode was that the DSP code had to be recompiled every time a parameter was changed. The VisualDSP++ development environment enables one to load the DSP code to the DSP itself and to start it. It also displays a graph of the memory region contents and saves them to a file.

4.1 General organisation

After considering several DSP Real Time Operating Systems (RTOS) and after evaluating the RTOS provided with VisualDSP++, it was decided to develop the DSP code as a simple executable, without RTOS support. The DSP code is divided into three tasks, namely slow-loop, fast-loop and external timing, carried out as different priority Interrupt Service Routines (ISR). They are described below, in order of increasing ISR priority.

1. **The slow-loop task** is a low-priority ISR triggered periodically by the internal DSP timer. During the fall 2004 tests the slow loop period T_{SLOW_LOOP} was 1 ms. This ISR executes background actions, such as updating GFAS data stored in the fine resolution table (described in paragraph 4.6), DSP initialising at the beginning of each cycle and communicating with the RTT level. As shown in Figure 10, the slow-loop is executed during the CPU time available between successive fast-loop executions. It is essential for the system to function properly that the slow-loop execution is completed before the ISR is newly triggered.

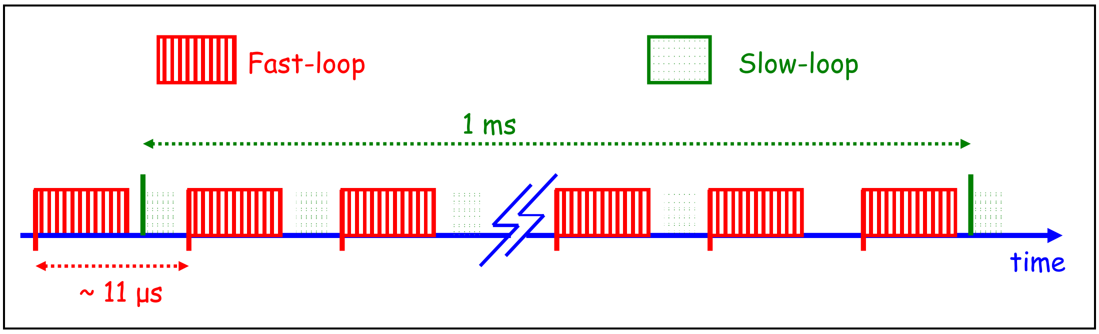


Figure 10: *Fast-loop and slow-loop interactions: schematic view. The fast-loop has priority over the slow-loop and interrupts it. The slow-loop is executed on the CPU time available between successive fast-loop executions.*

2. **The fast-loop task** is an ISR triggered periodically by the DSP sample clock. This ISR, described in Figure 11, works on the alternate register set, hence the time spent on context switch is the shortest possible, i.e. 0.55 µs in total. It carries out core functionalities, such as executing phase and radial loops, radial steering and soft-timing. Every time it runs, it writes to the MDDS the calculated f_{REV} value. Once every eight times it also updates the measured value of the beam radial position used in the radial loop. Finally, it saves digital data in external memory for further analysis, as detailed in paragraph 4.3. The fast-loop period T_{FAST_LOOP} must be as small as possible to minimise the group delay. For the tests described here T_{FAST_LOOP} corresponds to about 11 µs and allows satisfactory beam control. In LEIR, T_{FAST_LOOP} is planned to be as short as 5 µs. This will be achieved by splitting the beam control activities among three DSP carrier boards.
3. **The external timing task** is a high priority ISR triggered by the rear transition module timing input corresponding to the start cycle. This ISR reads on an on-board FPGA which events triggered it and executes the corresponding action.

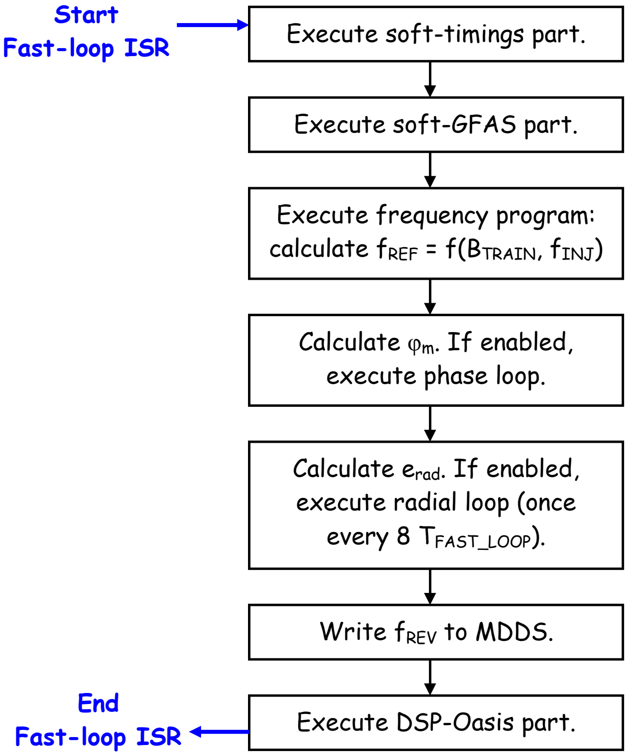

Start
Fast-loop ISR
Execute soft-timings part.
Execute soft-GFAS part.
Execute frequency program: calculate f_{REF} = $f(B_{TRAIN}, f_{INJ})$
Calculate φ_m. If enabled, execute phase loop.
Calculate e_{rad}. If enabled, execute radial loop (once every 8 T_{FAST_LOOP}).
Write f_{REV} to MDDS.
Execute DSP-Oasis part.
End
Fast-loop ISR

Figure 11: *Functionality implemented in the fast-loop ISR.*

4.2 Soft-timings

In a beam control system several actions, for example the phase and radial loops, need to be started at a precise time within a given machine cycle. In our digital implementation most of the timings are software events that modify the DSP behaviour. This has prompted the design and implementation of the DSP code for generating these events. We called them soft-timings to distinguish them from the pulses-on-a-cable timings, referred to as hard-timings. Figure 12 shows the soft-timing implementation scheme.

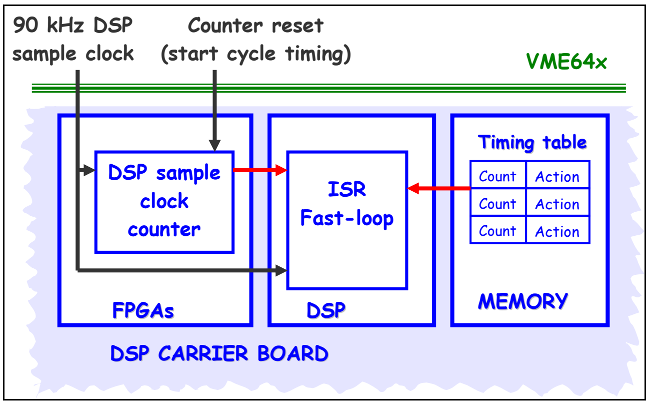
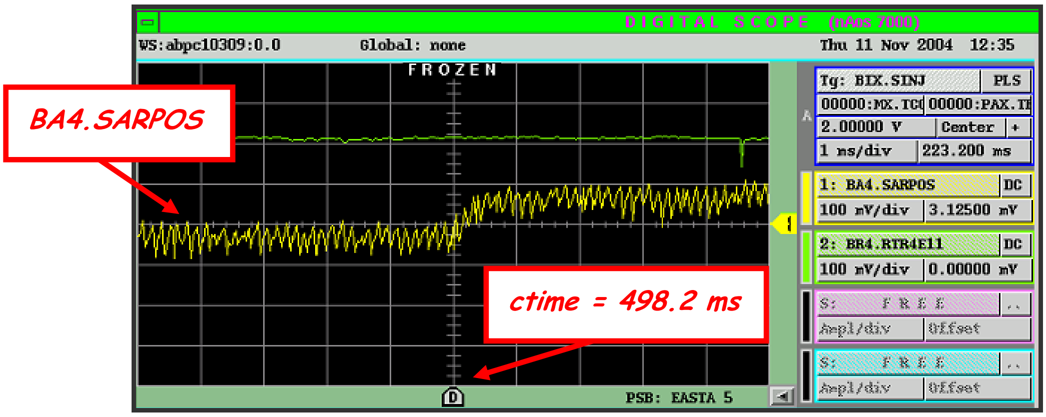


Figure 12: *Soft-timing unit schematics. The fast-loop task reads DSP sample clock counter and Timing Table, checks if an action needs to be executed and, if so, executes it.*

The DSP external memory stores a table giving the user-selectable DSP sample clock count at which a soft-timing must be triggered and the corresponding timing name. The table is ordered in increasing DSP sample clock count order (i.e. increasing time from the beginning of the cycle), so as to minimise the DSP processing load. This table is moved from external to internal

DSP memory during the initialisation phase proceeding each new cycle and the timing name is converted to point to the action to be executed. Each time the fast-loop task is triggered, it reads the current DSP sample clock counter and checks if this count corresponds to one or more counts in the timing table. If so, the fast-loop task executes the associated actions. Nineteen soft-timings are used in the beam control prototype described here. Examples of some actions triggered by the soft timings are phase loop closure, radial loop closure and start of digital data acquisition for channels 1 to 4. All soft-timings are counted from a ctime of zero ms with a time resolution of T_{FAST_LOOP}. This is acceptable as the time resolution needed is no better than 20 µs. The soft-timings mechanism is validated at DSP level by triggering an action with a soft-timing and observing the beam behaviour through an independent system, such as the Analog Signal Observation System NAOS [7]. For instance, Figure 13 shows the radial loop closed at a ctime of 498.23 ms while the beam radial position was observed by NAOS.



DIGITAL SCOPE (nAos 7000)

WS:abpc10309:0.0 Global: none Thu 11 Nov 2004 12:35

FROZEN

Tg: BIX.SINJ PLS
00000:MX.TC(00000:PAX.TI
2.00000 V Center +
1 ms/div 223.200 ms

1: BA4.SARPOS DC
100 mV/div 3.12500 mV

2: BR4.RTR4E11 DC
100 mV/div 0.00000 mV

S: FREE ..
Ampl/div Offset

S: FREE ..
Ampl/div Offset

PSB: EASTA 5

BA4.SARPOS

ctime = 498.2 ms

Figure 13: *Radial position (BA4.SARPOS) observed by the NAOS system.*

The acquisition trigger BIX.SINJ goes off at a ctime of 275 ms and the observation window centre is offset by 223.2 ms from the trigger time. The BA4.SARPOS yellow signal shows the beam changing its radial position at the window centre, located at a ctime of 498.2 ms. This value agrees with the soft-timings setup and with the radial position measured and acquired by the DSP from PU 12 and shown in Figure 14 (blue trace with diamonds). It should be noted that the radial position measured by the sampler application [8], shown in Figure 14 (red trace, squares), appears to change before the radial loop is actually closed. This is an artefact caused by the sampler application being advanced, as discussed in more details in paragraph 4.5.

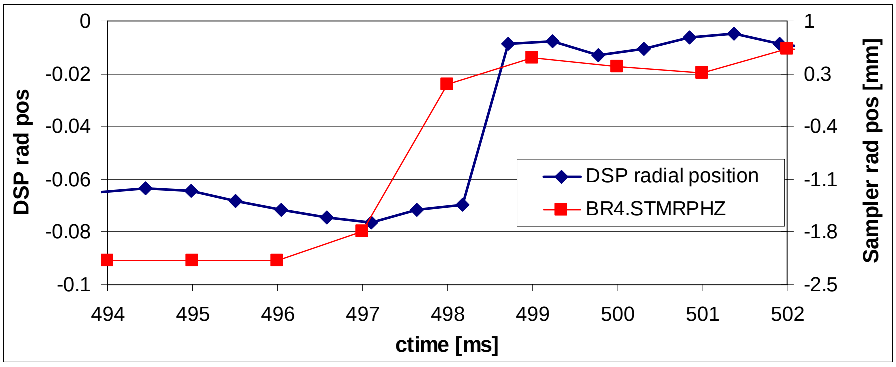


Figure 14: *Beam radial position measured and saved by the DSP every 530 µs (blue trace with diamonds). The sampler-measured radial position (red trace with squares) is displaced in time with respect to the DSP one (see also par. 4.3).*

4.3 Digital Data Acquisition: DSP-Oasis

In the operation of a digital system it is extremely important for the user to be able to see what is happening inside the system. Failing that, the system becomes a black box and its operation and control become extremely difficult. To avoid this risk, the DSP code has been equipped with the DSP-Oasis unit. This is a digital data acquisition subsystem allowing the user to store in memory up to four digital signals, chosen amongst more than 30 signals acquired or calculated by the DSP itself. Such signals are for instance GFAS functions, radial position, raw data from DDCs, phase error and so on. Users may store up to 1024 samples per signal. The sampling period must be chosen to be a multiple of T_{FAST_LOOP}. During the fall 2004 tests, neither application nor middleware layers were available, hence the DSP-Oasis data were shown using the VisualDSP++ facilities. In addition, data could be saved to a file and then analysed and displayed by Excel. In the following we present two examples of findings made possible by the DSP-Oasis implementation. First, a comparison of the B-train data acquired by the DSP to those acquired by the sampler system [8] showed that the sampler data were advanced by 1 ms. A plot showing the two data acquisitions for the same cycle is shown in Figure 15.

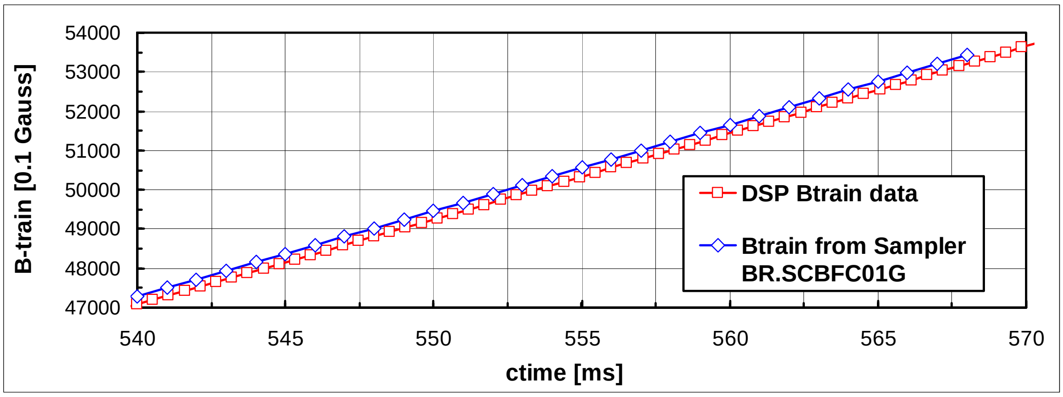


Figure 15: *B-train as acquired by DSP-Oasis (red trace and squares) and by the sampler (blue trace and diamonds). Sampler data are advanced by 1 ms with respect to DSP data. The DSP-Oasis sampling period is 530 µs.*

This was confirmed to be a sampler system problem. Once that was corrected, the two data acquisitions agreed, as shown in Figure 16. This finding was particularly useful for the standard beam control system, which relies on the B-train value coming from the sampler to determine the injection frequency. Finding and solving the problem allowed beam capture to be optimised.

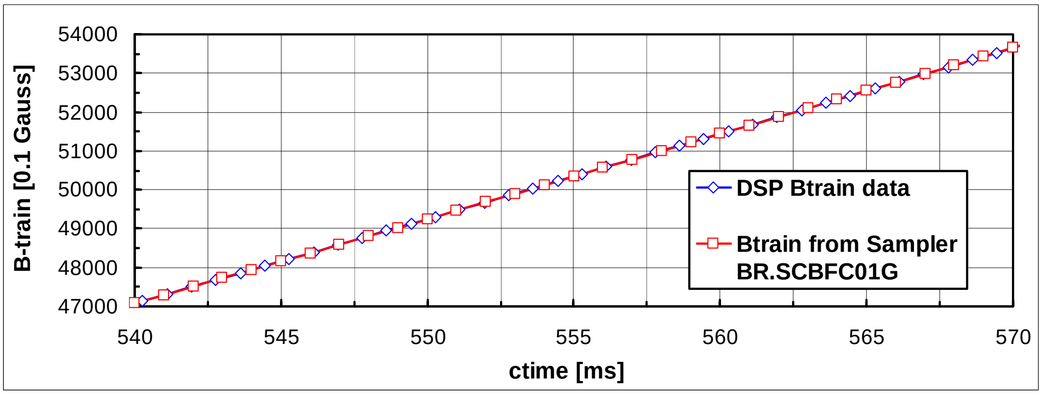


Figure 16: *The B-train acquired by the sampler agrees with the DSP-acquired one after the sampler correction. The DSP-Oasis sampling period is 830 µs.*

Another discrepancy concerns the radial position and has not been clarified yet. Figure 17 shows the time evolution of the mean radial position measured by the sampler and by the DSP. The sampler data are averages from all PUs data over a 1-ms period, while DSP data come from PU 12 only and are refreshed every 33 µs in this case. The radial loop is closed at a ctime of 498.23 ms, causing a steep radial displacement of the beam. However, data taken by the sampler show the beam moving before the radial loop is actually closed by the DSP. This appears to be again a sampler application problem, since the soft-timing scheme was validated versus NAOS, as described in paragraph 4.2. Finally, DSP-Oasis data reveal features that cannot be seen by the sampler, in this case the beam oscillations.

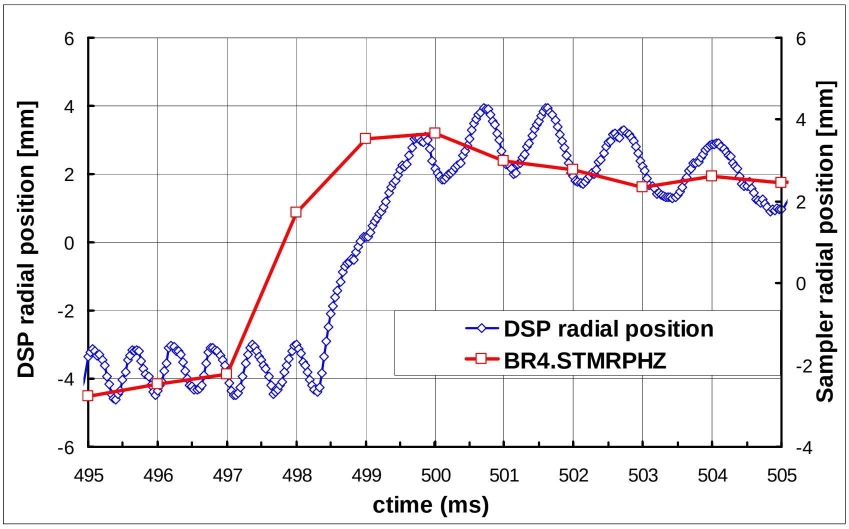


Figure 17: *The radial position as measured by the sampler (BR4.STMRPHZ trace) appears to be advanced in time with respect to the DSP-measured radial position. The DSP-Oasis sampling period is 33 µs.*

4.4 Digital reference function generation: soft-GFAS

In PS Complex (CPS) jargon, GFAS stands for *Générateur de Fonction Analogique Simplifié* [9], i.e. simplified analogue function generator. This is a software-plus-hardware, vector-based mechanism enabling the user to define a function in a dedicated application program and to have it generated by hardware as voltage. For our digital beam control system the reference functions are formed by means of digital values, rather than voltages, used by the DSP during its data processing. Therefore we devised a soft-GFAS unit, i.e. a part of the DSP software dedicated to producing such digital GFAS. The soft-GFAS interfaces with the RTT following the standard GFAS specifications [9]. Moreover, the soft-GFAS implements features such as internal stop and restart. The reference function to be generated is implemented as a GFAS software function table, i.e. as a table of vectors and corresponding time durations, as shown in Figure 18. This table is used by the slow loop to interpolate the values that will be passed to the fast-loop, in order to obtain more finely-spaced values which correspond to the fast-loop actual time in the cycle. In this way, the fast-loop is made to run as fast as possible. For each GFAS, the slow-loop generates the corresponding fine-resolution circular buffer, which it fills up every time the slow-loop is triggered. The fast-loop empties the fine-resolution buffer by reading its data.

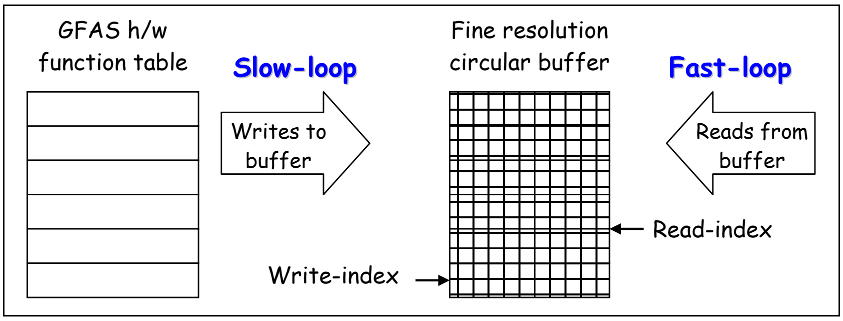


Figure 18: *DSP-based reference function generation. The slow-loop fills the fine resolution circular buffer and the fast-loop empties it, by reading the data.*

Currently a maximum of six GFAS can be generated in the same DSP, owing to the limited DSP hardware resources and in order to minimize the fast-loop period. The fast-loop updates the currently used GFAS value once every six cycles by fetching new data from the fine resolution circular buffer. As a consequence, in the fine-resolution circular buffer the time interval between two values is 6 times T_{FAST_LOOP}, i.e. about 66 µs for the tests described here. This scheme is applied even if fewer than six GFAS are used, hence the time difference between two points in the fine-resolution circular buffer remains 66 µs. During the tests described here only one GFAS was used to generate the radial steering. Figure 19 shows the beam radial position measured by the DSP when a trapezoidal radial steering function is applied.

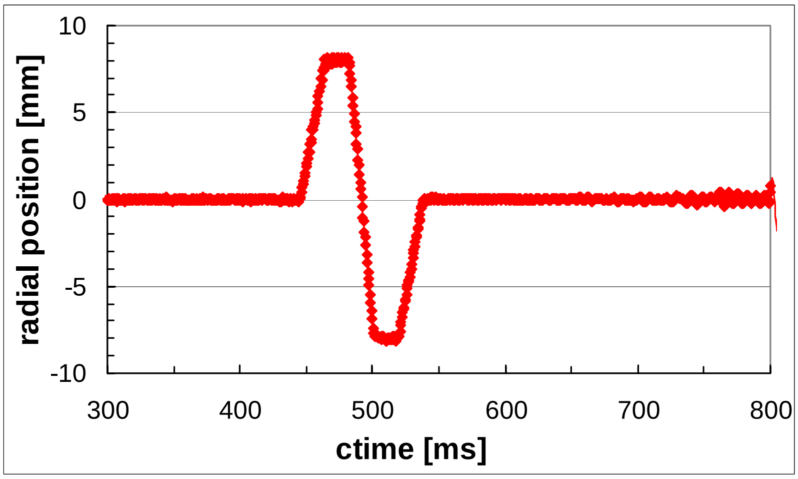


Figure 19: *Radial position as measured by the DSP when a trapezoidal radial steering function is used. The DSP-Oasis sampling period is 530 µs.*

4.5 Frequency program

The frequency program calculates the $f_{B\text{-}train}$ component of the RF frequency f_{RF} as a function of the magnetic field B in the machine:

$$f_{B-train} = frevInf_{MDDS} \cdot \sqrt{1 - \frac{1}{1 + \left(B \cdot \frac{q}{m_0 \cdot c} \cdot \rho \right)^2}}, \tag{4}$$

where c is the speed of light in vacuum, R = 25 m is the PSB machine radius, q is the proton charge, m_0 is the proton rest mass, ρ is the magnetic bending radius,

$$frevInf_{MDDS} = \frac{2^{32}}{f_{REF-CLOCK}} \cdot \frac{c}{2 \cdot \pi \cdot R}. \tag{5}$$

Here the reference clock $f_{REF\text{-}CLOCK}$ is equal to 100 MHz.

The magnetic field *B* is derived from the number of B-train ticks counted by an FPGA from *Bup* and *Bdown* signals. Each tick corresponds to 10^{-5} T and the FPGA counter is reset at the beginning of each cycle. At beam injection f_{RF} is obtained from a fixed injection frequency f_{INJ} value specified as a user-selectable parameter and not derived from the magnetic field *B*. This is so as to optimise the capture process. Beam injection in the PSB happens at a ctime of 275 ms and, typically one millisecond later, the '*End* f_{INJ}' soft-timing triggers the slow transition from f_{INJ} to $f_{B\text{-}train}$. This transition lasts for 500 fast-loop periods i.e. 5.5 ms for the tests described here. The actual frequency used during this time is given by:

$$f_{ACTUAL,k} = f_{INJ} + \frac{k}{500}\cdot\left(f_{B-train} - f_{INJ}\right) \quad , \quad k = 1 \;..\, 500 \tag{6}$$

where $k = \Delta t/T_{FAST\text{-}LOOP}$ and Δt is the interval elapsed since triggering '*End* f_{INJ}' soft-timing. Figure 20 illustrates the frequency program algorithm implemented by the DSP, where f_{REF} is the frequency program output.

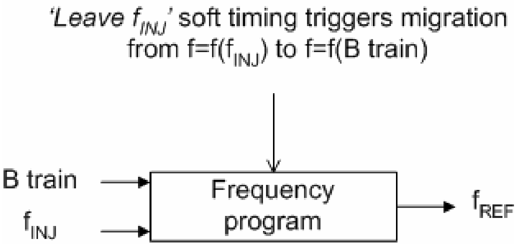

'Leave f_{INJ}' soft timing triggers migration from f=f(f_{INJ}) to f=f(B train)
B train
f_{INJ}
Frequency program
f_{REF}

Figure 20: *Frequency program algorithm implemented by the DSP code.*

Finally, Figure 21 shows data acquired with DSP-Oasis. The actual frequency is represented in pink and $f_{B\text{-}train}$ is in blue. The beam is injected at a ctime of 275 ms and f_{REF} is kept constant at f_{INJ}. Following the '*End* f_{INJ}' soft timing, f_{REF} is changed to reach $f_{B\text{-}train}$ after 5.5 ms.

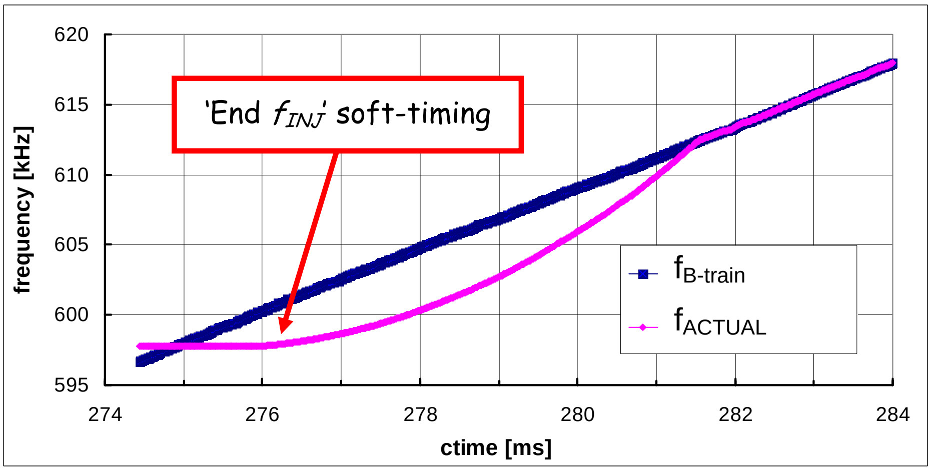


Figure 21: *B-train derived (blue trace) and actual (pink trace) frequencies.*

4.6 Phase loop

The phase loop is one of the two feedback loops implemented in the DSP code. It aims at reducing longitudinal emittance growth and coherent synchrotron oscillations caused by noise in the frequency program or in the magnet power supplies. It is also used to damp beam loading instabilities. The phase loop sampling period is T_{FAST_LOOP}, i.e. about 11 µs. The group delay $t_{GROUP\text{-}DELAY}$ is given by

$$t_{GROUP-DELAY} = t_{DDC-GRP-DELAY} + \frac{1}{2} \cdot T_{DDC-OUT} + \frac{1}{2} \cdot T_{FAST\_LOOP} + t_{CABLES} \tag{7}$$

where t_{CABLES} ~ 2 μs is the cable-generated delay. The values used in equation (7) are those shown in Table 3 and result in a group delay of 9.23 μs at injection and 8.1 μs at extraction.

Figure 22 gives an overview of the phase loop algorithm implemented for the PSB tests: the part contained inside the blue dashed box is implemented in the DSP. The phase loop is enabled by the '*Start Phase Loop*' soft timing after injection, typically at a ctime of 275.3 ms for the tests described here. Before then, the feedback loop is fed with zeroes, hence the phase loop contribution to the calculated f_{REF} is null. Once the phase loop is started, the feedback variable becomes the measured phase error ϕ_m, which is the difference between the measured and the desired phase. The feedback loop works to maintain the difference ($\phi_B - \phi_C$) small, where ϕ_B and ϕ_C are the phases of the beam and of the cavity signals, respectively. Therefore, in the approximation of small ϕ_m one has

$$\phi_m \approx \sin(\phi_m) = \sin(\phi_B - \phi_C) = \frac{C_I \cdot B_Q - B_I \cdot C_Q}{\sqrt{\left(B_I^{\,2} + B_Q^{\,2}\right) \cdot \left(C_I^{\,2} + C_Q^{\,2}\right)}} \tag{8}$$

where I and Q refer to the In-Phase and Quadrature components for cavity return (C) and beam (B) vectors. Prior to applying (8), the beam signal is delayed analogically by 310 ns to equalise the group delays in the phase pick-up and cavity return paths. Similarly, the cavity signal is rotated by 109.5 degrees, to compensate for the different position of the longitudinal PU and of the cavity in the ring. These corrections are described in paragraph 5.2.

Once the phase loop is started, the measured phase error ϕ_m is filtered by a first-order, high-pass IIR filter with a 10 Hz cutoff frequency. This makes the phase loop AC-coupled thus reducing static frequency errors. A programmable gain K_e enables one to change the phase loop gain. The phase loop contribution Δf_{ph_loop} and the radial loop contribution Δf_{rad_loop} are subtracted from the value f_{REF} produced as output of the frequency program, as described in paragraph 4.5. The multiplier $f_{REF-CLOCK}/2^{32}$ in Figure 22 is due to the filtered phase error Δf_{ph_loop} being directly used as the phase loop contribution to the MDDS frequency word *FW*. For h_{MDDS} the value 16 is chosen, so that the MDDS generates the higher possible frequency during the whole beam cycle. The SDDS and DDC daughtercards will then convert the signal back to baseband.

The MDDS uses the reference clock $f_{REF-CLOCK}$, equal to 100 MHz, and *FW* to generate an analogue signal with frequency f_{MDDS}:

$$f_{MDDS} = \frac{f_{REF-CLOCK} \cdot FW}{2^{32}} \tag{9}$$

The phase loop bandwidth BW_{PH_LOOP} is

$$BW_{PH\_LOOP}\,[Hz] = K_e \frac{f_{REF-CLOCK}}{2^{32}} \quad . \tag{10}$$

The gain K_e used in the fall 2004 PSB tests is 300000, giving a nominal BW_{PH_LOOP} of about 7 kHz. Assuming a zero-delay implementation, this is equal to the phase loop high frequency pole, f_H. The phase loop low frequency pole f_L is:

$$f_L = \frac{f_S^{\,2}}{f_H} \tag{11}$$

where f_S is the synchrotron frequency. Figure 23 shows f_S and momentum p variations during a typical PSB cycle. In particular, f_S is 2 kHz at injection and 470 Hz at extraction.

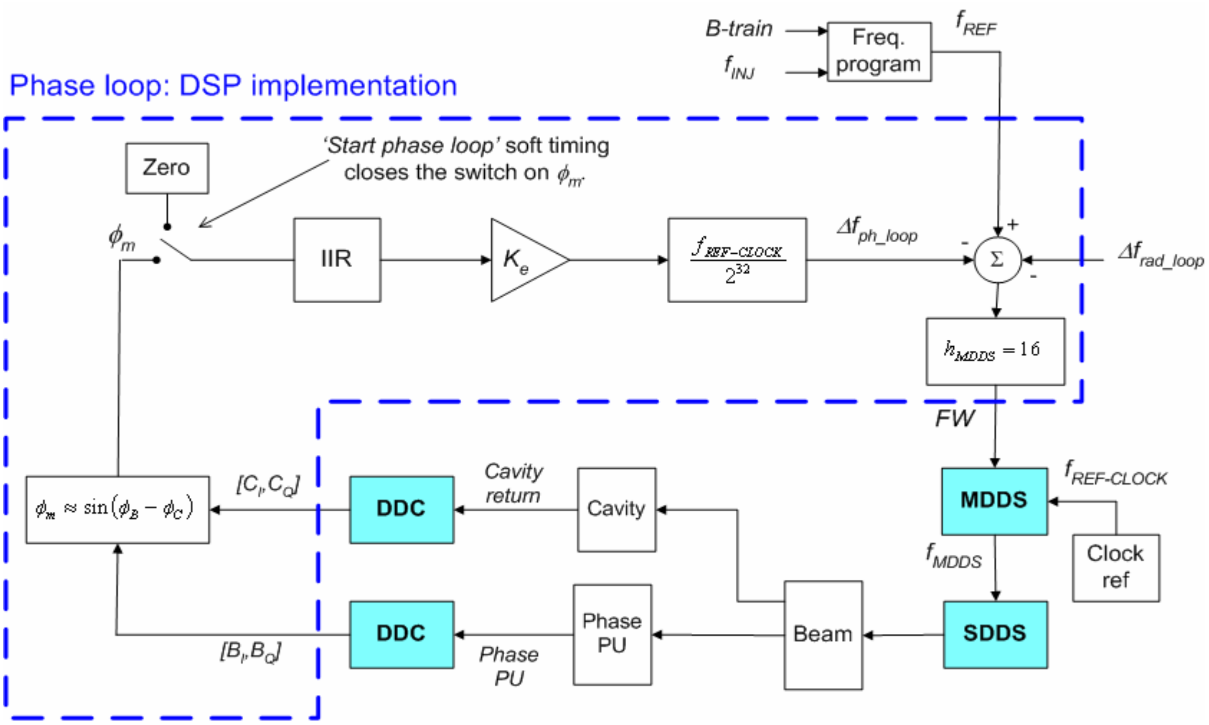


Figure 22: *Schematics of the phase loop implementation for the PSB tests. The dataflow part in the blue dashed box is implemented in the DSP. The blue boxes show data processing implemented in the daughtercards FPGAs.*

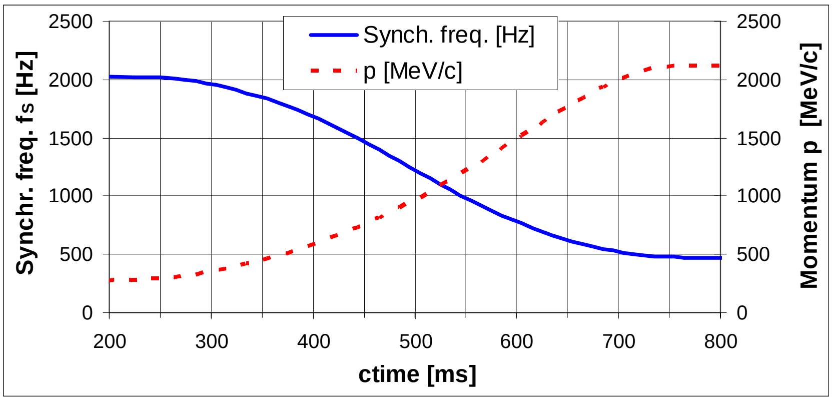


Figure 23: *Synchrotron frequency f_S and momentum p variations during a PSB cycle.*

4.7 Radial loop

The radial loop is the second feedback loop implemented in the DSP code and corrects errors in the frequency programme and allows adiabatic control of the beam radial position. Additionally, it is used for steering the beam by applying an offset to the measured beam radial position. The radial loop sampling period is 7 times T_{FAST_LOOP}, i.e. about 80 μs. The radial loop group delay depends on its sampling period, on the DDC settings and on the cables delay, as shown in equation (7). The DDC settings used for the phase loop are summarised in Table 3, t_{CABLES} is approximately 2 μs and the corresponding group delay is 118 μs at injection and 45.3 μs at extraction. Figure 24 shows the radial loop algorithm deployed for the PSB tests: the part contained inside the blue dashed box is implemented in the DSP. The radial loop is started by the '*Start radial loop*' soft timing. Prior to that, the feedback loop is fed with zeroes and the radial loop contribution Δf_{rad_loop} to f_{REF} is null. The feedback variable is the error in the radial position e_r , i.e. the difference between the measured radial position r and the desired one r_{des}, both expressed in millimetres. The former is obtained from the Δ and Σ signals by applying the normalisation algorithm:

$$r\,[mm] = M \cdot \mathrm{Re}\left(\frac{\vec{\Delta}}{\vec{\Sigma}}\right) = M \cdot \mathrm{Re}\left(\frac{\Delta_I + j \cdot \Delta_Q}{\Sigma_I + j \cdot \Sigma_Q}\right) \tag{12}$$

Both Δ and Σ signals are decomposed by the DDC in their I and Q components. The PU-dependent conversion factor M = 50 turns raw data r_{raw} into the actual r expressed in mm. A radial loop veto is implemented, which closes the switch to zero if $\sqrt{\Sigma_I{}^2 + \Sigma_Q{}^2}$ is below a given threshold. The error e_r is filtered by a Proportional-Integral (PI) regulator. An additional gain K_r of 350 is included. Similarly to the phase loop case described in paragraph 4.6, the factors $f_{\text{REF-CLOCK}}/2^{32}$ and h_{MDDS} are present.

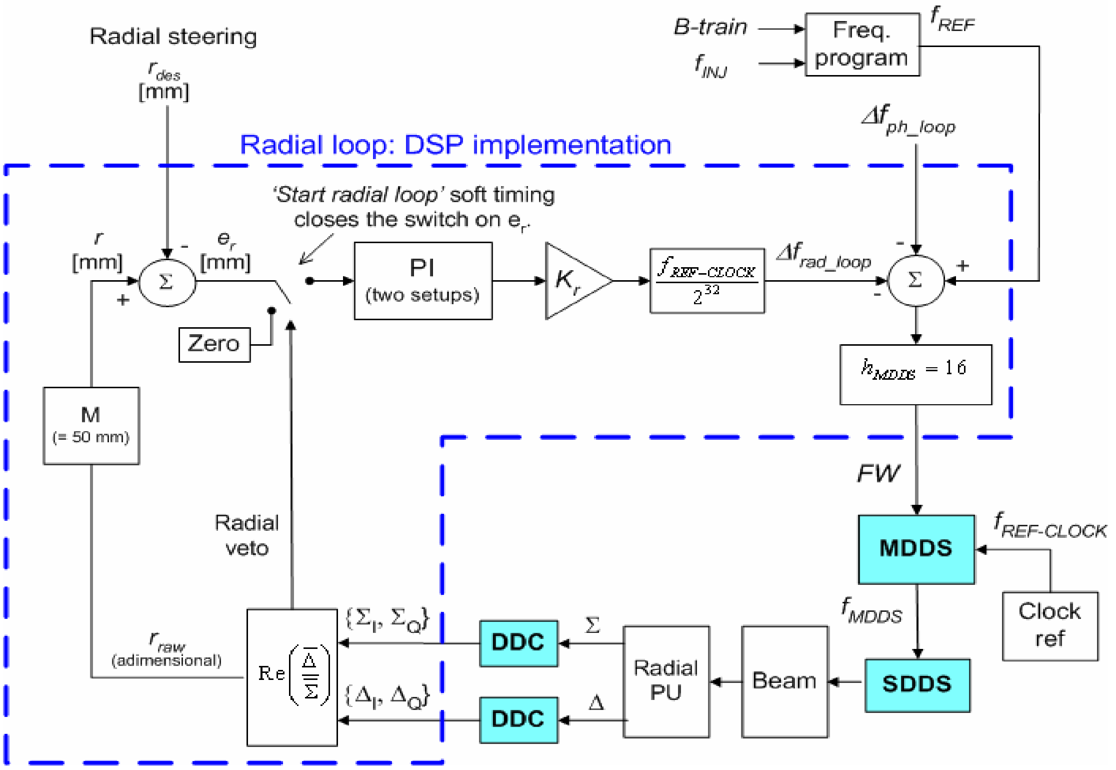


Figure 24: *Schematics of the radial loop implementation in the DSP code. The dataflow part in the blue dashed box is implemented in the DSP. The blue boxes show data processing implemented in the daughtercards FPGAs.*

The transfer function of a time-continuous PI regulator is

$$\frac{U(s)}{E(s)} = \frac{K_p}{s} \cdot \left(s + \frac{K_i}{K_p}\right), \tag{13}$$

where K_p and K_i are the proportional and integral gain, respectively. In the fall 2004 tests, two different PI settings were used in the same cycle, optimised for its early and late part, respectively. That was achieved by setting the zero in the PI regulator so as to cancel the phase loop low frequency pole f_L, i.e. $K_i/K_p = 2\,\pi\,f_L$. The PI parameters were chosen so that the radial loop rise time T_r equals 2 ms.

The first PI regulator setup is designed to optimise the radial loop at low energy, in particular for f_S = 1392 Hz and p = 810 MeV/c. These values are reached at a ctime of 467 ms. From (11) and recalling that f_H = 7 kHz, one finds f_L =276 Hz, hence the PI zero must be set to this f_L value. The resulting PI setup for the low energy case is given by

$$\begin{cases} \dfrac{K_i}{K_p} = 1733\,[rad/s] \\ K_p = 17.7 \end{cases} \qquad (14)$$

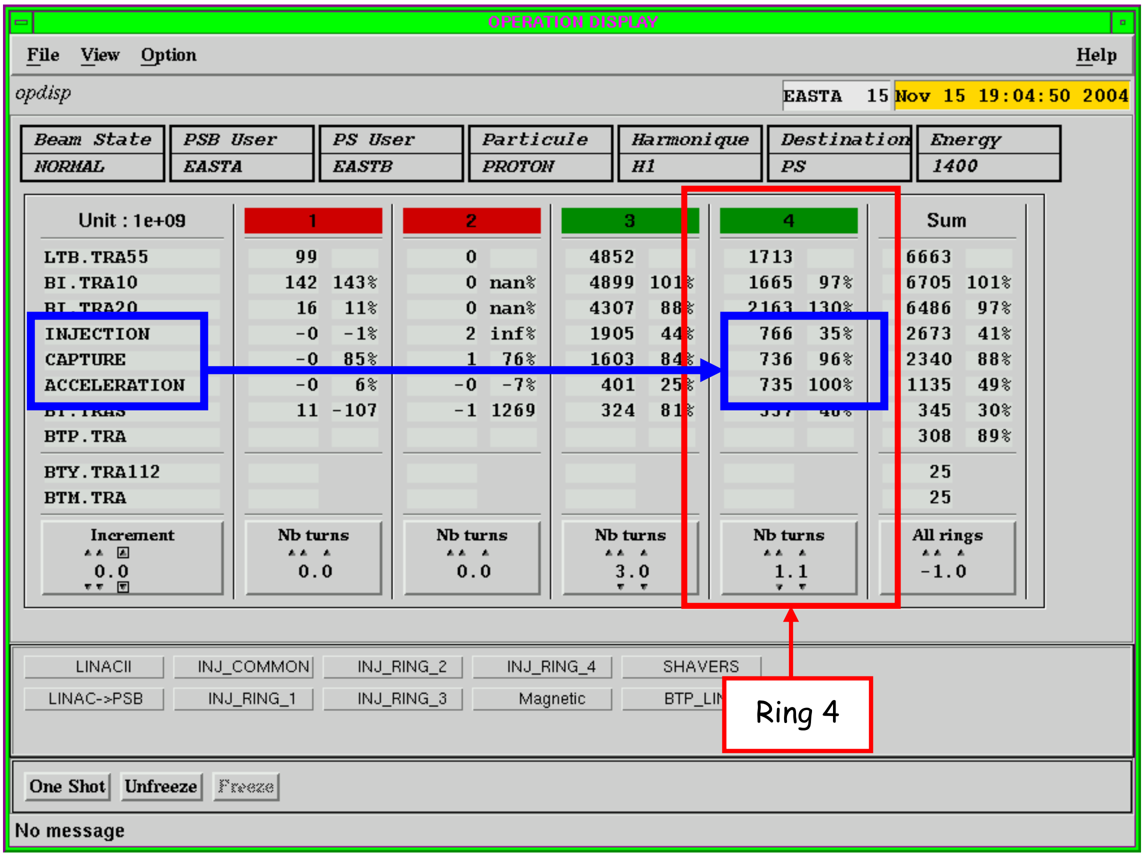
The second PI regulator setup is designed to optimise the radial loop at high energy, in particular for f_S = 743 Hz and p = 1578 MeV/c. Similarly to the low-energy PI setup, this corresponds to a ctime of 612 ms and f_L =276 Hz. The PI setup for the high energy case is then

$$\begin{cases} \dfrac{K_i}{K_p} = 471\,[rad/s] \\ K_p = 34.8 \end{cases} \qquad (15)$$

5. BEAM CONTROL TEST RESULTS

5.1 Capture and acceleration efficiency

The capture and acceleration efficiency were tested by continuously controlling the EASTA user beam in ring 4 and taking snapshots of the standard operational display. The beam intensity was also made to vary on purpose from one cycle to another. Figure 25 shows one such snapshot for the relatively low beam intensity of 7.66 10^{11} protons at injection. The number of captured protons shown in column 4 is 7.36 10^{11} while the number of accelerated protons is 7.35 10^{11}, which correspond to an efficiency of 95%. These results are at least comparable with those of the standard analogue PSB beam control.



opdisp

EASTA 15 Nov 15 19:04:50 2004

Beam State	PSB User	PS User	Particule	Harmonique	Destination	Energy
NORMAL	EASTA	EASTB	PROTON	H1	PS	1400

Unit : 1e+09	1		2		3		4		Sum	
LTB.TRA55	99		0		4852		1713		6663	
BI.TRA10	142	143%	0	nan%	4899	101%	1665	97%	6705	101%
BI.TRA20	16	11%	0	nan%	4307	88%	2163	130%	6486	97%
INJECTION	-0	-1%	2	inf%	1905	44%	766	35%	2673	41%
CAPTURE	-0	85%	1	76%	1603	84%	736	96%	2340	88%
ACCELERATION	-0	6%	-0	-7%	401	25%	735	100%	1135	49%
BI.TRAS	11	-107	-1	1269	324	81%	[illegible]	40%	345	30%
BTP.TRA									308	89%
BTY.TRA112									25	
BTM.TRA									25	
Increment 0.0	Nb turns 0.0		Nb turns 0.0		Nb turns 3.0		Nb turns 1.1		All rings -1.0	

No message

Figure 25: *Performance of the new digital beam control system: capture and acceleration capabilities are shown in the Ring 4 column.*

5.2 Phase offset

It is important to have a good zero reference at both low and high frequencies in order to measure the phase error ϕ_m. The zero reference is obtained by first adjusting the cable delay differences between cavity and Phase PU. An analogue delay of 310 ns is applied to the Phase PU signal before it is fed to the DDC. Additionally, a phase rotation of 109.5 degrees is applied to cavity data after the DDC to account for the azimuth difference between cavity and Phase PU. This value agrees with the position of the elements in the PSB, shown in Figure 3. Figure 26 shows the phase error ϕ_m measured by the DSP during a PSB cycle. Initial and final values are equal to those expected, i.e. 0.08 rad and 0.02 rad, respectively.

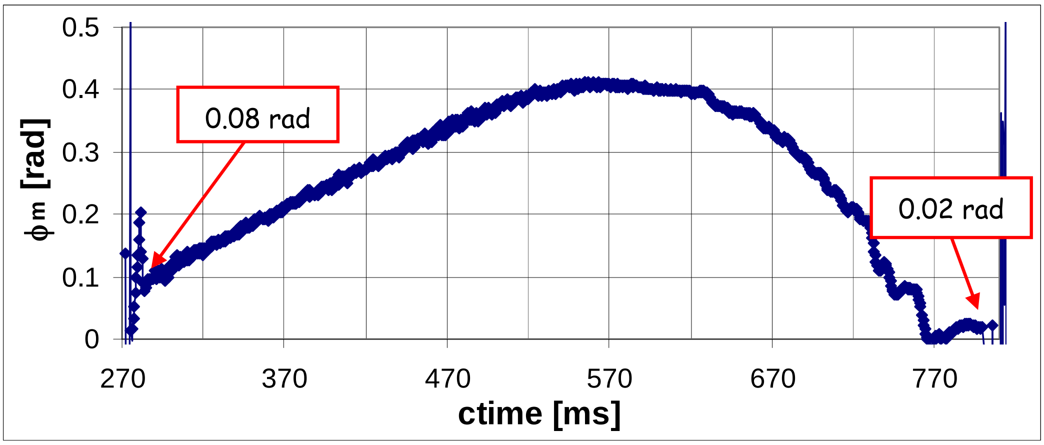


Figure 26: *Phase error ϕ_m measured by the DSP during a PSB cycle. The DSP-Oasis sampling period is 530 μs. The phase offset at injection and on the extraction plateau agrees with the values expected.*

Additionally, ϕ_m is expected to be higher than the synchronous phase angle ϕ_S as bunches are very long during the initial part of the cycle. This can be verified by comparing ϕ_m as shown in Figure 26 to ϕ_S, approximated by sin(ϕ_S) calculated from *dB/dt* and the RF voltage, as shown in Figure 27.

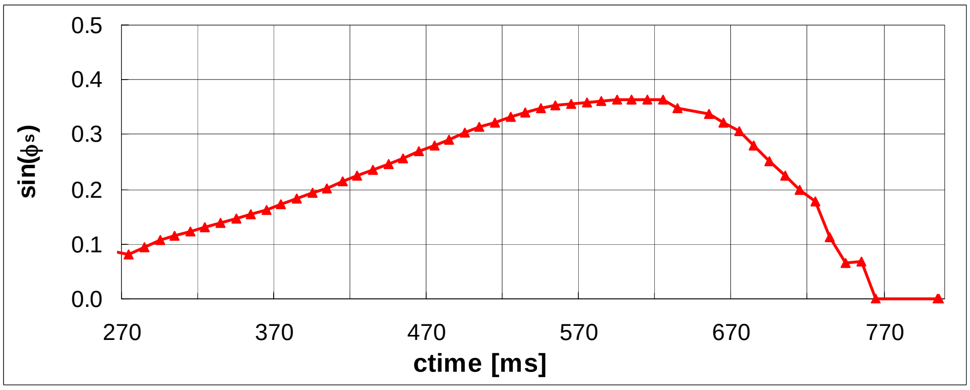


Figure 27: *Plot of sin(ϕ_S) vs. ctime, calculated from known dB/dt and RF voltage, as a first order approximation of the synchronous phase angle ϕ_S.*

5.3 Radial displacement due to a frequency step

The beam radial displacement for a given change of cavity frequency modulation varies during the PSB cycle, as shown for a typical cycle in Figure 28.

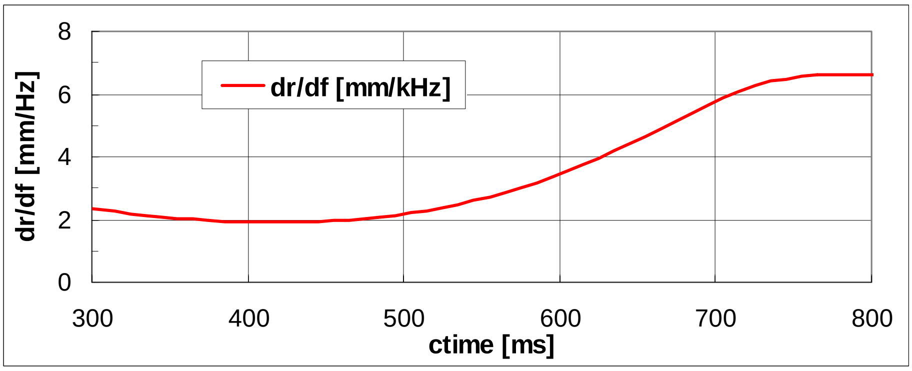
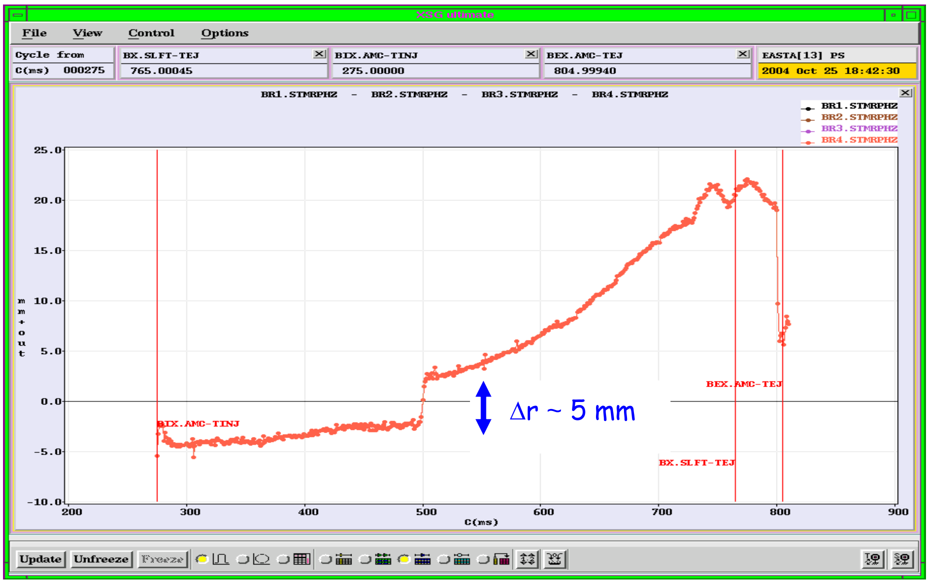


Figure 28: *Rate of variation with modulation frequency of the radial displacement, as a function of ctime, for a typical PSB cycle.*

To check the cavity voltage modulation and corresponding data acquisition path, the radial loop was closed at a ctime of 500 ms and the radial loop contribution was overwritten with FW_{rad_loop} = 100000. From equation (9) this corresponds to a modulation frequency excess Δf_{MDDS} = $FW_{rad\_loop} \cdot f_{REF\text{-}CLOCK}/2^{32}$ = 2.325 kHz. From Figure 28, at 500 ms one would expect a dr/df = 2.2 [mm/kHz]. This, multiplied by the Δf_{MDDS}, yields a radial position change of 2.2 times 2.32 = 5.1 mm. This is in good agreement with the radial position step-like change, measured by the sampler and shown in Figure 29. It should be noted that a Δf_{MDDS} of 2.32 kHz is kept constant during the cycle, resulting in a big beam radial displacement.


Cycle from C(ms) 000275

BX.SLFT-TEJ 765.00045

BIX.AMC-TINJ 275.00000

BEX.AMC-TEJ 804.99940

EASTA[13] PS 2004 Oct 25 18:42:30

Figure 29: *Beam radial displacement measured by the sampler application following a Δf_{MDDS} of 2.32 kHz added from ctime 500 ms until the end of the PSB cycle.*

5.4 Phase loop dynamics

At a ctime of 285 ms a 0.2 rad step function stimulus is added to the measured phase error ϕ_m, to examine the phase loop dynamic behaviour; the phase loop is closed at a ctime of 275.3 ms. The phase loop response is measured by observing the measured phase error ϕ_m via the DSP-Oasis subsystem. The phase loop gain K_e is set to 300000, giving a nominal BW_{PH_LOOP} of 7 kHz. The poles f_H and f_L of the closed loop system with the phase loop active are respectively 7 kHz and 570 Hz, with time constants of $T_{H,PL}$ = 23 µs and $T_{L,PL}$ = 280 µs, respectively. Figure 30 and 31 show the measured phase error ϕ_m zoomed on the fast and on the slow time constants, respectively. The measured fast and slow time constants are ~20 µs and ~300 µs respectively and they compare favourably to those expected.

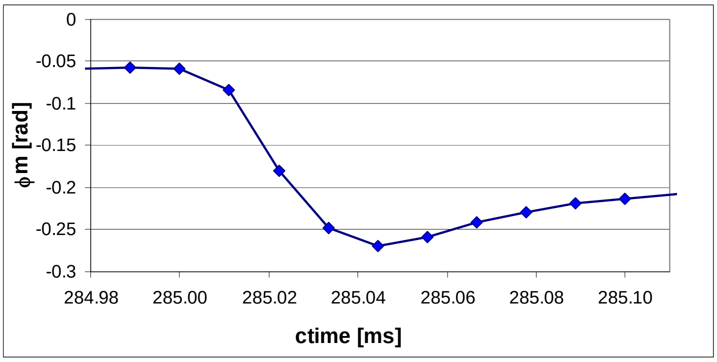


Figure 30: *Plot of the phase error ϕ_m showing a fast time constant of ~25 μs, in agreement with the expected $T_{H,PL}$. The DSP-Oasis sampling period is 11.1 μs.*

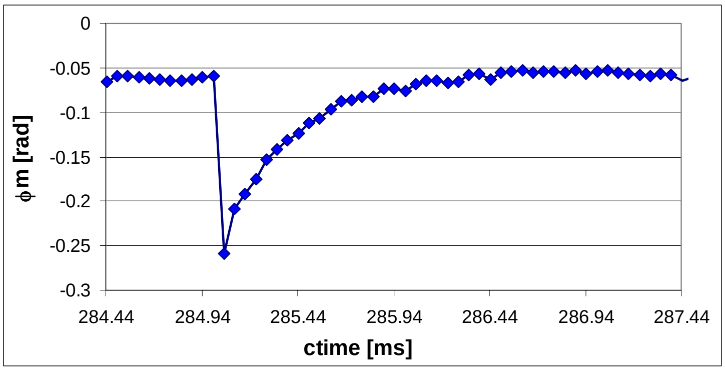


Figure 31: *Plot of the phase error ϕ_m showing a slow time constant of ~300 μs, in agreement with the expected $T_{L,PL}$. The DSP-Oasis sampling period is 55.6 μs.*

5.5 Radial loop dynamics

The radial loop dynamics was checked by applying a rectangular radial steering reference function to the beam; this changed the beam radial position from the centre of the vacuum pipe to -5 mm and then back to the centre. The beam radial position resulting from this steering and acquired by the DSP is shown in Figure 32.

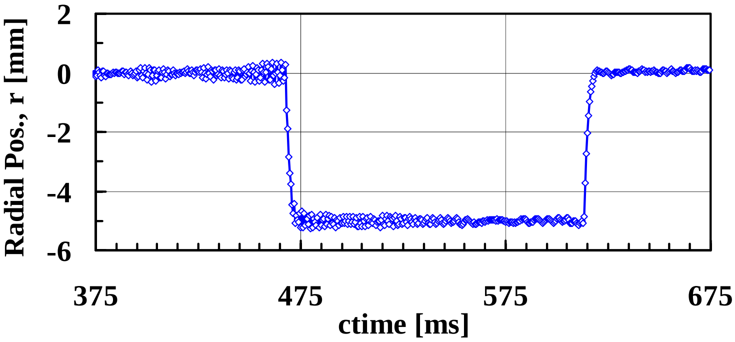


Figure 32: *DSP-measured beam radial position when a radial steering is applied. The DSP-Oasis sampling period is 530 μs.*

The same data are shown in an enlarged fashion in Figure 33, zoomed in coincidence with the steep radial position changes. In this way it can be seen that the corresponding ctimes are of

467.8 ms and 613.3 ms, i.e. those for which the radial loop is optimised with the PI settings (14) and (15). In addition, the radial response time constant can be determined to be about 1.5 ms, in reasonable agreement with the PI regulators design value.

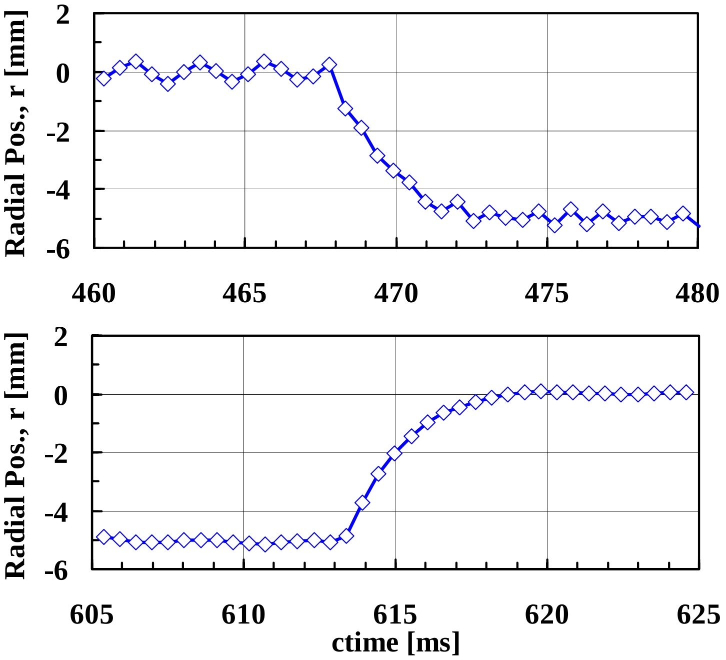
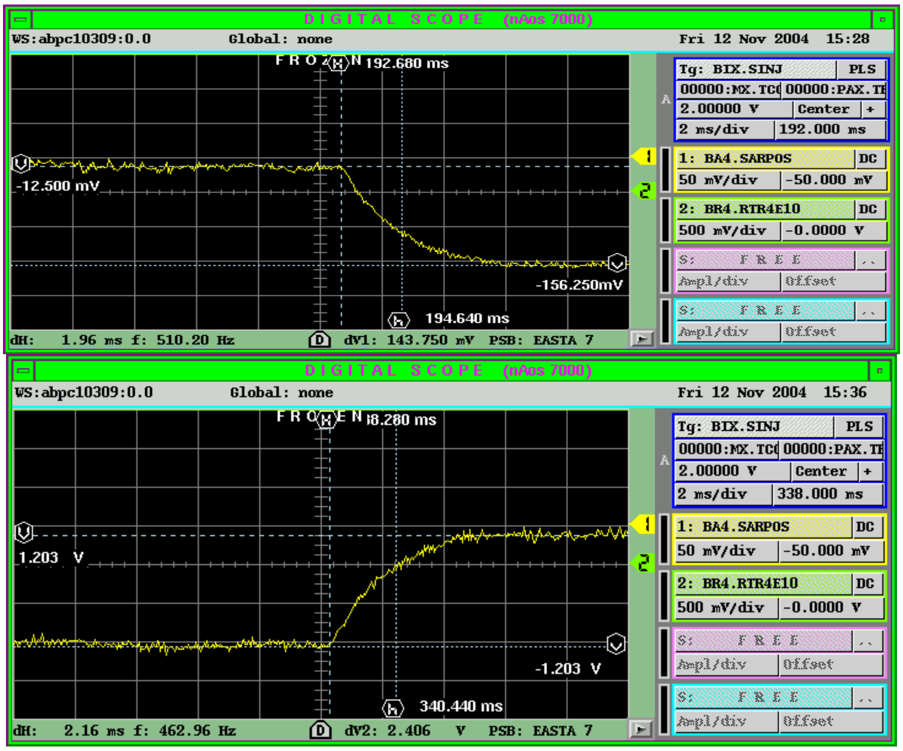


Figure 33: *DSP-measured beam radial position when a radial steering is applied. The DSP-Oasis sampling period is 530 µs.*

This behaviour was double-checked by a NAOS virtual oscilloscope, zoomed in correspondence of the steep radial position changes, as shown in Figure 34. The measured radial response time constant is again ~1.5 ms, in reasonable agreement with the PI regulators designed value.



```
DIGITAL SCOPE (nAos 7000)
WS:abpc10309:0.0          Global: none                    Fri 12 Nov 2004  15:28
FROZEN 192.680 ms
-12.500 mV
-156.250mV
194.640 ms
dH:   1.96 ms f: 510.20 Hz     dV1: 143.750 mV  PSB: EASTA 7
Tg: BIX.SINJ            PLS
00000:MX.TC( 00000:PAX.TI
2.00000 V       Center  +
2 ms/div        192.000 ms
1: BA4.SARPOS           DC
50 mV/div       -50.000 mV
2: BR4.RTR4E10          DC
500 mV/div      -0.0000 V
S:      F R E E
Ampl/div        Offset
S:      F R E E
Ampl/div        Offset

DIGITAL SCOPE (nAos 7000)
WS:abpc10309:0.0          Global: none                    Fri 12 Nov 2004  15:36
FROZEN 18.280 ms
1.203  V
-1.203  V
340.440 ms
dH:   2.16 ms f: 462.96 Hz     dV2: 2.406   V   PSB: EASTA 7
Tg: BIX.SINJ            PLS
00000:MX.TC( 00000:PAX.TI
2.00000 V       Center  +
2 ms/div        338.000 ms
1: BA4.SARPOS           DC
50 mV/div       -50.000 mV
2: BR4.RTR4E10          DC
500 mV/div      -0.0000 V
S:      F R E E
Ampl/div        Offset
S:      F R E E
Ampl/div        Offset
```

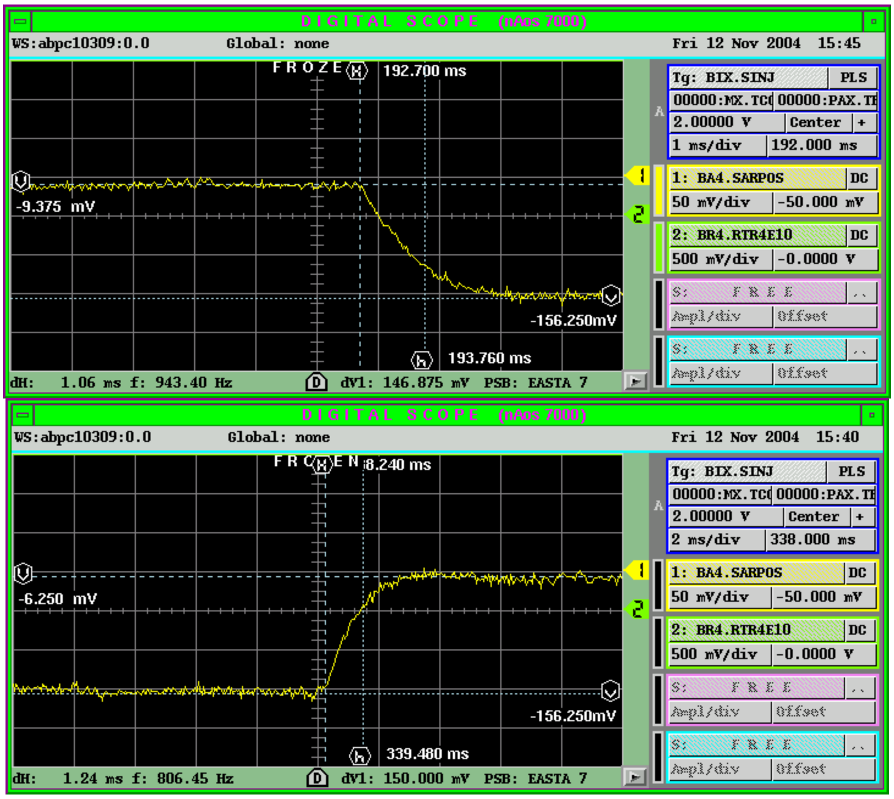
Figure 34: *Beam radial position BA4.SARPOS measured by the NAOS system and zoomed around the radial steering step. The measured response time is approximately 1.5 ms, reasonably in line with the PI design value.*

The same type of steering was repeated with a second set of PI regulators:

$$\begin{cases} \dfrac{K_i}{K_p} = 1733 \ \ [rad/s] \\ K_p = 35.4 \end{cases} \tag{16}$$

$$\begin{cases} \dfrac{K_i}{K_p} = 471 \, [rad\ /\ s] \\ K_p = 69.6 \end{cases} \tag{17}$$

These cancel the phase loop poles at the same ctimes as the first set, namely 467 ms and 612 ms, but with a radial response time of 1 ms. Figure 35 shows the beam radial position acquired by the NAOS virtual oscilloscope and zoomed in correspondence of the steep radial position change. Again, the measured radial response time constant is in reasonable agreement with the design value.



DIGITAL SCOPE (nAos 7000)
WS:abpc10309:0.0 Global: none Fri 12 Nov 2004 15:45
Tg: BIX.SINJ PLS
00000:MX.TC(00000:PAX.TI
2.00000 V Center +
1 ms/div 192.000 ms
1: BA4.SARPOS DC
50 mV/div -50.000 mV
2: BR4.RTR4E10 DC
500 mV/div -0.0000 V
S: FREE
Ampl/div Offset
S: FREE
Ampl/div Offset
dH: 1.06 ms f: 943.40 Hz dV1: 146.875 mV PSB: EASTA 7

DIGITAL SCOPE (nAos 7000)
WS:abpc10309:0.0 Global: none Fri 12 Nov 2004 15:40
Tg: BIX.SINJ PLS
00000:MX.TC(00000:PAX.TI
2.00000 V Center +
2 ms/div 338.000 ms
1: BA4.SARPOS DC
50 mV/div -50.000 mV
2: BR4.RTR4E10 DC
500 mV/div -0.0000 V
S: FREE
Ampl/div Offset
S: FREE
Ampl/div Offset
dH: 1.24 ms f: 806.45 Hz dV1: 150.000 mV PSB: EASTA 7

Figure 35: *Beam radial position BA4.SARPOS measured by the NAOS system and zoomed in correspondence of the radial steering. The measured response time is approximately 1 ms, reasonably in line with the PI design value.*

6. CONCLUSIONS AND FUTURE PLANS

A new beam control system for LEIR is under development. A set of beam tests has been carried out in the PSB, and this note has detailed the deployed system setup, hardware and software, as well as some test results. These tests follow a set of feasibility tests [2] carried out in 2003, which gave a feeling for the hardware flexibility, processing capabilities and strong and weak points. The tests carried out in autumn 2004 and described here, however, are much more sophisticated and focused on beam control; in addition, the deployed software architecture is more complex and closer to the one planned for LEIR. The tests described here were successful and allowed several new implementation concepts to be validated at DSP level, such as soft-GFAS, DSP-OASIS and soft-timings. The DSP-based system proved to be very flexible and performant, even if the RTT absence prevented remote operation and true PPM mode. Several further developments, both software (FPGA/DSP) and hardware, are under way for the final LEIR system. A tagged-clock scheme is being implemented, so as to synchronise in phase the NCOs of all daughtercards. For this purpose a new version of the MDDS daughtercard has been designed and manufactured at CERN, and the corresponding FPGA code is under development. In addition, a tagged clock fanout module is under design at CERN, which will be able to distribute the tagged master clock over cable and/or over optical fibre. We will design and manufacture DDC and SDDS daughtercard versions implementing the de-tagging scheme. The beam control system will also control the cavity gap relay through a dedicated module. The aim is to short-circuit the cavity when it is not under voltage, thus avoiding beam self-bunching due to cavity impedance.

From a software viewpoint, the DDC FPGA code needs to be completed, allowing DSP access to the SRAM located on the daughtercard. A more sophisticated SDDS code and corresponding digital interface with the cavities will also be implemented. Finally, the FPGA code of the DSP carrier board FPGAs needs to be upgraded. At DSP level, a demanding task is to implement a reliable DSP-to-DSP communication. This is mandatory as one DSP carrier board alone will not be able to interface with all the hardware, such as cavities and PUs. In fact, three DSP boards will be used for the LEIR beam control. Moreover, the cavity voltage servoing and PS-synchronisation code will have to be developed. An RTT will be written to allow data exchange with the user remotely and to allow the DSP boards to run in a PPM operating mode. Finally, appropriate application programs will be used to set control parameters and to display the results. Examples are timing-controlled knobs, the Trim application for controlling the reference functions and the OASIS virtual scope for visualising the DSP-acquired data. A dedicated RF application will also be developed.

In 2006 we plan to add a fourth DSP carrier board, carrying one 4-channel SDDS and one 4-channel DDC. This board will be used to verify the correct flight time compensation and PU-to-kicker phase advance of the transverse damping system throughout the LEIR cycle. That will be accomplished by tracking the betatron transverse damper Beam Transfer Function with absolute phase margins. The noise used to excite the beam will be generated digitally by the SDDS. In the future two DSP carrier boards with three DDC daughtercards will be installed in the PS for passive monitoring of the PS cavities phases. Finally, the long term plan is to migrate the AD, PSB and PS beam control systems to the same digital technology as used in LEIR, so as to standardise them and make their maintenance easier. This plan will be finalised after the LEIR commissioning experience.

7. REFERENCES

[1] M. Chanel, *"LEIR: The Low Energy Ion Ring at CERN",* EPAC'02, Paros, June 2002, p. 563.

[2] M.E. Angoletta, J.H. DeLong, A. Findlay, F. Pedersen, *"Feasibility Tests of a New All-Digital Beam Control Scheme for LEIR"*, AB-Note-2004-004 RF.

[3] A. Krusche, M. Paoluzzi, "The New Low Frequency Accelerating Systems For The CERN PS Booster", EPAC'98, Stockholm, June 1998, p. 1782.

[4] P. Alvarez, J. Serrano, *'The CTRP and CTRI GMT Receiver modules – Engineering Specification'*, EDMS document no 475441.

[5] S. Deghaye, D. Jacquet, I. Kozsar, J. Serrano, *'OASIS: a new system to acquire and display the analog signals for LHC'*, ICALEPCS 2003.

[6] http://project-fesa.web.cern.ch/project-fesa/

[7] B. Frammery, B. Dupuy, P. Fernier, S. Pasinelli, *'A VXI System for the Observation of Distributed Analog Signals'*, Eighth Conference on Real-Time Computer Applications in Nuclear, Particle and Plasma Physics, June 8-11, 1993, Vancouver, Canada.

[8] http://wwwpsco.cern.ch/private/gm/gmdescrip/SAMPAQ.html

[9] W. Heinze, *'The Equipment Module for the GFAS'*, PS/CO/Note 93-108 (Tech.) revised on 2001.