Radiation Qualification of Electronics Components used for the ATLAS Level-1 Muon Endcap Trigger System

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Abstract-- **The ATLAS end-cap muon level-1 trigger system is divided into three parts; one off-detector part and two on-detector parts. Application specific IC (ASIC) and anti-fuse FPGA (Field Programmable Gate Array) are actively used in on-detector parts. Data transfer with Low-Voltage Data Signaling serial link (LVDS link) is used between two on-detector parts (15m apart) and G-Link (Hewlett-Packard 1.4Gbaud high speed data link) with optical transmission(90m) is used from one of the on-detector parts to the off-detector part. These components will suffer for ten years the radiation of approximately 200Gy of total ionizing dose (TID) and a hadron fluence of $2x10^{10}$ hadrons/cm^2. We have investigated systematically the radiation susceptibility to both total ionizing dose and single event effects for ASIC, FPGA, and Commercial Off The Shelf (COTS) serializer and deserializer chipsets for LVDS (two candidates) and G-Link (one) together. In this presentation we report the result of irradiation tests for these devices and discuss validity of them to use in the system.**

I. Introduction

THREE types of ASIC are extensively used in the core part of the ATLAS end-cap muon level-1 system [1]. FPGA chips are also used for ancillary logics. The ASIC and FPGA chips are mounted on boards, which are just behind end-cap muon chamber discs (Thin Gap Chambers (TGC) with seven layers are used to identify a muon with p_T > 6GeV/c in the ATLAS endcap region) and the outer rim of a disc.

LVDS links are used to data transfer between two on-detector parts (15m) with STP (shielded twisted pair) category 6 cables. G-Link optical transmission lines are used from the on-detector one to the off-detector part over 90m distance. In overall ATLAS level-1 Muon Endcap system, we use about 1000 G-Link and 10000 LVDS link lines. As both links are serial transmission, we need a serializer at the transmitter and a deserializer at the receiver side.

The on-detector parts will be exposed to the estimated radiation of 3Gy of total ionizing dose and a hadron fluence of $2x10^{10}$ hadrons/cm^2 for ten year of the normal operation [2]. According to the ATLAS internal rules for the radiation hardness issues, we have to demonstrate that all the electronics components used in the on-detector part must work still in the 200Gy total ionizing dose (TID), which comes from 3Gy (actual dose simulated) times 70 (safety factors all in), and we have to anticipate the single event effect (SEE) rate for a component will be five (a safety factor) times more than σ_{SEE} (SEE cross section for the particular component) times the hadron fluence. We have made the radiation measurements of them using γ-ray from Cobalt-60(^{60}Co) for TID and 70MeV proton beam to derive σ_{SEE}.

We intend to use 0.35μm standard CMOS technology of ROHM [3] for ASIC fabrication and Actel [4] anti-fuse based FPGA chips. For the LVDS data transfer, we have selected two COTS serializer and deserializer chipsets (one from Texas Instruments (TI) [5] and one from National Semiconductor (NS) [6]). For the G-Link, we have uniquely selected one Agilent [7] chipset and an optical transceiver by Infineon [8].

In the next section, we discuss the setup and procedure of the radiation test for both TID and SEE level measurements. In Section III we list the results of the measurements. We discuss the characteristics similarity and difference for the radiation of CMOS and the Actel anti-fuse FPGA chips, and two candidates of the LVDS serializer and deserializer chipsets in detail. Finally in Section IV we give summaries of the results and conclusion.

II. Radiation Test Setup and Procedure

To estimate the TID tolerance we have used a γ-ray irradiation facility of Research Center for Nuclear Science and Technology (RCNST) of University of Tokyo. To obtain

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σ_{SEE} we have used a proton irradiation facility of Cyclotron and Radio Isotope Center (CYRIC) of Tohoku University.

A. Facility and Procedure for TID measurement

The γ-ray irradiation facility of RCNST is a two-story structure; an irradiation room on the downstairs and a store with a lead container for the irradiation sources on the upstairs. 48 pencil type rods as radiation sources are filled in a cylindrical vessel, which moves between the upstairs and the downstairs via remote control system. The maximum strength of the sources and the maximum dose rate are 22TBq and 1000Gy/hr in H_2O. The irradiation rate can be controlled by changing the radiation source and the location of the DUT (we call hereafter a target chip as DUT; Device Under Test). We used ^{60}Co as the source and the irradiation rate was set to 500Gy/hr. As this irradiation facility is widely being used, the dose rate is periodically calibrated using a Fricke Radiation Meter. The irradiation and the annealing were done at room temperature, around $25^{O}C$. During the irradiation and the annealing, DUTs were biased without clock and the current were monitored. The functionality was checked before and after the irradiation and the annealing.

B. Facility and Procedure for SEE measurement

From the cyclotron, 70MeV proton beam was extracted through a Ti foil of 20mmϕ and 100μm thickness into air and was impinged to a DUT. A target board and a ZnS fluorescence screen were mounted on an X-Y stage. The beam position was first monitored by the fluorescence screen and then the target board was moved to the beam position (The beam was stopped with a beam stopper during the X-Y stage was moving.). Actual beam profile and beam intensity were measured, individually for each chip with dosimetry of a 100μm thick Cu foil placed in front of the DUT. The beam intensity at the final beam stopper was around 0.5 - 4nA. The beam was intentionally broadened up to the size of around 20mmϕ.

III. Radiation Test Results

A. CMOS and Actel Anti-fuse FPGA

1) CMOS

We will use total three different types of ASIC in the system. Two chips are made using ROHM 0.35μm full custom CMOS technology. One is called Patch-Panel (PP) ASIC, and the other one is called Slave Board (SLB) ASIC. The detailed functionality of these chips has been discussed in [9]. While the SLB ASIC contains digital circuits only, the PP ASIC has some analog transistor circuits (for LVDS to TTL conversion and sub nano-second fine delay) beside digital ones.

In order to evaluate the TID condition of the 0.35μm ROHM CMOS chips, we have tested four PP ASIC chips. Three chips were irradiated up to 300Gy, and the other one was irradiated to 850Gy. As shown in Fig.1 (a), until 300Gy, we have observed no increase of the static current for all the chips. The current of the fourth one was increased from 49mA to 81mA monotonically as the irradiation level increased from 500Gy to 850Gy.

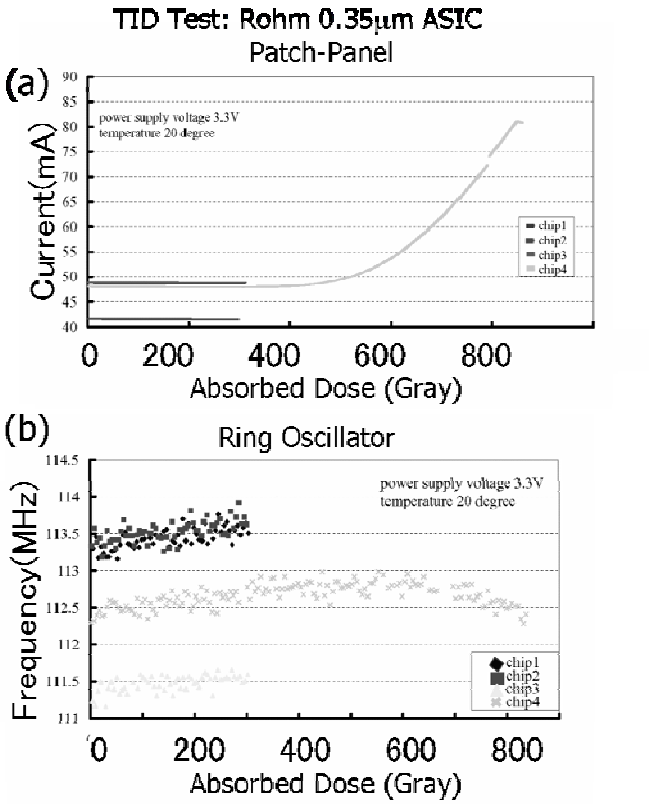

Fig.1 TID level measurement of ROHM 0.35μm ASIC chips. (a) is the supply current of the chips versus Dose for the Patch Panel ASIC chips which are actually used in the system. (b) is the frequency versus dose for specially processed ring oscillator circuit in ROHM 0.35μm ASIC(501 NAND).

In order to observe any characteristic change of a circuit more in detail caused by the irradiation, we have processed a ring-oscillator circuit in an independent chip with the same technology. The circuit is connected with 501 NAND gates to form a ring to make the oscillation frequency. We have also irradiated this chip as the same condition as the one for PP ASIC. Fig. 1 (b) shows the frequency change with the irradiation. We can find the frequency was increased till 600Gy, then it was decreased, namely the circuit response became once faster owing to the irradiation, and then it became slower.

We have processed a four-bit 256 stage shift register in an independent ASIC in order to evaluate σ_{SEE} for ROHM 0.35μm chips. We have produced four shift register chips. In the SEE test of this special ASIC, we have observed total 185 times of soft SEE (SEU; single event upset) and no hard SEE (SEL; single event Latch-up) for four chips with 6.3×10^{12} protons/cm^2 of the total integrated proton intensity injected (fluence). The σ_{SEU} is estimated as 2.8×10^{-14} cm^2/bit.

2) Actel Anti-fuse FPGA

Two different series of Actel anti-fuse FPGA (A54SX-A) and Axcelerator are used to implement various ancillary logic circuits in the system. Medium scale FPGA A54SX-A is used for a JTAG routing controller (JRC) and a VME interface, which is commonly used for modules mounted in the on-detector VME crate. The Axcelerator chip is a large scale FPGA with an embedded memory. We use this chip for both transceiver and receiver in a readout data concentrator module. Both the transceiver and the receiver need FIFO in order to absorb the different rates for the data transmission.

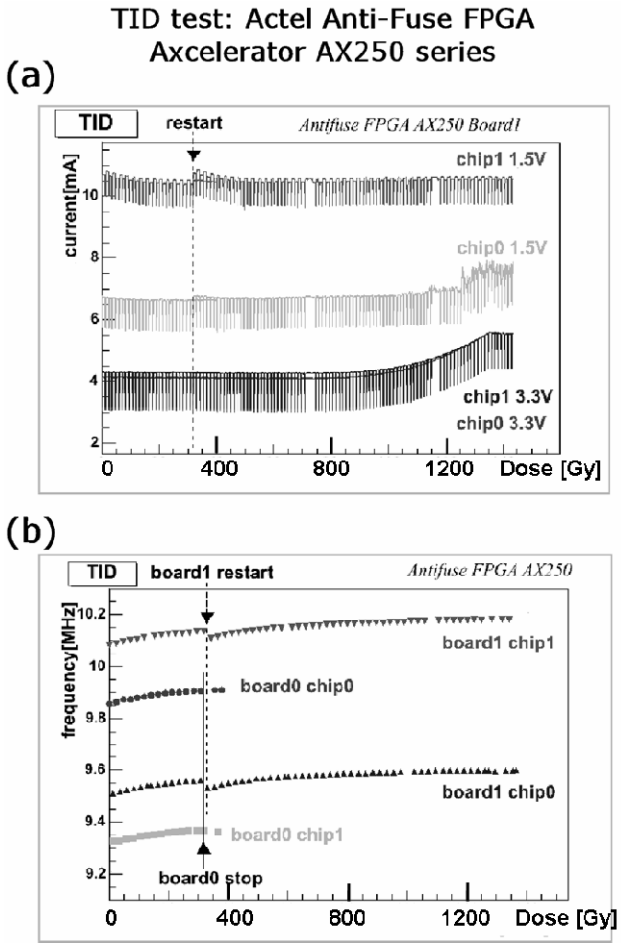

Fig.2 TID results for Actel anti-fuse FPGA Axcelerator series chips. In an FPGA chip, a ring oscillator with 101 NAND gates has been implemented. (a) is the supply current versus Dose level for the chips which were irradiated up to 1300Gy. During the irradiation, the ring oscillator has been paused its operation for ten seconds in every minute. This Axcelerator chips requires two power lines, one for the I/O cell (3.3V) and the other one for the core logic part (1.5V). (b) is the ring oscillator frequency versus dose level.

The static current for four Axcelerator series FPGA chips versus the absorbed dose is shown in Fig. 2(a). In the measurement, the operation of the built-in circuit (a ring oscillator with 101 NAND gates) has been paused for 10 seconds in every one minute regularly. This makes saw-toothed structure in the graph. The frequency of the ring oscillator versus the dose is shown in Fig. 2(b). We measured two different currents per chip, one is for the I/O cell which is operated with 3.3V, and the other one is for the core logic part which is operated with 1.5V.

From both figures, we found that neither significant current increase nor frequency change has been observed in all the four chips tested. We have done the same measurement for SX-A series chips. Dynamic range of the change with the dose for both the supply current and the frequency of the SX-A series chips were greater than one of the Axcelerator series ones.

We find that the radiation susceptivity of the Axcelerator chips is comparable with the ROHM 0.35μm ASIC. The Axcelerator chips were processed with more advanced technology of 0.15μm CMOS anti-fuse than SX-A ones. This makes presumably the radiation tolerance of the Axcelerator stronger than SX-A and comparable with ROHM ASIC chips.

For the SEE level measurement of SX-A series chips, we have installed a four bit shift register of 256 stages (1024 bit) as we have done in the ASIC case, and read and verified the data outputted. No soft SEE (SEU) has been observed with the fluence of 2.6×10^{12} protons/cm^2. σ_{SEU} is estimated, therefore, as $< 1.5 \times 10^{15}$cm^2/bit with 90% confidence level. We have also installed a four bit shift register in flip-flop cells (R-cells) of the Axcelerator chips. The length of the shift register was 345 stages (total 1380 bit) in this case. We have applied the SEE test also to the embedded memory whose size is 54Kbit. Since the memory is configured as a dual port memory, regularly we inputted a bit pattern to the memory, and compared it with the output bit pattern from the memory for verification. We have observed 32 SEU in the R-cell and 3869 in the embedded memory with 1.4×10^{12} protons/cm^2 of the proton fluence. σ_{SEU} for R-cell (Flip flop cells in FPGA) is estimated as 1.6×10^{-14}cm^2/bit, and σ_{SEU} for Memory is 4.9×10^{-14}cm^2/bit. No SEL has been observed in Actel anti-fuse FPGA chips. We have summarized the SEU level measurements for both CMOS and anti-fuse FPGA in table I.

3) Mitigation of SEU

For both ASIC and FPGA chips, we have many registers to keep parameters necessary to drive chips. In the case of the ASIC, we have installed total 3.4×10^6bits (NCHAN) for the registers in the whole system. The number of SEU anticipated for the ASIC chips in the system for ten years (10^8s) is calculated as σ_{SEU}xSRLxNCHAN, where SRL is the simulated radiation level for ten years, and the worst value in the region where our system occupies in the ATLAS detector is estimated as 2.11×10^{10}hadrons/cm^2 for hadrons with the energy greater than 21MeV [2]. The number of upsets in all the ASIC chips for a day is, therefore, estimated as 1.73. In order to provide the immunity of the system from SEU further, we keep every bit in the registers of both the ASIC and FPGA with three redundant flip-flops. Outputs of the flip-chips are connected to a voter logic to select majority values among two different values if one of the flip-flops is suffered an SEU.

TABLE I
COMPILATION OF SEU (SOFT SEE) TESTS

Technology	Proton fluence (protons/cm^2)	σ_{SEU} (1/cm^2/bit)
ROHM CMOS 0.35μm	$6.3x10^{12}$	$2.8x10^{-14}$
Actel FPGA SX-A	$2.6x10^{12}$	$<1.5x10^{-15}$
Actel FPGA Axcelerator (R-cell)	$1.4x10^{12}$	$1.6x10^{-14}$
Actel FPGA Axcelerator (Memory)	$1.4x10^{12}$	$4.9x10^{-14}$

B. Two LVDS serializer and deserializer chipsets

LVDS links are used for data transfer from the front-end on-detector one to the second on-detector part over 15m. While STP category 6 cables will be used in the ATLAS experiment, STP category 5e cables have been used throughout the radiation tests. For the serial data transfer with the LVDS link, we have two selections for Commercial-Off-The-Shelf serializer and deserializer chipsets (one from Texas Instruments (TI) [2]: SN65LV1023/1224 and one from National Semiconductor (NS) [3]: DS92LV1023/1224). Both chipsets have identical functionality and even the same pin allocation, though the frequency range is slightly different.

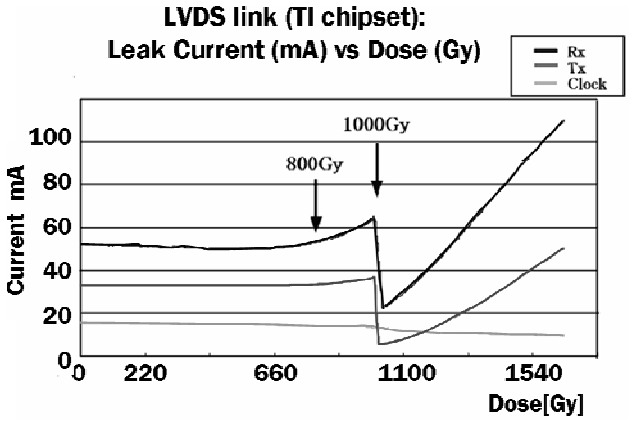

Fig.3 Supply current versus dose level for LVDS link serializer (Tx) and deserializer (Rx) of TI product. The clock means a clock chip (40.08MHz) irradiated together with the chipsets.

We have irradiated four samples from each LVDS chipset candidate with γ-ray till 300Gy. The supply current of all the samples were stable during irradiation, and kept pre-irradiation level up to 300Gy. One sample among four from each candidate was exposed further to 1600Gy. Figure 3 shows the dependence of the supply current on the absorbed dose up to 1600Gy for a TI sample. Both serializer (Tx) and deserializer (Rx) of the TI candidate showed increase of current after 800Gy till 1000Gy, and abrupt current drop immediately after 1000Gy. An LVDS link could no longer be established after the current drop while the chipset of NS candidate has no significant increase of the current even up to 1600Gy.

In the SEE test, the serializer and deserializer were mounted on a PC board, and these chips are connected each other for the data transfer between them on the board. We have checked the functionality during the proton irradiation remotely by sending some bit patterns to Tx on the board and receiving them from Rx on the board. We have tested two pairs for each NS and TI candidate. The data taken in the test for two LVDS chipsets are summarized in Table II.

In Table II, we have classified the abnormalities observed during the irradiation into two classes. If the monitor board detects different bit pattern rather than the pattern which it has sent, then it is regarded as an SEU error. The link failure means that Rx could not synchronize its clock with the clock embedded in the data sent, i.e. it could not phase-lock the clock with one sent from Tx.

Based on Table II, we have estimated σ_{SEE} independently with two error categories and listed in Table III. The simulated radiation level (SRL) for Tx and Rx for ten years are estimated as $2.11x10^{11}$ and $1.42x10^{11}$ hadrons/cm^2, respectively. The number of LVDS links we must install in the ATLAS will be 10^4. With these numbers we can estimate the total (Tx+Rx) failures rate in the system per day for both candidates as

- the number of SEU errors/day: 2.5 (NS) and 0.6 (TI),
- the number of link error/day: 1.7 (NS) and 0.4 (TI).

TABLE II
SEE TEST RESULTS FOR LVDS CHIPSETS OF TI AND NS. SEU MEANS THE NUMBER OF SEU OBSERVED WHILE LINK FAILURE MEANS THE NUMBER OF LINK OUT DURING IRRADIATION. F IS TOTAL INTEGRATED PROTON INTENSITY.

Vendor	Chip	SEU	Link failure	F (cm^{-2})
TI	Rx	6	2	$5.4x10^{12}$
	Tx	8	7	$7.6x10^{12}$
NS	Rx	55	36	$2.3x10^{12}$
	Tx	1	5	$3.7x10^{12}$

TABLE III
SEE TEST RESULTS: σ_{SEE} FOR THE CHIPSETS OF TWO DIFFERENT VENDORS. THEY WERE ESTIMATED INDEPENDENTLY FOR TWO ERROR CATEGORIES.

Chip	Vendor	σ_{SEU} (cm^2)	σ_{link} (cm^2)
Tx	NS	$1.3x10^{-13}$	$1.2x10^{-12}$
	TI	$2.5x10^{-12}$	$1.5x10^{-12}$
Rx	NS	$2.0x10^{-13}$	$1.2x10^{-11}$
	TI	$8.0x10^{-13}$	$6.3x10^{-13}$

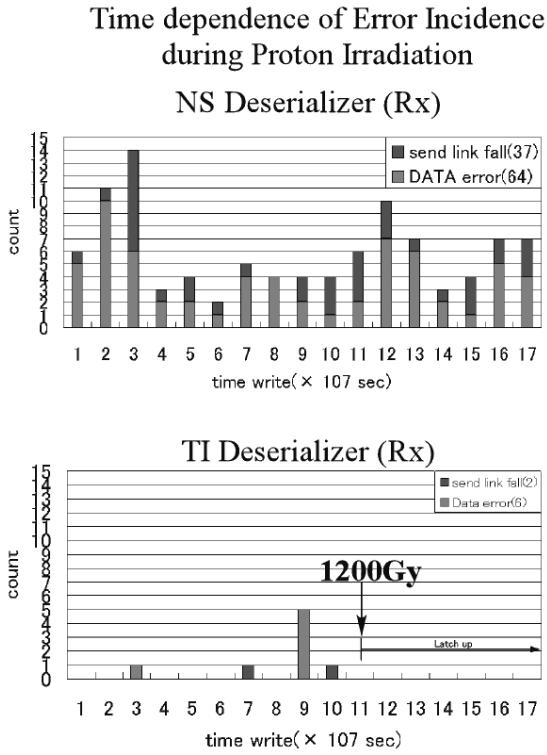

Fig.4 Time dependence of error (link failure and bit failure) incidence for deserializer (Rx) chips of NS and TI. Although TI chip has very small rate for the error occurrence, it has broken (due to Single Event Latch-up) after proton irradiation of 1200Gy.

If, however, we compare time dependence of error incidence of Rx, for example, for both vendors, we find very different characteristics between two vendors as shown in Fig.4. All the samples of NS Rx showed always SEU and link failures uniformly over irradiation period while ones of TI showed seldom SEU and link failures. All TI Rx showed, however, significant increase of the source current after the proton dose of 300Gy up to 1200Gy where all the TI Rx are broken. The increase of the source current has been observed already in the TID test for TI samples as shown in Fig.3.

As far as the SEE test results are concerned, the chipset of both vendors are satisfied with the condition for the criteria issued by the ATLAS radiation working group [2]. TI chipsets has been observed with significantly less number of SEUs and link failures than NS while TI Rx was broken at around 1200Gy irradiation level. For the ATLAS muon endcap electronics, however, as 1200Gy radiation level is beyond the maximum limit for the region we are concerned, we will use TI chipsets eventually in the electronics system.

C. G-Link serializer and deserializer chipset

Four Agilent G-Link chipsets with Infineon optical transceivers were irradiated with γ-ray up to 300Gy in the TID measurement. During the irradiation, we kept continued the data transfer between G-Link Tx and Rx via the optical transceivers monitoring the bit transfer error. None has shown distinct current increase till 300Gy dose, and no bit error has been observed in this test system setup.

In the SEE test, we have also measured data transfer errors and link failures as a similar way to the LVDS test. We have made also qualification test of an optical transceiver for the proton irradiation beside Tx and Rx. Total two samples for each chip have been tested. In Table IV, we summarized the aggregate sum for number of SEUs detected and number of link-lock failures with the total integrated proton intensity (F) for all three G-Link chips.

TABLE IV

SEE TEST RESULTS FOR G-LINK CHIPSET AND THE OPTICAL TRANSCEIVER. SEU MEANS THE NUMBER OF SEU OBSERVED WHILE LINK FAILURE MEANS THE NUMBER OF LINK LOCK FAILURE DURING IRRADIATION. F IS TOTAL INTEGRATED PROTON INTENSITY.

Chip	SEU	Link failure	F (cm^{-2})
Tx	4991	77	$2.3x10^{11}$
Rx	2802	162	$2.4x10^{11}$
Opt. Trans	69	0	$8.1x10^{11}$

Even after the link failure observed in Tx, synchronization were recovered autonomously for all 77 cases. The recovery time was 8μs in average, and it never exceeded 10μs as the longest. Three link failures out of total 162 link failures observed in Rx were failed to re-lock autonomously but recovered Rx by sending a synchronization pattern from Tx side. In this case the recovery for phase loop lock takes 38.4μs.

We have estimated separately the cross sections σ_{SEE} for SEU and link failure and summarized them in Table V.

TABLE V

G-LINK SEE TEST RESULTS: σ_{SEE} FOR THE CHIPSETS OF TWO DIFFERENT VENDORS ARE ESTIMATED INDEPENDENTLY WITH TWO ERROR CLASSIFICATIONS.

Chip	σ_{SEU} (cm^2)	σ_{link} (cm^2)
Tx	$2.2x10^{-8}$	$3.3x10^{-10}$
Rx	$1.2x10^{-8}$	$6.7x10^{-10}$
Opt.Trans.	$8.5x10^{-11}$	$< 3.0x10^{-12}$

With the simulated radiation level (SRL) of Tx and Optical Transmitter for 10 years as 6.54hadrons/cm^2 and the number of chips for both Tx and the optical transceivers as 1000, we can estimate the number of errors per day of Tx as 1.9 for SEU and 120 for link error, and of the optical transceiver as 0.5 for SEU and < 0.02 for link error.

IV. SUMMARY

The radiation tolerance of ROHM 0.35μm CMOS ASIC chips as well as two Actel Anti-fuse FPGA chips have been

examined with the TID and SEE measurements. From the estimations based on the measurements resulted in both tests, we found both ASIC and FPGA chips can be used in the ATLAS level-1 muon endcap trigger system without introducing serious degradation for the performance. We have found that Actel SX-A chips have more susceptive to radiation than the Axcelerator chips, and that the susceptibility of the Axcelerator ones is more-or-less the same as ROHM CMOS 0.35μm ASIC chips. Although there are several drawbacks in anti-fuse FPGAs like its one-time programmability or low logic density, we can elevate the usage of the anti-fuse FPGA chips even in the radiation condition rather than ASIC.

We have found very different radiation characteristics for two types of LVDS chipsets (NS and TI) both in TID and SEE measurements. The NS ones have many SEU or link failure but immune to TID while TI ones have relatively insusceptible to SEE if the absorbed dose is less than 1000Gy. From TID measurement, TI chips have a structure also at around 1000Gy as seen in Fig.3. TI chips are more qualified than NS chips if the dose is less than 1000Gy. TI Chipsets show less number of errors expected for both SEU and link (less than 1) than NS (~ a few) for a day. From the SEE test, the G-Link chipset has shown no problem for our usage either, though the number of link errors per day will be greater than 100.

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