Radiation Qualification of Commercial-Off-The-Shelf LVDS and G-link Serializers and Deserializers for the ATLAS Endcap Muon Level-1 Trigger System

R.Ichimiya[a], S.Tsuji[a], Y.Arai[b], M.Ikeno[b], O.Sasaki[b], H.Ohshita[c], N.Takada[c], Y.Hane[d], K.Hasuko[d], H.Nomoto[d], H.Sakamoto[d], K.Shibuya[d], T.Takemoto[d], C.Fukunaga[e](fukunaga@comp.metro-u.ac.jp), K.Toshima[e] and T.Sakuma[f]

[a]Kobe University, 657-8501, Kobe, Japan, [b]KEK, 305-0801, Ibaraki, Japan, [c]Shinshu University, 390-8621, Matsumoto, Japan, [d]ICEPP, University of Tokyo, 113-0033, Tokyo, Japan, [e]Tokyo Metropolitan University, 192-0397, Hachioji, Japan, [f]Tokyo University of Agriculture and Engineering, Tokyo, Japan

Abstract

The ATLAS endcap muon level-1 trigger system is divided into three parts; one off-detector part and two on-detector parts. Serialized data transfer with LVDS is used between two on-detector parts (15m apart) and serialized G-link transfer with optical transmission (90m) is used from the on-detector part to the off-detector part. Since the radiation damage of the components used in the on-detector parts is a matter of concern, we have investigate systematically the radiation susceptibility to both total ionizing dose and single event effects of COTS serializer/deserializer chipsets for LVDS (two candidates) and G-link (one) together. In this report we discuss in detail the characteristics of these LVDS chipsets and qualification of the G-link components for radiation.

I. Introduction

ATLAS endcap muon level-1 trigger system [1] will use about 1000 G-link and 10000 LVDS link lines. LVDS links are used to data transfer from front-end on-detector one to the second on-detector part over 15m with USTP (un-shielded twisted pair) category 5 cables. G-link optical transmission lines are used from the second on-detector one to the off-detector part over 90m distance. As both links are serial transmission, we need a serializer at the transmitter and a deserializer at the receiver side. We estimated the total dose of 200Gy for ten years operation (including safety factors) and a hadron fluence of $2x10^{10}n/cm^2$ at the on-detector parts.

For the LVDS, we have selected two Commercial-Off-The-Shelf serializer and deserializer chipsets (one from Texas Instruments (TI) [2]: SN65LV1023/1224 and one from National Semiconductor (NS) [3]: DS65LV1023/1224) as candidates for our system. Both chipsets have identical functionality and even the same pin allocation, though the frequency range is slightly different. For the G-link, we have uniquely selected one Agilent [4] chipset (HDMP-1032A/1034A) and an optical transmitter by Infineon [5] (V23818-K305-L57).

In order to avoid or keep minimum the link loss and miss-synchronization of the LVDS link in the ATLAS muon end-cap level 1 trigger system, we adopted a very simple parallel to serial data encoding scheme, which is i) to add start bit (1) and stop bit (0) to make 12 bit for 10 bit data encoding and ii) to fix a synchronization pattern of 10 bit [1111100000] with the start and stop bits. If we have no data to be sent over the LVDS link, we send the synchronization pattern for both the trigger stream and readout one. There is other kind of the data stream called control stream in the system. The data on the control stream come downward from the off-detector part to the on-detector front-end part while other two streams (trigger and readout) are directed to the off-detector part from the front-end. Between two on-detector parts, the control stream has been implemented with the LVDS serial transmission. The data are used to configure the initial setup for the registers embedded in the custom ICs as well as FPGAs in the front-end part. The control stream also conveys a command for the LVDS serializer to send the synchronization pattern.

We have set several restrictions also for the G-link serialization and deserialization sequence in order not to make link-loss, and to avoid the miss-synchronization. Several ideas have been gotten heuristically through several developments and tests of the slice system [6];

(1) PASS (Parallel Automatic Synchronization System) facility is disabled. PASS is to make automatic synchronization with the parallel reconstructed data at the Rx side with the clock used in the Rx chip. Since strict synchronization should be established only in the on-detector system but it should not be necessarily required between the on- and of-detector parts.

(2) We have also set our own DVI1 and DIV0 bit setting. These bits are used to specify the transmission baud rate. There are two choices in the control bits of DIV1 and DIV0 bit setting for the data transfer of 40MHz/word (800Mbaud). We set DIV1,0=0,1 instead of DIV1,0=0,0.

(3) We force Tx to send idle words when Rx is in the process of the synchronization. The idle words have the structures with the first 9 (7) bit with 1, 9 (11) bit with 0, and 1 in the last two bits. If no data is sent from the on-detector part, all 0 data should be sent.

(4) In order to ensure the DC balance for the serial line, Tx chip has so-called MASTER

TRANSITION to revert bit value assignment from high for 0 to low for 0 alternatively. If we send continuously data with 0 to 1 or 1 to 0 transitions at a certain position in the serial bit train, the Rx may misunderstand it as the MASTER TRANSITION. This misunderstanding may cause miss-synchronization. Thus we have to avoid sending constantly data with 0 to 1 or 1 to 0 transitions at the fix position in the bit train.

(5) If the Rx chip is in a false synchronization mode, we have to switch on/off DIV0 and DIV1 bit values to acquire the correct synchronization.

II. Tests for Total Ionizing Dose

A. Test Facility

The γ-ray irradiation facility is two-story structure; an irradiation room on the downstairs and a store with a lead container for the irradiation sources on the upstairs. 48 pencil type rods as radiation sources are filled in a cylindrical vessel, which moves between the upstairs and the downstairs via remote control system. The maximum strength of the sources and the maximum dose rate are 22TBq and 1000Gy/hr in H_2O. The irradiation rate can be controlled by changing the radiation source and the location of the DUT (we call hereafter a target chip DUT; Device Under Test). We used ^{60}Co as the source and the irradiation rate was set at 500Gy/hr. The irradiation facility of RCNST is widely being utilized in University of Tokyo; the dose rate is periodically calibrated using a Fricke Radiation Meter. The irradiation and the annealing were done at room temperature, around 25^{O}C. During the irradiation and the annealing, DUTs were biased without clock and the current were monitored. The functionality was checked before and after the irradiation and the room temperature annealing (one or a few day after the irradiation).

B. Results for LVDS chipsets

In order to test the functionality of the chipsets, we have made a special DUT PC board. A board mounts both Tx and Rx chips. The Rx on the board receives 10-bit data sent from a monitor system installed outside the control area, sends it to Tx in 10 bit parallel, and Tx sends back serialized data. The monitor system compares both the transmitted data and received data. During irradiation, we operated this sequence with several different bit patterns.

We have irradiated four samples from each LVDS chipset candidate with γ-ray till 300Gy. Static current (Icc) of all the samples were stable during irradiation, and kept pre-irradiation level up to 300Gy. One sample among four from each candidate was exposed further to 1600Gy. Figure 1 shows the dependence on the absorbed dose for the static current of the 1600Gy exposed TI sample. Both serializer (Tx) and deserializer (Rx) of the TI candidate showed increase of current after 800Gy till 1000Gy, and abrupt current drop immediately after 1000Gy. An LVDS link could no longer be established after the current drop while the chipset of NS candidate has no significant increase of the current even up to 1600Gy. After annealing for two days, we tried to make the functionality check of the board which mount two TI chips and 40.08MHz clock, and found the board did not work at all. The board has, however, revived if we exchanged the clock. Simply the clock chip has been damaged by the total ionizing dose, and TI chipsets themselves might have no serious damage. The samples from two (NS and TI) candidates were found to survive till 800Gy.

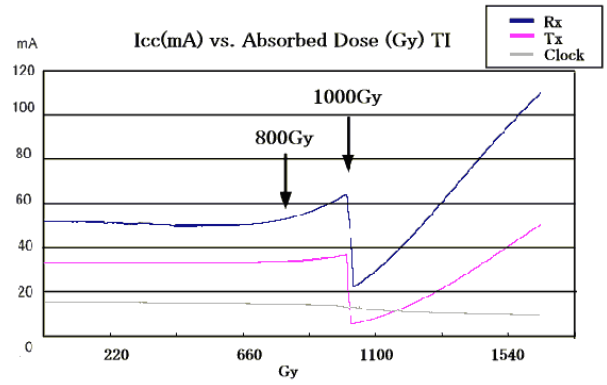

Figure 1: Static current versus g absorbed dose (gy) for TI Serializer (Tx) and Deserializer (Rx)

C. Results for G-link chipset

We have made a similar DUT PC board as one used in the LVDS link test also for the G-link. Figure 2 shows a connection diagram of the DUT PC board together with the monitor board which is put outside the control area.

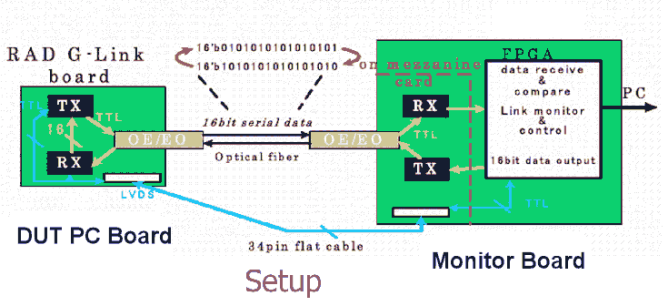

Figure 2: Setup diagram of G-link test boards. DUT board is located in the radiation area while the monitor board is put outside the control area. This setup is common for both TID and SEE tests.

Four Agilent G-link chipsets with OE/EO converters were irradiated with γ-ray up to 300Gy. During the irradiation, we kept continued the data transfer between G-link Tx and Rx via EO and OE converters monitoring the bit transfer error. As shown in Fig.4, none has shown distinct current increase till 300Gy dose, and no bit error has been observed in this test system setup.

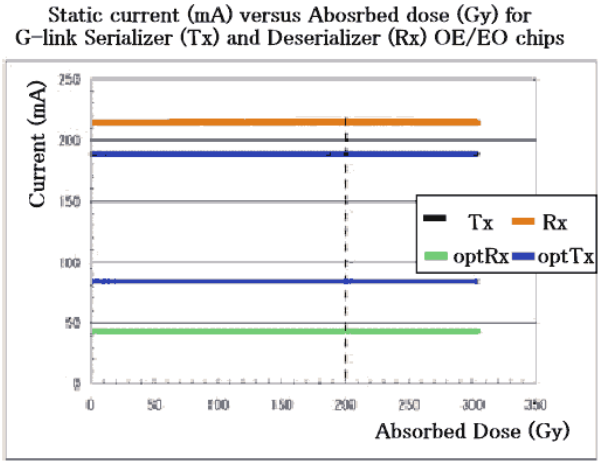

Figure 3: Static current versus γ absorbed dose (gy) for Agilent G-link Serializer (Tx) , Deserializer (Rx), and Infineon OE/EO chips.

III. TESTS FOR SINGLE EVENT EFFECTS

A Soft SEE (Single Event Effect) is phenomenon of radiation induced bit flip (non-permanent). A Hard SEE is also the same as the soft SEE but a destructive SEE produces permanent short circuits in a chip, like a latch-up. Whatever effect is concerned, any SEE rate for a chip can be determined from the SEE test as follows;

$$SEE\ rate = (\sigma_{SEE}) \times Nbits \times SRLsee \times SFsim$$

where σ_{SEE} is the cross section of either soft or hard SEE in a given location (cm^2/bit), *Nbits* is the number of bits affected by SEE (we have set this as 1 for the serializer (Tx) and deserializer (Rx) of both the LVDS and G-link), *SRLsee* is the simulated Radiation Level in a second (hadrons/cm^2/s), and *SFsim* is the safety factor of the simulation, and is '5'.

The maximum value of the *SRLsee* of the LVDS Tx is seen on the electronics module at the most inner part of the ATLAS endcap (r=775mm, and z= 1250mm) and is estimated as 2.11×10^2 hadrons/cm^2/s (for hadrons energy > 21MeV). The position where LVDS Rx and G-link Tx are placed is on the outer rim of the ATLAS endcap, and the *SRLsee* is estimated to be 1.42×10^2 h/cm^2/s. These values are taken from a simulation done by the ATLAS radiation hardness assurance group [7].

To estimate the SEE rate for any particular chip in a test, we must count occurrence of soft (hard) SEEs for certain amount of time, estimate integrated proton intensity into the chip, and derive soft (hard) σ_{SEE} from them.

For the estimation of the proton intensity for a chip in a test, we made dosimetry measurement for a cu foil. Thickness of the Cu foil is 0.1 mm and its purity is 99.99+%.

The size of the Cu foil is 25 mm by 25 mm and attached on top of the chip just being tested. After one hour of a run of the SEE test, γ-ray spectrum from activated radioisotopes was measured for 1,000 sec with a Ge detector.

We can estimate the number of nucleus generated (*N*) in the irradiation for period Tr seconds from the number of γs observed (C_γ) in the dosimetry measurement. Then if we know the effective cross section of proton and cu and number of cu atoms in the target, we can deduce the proton intensity (number of protons/cm^2/s). Then we calculated the integrated proton intensity (*F*) actually injected in the die of a chip in the irradiation period taking into account the beam profile information. For the beam profile measurement, we exposed the g rays emitted from a cu foil on an imaging plate, and scan the intensity of the exposed imaging plate with a commercial imaging plate reader. The unit of *F* is given as protons/cm^2. σ_{SEE} is given with a following relation,

$$\sigma_{SEE} = (\text{number of SEE counted}) / F / Nbits.$$

A. Test Procedure

For the SEE test, we have used an experimental facility of Tohoku University Proton cyclotron (CYRIC). Proton 70MeV beam was extracted through a Ti foil of 20mmϕ and 100μm thickness into air and was impinged to a DUT. The photograph of the experimental setup with the DUT board along the proton beam line is shown in Fig. 4. A target board and a ZnS fluorescence screen were mounted on an X-Y stage. The beam position was first monitored by the fluorescence screen and then the target board was moved to the beam position (The beam was stopped with a final beam stopper during the X-Y stage was moving.). Actual beam profile and beam intensity were measured, individually for each chip with dosimetry of a 100μm thick Cu foil placed in front of the DUT. The beam intensity at the final beam stopper was around 2 - 4nA. The beam was intentionally broadened up to the size of around 20mmϕ.

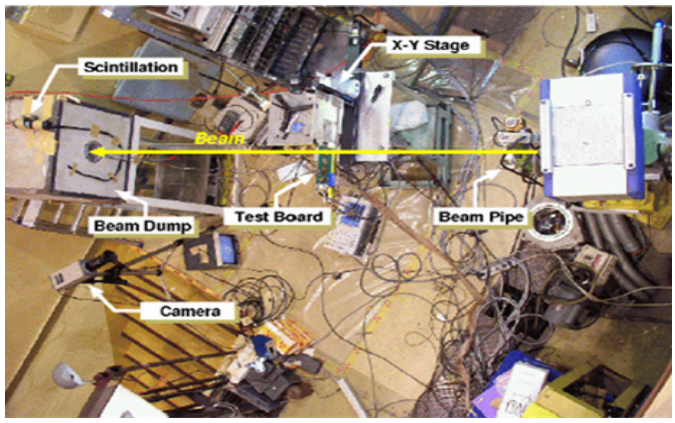

Figure 4: SEE test experiment setup for 70MeV proton beam of Tohoku University Cyclotron

B. Results for LVDS chipsets

The serializer and deserializer were mounted on the identical DUT PC board used in the TID test. We have checked the functionality during the proton irradiation remotely by sending and receiving some bit patterns with the monitor board. We have tested two pairs for each NS and TI candidate. The data taken in the test for two LVDS chipsets are summarized in Table 1.

Table 1: SEE test results for LVDS chipsets of TI and NS. SEU means the number of SEU observed while link failure means the number of link out during irradiation. F is total integrated proton intensity.

Vendor	Chip	SEU	Link failure	F (cm^{-2})
TI	Rx	6	2	$5.4x10^{12}$
	Tx	8	7	$7.6x10^{12}$
NS	Rx	55	36	$2.3x10^{12}$
	Tx	1	5	$3.7x10^{12}$

In Table 1, we have classified the abnormalities observed during the irradiation into two classes. If the monitor board detects different bit pattern rather than the pattern which it has sent, then it is regarded as an SEU (single Event Upset) error. The link failure means that the deserializer could not synchronize its clock with the clock embedded in the data sent, i.e. it could not phase-loop lock the clock with one sent from the serializer. Based on Table 1, we have estimated σ_{SEE} independently with two error categories and listed in Table 2.

Table 2: SEE test results: σ_{SEE} for the chipsets of two different vendors. They were estimated independently for two error categories.

Chip	Vendor	σ_{SEU} (cm^2)	σ_{link} (cm^2)
Tx	NS	$1.3x10^{-13}$	$1.2x10^{-12}$
	TI	$2.5x10^{-12}$	$1.5x10^{-12}$
Rx	NS	$2.0x10^{-13}$	$1.2x10^{-11}$
	TI	$8.0x10^{-13}$	$6.3x10^{-13}$

Since we have about 10000 LVDS link connections in on-detector part, we can estimate 0.6 SEU errors and 0.4 link failures per day regardless of the product vendors.

If, however, we compare time dependence of error incidence of Rx, for example, for both vendors, we find very different characteristics between two vendors as shown in Fig.5. All the samples of NS Rx showed always SEU and link failures uniformly over irradiation period while ones of TI showed seldom SEU and link failures. All TI Rx showed, however, significant increase of the source current after the proton dose of 300Gy up to 1200Gy where all the TI Rx are broken. The increase of the source current has been observed already in the TID test for TI samples as shown in Fig.1.

As far as the SEE test results are concerned, the chipset of both vendors are satisfied with the condition for the criteria issued by the ATLAS radiation working group [7]. TI chipsets has been observed with significantly less number of SEUs and link failures than NS while TI Rx was broken at around 1200Gy irradiation level. For the ATLAS muon endcap electronics, however, as 1200Gy radiation level is beyond the maximum limit for the region we are concerned, we will use TI chipsets eventually in the electronics system.

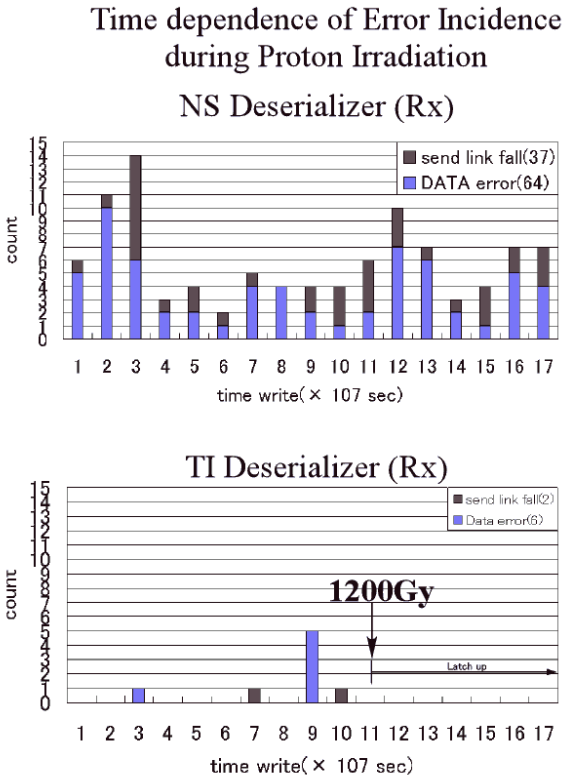

Figure 5: Time dependence of error incidence versus proton irradiation time for deserializer (Rx) chips of NS and TI. TI one was broken after 1200Gy irradiation.

C. *Results for the G-link chipset*

For the G-link chipset, we have also measured data transfer errors and link failures as the similar way to the LVDS test. But in this G-link test, we have made also qualification test of an optical transceiver for the proton irradiation beside Tx and Rx.

We have made the SEE test for the chipset together with the OE/EO transceiver mounting on an identical PC board as used in TID test (as shown in Fig. 2). We have exposed 70MeV proton beam to these chips. (Total two samples for each chip have been tested). In Table 3, we summarized the aggregate sum for number of SEUs detected and number of link-lock failures with the total integrated proton intensity (F) for all three G-link chips.

Table 3: SEE test results for G-link chipset and the optical transceiver. SEU means the number of SEU observed while link failure means the number of link lock failure during irradiation. F is total integrated proton intensity.

Chip	SEU	Link failure	F (cm^{-2})
Tx	4991	77	$2.3x10^{11}$
Rx	2802	162	$2.4x10^{11}$
OE/EO	0	69	$8.1x10^{11}$

All the 77 link failures observed in Tx synchronization were recovered autonomously. The recovery time was 8us in average, and it never exceeded 10us as longest. Three link failures out of total 162 link failures observed in Rx were failed to re-lock autonomously but recovered using self-recovery method installed in Rx chip. In this case the recovery for phase loop lock takes 38.4us.

We have estimated separately the cross sections σ_{SEE} for SEU and link failure and summarized them in Table 4.

Table 4: G-link SEE test results: σ_{SEE} for the chipsets of two different vendors. is estimated independently with two error classification.

Chip	σ_{SEU} (cm^2)	σ_{link} (cm^2)
Tx	$2.2x10^{-8}$	$3.3x10^{-10}$
Rx	$1.2x10^{-8}$	$6.7x10^{-10}$
OE/EO	$8.6x10^{-11}$	$< 3.010^{-12}$

Estimated SEE error rates in the whole ATLAS muon endcap electronics system for various G-link categories are summarized in Table 5.

Table 5: Estimated error rate caused by SEE for three different usages of G-link connection.

Category	Number of links	Duty	SEU rate	Link failure rate
Trigger	1000	100%	0.19/min.	0.17/hr.
Readout	200	10%	0.23/hr.	0.1/day
Control	28 (2-ways)	1%	0.1/day	

IV. SUMMARY

In summary, we have found very different characteristics of two type of LVDS chipsets (NS and TI) in the data analysis of both the γ-ray (for TID) and proton irradiation (for SEE) tests. The NS one has many SEU or link failure but immune to TID while TI has relatively qualified for SEE if the proton dose is less than 1200Gy, but is fragile for the absorbed dose greater than 80krad, although both chipsets has no problem to be used anyway in the ATLAS muon endcap level-1 system because the total dose estimated with 10 years would be at most 300Gy. The G-link chipset has shown also no problem for our usage.

V. REFERENCES

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