

The ATLAS Level-1 Central Trigger Processor Core Module (CTP_CORE)

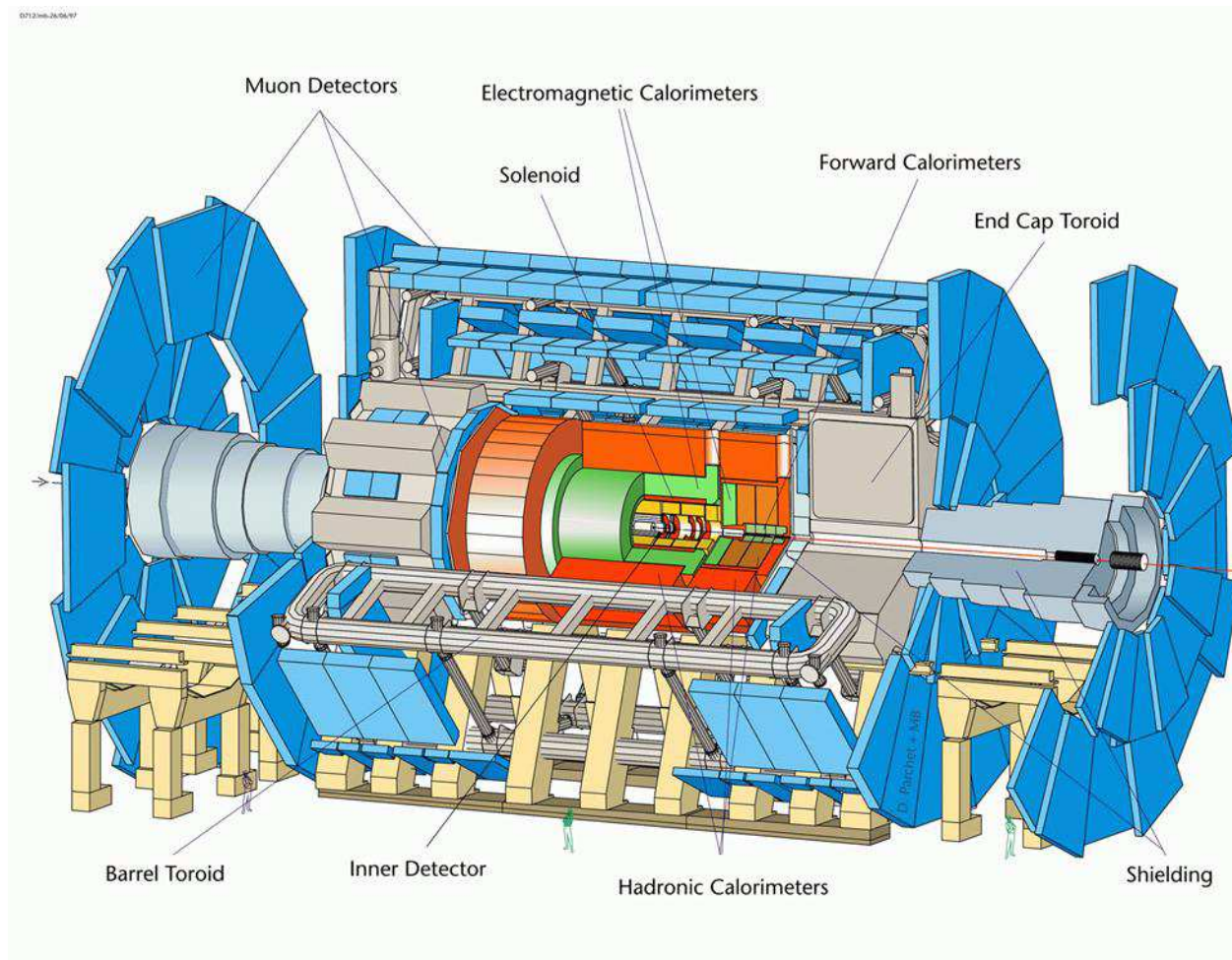
- **Introduction**
- **Central Trigger Processor (CTP)**
- **Core Module (CTP_CORE)**
- **Testbeam Results**

On behalf of

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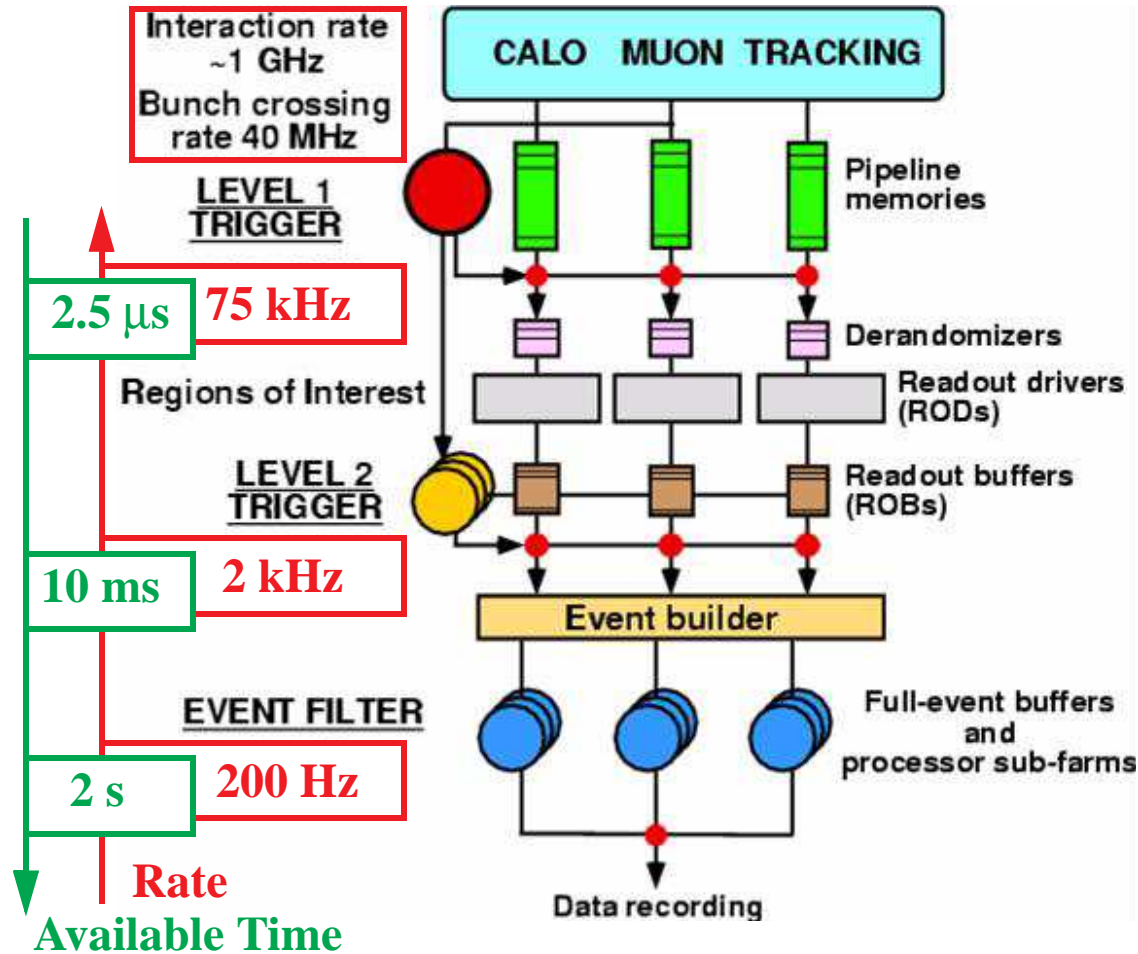
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The ATLAS Experiment



General-purpose Experiment at CERN's **Large Hadron Collider (LHC)**:
Proton-Proton collisions at 14 TeV centre-of-mass energy.
About 25 collisions per bunch crossing (**BC**) every 25 ns (40 MHz)
⇒ **Interaction rate of 1 GHz.**

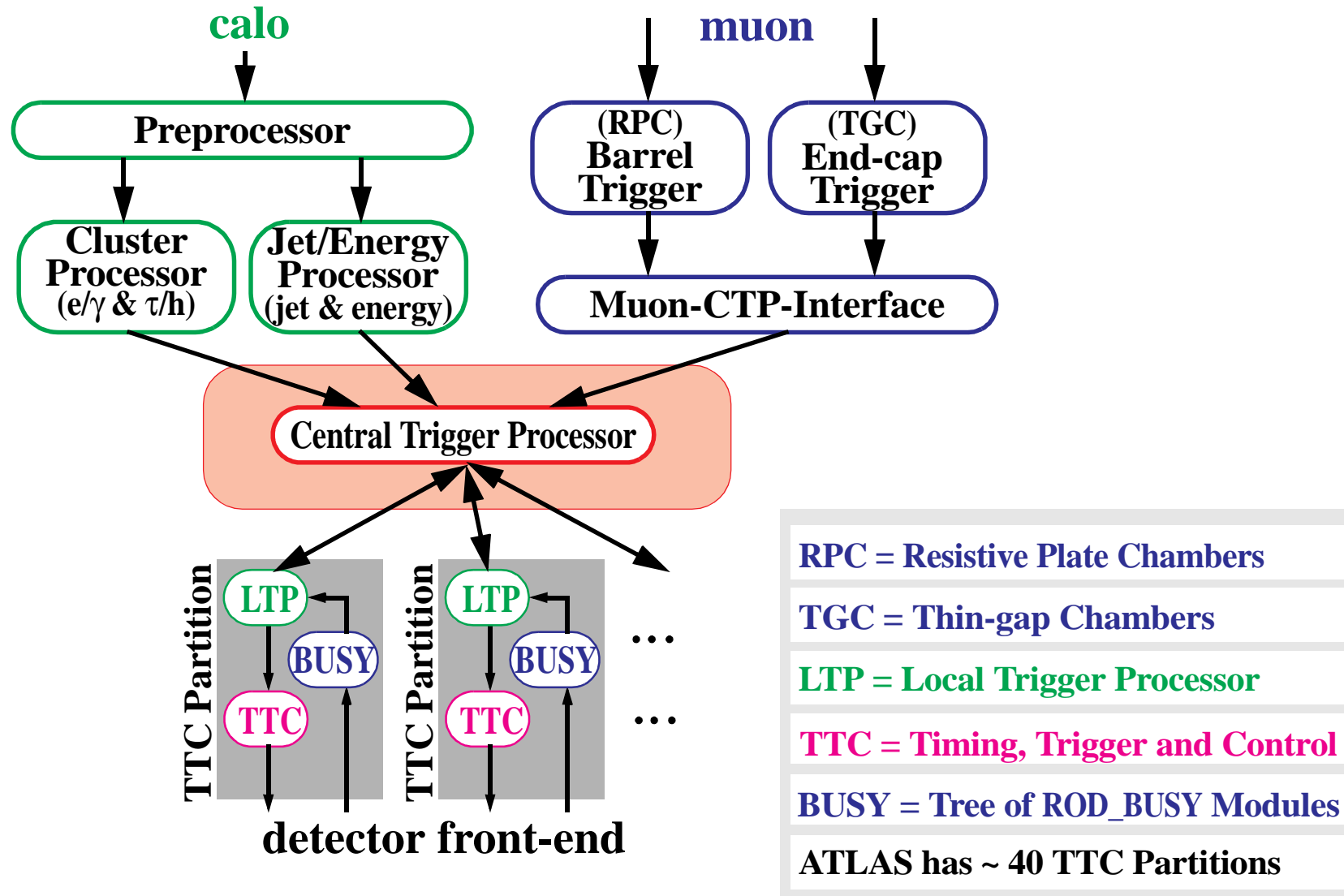
The Trigger/DAQ System



Level-1 Trigger:
Electronics + Firmware

Level-2 Trigger + Event Filter:
Computers + Networks + Software

The Level-1 Trigger System



See Poster N33-103 on the ATLAS Level-1 Central Trigger System.
 See Poster N33-104 on the ATLAS Local Trigger Processor.

The Central Trigger Processor (1)

- Trigger Input:

- **Multiplicities** from Calorimeter and Muon Triggers:
electrons/photons, taus/hadrons, jets, and muons;

- **Energy flags** from Calorimeter Trigger:
 ΣE_T , E_T^{miss} , ΣE_T^{jet}

- **Calibration requests** from sub-detectors.

- Other **specialized triggers**: scintillators, beam pick-ups, etc.

⇒ Up to a total number of **160 trigger inputs** at any one time.

Plus **internal triggers** from CTP core module:

random triggers, prescaled clock, bunch crossing groups.

The Central Trigger Processor (2)

- Level-1 Accept (L1A)

- Derived from trigger inputs according to **trigger menu**:

- Up to **256 trigger items** are made from combinations of conditions on the trigger inputs, e.g.

- 1EM10** \equiv at least one electron/photon with $E_T \geq 10$ GeV

- 1MU6** \equiv at least one muon with $p_T \geq 10$ GeV/c

- XE20** \equiv missing energy of at least 20 GeV

- Each trigger item has a mask, a priority¹ and a prescaling factor.
¹ for dead-time (see later, CTP Core Module)

- L1A is the OR of all trigger items.

- An example of a trigger menu might contain

- 1MU6** mask = ON, priority = LOW, prescaling = 1000

- 2MU6** mask = ON, priority = HIGH, prescaling = 1

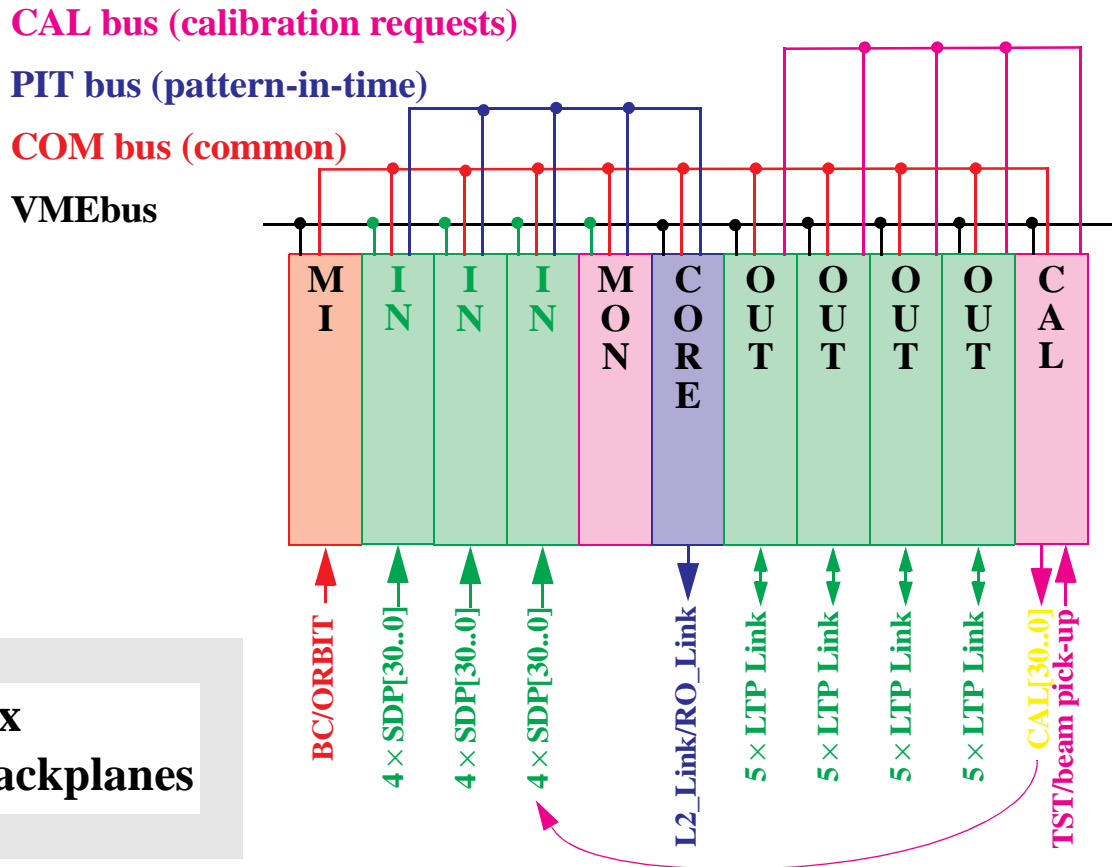
- 1EM20 AND XE20** mask = ON, priority = LOW, prescaling = 1

- ...

The Central Trigger Processor (3)

- **Additional Functionality:**
 - **Trigger type** word (8 bits) accompanying every L1A.
 - **Dead-time** in order to prevent front-end buffers becoming full (see later, CTP Core Module).
 - **Region-of-Interest (RoI)** for the Level-2 Trigger and **event data** for the **Read-out System (ROS)** and for **monitoring**.
 - **Timing signals**, e.g Event Counter Reset (ECR), ...
- **Constraints:**
 - **Trigger latency target, i.e. from trigger input to L1A:**
100 ns \equiv 4 BC.
 - **Trigger menu changes with physics/beam/detector conditions.**

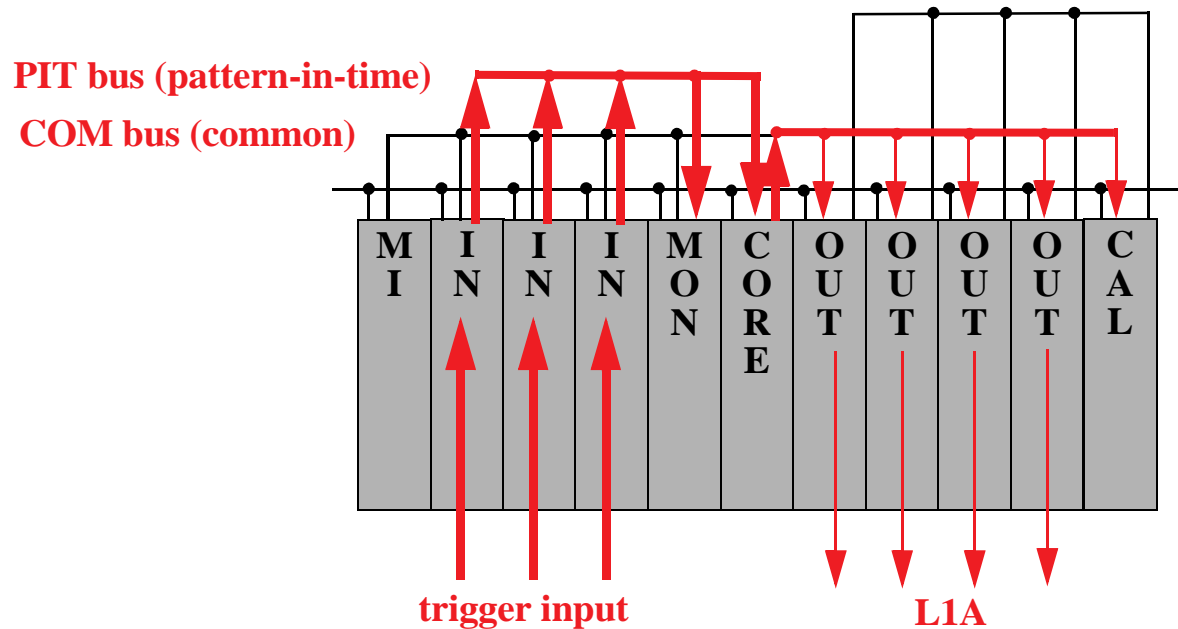
CTP - The Design



9U VME64x
+ custom backplanes

CTP_MI	(Machine Interface)	Timing
CTP_IN	(Input Module)	Trigger input
CTP_MON	(Monitoring Module)	Bunch-to-bunch monitoring
CTP_CORE	(Core Module)	Trigger menu + Readout
CTP_OUT	(Output Module)	Trigger fan-out
CTP_CAL	(Calibration Module)	Sub-detector calibration requests

CTP - The Trigger Path

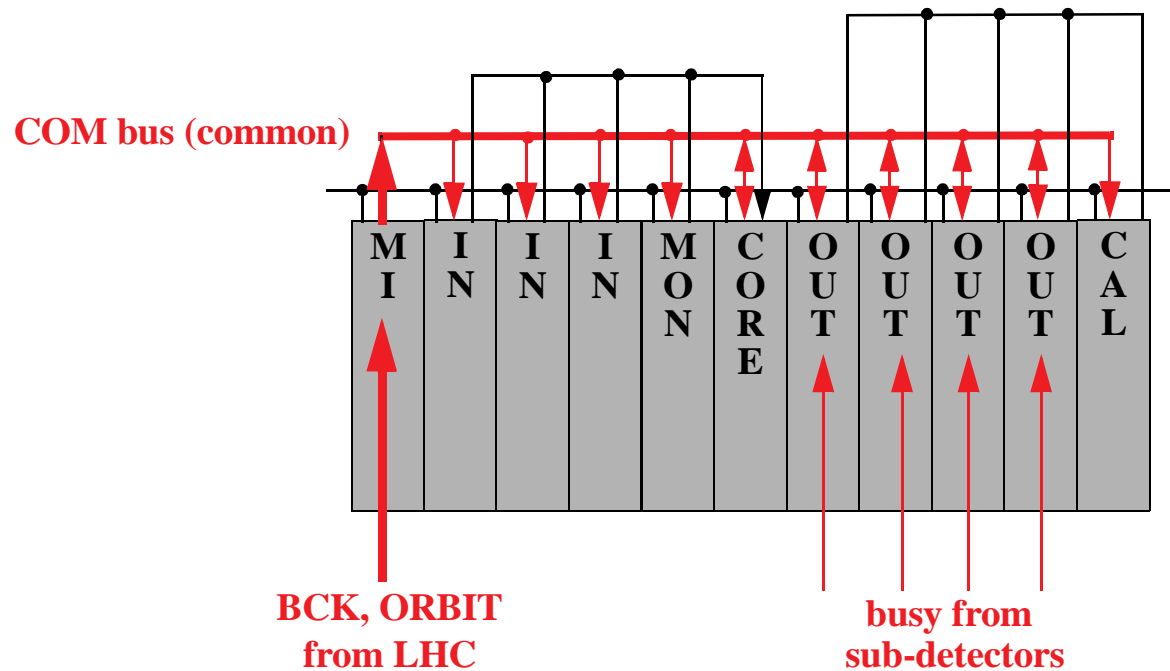


CTP_IN modules receive, synchronize and align the trigger inputs, and route them to the PIT bus (Pattern-in-time).

CTP_CORE module receives and synchronizes the PITs, compares with trigger menu and generates Level-1 Accept (L1A), sends L1A to the COM bus.

CTP_OUT receives L1A from the COM bus and fans it out to sub-detector LTPs.

CTP - The Timing Path

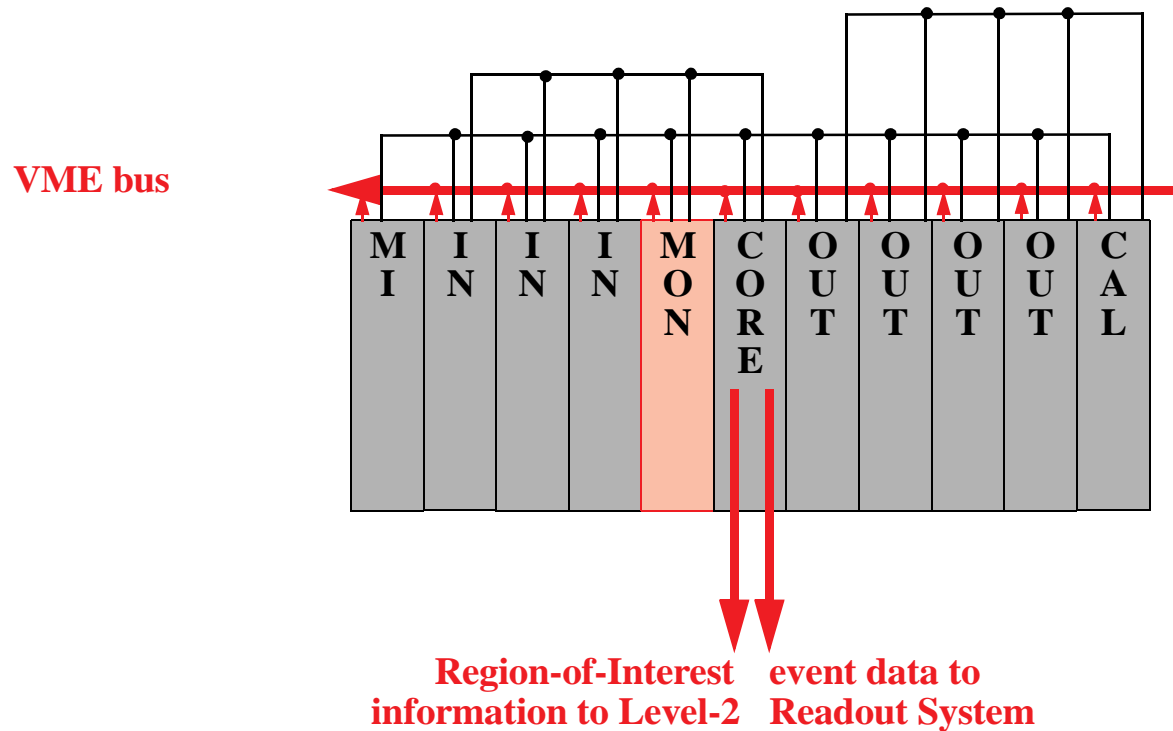


CTP_MI module receives timing signals from LHC, generates additional timing signals and sends all to the COM bus.

CTP_OUT modules receive busy signals from sub-detector LTPs and send them to the COM bus.

All CTP modules receive timing signals from the COM bus.

CTP - The Readout & Monitoring



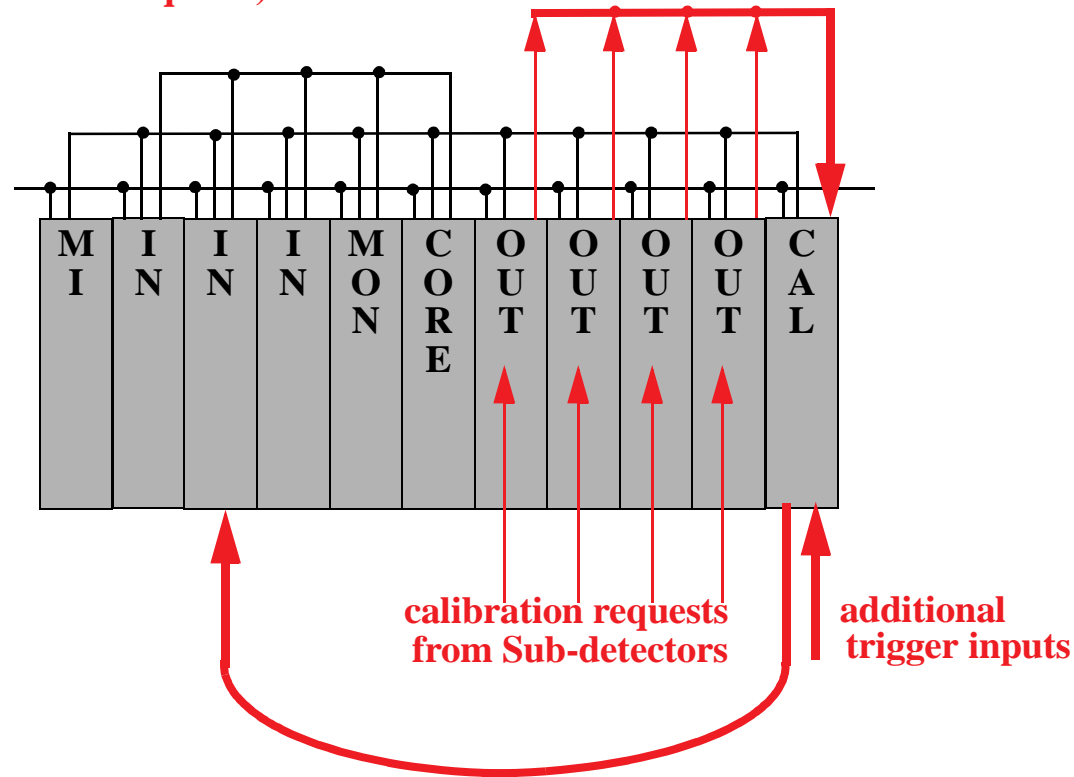
CTP_CORE module sends Region-of-Interest (RoI) information to the Level-2 Trigger and event data to the Readout System.

CTP_MON produces a bunch-by-bunch histogram of signals from the PIT bus.

All CTP modules provide monitoring data to the VMEbus.

CTP - The Calibration Requests

CAL bus (calibration requests)



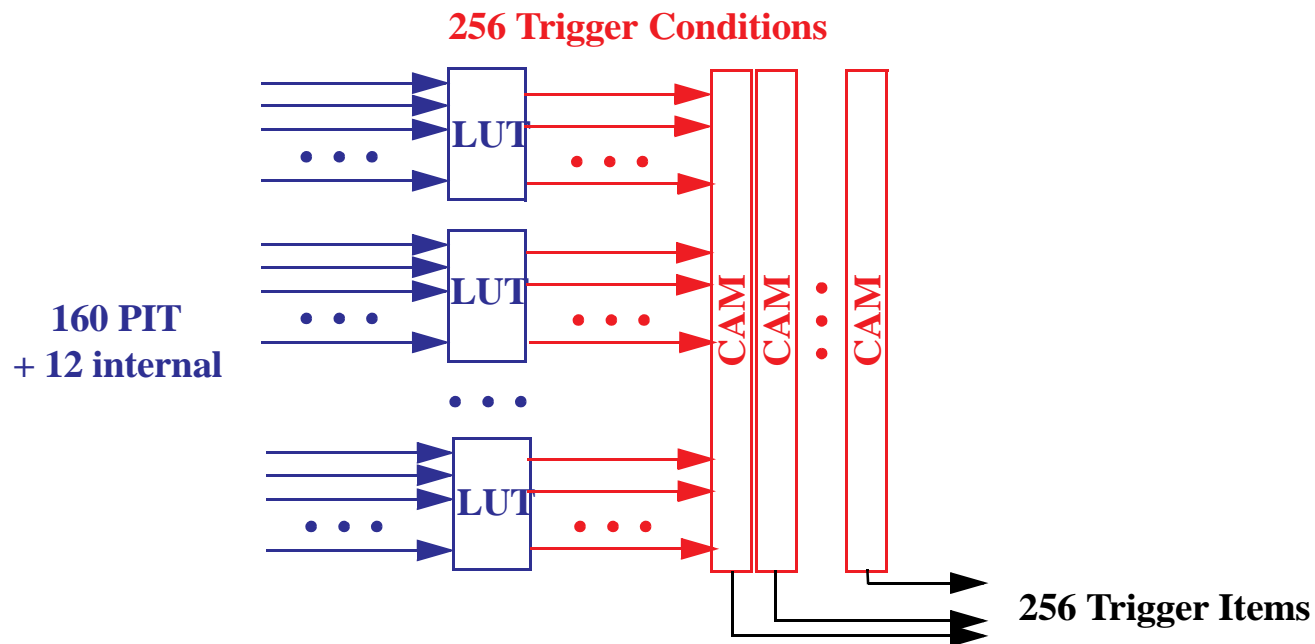
CTP_OUT modules receive calibration requests from sub-detector LTPs and send them to the CAL bus.

CTP_CAL time-multiplexes calibration requests, receives additional trigger inputs and sends all to a CTP_IN module.

The CTP Core Module (1)

- Trigger Combinations:

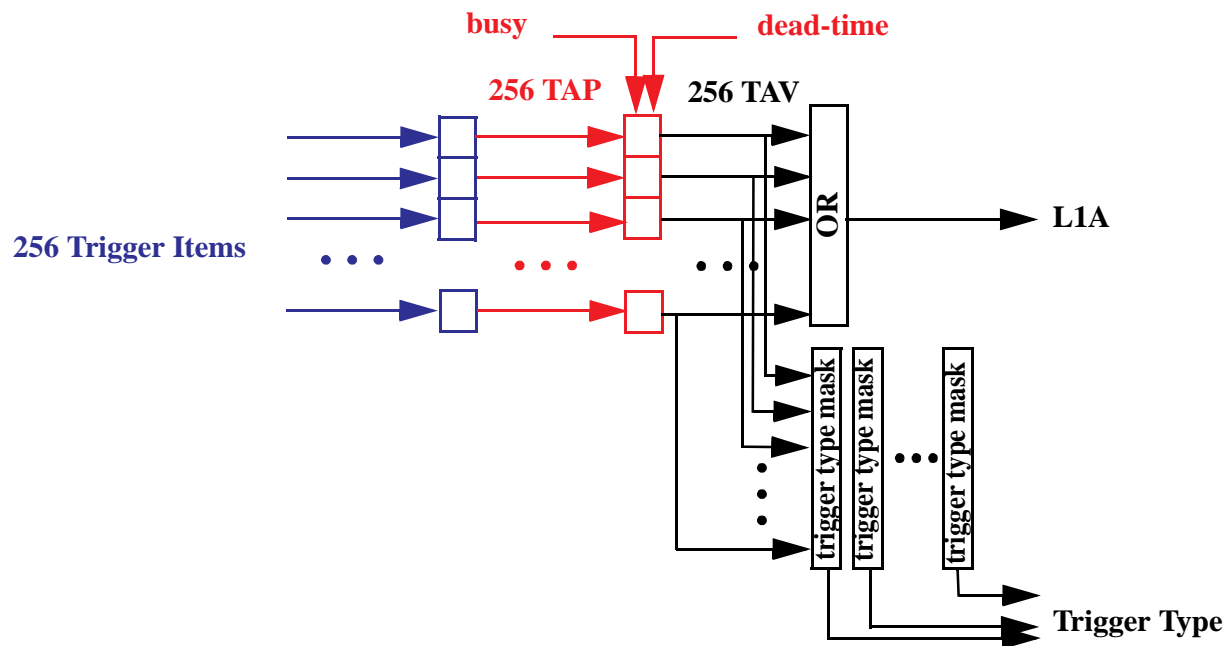
Combinations of signals from the PIT bus + internal to CTP_CORE using Look-up Tables (LUT) for trigger conditions, and Content-addressable Memories (CAM) for combinations of trigger conditions. Each CAM contains a 256-bit word and is ternary, i.e. allows bitwise matching of “0”, “1” or “don’t care”.



Implemented using Xilinx Virtex II Pro (XC2VP50).

The CTP Core Module (2)

- Prescaling and Masking:
 - Prescale: programmable 24-bit down-counter
⇒ 256 TAP (Trigger items after Prescaling).
 - Mask: programmable mask + dead-time + busy
⇒ 256 TAV (Trigger items after Veto).
 - OR: over all 256 TAVs
⇒ 1 L1A (Level-1 Accept).
 - Generate 8-bit trigger type using eight 256-bit masks.



Implemented using Altera Stratix (EP1S60).

The CTP Core Module (3)

- Dead-time:

- Simple deadtime:**

- Constant time after each L1A:

- No L1As for n BCs after each L1A.*

- Current baseline (programmable): $n = 4$.**

- Complex deadtime:**

- Leaky-bucket algorithm:

- Not more than n L1As in m BCs.*

- Current baseline (programmable): 8 L1As in 80 μ s.**

- \Rightarrow Two leaky-bucket algorithms are used,
associated to the priority of each trigger item (high/low).

- Implemented using same FPGA as for Prescaling and Masking.

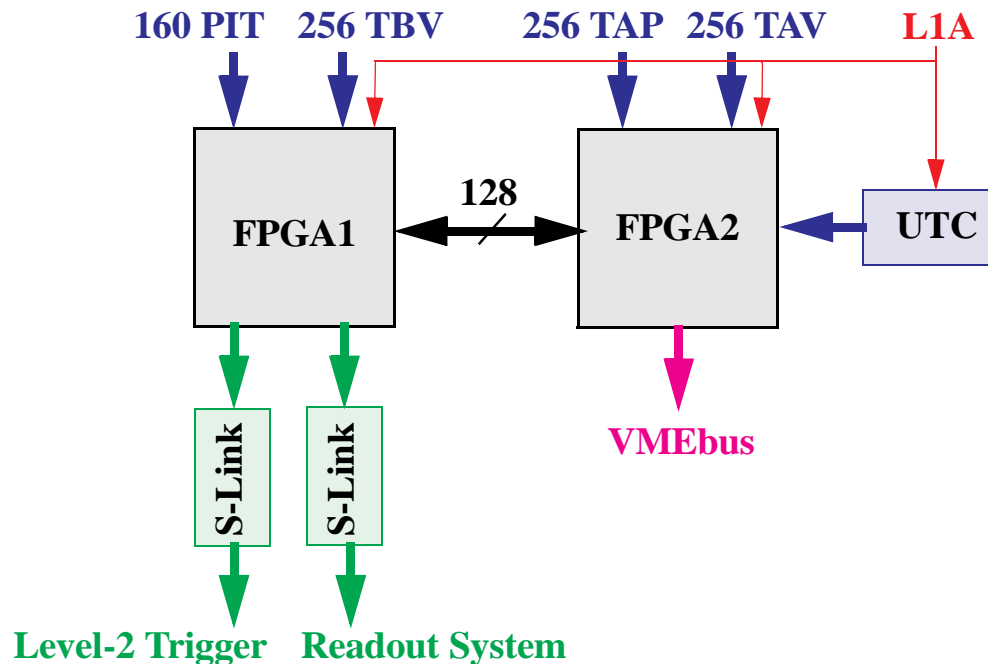
The CTP Core Module (4)

- Readout & Monitoring:

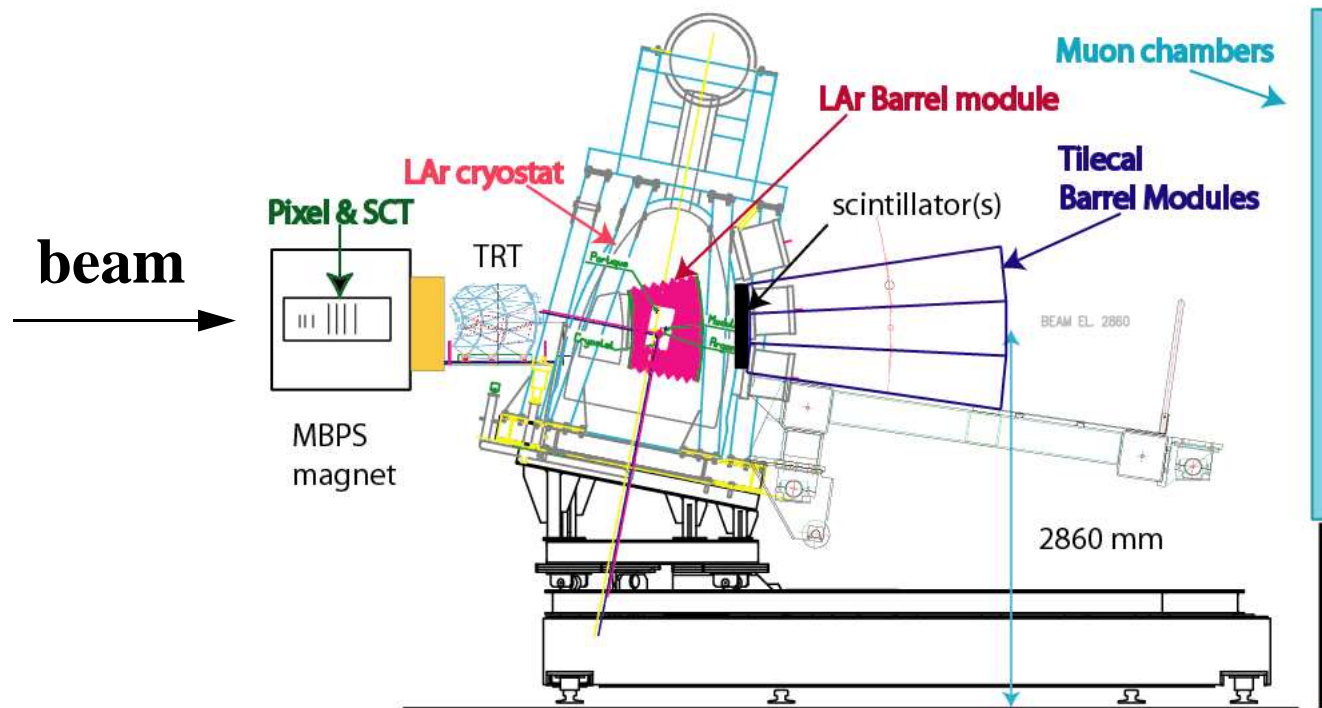
- Copied into FIFOs at every L1A:**

- 160 Signals from the **PIT** bus + 12 internal triggers;
 - 256 Trigger items before prescaling (**TBP**);
 - 256 Trigger items after prescaling (**TAP**);
 - 256 Trigger items after veto (**TAV**);
 - 64-bit UTC time-stamp (linked to GPS) with 5-ns jitter.

Implemented in two Altera Stratix (EP1S60) with 128 signals for data exchange between them (firmware to be written):

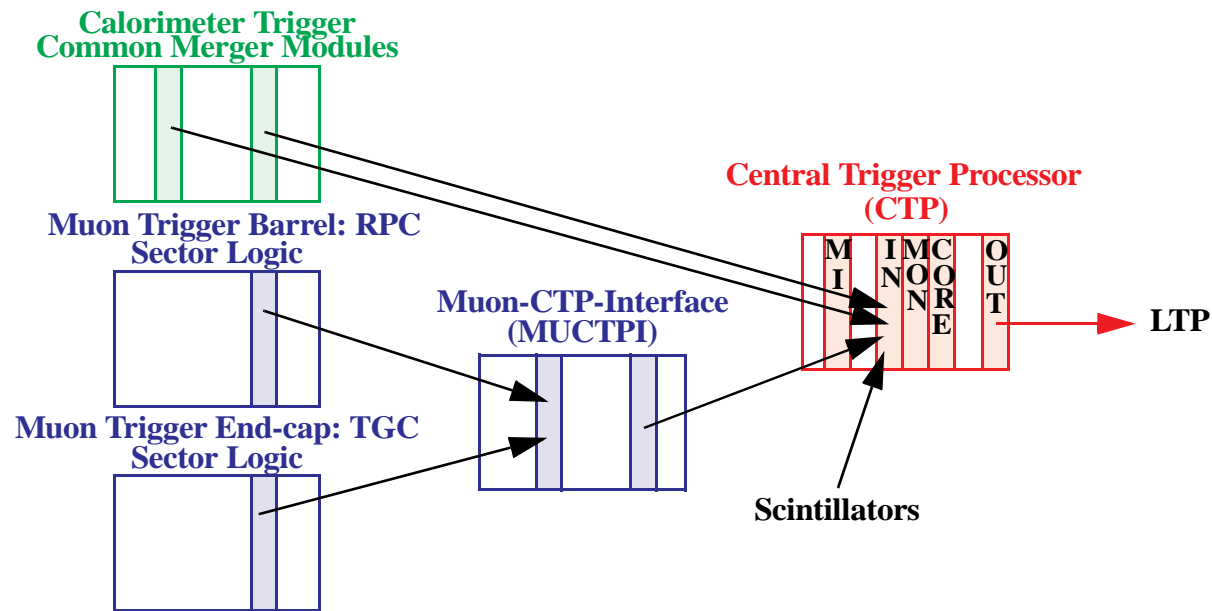


The ATLAS Combined Testbeam



Test beam programme during 2004
for prototypes and final modules
of all ATLAS sub-detectors and trigger and data acquisition.

The Level-1 Trigger at the Combined Testbeam



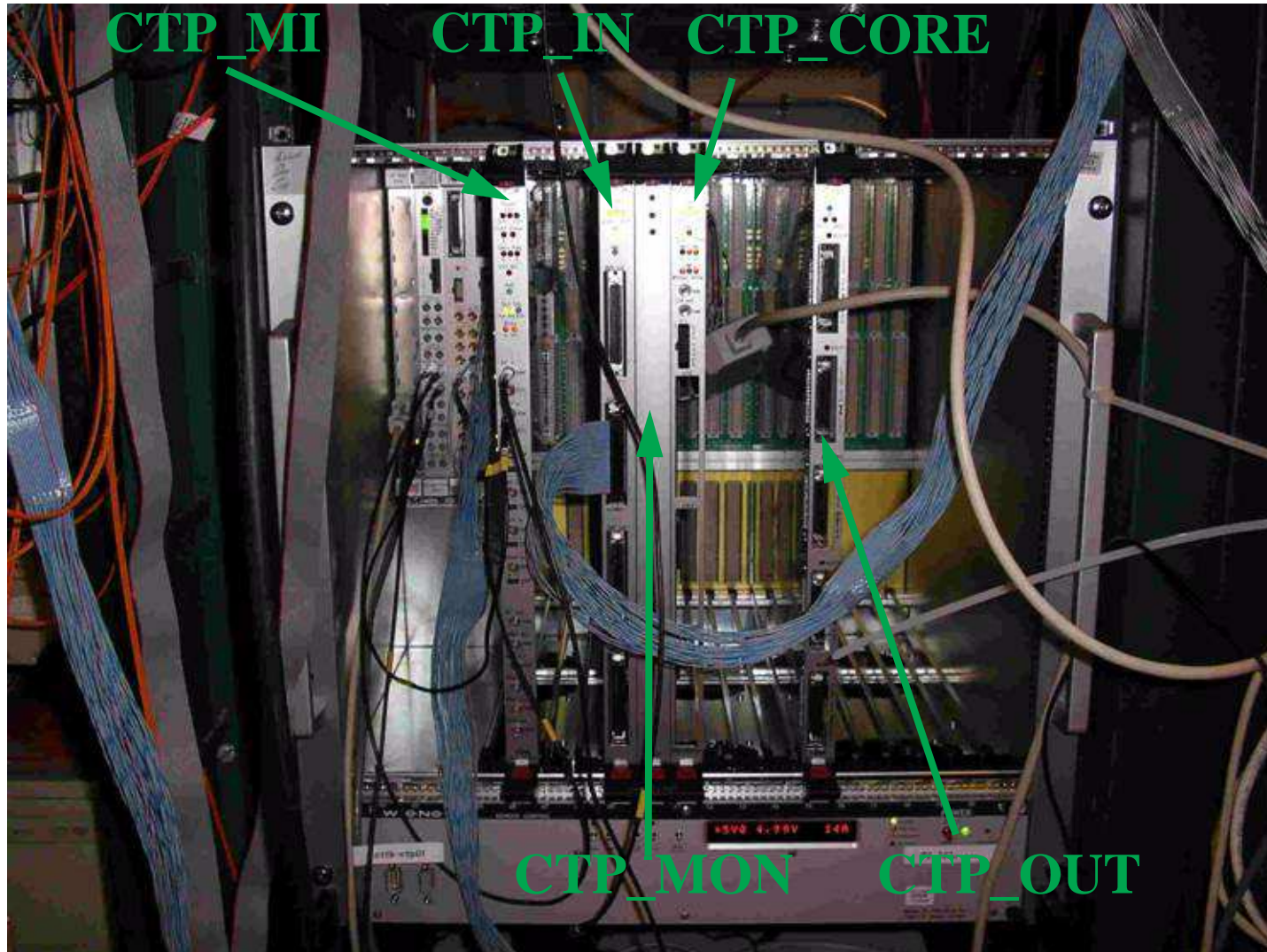
Trigger Input:

Calorimeter Trigger: 4×3 bit e/γ + 4×3 bit jet multiplicities + 1 bit total E_T ,
Muon Trigger: 6×3 bit muon multiplicities,
Scintillators: 3×1 bit scintillators.

CTP:

1 CTP_MI,
1 CTP_IN (out of up to 3),
1 CTP_CORE,
1 CTP_OUT (out of up to 4),
1 CTP_MON.

The CTP at the Combined Testbeam



CTP - Some Results

- Trigger Generation:

51 signals from PIT bus used to form 18 trigger items.
Prescaling and masking tested to work correctly.

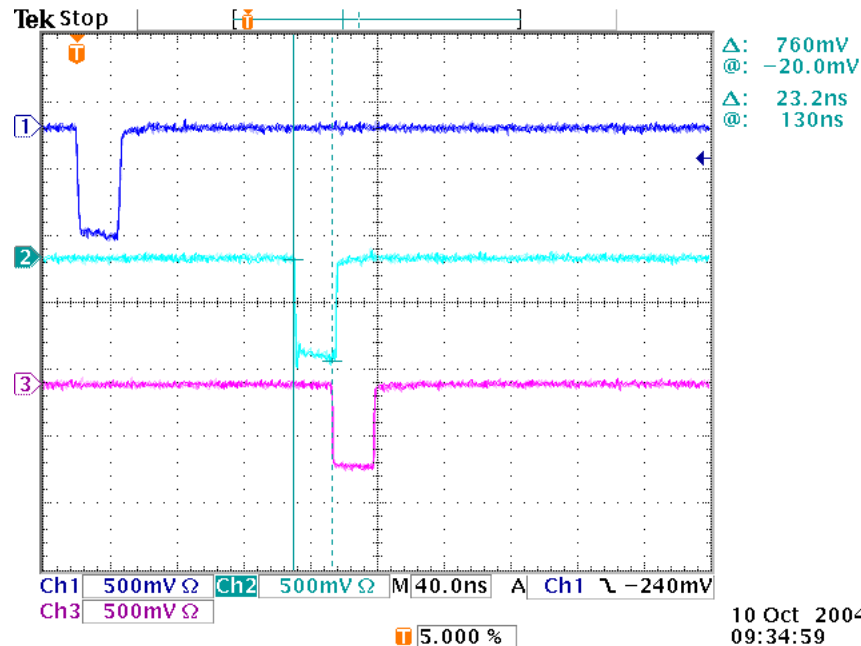
L1A used as trigger for readout of the combined sub-detectors.

- Latency Measurement (preliminary!):

Scintillator Trigger

L1A at CTP_CORE

L1A at LTP



Scintillator Trigger → L1A at CTP_CORE ≈ 130 ns.

**But some cable delays not taken into account and
CTP timing not yet optimised.**

Conclusion

CTP_CORE has been used during testbeam to generate trigger using 51 trigger inputs and 18 trigger items.

CTP latency is already close to the target of 100 ns.

**Work on the CTP will continue in laboratory,
e.g. CTP_CORE readout and corrections to firmware
which were identified during the testbeam.**

CTP will be available for ATLAS commissioning next year.