The ATLAS Level-1 Central Trigger System

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Abstract

The central part of the ATLAS Level-1 trigger system consists of the Central Trigger Processor (CTP), the Local Trigger Processors (LTPs), the Timing, Trigger and Control (TTC) system, and the Read-out Driver Busy (ROD_BUSY) modules. The CTP combines information from calorimeter and muon trigger processors, as well as from other sources and makes the final Level-1 Accept decision (L1A) on the basis of lists of selection criteria, implemented as a trigger menu. Timing and trigger signals are fanned out to about 40 LTPs which inject them into the sub-detector TTC partitions. The LTPs also support stand-alone running and can generate all necessary signals from memory. The TTC partitions fan out the timing and trigger signals to the sub-detector front-end electronics. The ROD_BUSY modules receive busy signals from the front-end electronics and send them to the CTP (via an LTP) to throttle the generation of L1As. An overview of the ATLAS Level-1 Central trigger system will be presented, with emphasis on the design and tests of the CTP modules.

I. The Central Trigger System

The ATLAS Level-1 trigger [1] is a synchronous system operating at the bunch crossing (BC) frequency (40.08 MHz) of the LHC (Large Hadron Collider) accelerator. It uses information on clusters and global energy in the calorimeters and from tracks found in dedicated muon trigger detectors. An overview of the ATLAS Level-1 trigger is shown in Fig. 1.

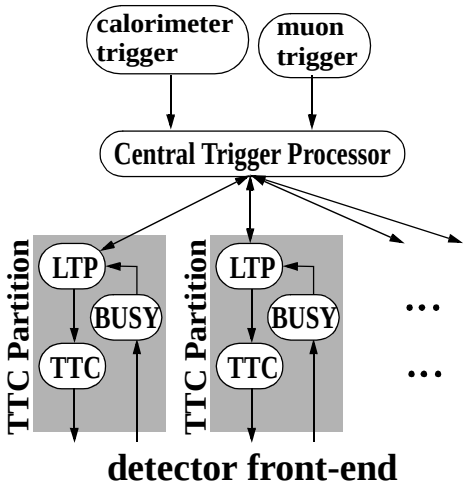

Figure 1: Overview of the ATLAS level-1 trigger

The central trigger system consists of the CTP and the TTC partitions.

The CTP itself forms the Level-1 Decision (accept or not) every 25 ns, and distributes it to the TTC partitions. It also receives the timing signals from the LHC and fans them out to the TTC partitions.

The TTC partitions perform the distribution of the Timing, Trigger and Control signals to all sub-detector front-end electronics. In the ATLAS experiment there are about 40 TTC partitions. Each contains one Local Trigger Processor (LTP) [2][3], a TTC system proper [4][5], and a busy tree. The TTC system proper encodes the signals receivd from the CTP, converts them into optical signals and fans them out to the detector front-end electronics, where they are recovered by a dedicated ASIC chip. The busy tree is a fast feed-back tree for the front-end electronics to throttle the generation of L1As. It is based on the ATLAS ROD_BUSY module [6].

On October 2004, the system will be tested at CERN in a combined test-beam with 25 ns bunch structure.

II. Overview of the Central Trigger Processor

The CTP has many functions that can be divided into three groups: it synchronizes and aligns in time trigger information coming from different sources; it forms the Level-1 trigger decision and distributes it to the TTC partitions; it provides readout data to, and is controlled by the Data Acquisition system.

A. Trigger inputs

The CTP receives information from the calorimeter and muon trigger processors. The trigger information consists of multiplicities for electrons/photons, taus/hadrons, jets, and muons, and of threshold flags for total transverse energy, total missing energy, and total jet transverse energy. Other external inputs such as beam-pickup signals, cosmic rays triggers, minimum bias and luminosity triggers, will also be used. A total of 160 external input bits can be taken into account by the CTP at any given time. The total number of available input bits can be higher because of selection at the input to the CTP. Finally, the CTP provides internal triggers from random generators, for bunch-crossing groups, and pre-scaled clocks. The CTP first has to synchronize and align all these inputs coming from different sources so that the subsequent processing stage sees all

of the selected data coming from the same BC.

B. Trigger Formation

The CTP generates a L1A derived from the trigger inputs according to the Level-1 trigger menu, which describes the Level-1 Physics selection. It consists of up to 256 trigger items, each of which is a combination of one or more conditions on any of the trigger inputs. For example, “At least one Muon with transverse momentum greater than 10 GeV AND missing transverse energy greater than 20 GeV AND a filled bunch (as obtained from the beam pickups)”. Each trigger item also has a mask, a priority for the dead-time generated by the CTP (see Section III.D) and a pre-scaling factor. The L1A is the logical OR of all (masked and prescaled) trigger items.

The rate of L1A is limited by introducing dead-time, according to two algorithms. This limits the rate of L1A up to a maximum of 75-100 KHz, that the front-end electronics should be able to sustain. The CTP also receives the busy signals from the sub-detectors to throttle the L1A generation, so that further L1As are inhibited until the busy condition set by the sub-detectors is cleared.

The CTP not only generates the L1A but also provides with each L1A an 8-bit trigger type summary word which indicates the type of trigger and which can be used to steer event data processing in the detector front-end electronics. The CTP provides an event counter reset (ECR) signal.

The formation of the trigger is required to be performed within four bunch crossings from input to the CTP until output of the L1A out of the CTP. This corresponds to a latency budget of 100 ns, out of a total Level-1 latency of less than 2.5 μs. The Level-1 trigger menu used for the trigger formation is likely to change frequently depending on the physics, beam and detector conditions. Hence it must be easy to reload a new trigger menu into the CTP.

C. Data Acquisition

The CTP sends, at every L1A, Region-of-Interest (RoI) information to the Region-of-Interest Builder (RoIB) of the Level-2 trigger system for guidance of the Level-2 trigger algorithms. The CTP further sends, at every L1A, information to the Read-Out System (ROS) of the data acquisition system. The CTP also provides monitoring data, to be read out via VMEbus: snapshots of incoming data, bunch-by-bunch monitoring of inputs, and scalers of trigger inputs and trigger items before and after pre-scaling integrated over all bunches.

The CTP and the LTPs as well as the TTC system and ROD_BUSY modules are configured, controlled and monitored by the ATLAS Online System [7][8]. This is performed via single-board computers that communicate with the modules via VMEbuses.

III. Design and Status of the CTP

An overview of the design of the CTP is shown in Figure 2.

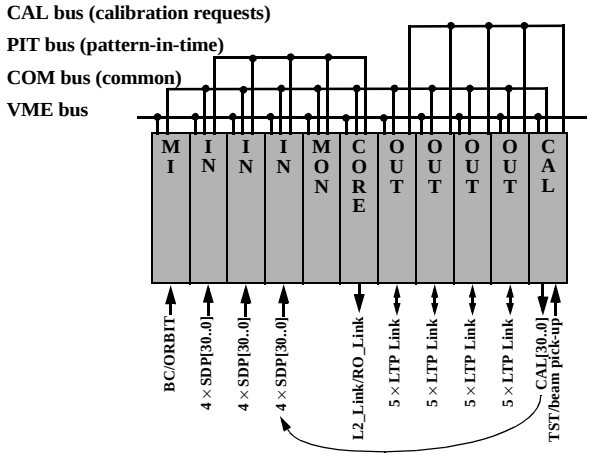

Figure 2: CTP design with its modules, backplanes, and signals

The CTP consists of a machine interface module for timing (CTP_MI), up to three input modules (CTP_IN), a bunch-by-bunch monitoring module (CTP_MON), a core module for trigger formation and read-out (CTP_CORE), up to four output modules connecting to the LTPs (CTP_OUT), and a module to handle calibration requests from the sub-detectors (CTP_CAL).

The CTP modules are housed in a 9U VME64x crate. In addition to the standard VMEbus, the CTP modules also use dedicated buses for synchronized and aligned trigger inputs (PITbus, PIT = pattern in time), for the common timing and trigger signals (COMbus), and for the calibration requests from the sub-detectors (CALbus). For further information on the CTP design, see Ref. [9].

A. The CTP backplanes

The CTP uses two dedicated backplanes, which are shown in Fig. 3.

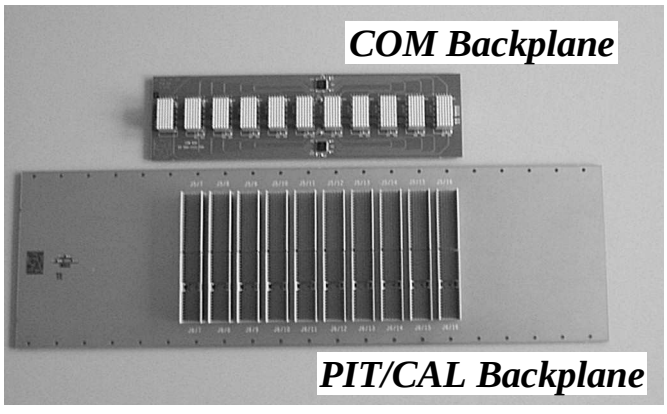

Figure 3: CTP backplanes

One backplane contains both the PITbus and the CALbus, since they do not overlap. The PITbus carries the synchronized and aligned trigger inputs from up to three CTP_IN modules to the CTP_MON and the CTP_CORE modules. The PITbus contains 160 signals, and extends over only five VMEbus slots. Hence it was implemented as a single-ended, multi-drop,

SSTL-2 like bus. It is terminated at the destination, namely the (parallel) resistances of the CTP_MON and CTP_CORE modules. The CALbus carries the calibration requests from up to four CTP_OUT modules to the CTP_CAL module. The CALbus contains 64 signals, extending over five VMEbus slots and was implemented as point-to-point LVDS. The PIT/CAL backplane is a four layers, impedance controlled PCB, mounted in the position of the J5/J6 connectors.

The other backplane contains the COMbus. The COMbus carries the timing signals, i.e. bunch crossing clock (BC) and LHC orbit (ORBIT), the trigger signals, i.e. L1A, the trigger type and the busy signal. It also carries the control signals, i.e. event counter reset (ECR), synchronization signal (SYN) and calibration pre-pulse. The COMbus extends over all eleven CTP modules, except for L1A, trigger type and pre-pulse which only go from the CTP_CORE module to all CTP_OUT modules and the CTP_CAL module. For the timing signals (BC, ORBIT, SYN, ECR) a differential LVPECL point-to-point differential fan-out is used from the CTP_MI to all other modules. The trigger signals (L1A, trigger type, pre-pulse), are distributed from the CTP_CORE using a multi-drop differential LVPECL bus, terminated at a single location, at the end of the backplane. Finally, the busy signal is the wired-OR signal of the individual busy signals of all CTP modules. The busy bus was implemented as multipoint-LVDS, terminated on the backplane. The COM backplane is a nine layer, impedance-controlled PCB and is mounted at the back of the J0 connector.

Both backplanes have been successfully manufactured and tested, after careful pre-layout simulation of the signals propagation and integrity.

B. CTP_MI Module

The CTP_MI [10] is the timing module of the CTP: it receives the timing signals (BC, ORBIT) from the LHC via the TTC-mi or generates them locally. It also generates the ECR and SYN control signals. Both the timing and control signals are sent to the COMbus, to be distributed to the other modules. The CTP_MI also receives, monitors and masks the busy signals that may be received from the subdetectors, other external inputs or internally generated. The block diagram of the CTP_MI module is shown in Fig. 4.

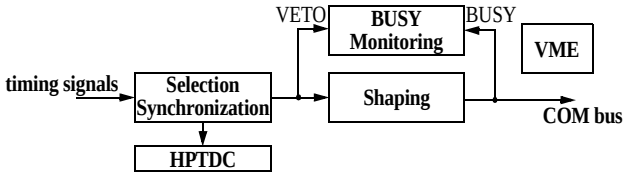

Figure 4: Block diagram of the CTP_MI module

The CTP_MI module is based on FPGAs (ALTERA Cyclone) and the CERN high-performance TDC (HPTDC) [11] for phase measurement. The module shown in Figure 5 was tested successfully.

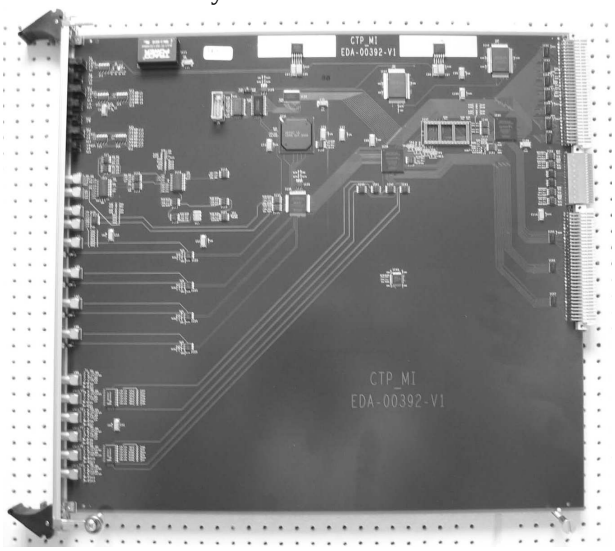

Figure 5: Photograph of the CTP_MI module

C. CTP_IN Module

The block diagram of the CTP input module (CTP_IN) is shown in Fig. 6.

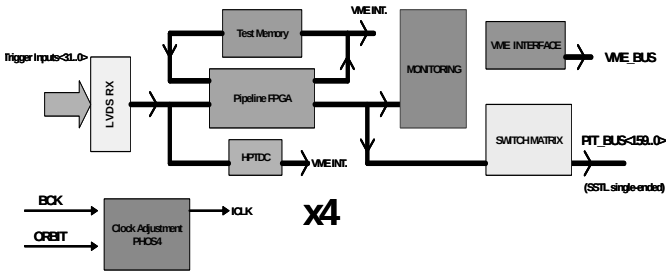

Figure 6: Block diagram of the CTP_IN module

The CTP_IN module [12] receives trigger inputs from the trigger processors, i.e. the calorimeter and muon trigger processors or other sources. The link between the muon and calorimeter trigger processors and the CTP_IN is implemented in LVDS. Each module can receive up to 4x31 trigger inputs, for a total of 372 trigger inputs, if all three CTP_IN modules are used. In the pipeline block of each CTP_IN, each of the trigger inputs is synchronized with respect to the internal clock, the parity is checked, and the data are aligned with respect to the bunch-crossing identifier (BCID). The alignment delay of each input is programmable via VME, from 1 to 63 BC clock cycles. The CTP_IN module then selects and routes 160 trigger inputs to be sent to the PITbus, via a switch matrix. It can store a snapshot of the trigger inputs in a test memory or provide trigger inputs from the test memory. The test memory has a capacity to store or emulate trigger inputs for 18 LHC orbits. Finally, the CTP_IN module also monitors the trigger inputs using scalers that integrate over all bunches.

The CTP_IN module is based on ALTERA Stratix FPGAs for the pipeline block, (Cypress) dual-port memory for the test memory, XPLD (Lattice) for the switch matrix, as well as on a CERN High-performance TDC (HPTDC) [11] for the phase measurement of the trigger inputs. The monitoring block is

implemented with an Altera Cyclone FPGA. A first prototype of the CTP_IN, shown in Fig. 7 has been designed, manufactured and tested.

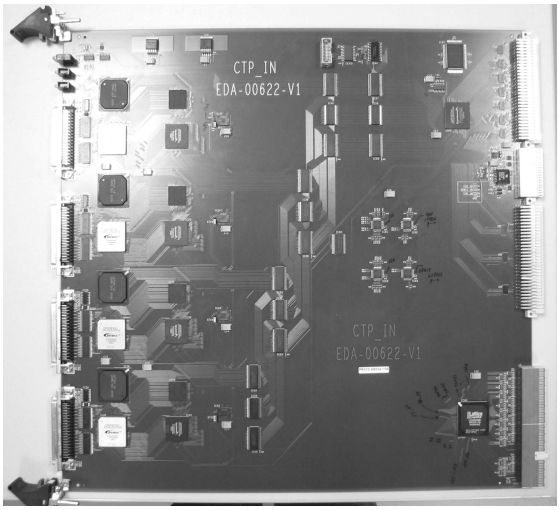

Figure 7: Photograph of the CTP_IN module

D. CTP_CORE Module

The CTP_CORE module [13] receives and synchronizes the 160 trigger *inputs* from the PITbus, coming from the CTP_IN modules. It combines these with additional internal triggers in a Look-Up-Table (LUT) to form 256 trigger *conditions*. This LUT mapping is necessary to decode the incoming multiplicities and energy flags, while allowing for maximum flexibility in the mapping. The trigger conditions are then mapped onto 256 trigger *items* (i.e., the trigger menu) using a ternary Content-Addressable-Memory (CAM). With the CAM implementation, each trigger item can be a combination of any of the 256 trigger conditions, while respecting the latency budget. Moreover, the trigger menu can be changed easily, by downloading the LUT and CAM memories via VME access to the CTP_CORE module. The LUT and CAM are implemented with a Xilinx Virtex-II FPGA.

Each of the 256 trigger items is individually masked, prescaled and assigned a priority level, using an ALTERA Stratix FPGA. The CTP_CORE module adds dead-time in order to prevent the detector front-end buffers from overrunning. Two leaky-bucket algorithms are used to count and limit the number of L1As generated over a given period of time. The two deadtimes are associated to two different priorities of trigger items. The final L1A is the OR of the masked and prescaled trigger items, where items might be vetoed by the deadtime logic (depending on the priority level) or by the busy signal received by the CTP_CORE. A trigger type word is also formed, depending on which trigger items caused the L1A. Both the L1A and the trigger type are sent to the COMbus to be distributed to the subdetectors via the CTP_OUT and LTPs.

Upon a L1A, the module sends Region-of-Interest (RoI) information to the RoI-Builder (RoIB) of the Level-2 trigger system. Also trigger summary information is sent to the Read-Out System (ROS) of the Data Acquisition System (DAQ). This information is a superset of the RoI information and can contain several bunches before and after the triggering bunch for debugging and monitoring purposes. For each bunch, it contains the 160 trigger inputs, and the 256 trigger items both before and after masking and prescaling. This readout block is implemented in a second ALTERA Stratix FPGA. Within this FPGA, monitoring scalers of the trigger items are also implemented, to be read via VME.

As for the physics capabilities of the current implementation of the trigger menu, it is worth noting that the total number of trigger inputs (160), as well as of (individually masked and prescaled) trigger items (256) is substantially larger than in the trigger tables currently foreseen for the LHC startup [1].

The CTP_CORE module has been designed and built, see Fig. 8. The critical functionality, namely the part necessary for the trigger formation, has been successfully tested.

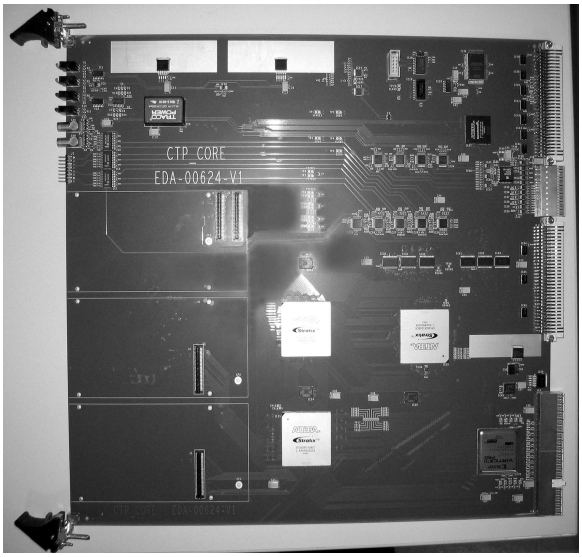

Figure 8: Photograph of the CTP_CORE module

E. CTP_MON Module

The block diagram of the CTP monitoring module (CTP_MON), see also Refs. [14][15], is shown in Figure 9.

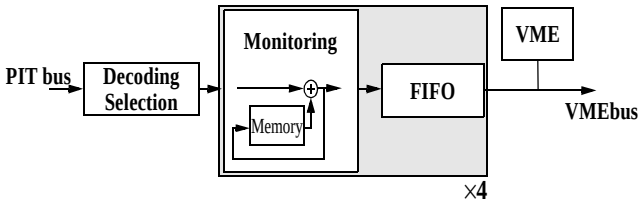

Figure 9: Block diagram of the CTP_MON module

The CTP_MON module receives and synchronizes the trigger inputs from the PITbus. It decodes and selects the trigger inputs to be monitored. The CTP_MON module monitors trigger information on a bunch-by-bunch basis. Specifically, for each selected trigger input, the histogram occupancy versus BCID is updated every 25 ns. The CTP_MON module uses numerous segmented memories in four Altera Stratix FPGAs for the counters. A total of 2 MByte are required, i.e. 160 trigger inputs times 3564 bunch crossings times 30 bits per counter. Using 30-bit counters the CTP_MON can perform the histogramming for 26 hours, without overflow even for an input always active (counter increments once per LHC turn, i.e. every 89 μs). To read the histograms stored in memory, exter-

nal IDT FIFOS and an ALTERA Apex FPGA are used. The CTP_MON, shown in Fig. 10, was tested successfully. Note that only one out of the four Stratix devices was mounted, which is enough for validation of the design in the October 200 4 test-beam.

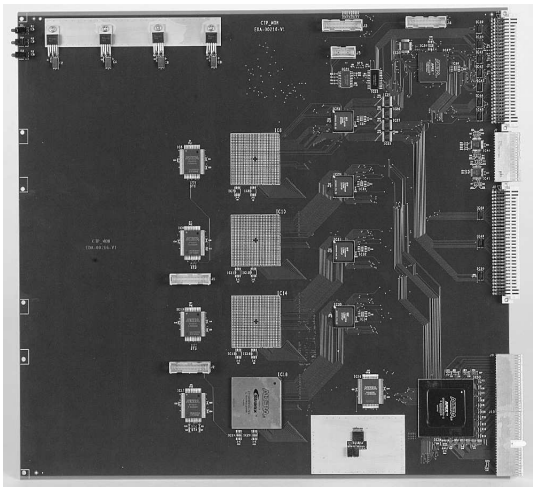

Figure 10: Photograph of the CTP_MON module

F. CTP_OUT Module

The CTP_OUT [16] is the fan-in/fan-out module of the CTP providing the connection to the LTPs. It receives timing and trigger signals (13 bits) from the COMbus and fans them out to five LTPs. In turn, it receives 4 bits (busy signals and calibration requests) from the LTPs. In the same way as the ROD_BUSY module, the CTP_OUT combines, masks and monitors the busy signal, and provides the busy-or to the COMbus. The calibration requests are sent to the CALbus.

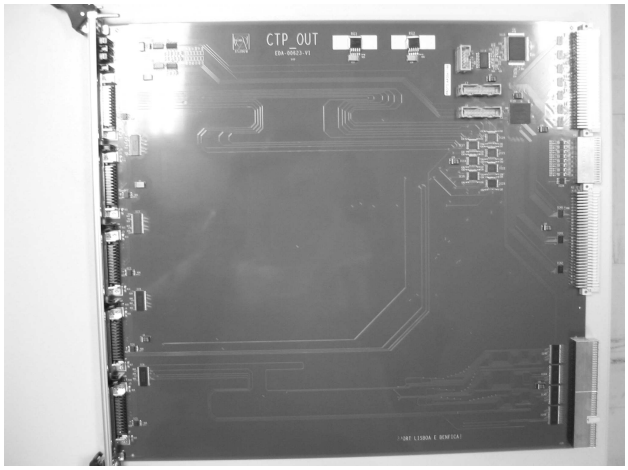

Figure 11: Photograph of the CTP_OUT module

The busy logic and interface to the VMEbus were implemented with an ALTERA Cyclone FPGA. The CTP_OUT link to the LTPs is done in LVDS with low-skew cables. The first prototype of the CTP_OUT module was designed and tested and is shown in Figure 11.

G. CTP_CAL Module

Some ATLAS sub-detectors have expressed the need for calibration triggers during the orbit gap of a physics run. The CTP_CAL module tries to address this requirement, by time-multiplexing the calibration requests on the CALbus per LHC ORBIT and sending them to the CTP_IN. The CTP_CAL can also serve as a patch-panel to receive other external trigger inputs from beam pick-up monitors and test triggers which are then provided to the CTP_IN module. The CTP_CAL module needs to be designed and is not needed for the test of the CTP system during the October 2004 test-beam.

H. Local Trigger Processor (LTP)

The LTP, see also Ref. [3], is a programmable input/output switch for timing, trigger and control signals. One LTP will be used per partition in ATLAS, for a total of about 40 modules. The input can be chosen among the signals from the CTP (from the CTP_OUT module) or from the LTP daisy-chain, from local input, or from the LTP's pattern generator.

Outputs are available to the LTP daisy-chain and to the TTC system local to the same partition. In addition test outputs are provided. The LTP also receives the busy signals from the ROD_BUSY modules and sends them to a CTP_OUT or another LTP. Hence the LTP allows each partition to run in one of the following modes:

- In *common* mode the CTP drives the TTC partition. The LTP is then an interface between the CTP and the TTC system. This is the normal mode for physics running.
- In *stand-alone* mode the LTP drives the TTC partition from local inputs or its pattern generator. This is the mode for calibration or debugging of a single partition.
- Two or more TTC partitions can be used in *combined mode* by programming one LTP as the master and by programming the other LTPs as slaves. This mode allows one to run several TTC partitions together for calibration runs with more than one sub-detector, e.g. calorimeter detector and calorimeter trigger.

The LTP has been designed as a 6U VME double width module using CPLDs and external RAMs for the pattern generator. Six prototypes have been built and testing by the sub-detectors at the test-beam is under way.

I. ROD_BUSY module

The ROD_BUSY module [6] receives 16 input busy signals from the detector's Read Out Drivers (RODs) or from other ROD_BUSYs. Each individual input (TTL open-collector) can be masked, and the overall OR of the masked inputs is formed. The ROD_BUSYs can be daisy-chained, until the last one feeds an LTP, from which the busy signal will arrive at the CTP_OUT to throttle the L1A generation. The busy inputs are monitored so that the history of the first (or last) 3.3 seconds of all the 16 inputs is stored in FIFOs. An interrupt request might be asserted if the overall BUSY_OR is active for longer than a preset time limit.

The ROD_BUSY is a 6U single-width module, implemented using ALTERA CPLDs and discrete FIFOs. A total of 60 modules will be used in ATLAS, and 12 have been produced and tested. The ROD_BUSY module is already being used at the test-beam.

IV. Conclusion

The Level-1 central trigger system of ATLAS is now designed and the full chain will be tested in a realistic environment in October 2004, in a combined test-beam with 25 ns bunch structure, along with other ATLAS sub-detectors and trigger processors.

Substantial progress has been achieved on the CTP over the last year: all the modules and backplanes implementing the core functionality have been designed, with the exception of the CTP_CAL which is a comparatively simple interface module. A prototype of the system has been built, with each type of module having already the final foreseen functionality. The test and integration with the trigger processors at the test-beam is well under way.

Regarding the TTC partitions, the hardware is now available with the complete functionality. Besides the TTC system itself which is by now in a mature state, twelve final prototypes of the ROD_BUSY modules have been tested. The first six prototypes of the LTP have been produced and started to be used at the test-beam by the sub-detectors.

The October 2004 test-beam will allow a final validation of the central trigger system design. After incorporating any final changes to the design, construction, installation and commissioning of the full system in the experimental area can proceed.

V. References

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